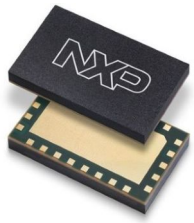
A5M36TG240

Airfast Power Amplifier Module

Rev. 1 — 31 May 2024 Product data sheet



1 General description

The A5M36TG240 is a fully integrated Doherty power amplifier module designed for wireless infrastructure applications that demand high performance in the smallest footprint. Ideal for applications in massive MIMO systems, outdoor small cells and low power remote radio heads. The field-proven LDMOS and GaN power amplifiers are designed for TDD LTE and 5G systems.

2 Features and benefits

- 2-stage module solution that includes an LDMOS integrated circuit as a driver and a GaN final stage amplifier
- Advanced high performance in-package Doherty
- Fully matched (50 ohm input/output, DC blocked)
- Designed for low complexity digital linearization systems
- Reduced memory effects for improved linearized error vector magnitude

3 Typical performance

Table 1. 3400–3800 MHz — Typical LTE performance

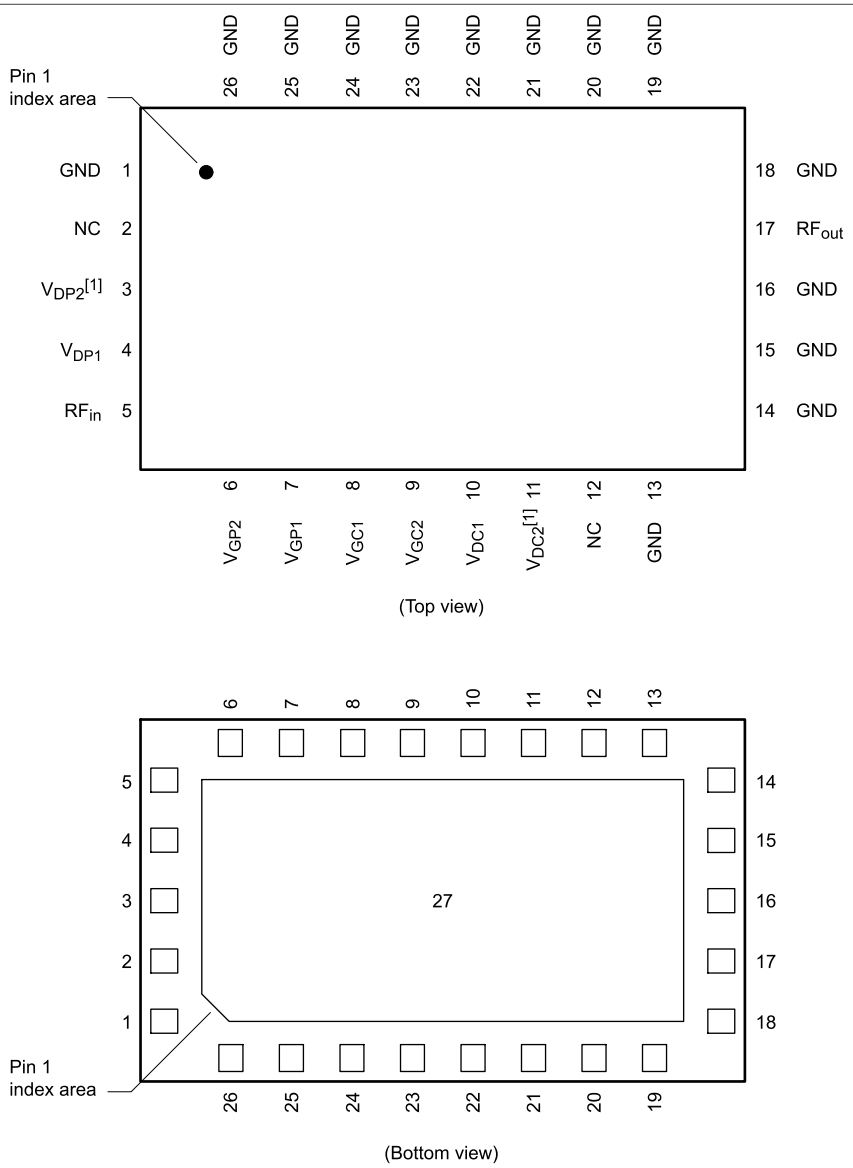
P_{out} = 9 W Avg., V_{DC1} = V_{DP1} = 5 Vdc, V_{DC2} = V_{DP2} = 48 Vdc, 1 × 20 MHz LTE, input signal PAR = 8 dB @ 0.01% probability on CCDF.[1]

Carrier center frequency	Gain (dB)	ACPR (dBc)	PAE (%)
3410 MHz	31.4	–26.4	45.2
3500 MHz	31.7	–27.0	49.4
3600 MHz	31.8	–27.8	51.7
3700 MHz	31.9	–29.4	51.6
3790 MHz	32.0	–30.9	50.0

[1] All data measured with device soldered to NXP reference circuit.

4 Pinning information

4.1 Pinning



Note: Exposed backside of the package is DC and RF ground.

[1] V_{DP2} and V_{DC2} are DC coupled internal to the package and must be powered by a single DC power supply.

Figure 1. Pin configuration

4.2 Pin description

Table 2. Pin description

Pin number	Pin function	Pin description
1, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27	GND	Ground
2, 12	NC	No connection
3	V_{DP2}	Peaking drain supply, stage 2
4	V_{DP1}	Peaking drain supply, stage 1
5	RF_{in}	RF input
6	V_{GP2}	Peaking gate supply, stage 2
7	V_{GP1}	Peaking gate supply, stage 1
8	V_{GC1}	Carrier gate supply, stage 1
9	V_{GC2}	Carrier gate supply, stage 2
10	V_{DC1}	Carrier drain supply, stage 1
11	V_{DC2}	Carrier drain supply, stage 2
17	RF_{out}	RF output

5 Functional electrical routing diagram

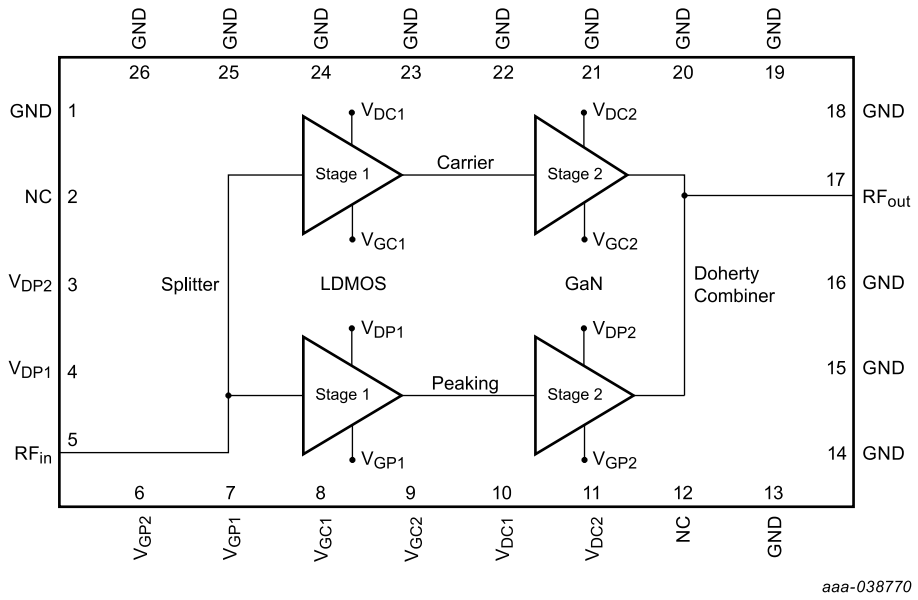


Figure 2. Functional electrical routing diagram

6 Ordering information

Table 3. Ordering information

Device	Tape and reel information	Package
A5M36TG240T2	T2 suffix = 2,000 units, 24 mm tape width, 13-inch reel	10 mm × 6 mm Module

7 Product marking

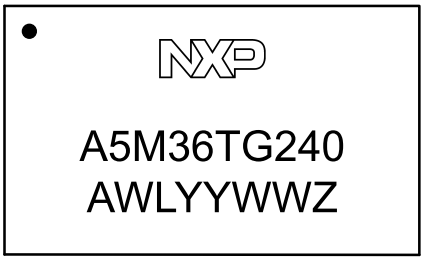


Figure 3. Product marking

Table 4. Product marking trace code

Identifier	Description
A	Assembly location
WL	Wafer lot indicator
YYWW	Date code
Z	Assembly lot

8 Limiting values

Table 5. Limiting values

Rating	Symbol	Value	Unit
Gate-bias voltage range	V_{G1} V_{G2}	–0.5 to +10 –8, 0	Vdc
Operating voltage range	V_{DD1} V_{DD2}	4.75 to 5.25 +38 to +55	Vdc
Maximum forward gate current, $I_{G\ (A+B)}$, @ T_C = 25°C	I_{GMAX}	8.7	mA
Storage temperature range	T_{stg}	–65 to +150	°C
Case operating temperature	T_C	125	°C
Maximum channel temperature	T_{CH}	225	°C
Peak input power (3600 MHz, pulsed CW, 10 µsec(on), 10% duty cycle, V_{DC1} = V_{DP1} = 5 Vdc, V_{DC2} = V_{DP2} = 48 Vdc)	P_{in}	28	dBm

9 Lifetime

Table 6. Lifetime

Characteristic	Symbol	Value	Unit
Mean time to failure (Case temperature 125°C, 75% duty cycle, 9 W Avg., V_{DC1} = V_{DP1} = 5 Vdc, V_{DC2} = V_{DP2} = 48 Vdc)	MTTF	> 10	Years

10 Thermal characteristics

Table 7. Thermal characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance by infrared measurement, active die surface-to-case (Case temperature 125°C, P_D = 16.2 W)	$R_{\theta SC}$ (IR)	4.6[1]	°C/W
Thermal resistance by finite element analysis, channel-to-case (Case temperature 125°C, P_D = 9.5 W) (Case temperature 110°C, P_D = 12.3 W)	$R_{\theta CHC}$ (FEA)	 10.5[2] 9.3[2]	°C/W

[1] Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to http://www.nxp.com/RF and search for AN1955.
[2] $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where T is the channel temperature in degrees Celsius, A = –12.47 and B = 9729.

11 ESD protection characteristics

Table 8. ESD protection characteristics

Test methodology	Class
Human Body Model (per JS-001-2023)	2
Charge Device Model (per JS-002-2022)	C3

12 Moisture sensitivity level

Table 9. Moisture sensitivity level

Test methodology	Rating	Package peak temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

13 Electrical characteristics

13.1 DC characteristics — off characteristics

Table 10. DC characteristics — off characteristics

(T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Carrier + peaking stage 2, GaN — off characteristics					
Off-state drain leakage[1] (V_{DS} = 150 Vdc, V_{GS} = –8 Vdc)	$I_{D(BR)}$	—	—	4.0	mAdc
Off-state gate leakage (V_{DS} = 48 Vdc, V_{GS} = –7 Vdc)	I_{GLK}	–4.0	—	—	mAdc

[1] Carrier side and peaking side are tied together for these measurements.

13.2 DC characteristics — on characteristics

Table 11. DC characteristics — on characteristics

(T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Typ	Range	Unit
Carrier stage 1, LDMOS — on characteristics				
Gate threshold voltage (V_{DS} = 5 Vdc, I_{DC1} = 120 µAdc)	$V_{GS(th)}$	1.4	±0.4	Vdc
Gate quiescent voltage (V_{DS} = 5 Vdc, I_{DQC1} = 85 mAdc, measured in functional test)	$V_{GS(Q)}$	2.0	±0.4	Vdc
Carrier stage 2, GaN — on characteristics				
Gate threshold voltage[1] (V_{DS} = 10 Vdc, I_D = 8.7 mAdc)	$V_{GS(th)}$	–2.6	±1.0	Vdc
Gate quiescent voltage (V_{DS} = 48 Vdc, I_{DQC2} = 28 mAdc, measured in functional test)	$V_{GS(Q)}$	–2.7	±1.0	Vdc
Peaking stage 1, LDMOS — on characteristics				
Gate threshold voltage (V_{DS} = 5 Vdc, I_{DP1} = 120 µAdc)	$V_{GS(th)}$	1.4	±0.4	Vdc
Gate quiescent voltage (V_{DS} = 5 Vdc, I_{DQP1} = 40 mAdc, measured in functional test)	$V_{GS(Q)}$	2.0	±0.4	Vdc
Peaking stage 2, GaN — on characteristics				
Gate threshold voltage[1] (V_{DS} = 10 Vdc, I_D = 8.7 mAdc)	$V_{GS(th)}$	–2.6	±1.0	Vdc
Gate quiescent voltage (V_{DS} = 48 Vdc, I_{DQP2} = 0 mAdc, measured in functional test)	$V_{GS(Q)}$	–3.5	±1.0	Vdc

[1] Carrier side and peaking side are tied together for these measurements.

13.3 Functional tests

Table 12. Functional tests — 3400 MHz

(In NXP Doherty production ATE[1] test fixture, T_A = 25°C unless otherwise noted, 50 ohm system)[2] V_{DD1} = 5 Vdc, V_{DD2} = 48 Vdc, I_{DQC1} = 85 mA, I_{DQC2} = 28 mA, I_{DQP1} = 40 mA, V_{GP2} = (V_{BIAS} – 0.64)[3] Vdc, P_{out} = 9 W Avg., 1-tone CW, f = 3400 MHz.

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G	27.3	31.0	—	dB
Drain efficiency	η_D	38.0	43.8	—	%
Saturated power[4] (Pulsed CW, 5% duty cycle)	P_{sat}	46.4	48.0	—	dBm

[1] ATE is a socketed test environment.
[2] Part input and output matched to 50 ohms.
[3] Increase V_{GP2} (peaking side) until I_{DQP2} = 20 mA current is attained, and then subtract 0.64 V for final V_{GP2} bias voltage.
[4] P_{sat} is defined at P6dB compression point.

13.4 Wideband ruggedness

Table 13. Wideband ruggedness

(In NXP Doherty power amplifier module reference circuit, T_A = 25°C unless otherwise noted, 50 ohm system)[1]
I_{DQC1} = 85 mA, I_{DQC2} = 28 mA, I_{DQP1} = 40 mA, V_{GP2} = (V_{BIAS} – 0.64)[2] *Vdc, f = 3600 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR.*

Characteristic	Test results
ISBW of 400 MHz at 55 Vdc, 3 dB input overdrive from 9 W Avg. modulated output power	No device degradation

[1] All data measured with device soldered to NXP reference circuit.
[2] Increase V_{GP2} (peaking side) until I_{DQP2} = 20 mA current is attained, and then subtract 0.64 V for final V_{GP2} bias voltage.

13.5 Typical performance

Table 14. Typical performance

(In NXP Doherty power amplifier module reference circuit, T_A = 25°C unless otherwise noted, 50 ohm system)[1]
V_{DD1} = 5 Vdc, V_{DD2} = 48 Vdc, I_{DQC1} = 85 mA, I_{DQC2} = 28 mA, I_{DQP1} = 40 mA, V_{GP2} = (V_{BIAS} – 0.64)[2] *Vdc, f = 3600 MHz.*

Characteristic	Symbol	Min	Typ	Max	Unit
VBW resonance point, 2-tone, 1 MHz tone spacing (IMD third order intermodulation inflection point)	VBW_{res}	—	300	—	MHz
1-carrier 20 MHz LTE, 8 dB input signal PAR					
Gain	G	—	31.8	—	dB
Power added efficiency	PAE	—	51.7	—	%
Adjacent channel power ratio	ACPR	—	–27.8	—	dBc
Adjacent channel power ratio	ALT1	—	–40.5	—	dBc
Adjacent channel power ratio	ALT2	—	–46.5	—	dBc
Gain flatness[3]	G_F	—	0.6	—	dB
Pulsed CW, 10% duty cycle					
Saturated power[4]	P_{sat}	—	48.2	—	dBm
AM/PM @ saturated power[4]	Φ	—	–36.0	—	°
Gain variation @ Avg. power over temperature (–40°C to +105°C)	ΔG	—	0.056	—	dB/°C
Output power variation @ saturated power over temperature[4] (–40°C to +105°C)	ΔP_{sat}	—	0.002	—	dB/°C

[1] All data measured with device soldered to NXP reference circuit.
[2] Increase V_{GP2} (peaking side) until I_{DQP2} = 20 mA current is attained, and then subtract 0.64 V for final V_{GP2} bias voltage.
[3] Gain flatness = Max(G(f_{Low} to f_{High})) – Min(G(f_{Low} to f_{High})).
[4] P_{sat} is defined at P6dB compression point.

Correct Biasing Sequence

Turn ON:

Bias ON the GaN final stage first

1. Set gate voltage V_{GC2} and V_{GP2} to –5 V.
2. Set drain voltage V_{DC2} and V_{DP2} to nominal supply voltage (+48 V).
3. Increase V_{GP2} (peaking side) until I_{DQP2} = 20 mA current is attained, and then subtract 0.64 V for final V_{GP2} bias voltage.
4. Increase V_{GC2} (carrier side) until I_{DQC2} current is attained.

Bias ON the LDMOS driver stage second

5. Set drain voltage V_{DC1} and V_{DP1} to nominal supply voltage (+5 V).
6. Increase V_{GC1} (carrier side) until I_{DQC1} current is attained.
7. Increase V_{GP1} (peaking side) until I_{DQP1} current is attained.
8. Apply RF input power to desired level.

Turn OFF:

Bias OFF the GaN final stage first

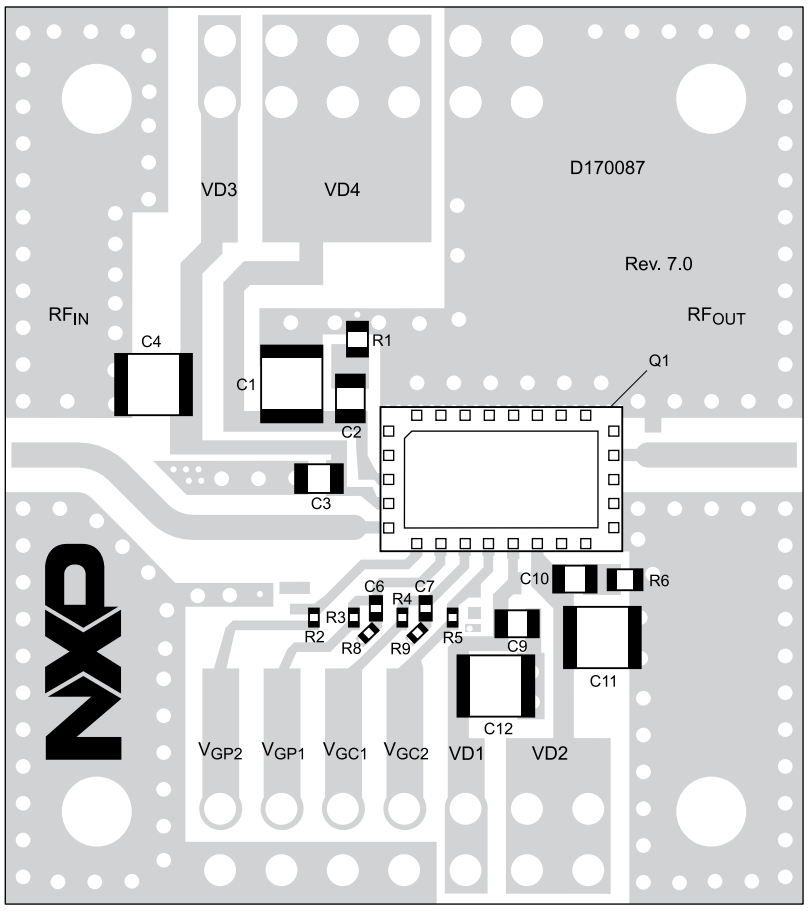
1. Disable RF input power.
2. Adjust gate voltage V_{GC2} and V_{GP2} to –5 V.
3. Adjust drain voltage V_{DC2} and V_{DP2} to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
4. Disable V_{GC2} and V_{GP2}.

Bias OFF the LDMOS driver stage second

5. Adjust gate voltage V_{GC1} and V_{GP1} to 0 V.
6. Adjust drain voltage V_{DC1} and V_{DP1} to 0 V.

14 Component layout and parts list

14.1 Component layout



Board label	Pin description	Pin function
VD1	Carrier drain supply, stage 1	V_{DC1}
VD2	Carrier drain supply, stage 2	V_{DC2}
VD3	Peaking drain supply, stage 1	V_{DP1}
VD4	Peaking drain supply, stage 2	V_{DP2}

Figure 4. A5M36TG240 reference circuit component layout

14.2 Component designations and values

Table 15. A5M36TG240 reference circuit component designations and values

Part	Description	Part number	Manufacturer
C1, C4, C11, C12	10 µF chip capacitor	GRM32EC72A106KE05L	Murata
C2, C3, C9, C10	1 µF chip capacitor	GRM21BC72A105KE01L	Murata
C6, C7	1000 pF chip capacitor	GRM155R72A102KA01D	Murata
Q1	Power amplifier module	A5M36TG240	NXP
R1, R6	0 Ω, 0.063 W chip resistor	6-1622826-4	TE Connectivity
R2, R5, R8, R9	0 Ω, 1/20 W chip resistor	RC0201JR-070RL	Yageo
R3, R4	10 Ω, 1/20 W chip resistor	RC0201FR-0710RL	Yageo
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D170087	MTL

Note: Component numbers C5, C8 and R7 are intentionally omitted.

15 Package information

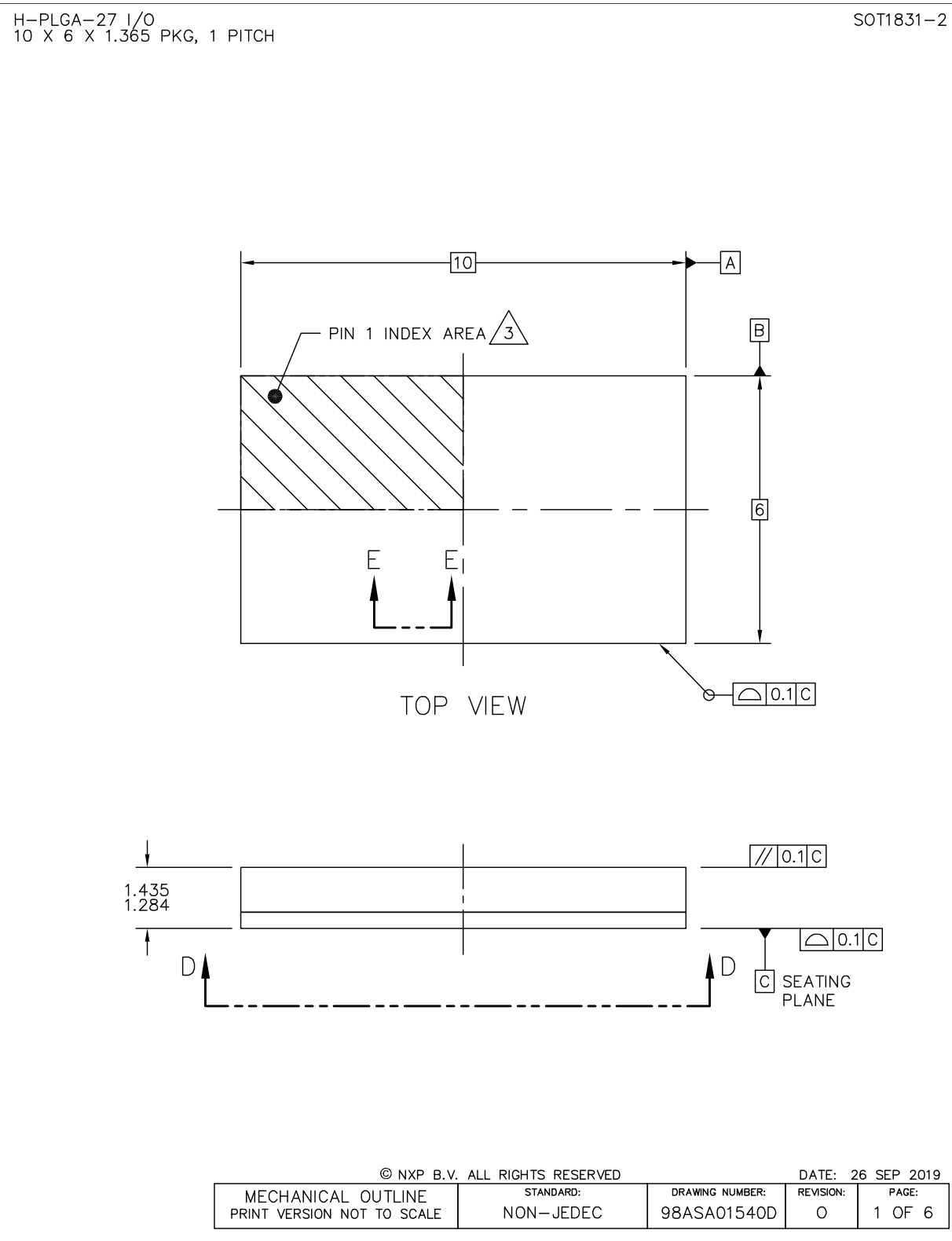


Figure 5. Package outline (10 mm × 6 mm Module) — top view

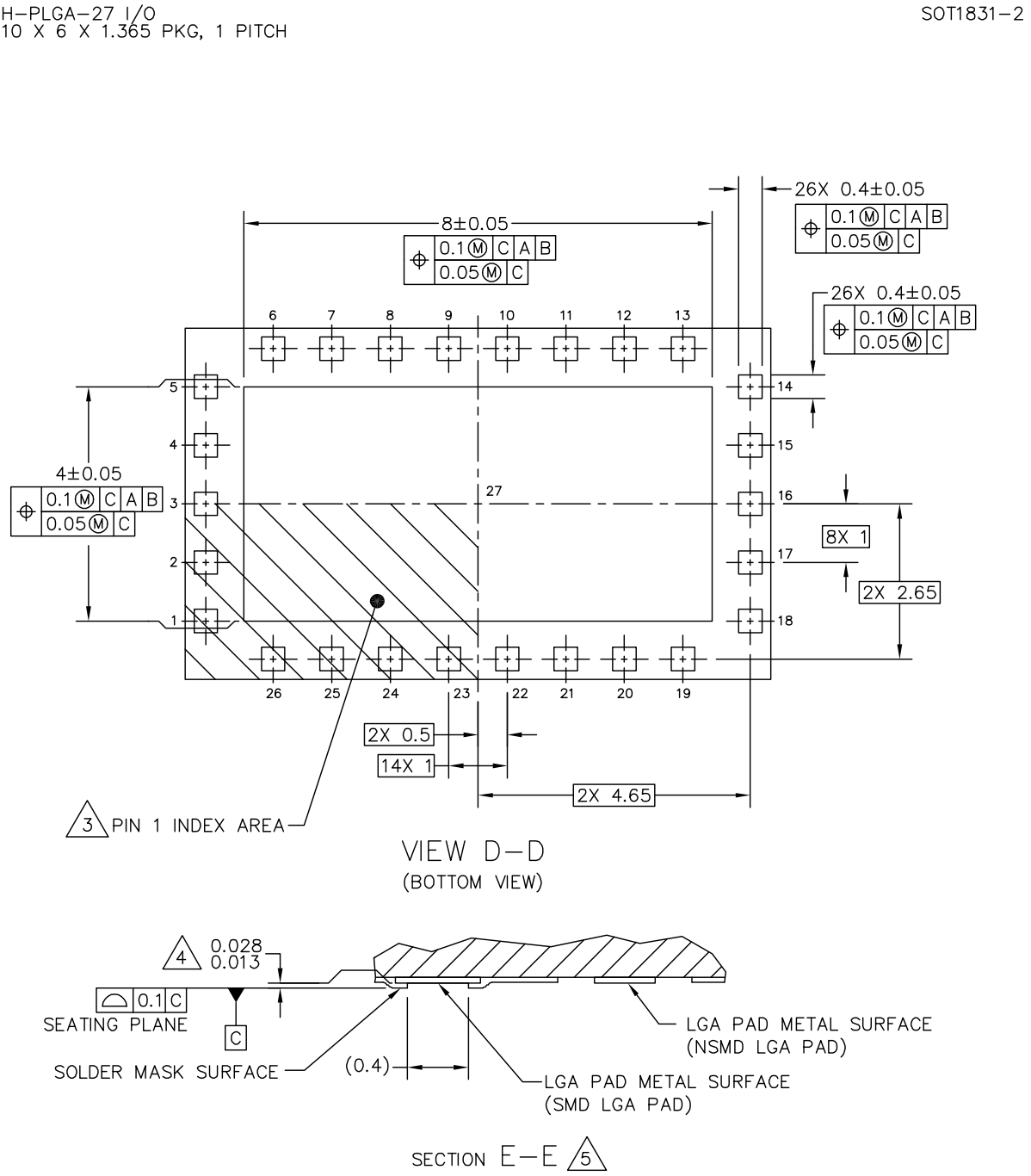
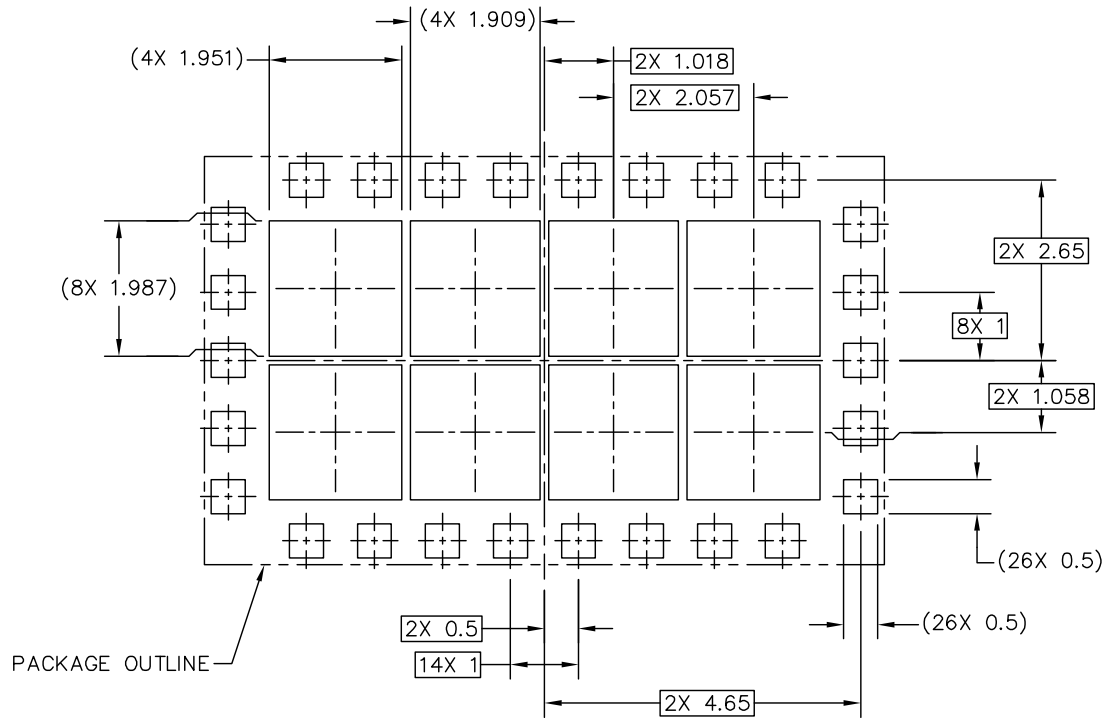


Figure 6. Package outline (10 mm × 6 mm Module) — bottom view



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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DATE: 26 SEP 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON–JEDEC	DRAWING NUMBER: 98ASA01540D	REVISION: O	PAGE: 3

Figure 7. Package outline (10 mm × 6 mm Module) — PCB design guidelines: solder mask opening pattern

H–PLGA–27 I/O
10 X 6 X 1.365 PKG, 1 PITCH

SOT1831–2

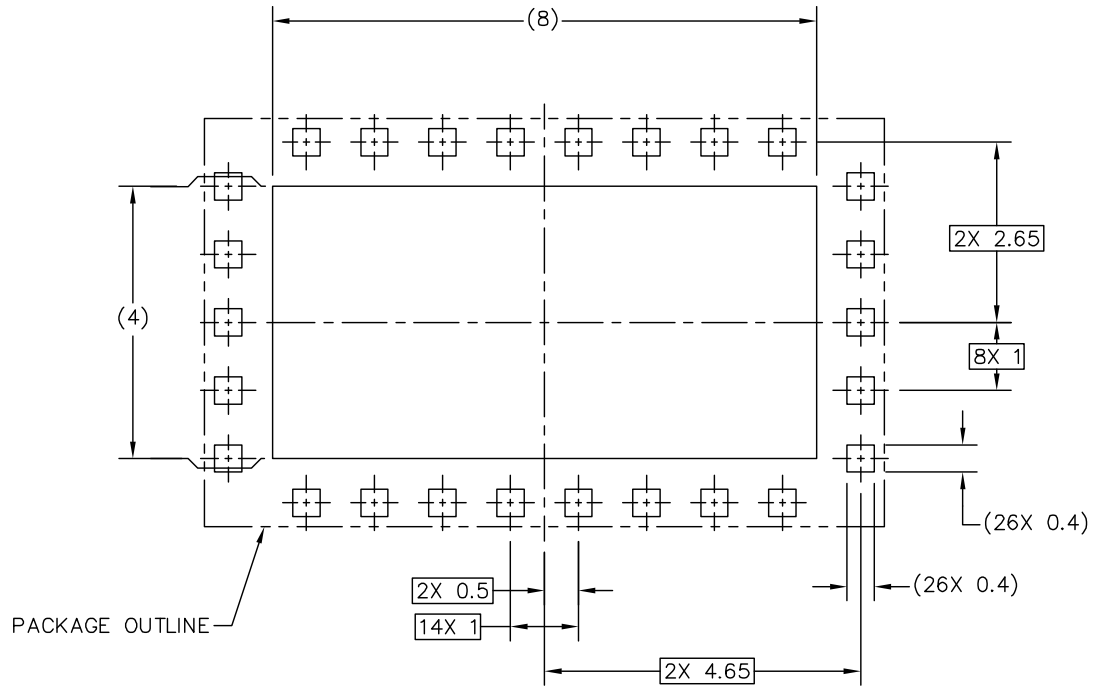

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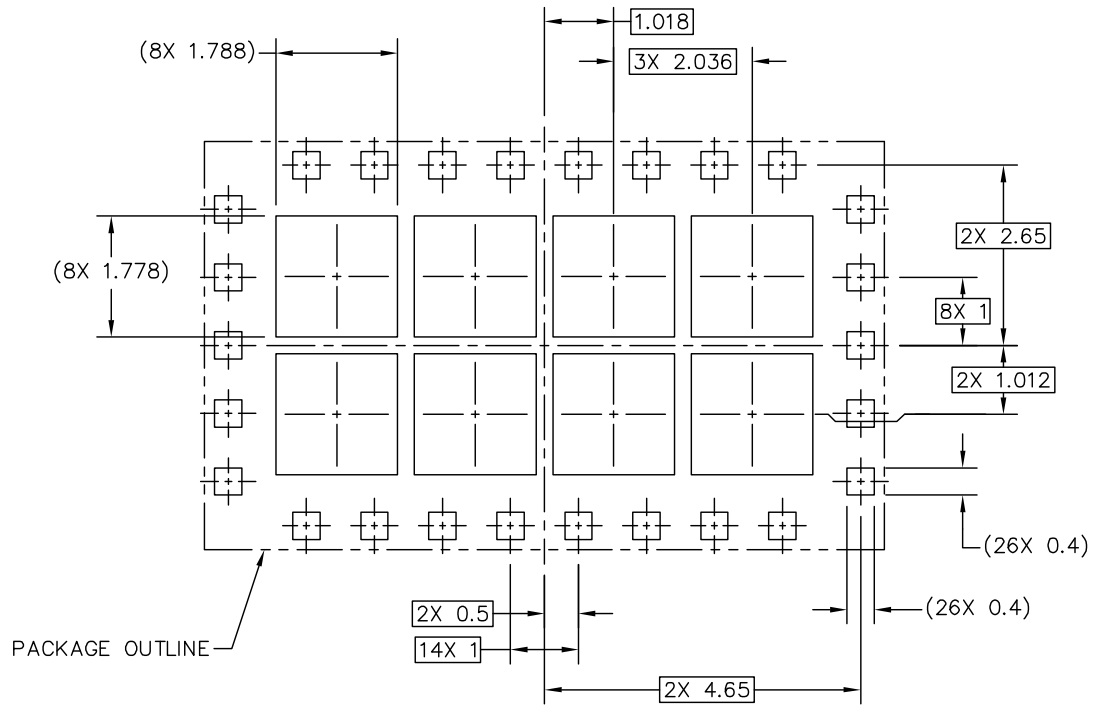
Figure 8. Package outline (10 mm × 6 mm Module) — PCB design guidelines: I/O pads and solderable areas



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 9. Package outline (10 mm × 6 mm Module) — PCB design guidelines: solder paste stencil

H–PLGA–27 I/O
10 X 6 X 1.365 PKG, 1 PITCH

SOT1831–2

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. DIMENSION APPLIES TO ALL LEADS AND FLAG.
5. THE BOTTOM VIEW SHOWS THE SOLDERABLE AREA OF THE PADS. THE CENTER PAD (PIN 27) IS SOLDER MASK DEFINED. SOME PERIPHERAL PADS ARE SOLDER MASK DEFINED (SMD) AND OTHERS ARE NON–SOLDERMASK DEFINED (NSMD).

DATE: 26 SEP 2019

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Figure 10. Package outline (10 mm × 6 mm Module) — notes

16 Product documentation and tools

Refer to the following resources to aid your design process.

Application notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Development tools

- Printed circuit boards

17 Failure analysis

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where NXP is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local NXP Sales Office.

18 Revision history

The following table summarizes revisions to this document.

Table 16. Revision history

Document ID	Release date	Description
A5M36TG240 Rev. 1	31 May 2024	• Initial release of product data sheet

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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