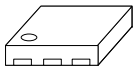
# 1-Channel Low Side Switch

## ■ GENERAL DESCRIPTION

The NJW4822 is the single low-side switch that can supply 0.2A. The active clamp, overcurrent, error flag output and thermal shutdown are built in with Nch MOS FET.
It can be controlled by a logic signal (3V/5V) directly. Especially, the NJW4822 is suitable for various Sensors output block as NPN type. The FLT logic has two versions: Active-high (A-ver) and Active-low (B-ver).
Also, The NJW4822 is a complementary product to the NJW4832.

## ■ PACKAGE OUTLINE

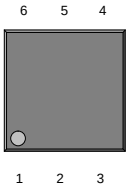


NJW4822KH1

## ■ FEATURES

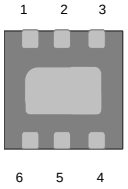
- Drain-Source Voltage 43V
- Drain Current 0.2A
- Corresponding with Logic Voltage Operation: 3V/5V
- Low On-Resistance 1.1Ω (typ.) ($V_{IN}$=5V)
  1.3Ω (typ.) ($V_{IN}$=3.3V)
- Low Consumption Current 160μA (typ.) ($V_{IN}$=5V)
  135μA (typ.) ($V_{IN}$=3.3V)
- Active Clamp Circuit
- Over Current Protection
- Thermal Shutdown
- Package Outline DFN6-H1 (ESON6-H1)

## ■ PIN CONFIGURATION




(Top View)

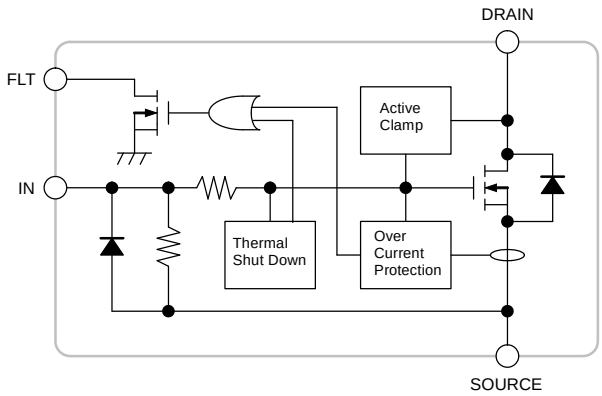
1. NC
2. NC
3. DRAIN
4. IN
5. SOURCE
6. FLT




(Bottom View)

Exposed PAD on backside connect to GND.

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

| PARAMETER | SYMBOL | RATINGS | UNIT | REMARK |
|---|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | +43 | V | DRAIN–SOURCE Pin |
| Input Pin Voltage | $V_{IN}$ | –0.3 to +6 | V | IN–SOURCE Pin |
| FLT Pin Voltage | $V_{FLT}$ | –0.3 to +6 | V | FLT–SOURCE Pin |
| Power Dissipation | $P_D$ | 445 (*1)<br>1135 (*2) | mW | – |
| Active Clamp Tolerance (Single Pulse) | $E_{AS}$ | 100 | mJ | – |
| Active Clamp Current | $I_{AP}$ | 0.2 | A | – |
| Junction Temperature | $T_j$ | –40 to +150 | °C | – |
| Operating Temperature | $T_{opr}$ | –40 to +125 | °C | – |
| Storage Temperature | $T_{stg}$ | –50 to +150 | °C | – |

(*1): Mounted on glass epoxy board (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)

(*2): Mounted on glass epoxy board (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)
(4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

## ■ RECOMMENDED OPERATING CONDITIONS

(Ta=25°C)

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | REMARK |
|---|---|---|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 0 | – | 40 | V | DRAIN–SOURCE Pin |
| Drain Current | $I_D$ | 0 | – | 0.2 | A | DRAIN–SOURCE Pin |
| Input Pin Voltage | $V_{IN}$ | 0 | – | 5.5 | V | IN–SOURCE Pin |
| FLT Pin Voltage | $V_{FLT}$ | 0 | – | 5.5 | V | FLT–SOURCE Pin |

## ■ PRODUCT VERSION

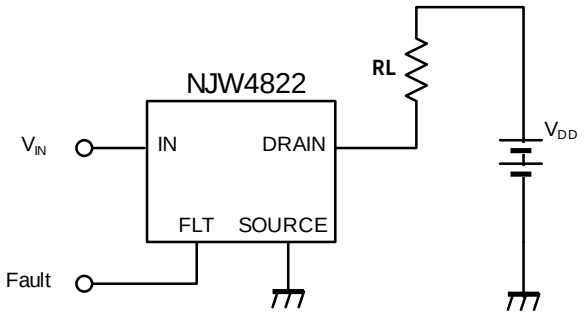
| PRODUCT NAME | FLT LOGIC |
|---|---|
| NJW4822KH1-A | Active High |
| NJW4822KH1-B | Active Low |

## ■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, $V_{DS}$=13V, Ta=25°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Drain-Source Clamp Voltage | $V_{DSS\_CL}$ | $V_{IN}$=0V, $I_D$=1mA | 43 | – | – | V |
| Input Threshold Voltage | $V_{th}$ | $V_{DS}$=13V, $I_D$=10mA | 0.55 | 0.8 | 1.05 | V |
| Protection Circuit Function Input Voltage Range | $V_{IN\_opr}$ | | 2.64 | – | 5.5 | V |
| Zero-gate-voltage drain Current | $I_{DSS}$ | $V_{IN}$=0V, $V_{DS}$=40V | – | – | 1 | μA |
| Input Current 1 (at Normal Operation) | $I_{IN1}$ | $V_{IN}$=5V | – | 160 | 225 | μA |
| Input Current 2 (at Normal Operation) | $I_{IN2}$ | $V_{IN}$=3.3V | – | 135 | 195 | μA |
| Input Current 3 (at OCP Operation) | $I_{IN3}$ | $V_{IN}$=5V, $V_{DD}$=13V | – | 260 | 345 | μA |
| Input Current 4 (at OCP Operation) | $I_{IN4}$ | $V_{IN}$=3.3V, $V_{DD}$=13V | – | 175 | 240 | μA |
| On-state Resistance 1 | $R_{DS\_ON1}$ | $V_{IN}$=5V, $I_D$=0.2A | – | 1.1 | 1.45 | Ω |
| On-state Resistance 2 | $R_{DS\_ON2}$ | $V_{IN}$=3.3V, $I_D$=0.2A | – | 1.2 | 1.6 | Ω |
| Over Current Protection 1 | $I_{LIMIT1}$ | $V_{IN}$=5V, $V_{DD}$=13V | 0.2 | 0.45 | 0.85 | A |
| Over Current Protection 2 | $I_{LIMIT2}$ | $V_{IN}$=3.3V, $V_{DD}$=13V | 0.2 | 0.4 | 0.8 | A |
| Turn-on Time 1 | $t_{ON1}$ | $V_{IN}$=0 to 5V, $V_{DD}$=13V, $I_D$=0.2A | – | 2 | – | μs |
| Turn-on Time 2 | $t_{ON2}$ | $V_{IN}$=0 to 3.3V, $V_{DD}$=13V, $I_D$=0.2A | – | 4 | – | μs |
| Turn-off Time 1 | $t_{OFF1}$ | $V_{IN}$=5 to 0V, $V_{DD}$=13V, $I_D$=0.2A | – | 13 | – | μs |
| Turn-off Time 2 | $t_{OFF2}$ | $V_{IN}$=3.3 to 0V, $V_{DD}$=13V, $I_D$=0.2A | – | 8 | – | μs |
| Source–Drain Voltage Difference | $V_{PDSD}$ | $V_{IN}$=0V, $I_{DR}$=0.2A | – | 0.95 | 1.25 | V |
| FLT Pin Low Level Output Voltage | $V_{LFLT}$ | $I_{FLT}$=500μA | – | 0.25 | 0.5 | V |
| FLT Pin Leak Current at OFF State | $I_{OLEAKFLT}$ | $V_{FLT}$=5.5V | – | – | 1 | μA |
| FLT delay Time at OCP Detection | $T_{dDFLT}$ | $I_D$<$I_{LIMIT}$→$I_D$≥$I_{LIMIT}$ | – | 0.85 | – | ms |
| FLT delay Time at OCP Release | $T_{dRFLT}$ | $I_D$≥$I_{LIMIT}$→$I_D$<$I_{LIMIT}$ | – | 0.3 | – | ms |

## ■ MEASUREMENT CIRCUIT



## ■ TRUTH TABLE

[A-version: Active-high]

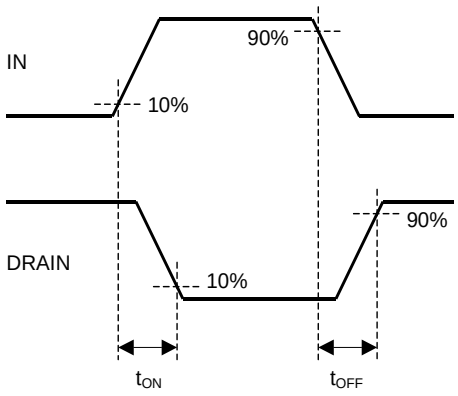
| Input Signal | Operating Condition | FLT Pin | Output Status |
|---|---|---|---|
| L | Normal | H | OFF |
| H | | L | ON |
| L | Over Current $I_{LIMIT}$ | H | OFF |
| H | | H | $I_{LIMIT}$ |
| L | $T_j$>150°C | H | OFF |
| H | | H | OFF |

[B-version: Active-low]

| Input Signal | Operating Condition | FLT Pin | Output Status |
|---|---|---|---|
| L | Normal | H | OFF |
| H | | H | ON |
| L | Over Current $I_{LIMIT}$ | H | OFF |
| H | | L | $I_{LIMIT}$ |
| L | $T_j$>150°C | H | OFF |
| H | | L | OFF |

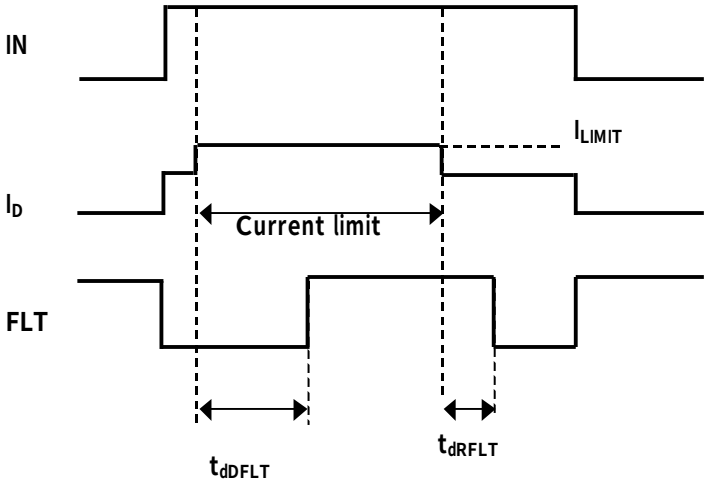
## ■ TIMING CHART

ON, OFF Switching Time ($V_{IN}$=0 to 5V, $V_{DS}$=13V, $I_D$=0.2A)

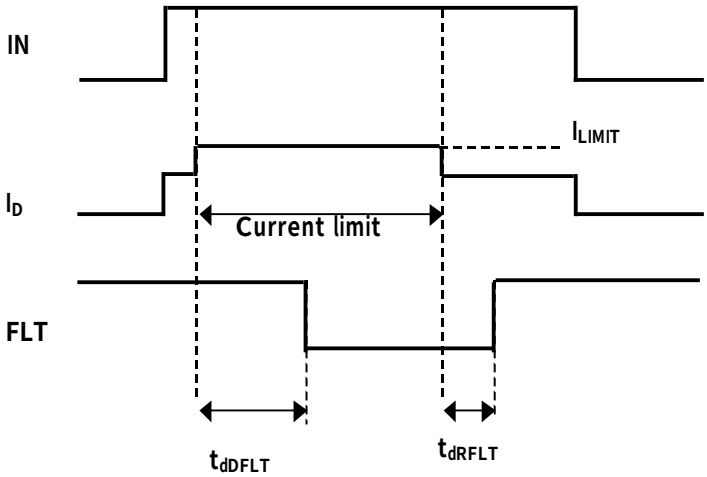



FLT delay at OCP detection and OCP release ($V_{IN}$=0 to 5V, FLT=Pull-up)

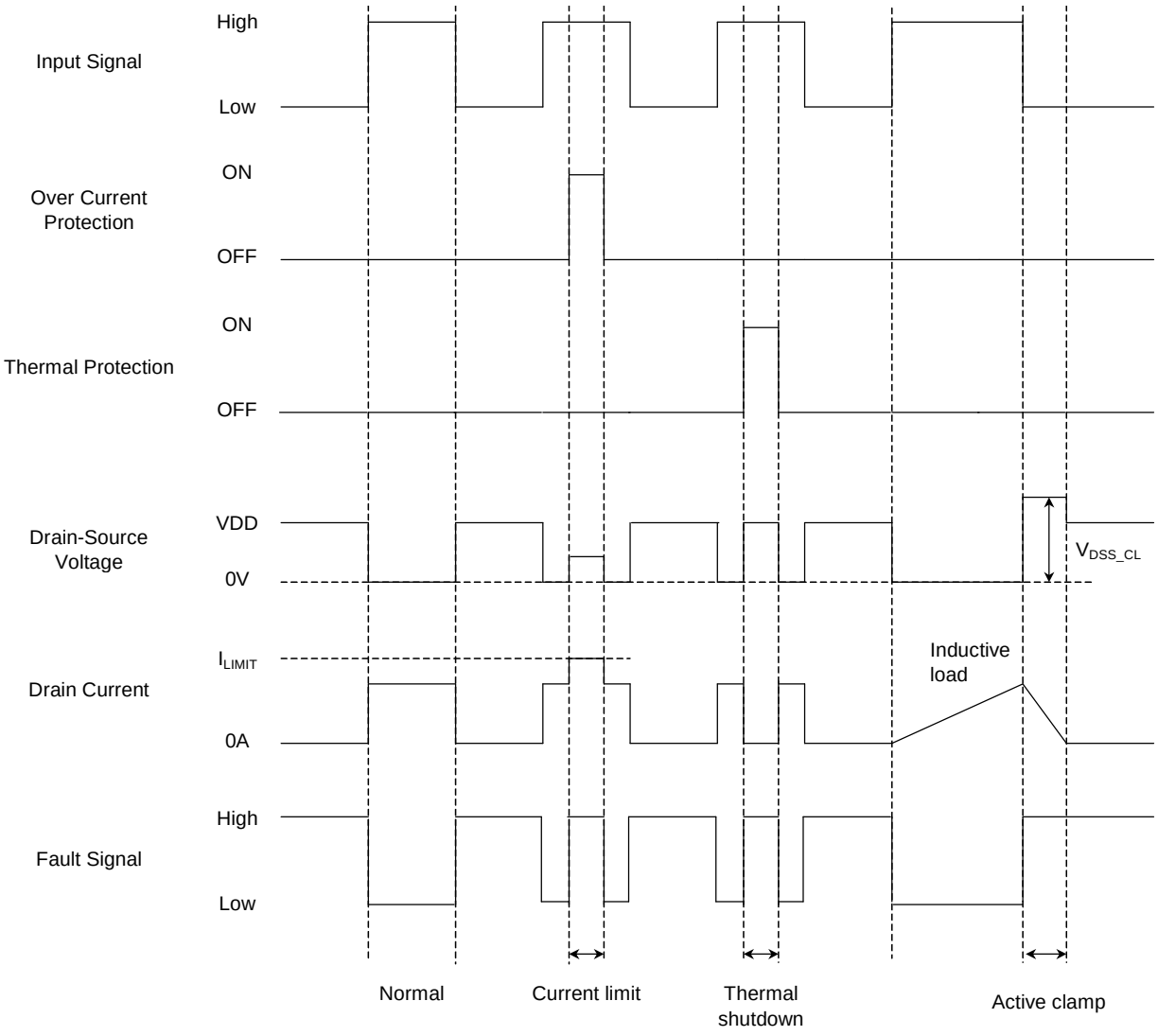
[A-version: Active-high]



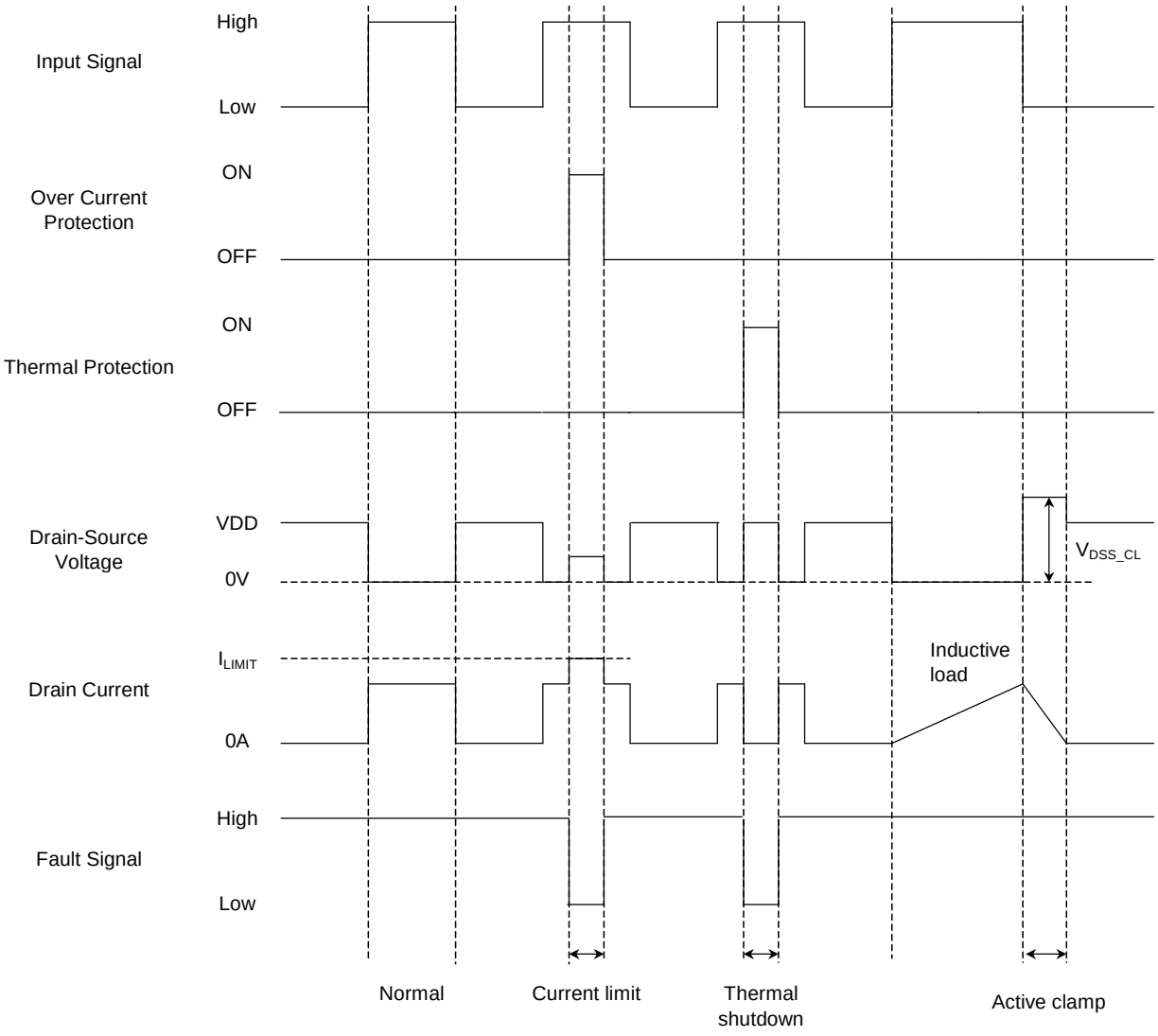

[B-version: Active-low]



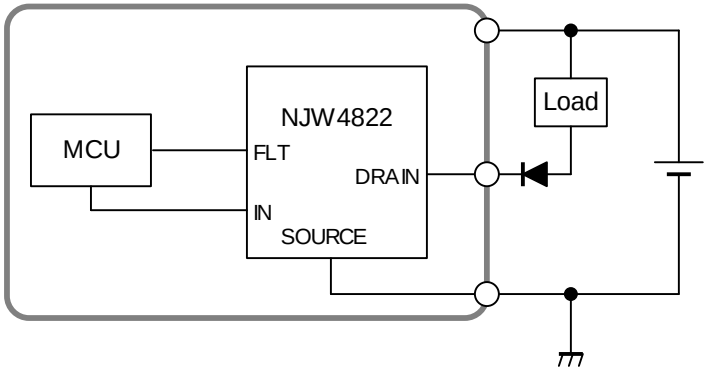
[A-version: Active-high]



[B-version: Active-low]



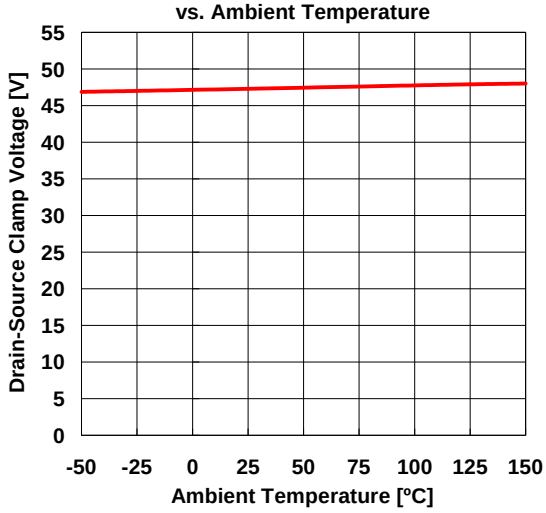
## ■ TYPICAL APPLICATION



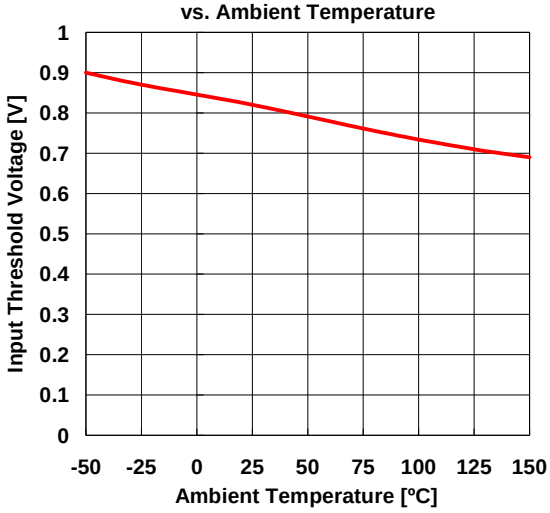

You should insert a pull-up resistor when you connect the FLT pin with other power supplies etc.

## ■ CHRACTERISTICS

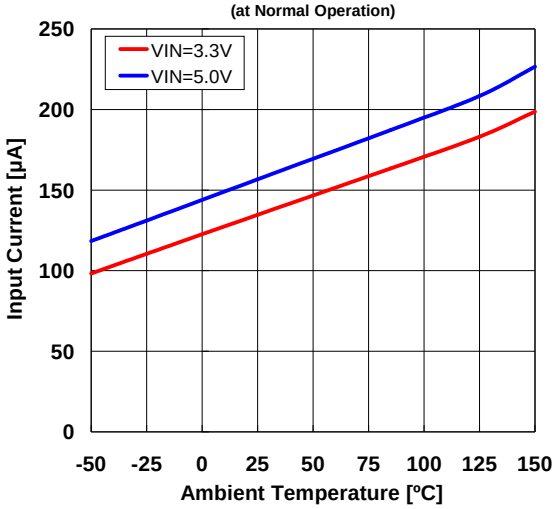
Drain-Source Clamp Voltage vs. Ambient Temperature



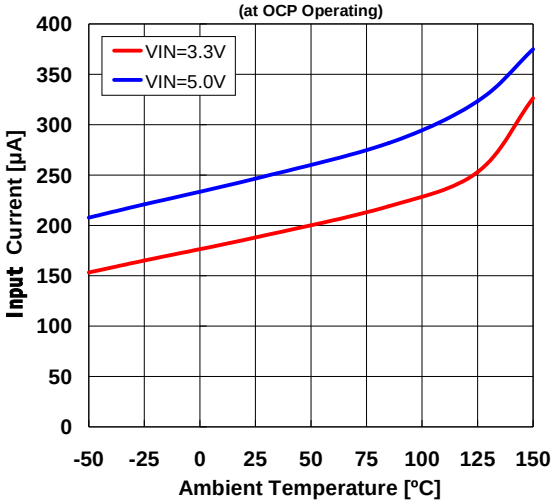

Input Threshold Voltage vs. Ambient Temperature



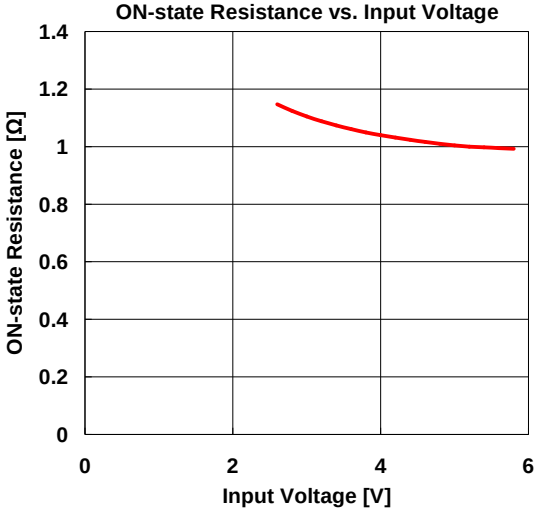

Input Current vs. Ambient Temperature (at Normal Operation)



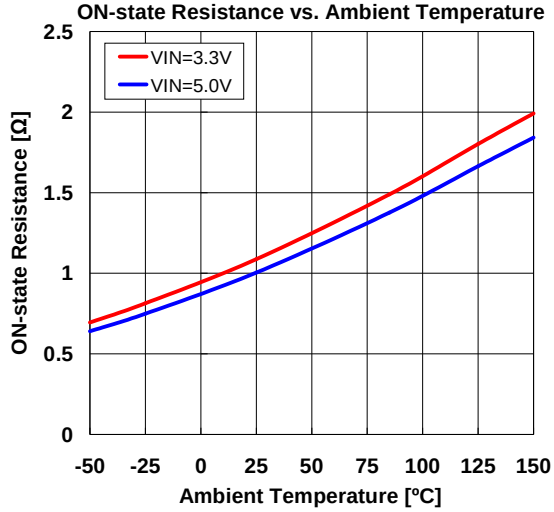

Input Current vs. Ambient Temperature (at OCP Operating)



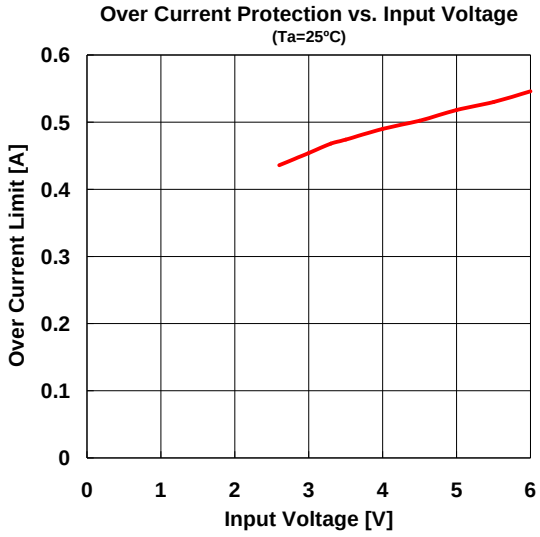

ON-state Resistance vs. Input Voltage

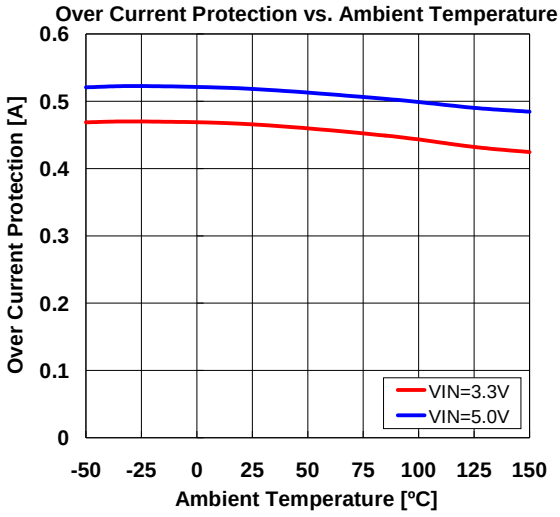


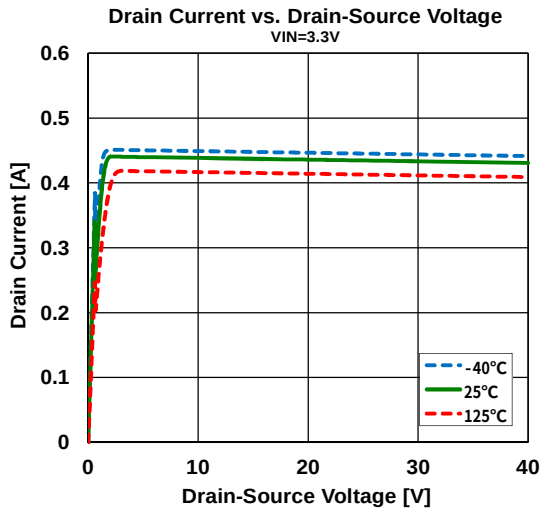

ON-state Resistance vs. Ambient Temperature

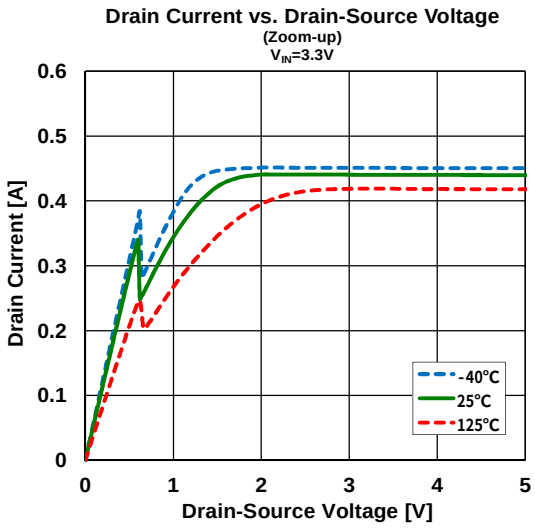


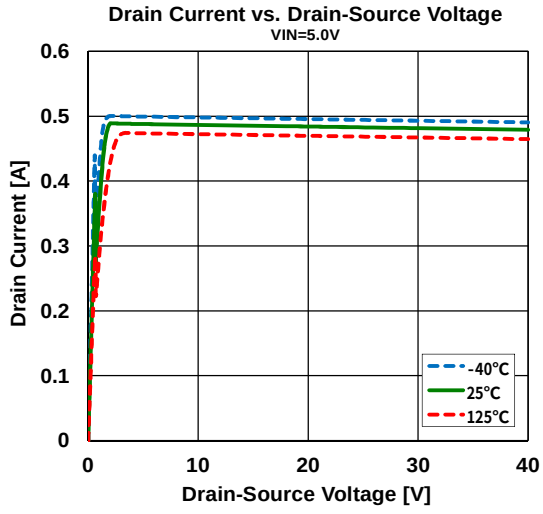
## ■ CHARACTERISTICS

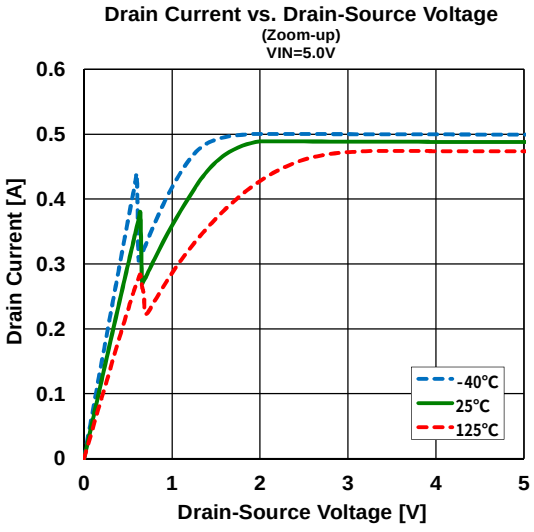


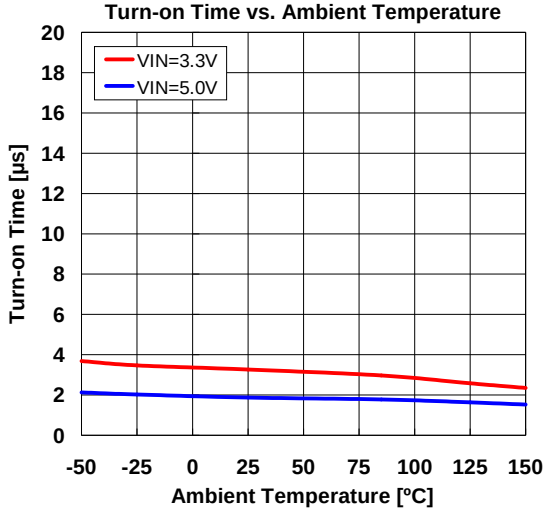



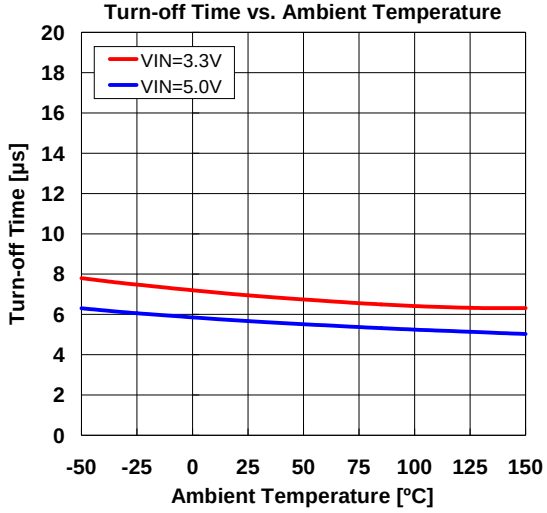



## ■ CHARACTERISTICS

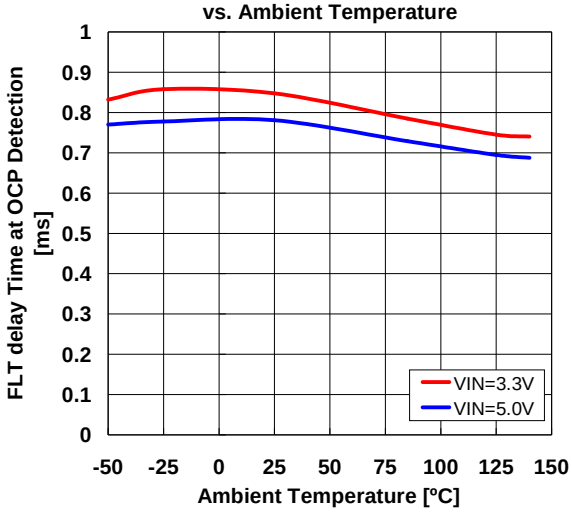
Turn-on Time vs. Ambient Temperature



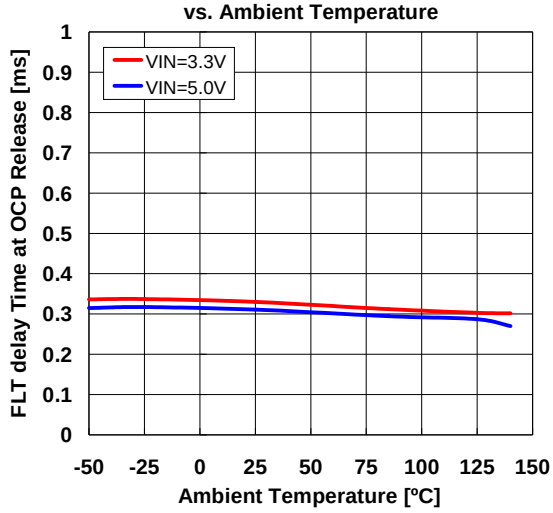

Turn-off Time vs. Ambient Temperature



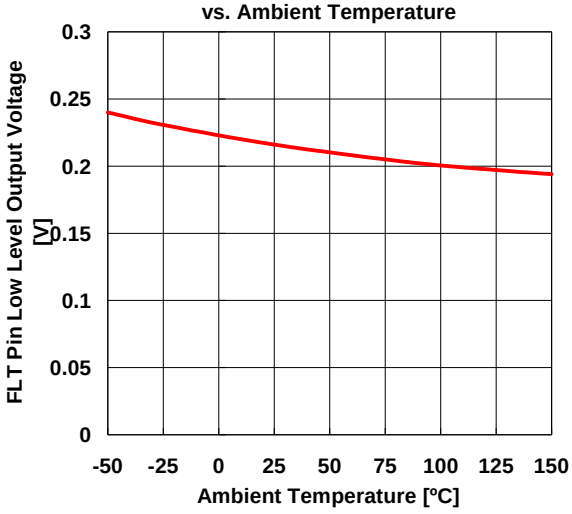

FLT delay Time at OCP Detection vs. Ambient Temperature



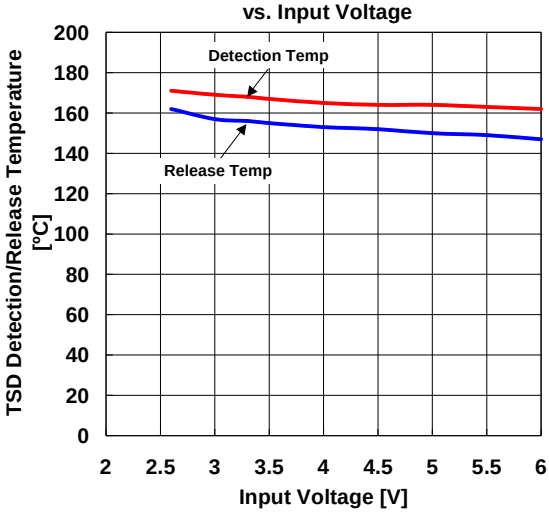

FLT delay Time at OCP Release vs. Ambient Temperature




FLT Pin Low Level Output Voltage vs. Ambient Temperature




TSD Detection/Release Temperature vs. Input Voltage



## ■ Regarding Active Clamp Capacity of High/Low side Switch Products

● What is “Active Clamp Capacity”.

The IC might suffer to damage by the inductive kickback at the transient time of ON state to OFF state, when an inductive load such as a solenoid or motor is used for the load of the high-side/low-side switch.

The protection circuit for the inductive kickback is the active clamp circuit. The energy that can be tolerated by the active clamp circuit is called "Active Clamp Capacity ($E_{AS}$)".

When using an inductive load to the high-side/low-side switch, you should design so that the $E_{SW}$ does not exceed the active clamp capability.

- IC operation without an external protection parts (Fig 1)

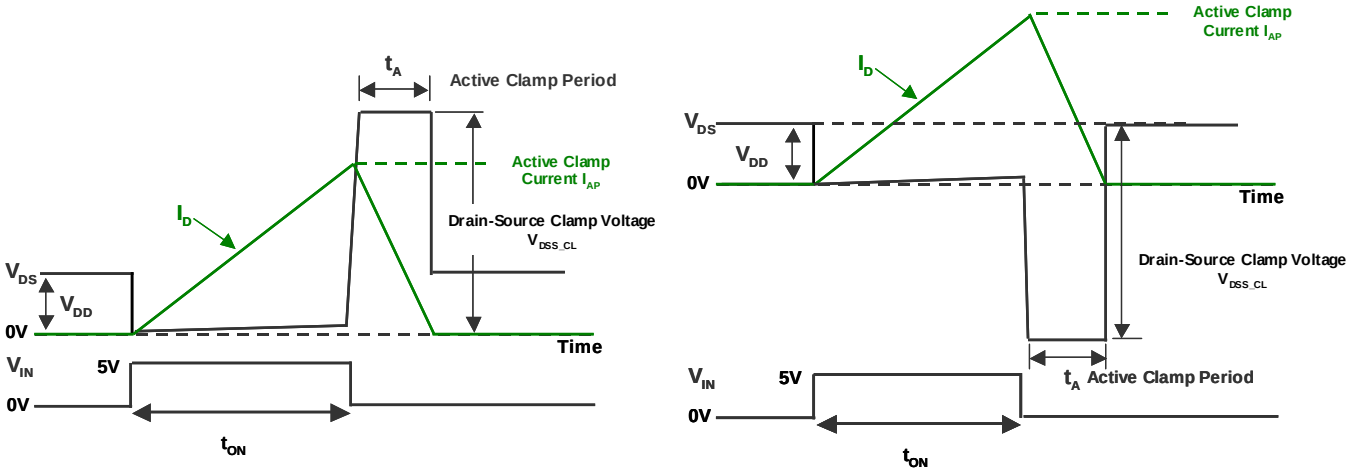



Fig1. Active Clamp Waveform (Left: Low-side Switch / Light High-side Switch)

At when the $V_{IN}$ turns off, the drain-source voltage ($V_{DS}$) increases rapidly by the behavior of the inductive load that is keeping current flowing. However, it will be clamped at $V_{DSS\_CL}$ by the active clamp circuit. At the same time, the drain current is flowed by adjusting the gate voltage of the output transistor, and the energy is dissipated at the output transistor. The energy: $E_{SW}$ is shown by the following formula.

$$E_{SW} = \int_0^{t_A} V_{DS}(t) \cdot I_D(t)dt = \frac{1}{2} L I_{AP}^{\ 2} \cdot \frac{V_{DSS\_CL}}{V_{DSS\_CL} - V_{DD}}$$

The $E_{SW}$ is consumed inside IC as heat energy. However, the thermal shutdown does not work when the $V_{IN}$ is 0V. Therefore in worst case the IC might break down. When using the active clamp, you should design $E_{SW}$ does not exceed the $E_{AS}$.

- Application Hint

The simplest protection example is to add an external flywheel diode at the load to protect IC from an inductive kickback. (Fig.2)

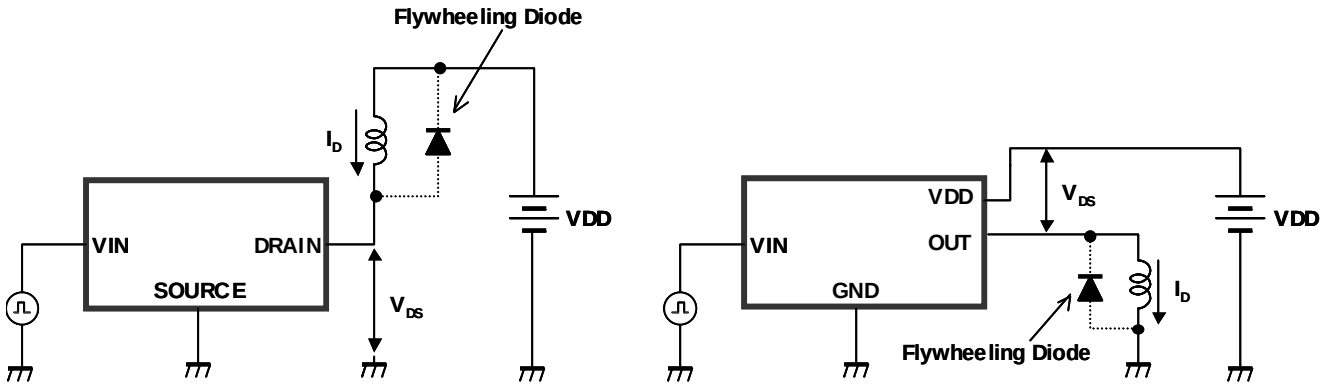
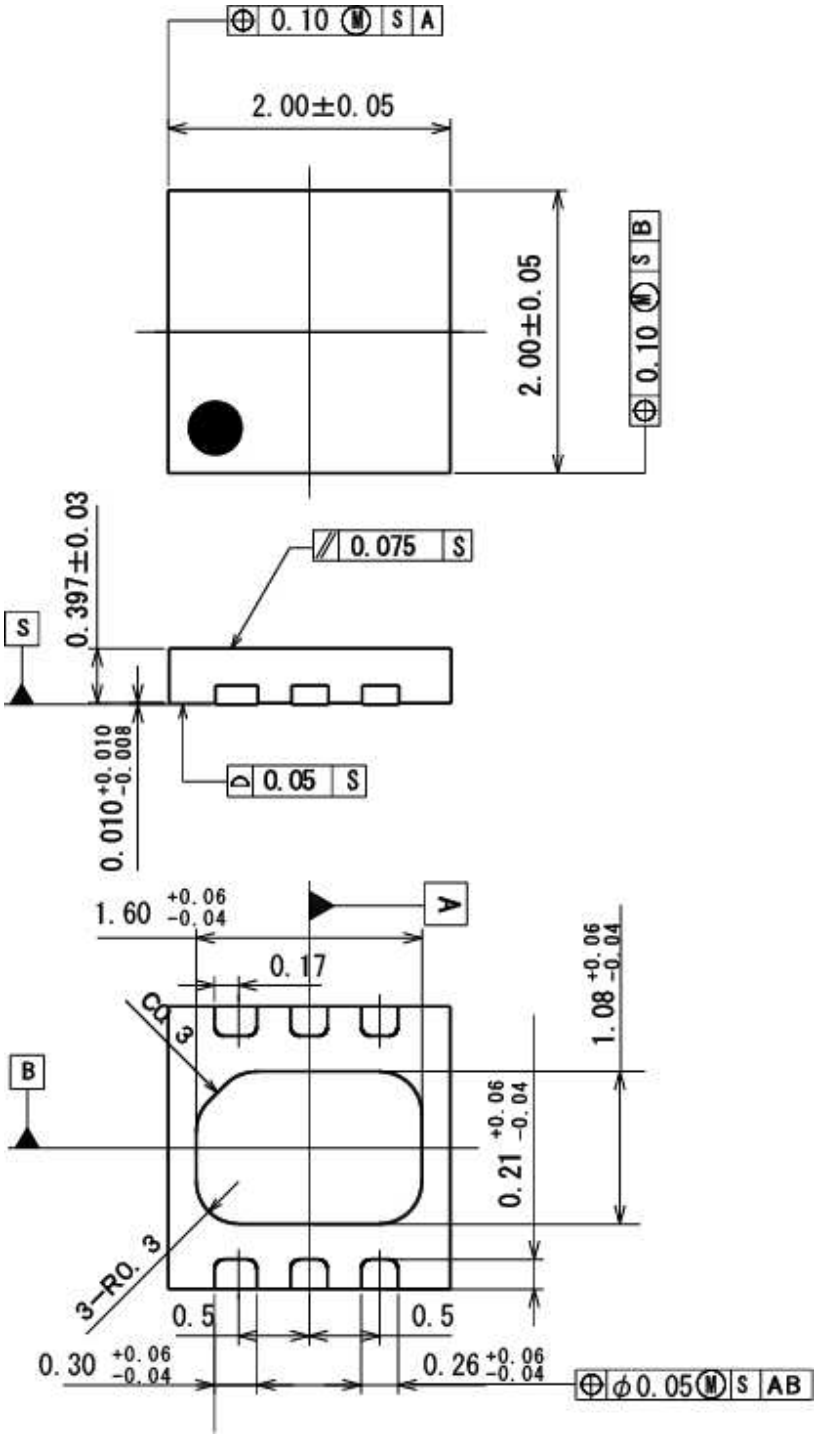



Fig 2. Application Circuit of Inductance Load Driving (Left: Low-side Switch / Light High-side Switch)

■ **PACKAGE OUT LINE**




GD-N00602A-0

UNIT: mm

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