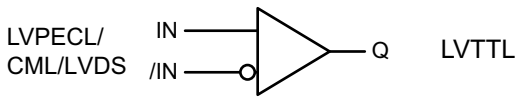
FEATURES

- 3.3V power supply
- 1.9ns typical propagation delay
- 275MHz f_{MAX}
- Differential LVPECL/CML/LVDS inputs
- 24mA LVTTL outputs
- Flow-through pinouts
- Internal input resistors: pulldown on IN, pulldown and pullup on /IN
- Q output will default LOW with inputs open
- V_{BB} output
- Available in ultra-small 8-pin MLF® (2mm x 2mm) package

BLOCK DIAGRAM



Precision Edge®

DESCRIPTION

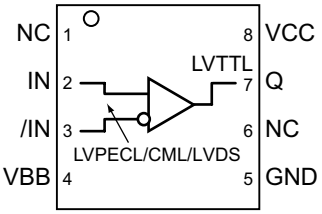
The SY89321L is a differential LVPECL/CML/LVDS-to-LVTTL translator requiring only a single +3.3V power. The SY89321L is functionally equivalent to the SY100EPT21L, but in an ultra-small 8-pin MLF® package that features a 70% smaller footprint. This ultra-small package and low skew single gate design make the SY89321L ideal for applications that require the translation of a clock or data signal where minimal space, low power and low cost are critical.

V_{BB} allows a differential, single-ended, or AC-coupled interface to the device. If used, the V_{BB} output should be bypassed to V_{CC} with 0.01µF capacitor.

Under open input conditions, the /IN will be biased at a $V_{CC}/2$ voltage level and the IN input will be pulled to ground. This condition will force the Q output low to provide added stability.

The SY89321L is compatible with positive ECL 100k logic levels.

PACKAGE/ORDERING INFORMATION



8-Pin MLF®
Ultra-Small Outline (2mm x 2mm)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89321LMITR	MLF-8	Industrial	321	Sn-Pb
SY89321LMGTR(1)	MLF-8	Industrial	321 with Pb-Free bar-line indicator	Pb-Free NiPdAu

Note:

1. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Type	Pin Function
1,6	NC		No connection.
2	IN	100K LVPECL/ CML/LVDS Input	Differential PECL/CML/LVDS Input: Internal 75kΩ pull-down resistor. If left open, piN defaults LOW. Q output will be LOW. See “Input Interface Applications” section for CML, LVDS and single-ended inputs.
3	/IN	100K LVPECL/ CML/LVDS Input	Differential PECL/CML/LVDS Input: Internal 75kΩ pull-up and pull-down resistors. If left floating, pin defaults to $V_{CC}/2$. When not used, this input can be left open. See “Input Interface Applications” section for CML, LVDS and single-ended inputs.
4	VBB	Reference Voltage Output	Bias Reference Voltage: V_{CC}–1.3V. Used as reference voltage for single-ended inputs or AC-coupling to the IN, /IN inputs. Limit sink / source ≤ 0.5mA.
5	GND, Exposed Pad	Ground	GND and Exposed pad must be tied to ground plane.
7	Q	LVTTL Output	Single-ended LVTTL Output: Defaults to LOW if IN inputs left open.
8	VCC	Positive Power Supply	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC}) ..... –0.5V to +3.8V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVTT Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Current (V_{BB})
  Source or sink current on V_{BB}, **Note 3** ..... ±1.5mA
Lead Temperature (soldering, 20 sec.) ..... +260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings(Note 2)

Supply Voltage (V_{CC}) ..... 3.0V to 3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance, **Note 4**
MLF® (θ_{JA})
  Still-Air ..... 93°C/W
  500lfpm ..... 87°C/W
MLF® (Ψ_{JB})
  Junction-to-Board ..... 60°C/W

LVTTL DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±10%

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, **Note 5**	–80	—	–275	mA
I_{CC}	Power Supply Current		—	14	20	mA
V_{OH}	Output HIGH Voltage	I_{OH} = –3.0mA	2.0	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 24mA	—	—	0.5	V

LVPECL/CML/LVDS DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±10%; T_A = –40°C to +85°C unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH_LVPECL}	Input HIGH Voltage		V_{CC}–1.165	—	V_{CC}–0.880	V
V_{IL_LVPECL}	Input LOW Voltage		V_{CC}–1.810	—	V_{CC}–1.475	V
V_{BB}	Bias Voltage		V_{CC}–1.38	V_{CC}–1.32	V_{CC}–1.26	V
V_{IH_CML}	Input HIGH Voltage		V_{CC}–0.400	—	V_{CC}	V
V_{IL_CML}	Input LOW Voltage		V_{CC}–0.800	—	V_{IH}–0.400	V
V_{IH_LVDS}	Input HIGH Voltage		1.4	—	1.5	V
V_{IL_LVDS}	Input LOW Voltage		1.1	—	1.2	V
I_{IH}	Input HIGH Current		—	—	150	µA
I_{IL}	Input LOW Current IN		0.5	—	—	µA
	Input LOW Current /IN		–300	—	—	µA

Note 1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Due to the limited drive capability use for input of the same package only.

Note 4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential (GND) on the PCB.

Note 5. Max. limit only applicable for short durations, not for continuous operation!

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±10%; C_L = 20pF, T_A = –40°C to +85°C unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Input Frequency	**Note 6**	275	—	—	MHz
t_{pd}	Propagation Delay		1.5	1.9	2.5	ns
t_{skpp}	Part-to-Part Skew	$V_{IN} \geq$ 100mV, **Note 7**	—	—	0.5	ns
V_{CMR}	Common Mode Range		1.2	—	V_{CC}	V
V_{PP}	Minimum Peak-to-Peak Input	**Note 8**	100	—	—	mV
t_r t_f	Output Rise/Fall Time (1.0V to 2.0V)		0.5	—	1.0	ns
t_{JITTER}	Cycle-to-cycle (rms)	**Note 9**			2	ps_{RMS}
	Total jitter (pk-pk)	**Note 10**			15	ps_{PP}

Note 6. The f_{MAX} value is specified as the minimum guaranteed maximum frequency (While maintaining TTL swing of 0.8V to 2.0V). Actual operational maximum frequency may be greater.

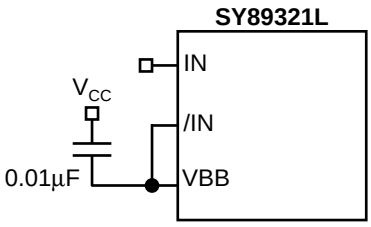
Note 7. Part-to-Part Skew considering HIGH-to-HIGH transitions at common V_{CC} level.

Note 8. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed.

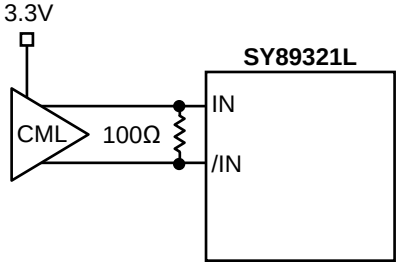
Note 9. Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles, $T_n - T_{n-1}$,where T is the time between rising edges of the output signal.

Note 10. Total jitter definition: with an ideal clock input of frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edge will deviate by more than the specified peak-to-peak jitter value.

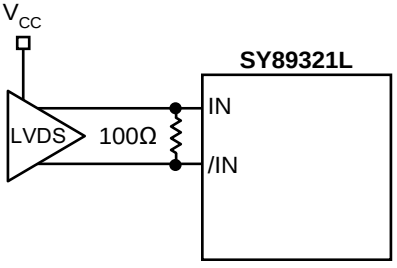
INPUT INTERFACE APPLICATIONS



Single-Ended Input
(Terminating unused input)

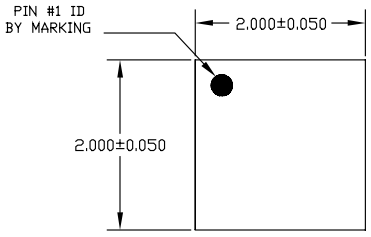


CML Input

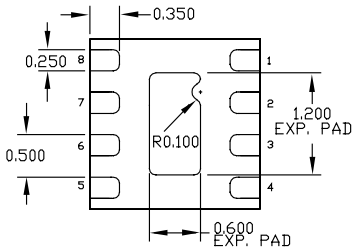


LVDS Input

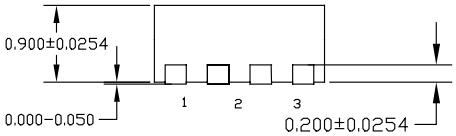
8 LEAD ULTRA-SMALL EPAD-*Micro*LeadFrame® (MLF-8)



TOP VIEW

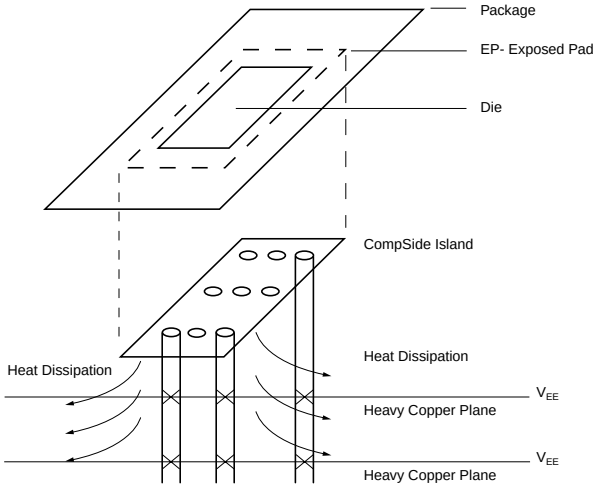


BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 8-Pin MLF® Package

Package Notes:

Note 1. Package meets Level 2 qualification.

Note 2. All parts are dry-packaged before shipment.

Note 3. Exposed pads must be soldered to a ground for proper thermal management.

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