

Electronic Line Switch

Features

- ▶ 15Ω maximum switch resistance
- ▶ Current limiting protection
- ▶ 4 logic control inputs
- ▶ Operates at 2.0V input
- ▶ 2.0μA maximum quiescent current at 100V

Applications

- ▶ Telephone handsets
- ▶ Fax machines
- ▶ Answering machines
- ▶ Auto-dial alarm systems

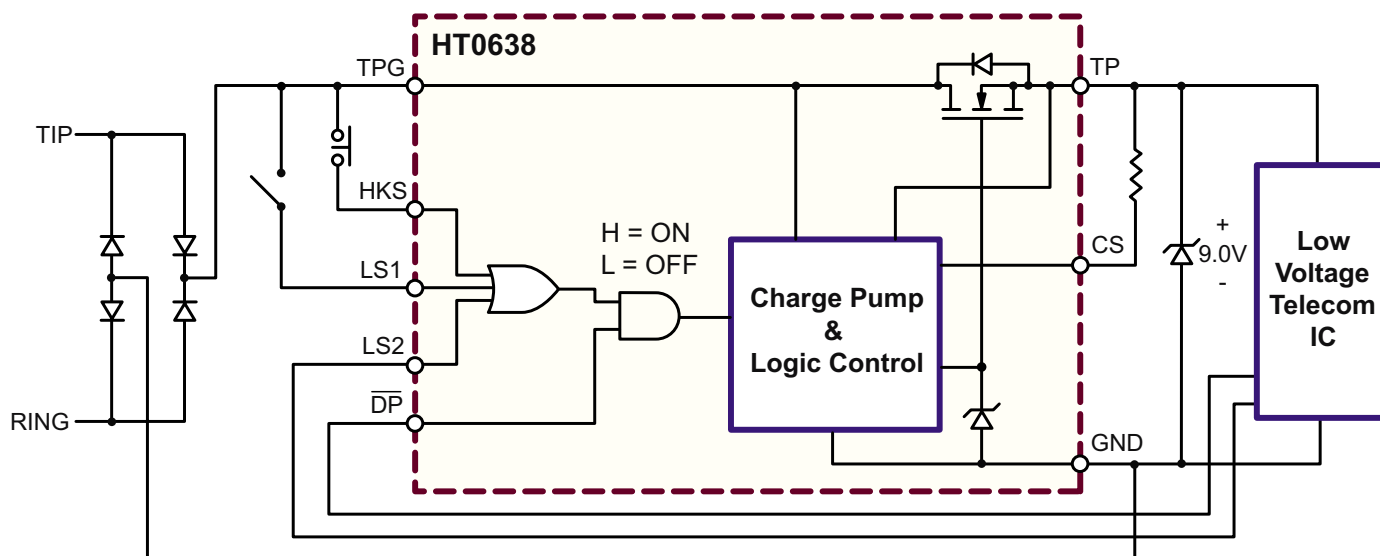
General Description

The Supertex HT0638 is an integrated, electronic line switch controllable from four logic-level inputs. This device is intended as a replacement for mechanical hook switches and relays in telephones, answering machines, and similar telecommunications equipment. It switches the positive (TIP) side of the telephone line using control inputs that are referenced to the negative (RING) side of the line. In the off state, it can hold-off 375V. In the on state, the series resistance is 15Ω maximum. This device provides adjustable current limiting via an external sense resistor. Three of the control inputs are general purpose and one is an override input that forces the switch to an off state regardless of the state of the other inputs. This override input is useful for 'flash' and pulse dialing purposes. Internal pull-up/down resistors allow the inputs to be driven from single-ended sources, push-pull sources, or left unconnected.

The HT0638 is powered by the telephone line, and so it is especially useful in applications where external power is not available. Due to its low quiescent current, this device exceeds the on-hook resistance requirements of the telecom standard EIA-470-A.

For additional information, refer to application note AN-H32.

Typical Application Circuit



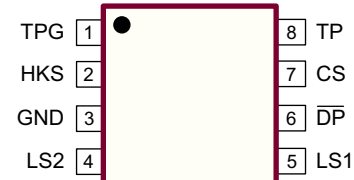
Ordering Information

Device	Package Option
	8-Lead SOIC (Narrow Body) 4.90x3.90mm body 1.75mm height (max) 1.27mm pitch
HT0638	HT0638LG-G

-G indicates package is RoHS compliant ("Green")



Pin Configuration



8-Lead SOIC (Narrow Body) (LG)
(top view)

Absolute Maximum Ratings

Parameter	Value
V_{TPG} , Input line voltage	+375V
V_{TP} , Output line voltage	+18V
HKS continuous input voltage	V_{TPG}
LS1, LS2 continuous input voltage	+20V
\overline{DP} continuous input voltage	+5V
Storage temperature	-65°C to +150°C
Soldering temperature*	300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* Distance of 1.6mm from case for 10 seconds.

Product Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC (Narrow Body) (LG)

Electrical Characteristics ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{TPG}	High voltage positive supply	-	-	375	V	$I_{TP} = 10\mu\text{A}$, HKS, LS1, LS2, \overline{DP} = open circuit
I_{TPQ}	Input leakage current	-	-	2.0	μA	$V_{TPG} = 100\text{V}$, HKS, LS1, LS2, \overline{DP} = open circuit
		-	-	10		$V_{TPG} = 375\text{V}$, HKS, LS1, LS2, \overline{DP} = open circuit
V_{TP}	Output voltage	16	18	20	V	$V_{TPG} = 50\text{V}$, No Load
R_{SW}	TPG to TP switch resistance	-	-	15	Ω	$V_{TPG} = 4.3\text{V}$, $I_{TPG} = 180\text{mA}$, SW = ON
		-	-	15		$V_{TPG} = 3.0\text{V}$, $I_{TPG} = 20\text{mA}$, SW = ON, $T_A = 0^\circ\text{C}$ to 50°C
		-	-	30		$V_{TPG} = 2.0\text{V}$, $I_{TPG} = 5.0\text{mA}$, SW = ON, $T_A = 0^\circ\text{C}$ to 50°C
$I_{TPG} - I_{TP}$	Bias current	-	-	50	μA	$V_{TPG} = 5.0\text{V}$, SW = ON
		-	-	100		$V_{TPG} = 10\text{V}$, SW = ON
I_{LIM}	I_{TPG} current limiting	200	-	300	mA	$R_{EXT} = 430\Omega$
I_{HKS}	HKS input current	-	-	200	μA	$V_{HKS} = 50\text{V}$
I_{LS1}	LS1 input current	-	-	136	μA	$V_{LS1} = 3.0\text{V}$, $V_{DP} = 0\text{V}$
I_{LS2}	LS2 input current	-	-	136	μA	$V_{LS2} = 3.0\text{V}$, $V_{DP} = 0\text{V}$
I_{DP}	\overline{DP} output current	-	-	500	μA	$V_{DP} = 0\text{V}$, $V_{HKS} = 50\text{V}$, $V_{LS1} = V_{LS2} = 3.0\text{V}$
$V_{IL(HKS)}$	HKS input low	0	-	0.2	V	---
$V_{IH(HKS)}$	HKS input high	2.0	-	V_{TPG}	V	---

Electrical Characteristics (cont.)

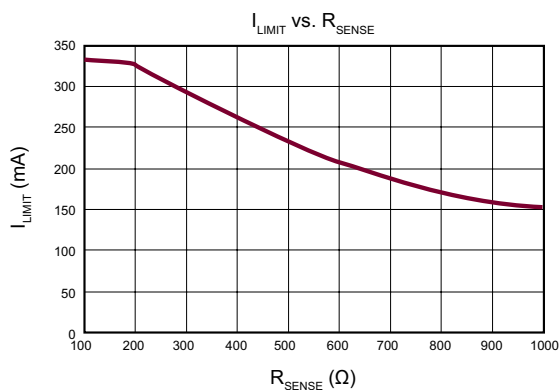
Sym	Parameter	Min	Typ	Max	Units	Conditions
$V_{IL(LS1)}$ $V_{IL(LS2)}$	LS1 and LS2 input low	0	-	0.2	V	---
$V_{IH(LS1)}$ $V_{IH(LS2)}$	LS1 and LS2 input high	1.0	-	20	V	---
$V_{IL(DP)}$	\overline{DP} input low	0	-	0.2	V	---
$V_{IH(DP)}$	\overline{DP} input high	1.0	-	5.0	V	---
T_{ON}	Turn on time	-	-	1.0	ms	$V_{TPG} = 4.5V$
T_{OFF}	Turn off time	-	-	1.0	ms	$V_{TPG} = 4.5V$

Logic Truth Table

HKS	LS1	LS2	\overline{DP}	Switch State
X	X	H	H or Z	ON
X	H	X	H or Z	ON
H	X	X	H or Z	ON
L or Z	L or Z	L or Z	X	OFF
X	X	X	L	OFF

Z = high impedance, open circuit, X = don't care, L = logic, level low, H = logic level high.

Typical Performance Curve

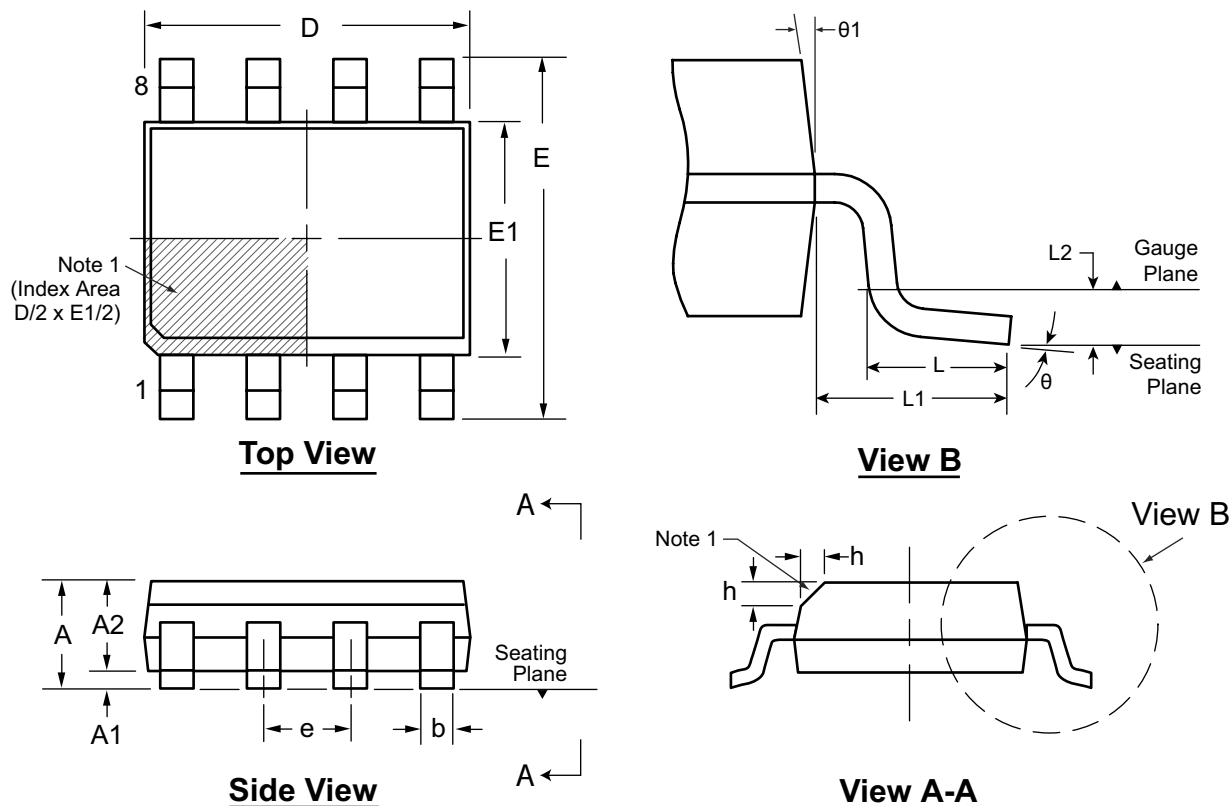


Pin Description

Pin	Name	Description
1	TPG	Positive input side of a telephone line, typically tip side.
2	HKS	Hookswitch input. Connect HKS to TPG to turn on the electronic switch. Internally pulled low.
3	GND	Device ground. Negative side of a telephone line, typically ring side.
4	LS2	Line switch 2 input. Positive input turns on the electronic switch. Internally pulled low.
5	LS1	Line switch 1 input. Positive input turns on the electronic switch. Internally pulled low.
6	\overline{DP}	Dial pulse input. A low input turns off the electronic switch. Use for pulse dialing. Internally pulled high.
7	CS	Current sense input. An external resistor connected between CS and TP sets the current limit. Short CS to TP if current limiting is not used.
8	TP	Positive output side of a telephone line.

8-Lead SOIC (Narrow Body) Package Outline (LG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note:
 1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ_1	
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

Supertex Doc. #: DSPD-8SOLGTG, Version I041309.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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