ZL40235

Low Skew, Low Additive Jitter, 3 x 5 LVPECL/LVDS/ HCSL Fanout Buffer with One LVCMOS Output

Features

- 3-to-1 Input Multiplexer: Two Inputs Accept Any Differential (LVPECL, HCSL, LVDS, SSTL, CML, LVCMOS) or a Single-Ended Signal and the Third Input Accepts a Crystal or a Single-Ended Signal
- Five Differential LVPECL/LVDS/HCSL Outputs
- One LVCMOS Output
- Ultra-Low Additive Jitter: 24 fs (Integration Band: 12 kHz to 20 MHz at 625 MHz Clock Frequency)
- Supports Clock Frequencies from 0 to 1.6 GHz
- Supports 2.5V or 3.3V Power Supplies for LVPECL/LVDS/HCSL Outputs
- Supports 1.5V, 1.8V, 2.5V, or 3.3V Power Supplies for LVCMOS Output
- Embedded Low Dropout (LDO) Voltage Regulator Provides Superior Power Supply Noise Rejection
- Maximum Output to Output Skew of 40 ps
- Device Controlled via SPI or Hardware Pins

Applications

- PCIe Gen1/2/3/4/5/6 Clock Distribution
- Low-Jitter Clock Trees
- Logic Translation
- Clock and Data Signal Restoration
- Wired Communications: OTN, SONET/SDH, GE, 10GE, FC and 10G FC
- General Purpose Clock Distribution
- Wireless Communications
- High Performance Microprocessor Clock Distribution
- Test Equipment

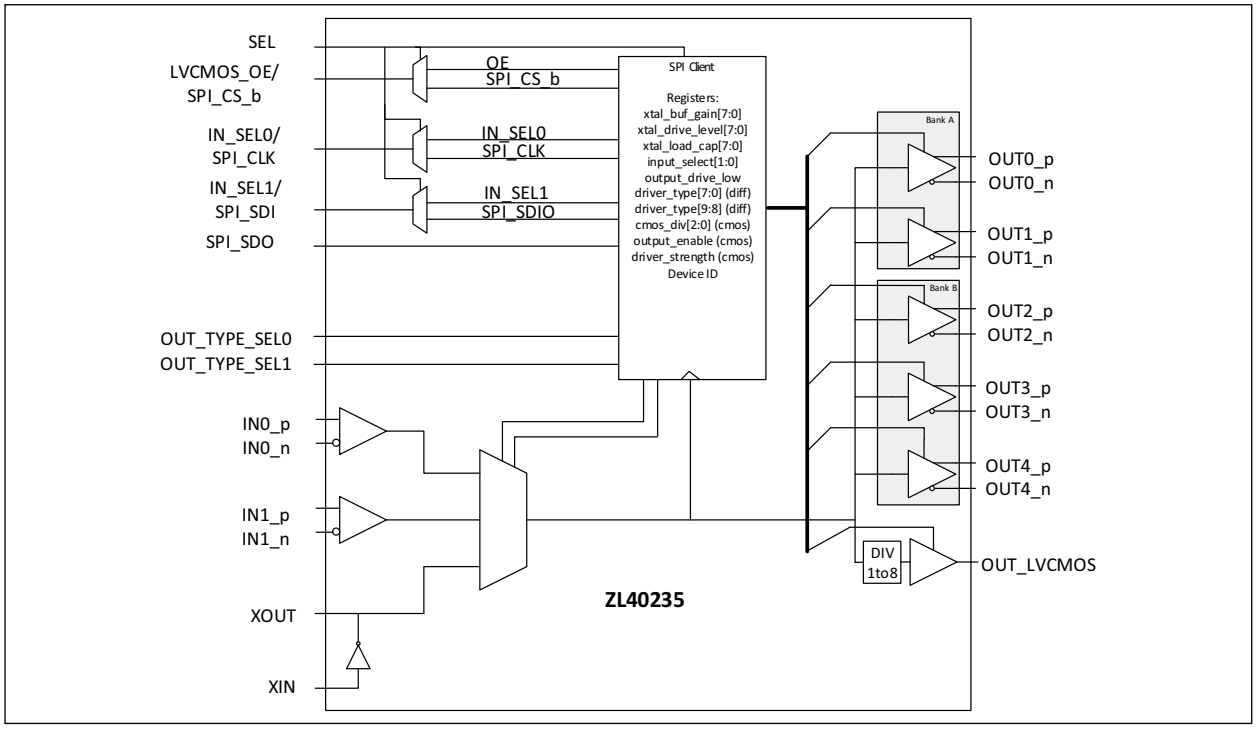

FIGURE 0-1: *Functional Block Diagram.*

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1.0 PIN DESCRIPTION AND CONFIGURATION

The ZL40235 is packaged in a 6 mm x 6 mm, 40-lead VQFN.

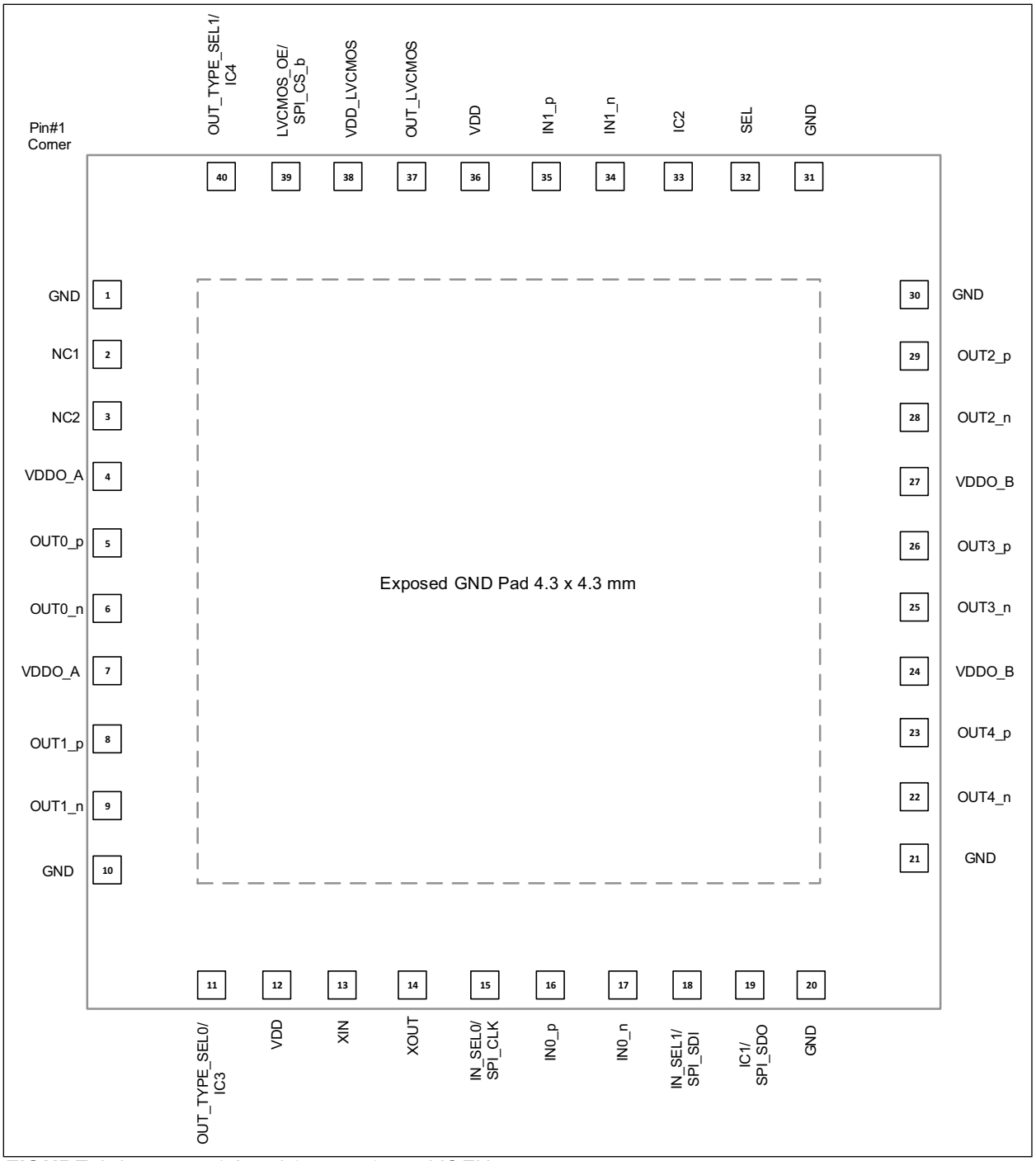


FIGURE 1-1: *40-Lead 6 mm x 6 mm VQFN.*

1.1 Pin Descriptions

All device inputs and outputs are LVPECL unless described otherwise. The I/O column uses the following symbols: I – input, I_{PU} – input with 300 kΩ internal pull-up resistor, I_{PD} – input with 300 kΩ internal pull-down resistor, I_{APU} – input with 31 kΩ internal pull-up resistor, I_{APD} – input with 30 kΩ internal pull-down resistor, $I_{APU/APD}$ – input with 60 kΩ internal pull-up and pull-down resistors (30 kΩ equivalent), O – output, I/O – Input/Output pin, NC – No connect, P – power supply pin.

TABLE 1-1: PIN DESCRIPTION

Pin Number	Pin Name	Type	Description
Input Reference			
16	IN0_p	I_{APD}	**Input Differential or Single-Ended References 0 and 1** Input frequency range 0 Hz to 1.6 GHz. Non-inverting inputs (_p) are pulled down with internal 30 kΩ pull-down resistors. Inverting inputs (_n) are biased at $V_{DD}/2$ with 60 kΩ pull-up pull-down resistors to keep inverting input voltages at $V_{DD}/2$ when inverting inputs are left floating (device fed with a single-ended reference).
17	IN0_n	$I_{APU/APD}$	
35	IN1_p	I_{APD}	
34	IN1_n	$I_{APU/APD}$	
Output Clocks			
5	OUT0_p	O	**Ultra-Low Additive Jitter Differential LVPECL/HCSL/LVDS Outputs 0 to 4** Output frequency range 0 Hz to 1.6 GHz In SPI bus controlled mode (SEL pin pulled high on the power up) type (LVPECL/HCSL/LVDS/High-Z) of each output is programmable via SPI bus. In Hardware control mode (SEL pin pulled low on the power up) type (LVPECL/HCSL/LVDS/High-Z) of each output bank is controlled via OUTA/B_TYPE_SEL0/1 pins.
6	OUT0_n		
8	OUT1_p		
9	OUT1_n		
29	OUT2_p		
28	OUT2_n		
26	OUT3_p		
25	OUT3_n		
23	OUT4_p		
22	OUT4_n		
37	OUT_LVCMOS	O	**Ultra-Low Additive Jitter LVCMOS Output** Output frequency range 0 Hz to 250 MHz

TABLE 1-1: PIN DESCRIPTION (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">Control</td></tr>
<tr><td>32</td><td>SEL</td><td>I_{PD}</td><td>Select control.
When this pin is low, the device is controlled via hardware pins, IN_SEL0/1 and OE.
When this pin is high, the device is controlled via SPI port.

Any change of SEL pin value requires power cycle. Hence, SEL pin cannot be changed on the fly.</td></tr>
<tr><td rowspan="6">15</td><td rowspan="6">IN_SEL0/
SPI_SCL</td><td rowspan="6">I_{PD}
or
I_{PU}</td><td>Input Select 0 or Clock for Serial Interface. When SEL pin is low, this pin is Input Select 0 hardware control input pin and it is pulled down with a 300 kΩ resistor. When SEL pin is high, this pin provides clock for serial micro-port interface and it is pulled up with a 300 kΩ resistor.</td></tr>
<tr><td>IN_SEL1 | IN_SEL0 | OUTN</td></tr>
<tr><td>0 | 0 | Input 0 (IN0)</td></tr>
<tr><td>0 | 1 | Input 1 (IN1)</td></tr>
<tr><td>1 | 0 | Crystal Oscillator or Overdrive</td></tr>
<tr><td>1 | 1 | Crystal Bypass</td></tr>
<tr><td>18</td><td>IN_SEL1/
SPI_SDI</td><td>I_{PD}
or
I_{PU}</td><td>Input Select 1 or Serial Interface Input. When SEL pin is low, this pin is Input Select 1 hardware control pin and it is pulled down with a 300 kΩ resistor. When SEL pin is high, this pin is serial interface input stream and it is pulled up with a 300 kΩ resistor. The serial data stream holds the access command, the address and the write data bits.</td></tr>
<tr><td>19</td><td>IC1/
SPI_SDO</td><td>I/O</td><td>Internal Connection 1 or Serial Interface Output.
When SEL pin is low, this pin is in an internal connection. Leave open.

When SEL pin is high, this pin is the Serial Interface Output stream. As an output, the serial stream holds the read data bits.</td></tr>
<tr><td>33</td><td>IC2</td><td>I_{PD}</td><td>Internal Connection 2
This pin should be left open.</td></tr>
<tr><td>39</td><td>LVCMOS_OE/
SPI_CS_b</td><td>I_{PD}
or
I_{PU}</td><td>LVCMOS Output Enable or Chip Select for Serial Interface.
When SEL pin is low, this pin is LVCMOS Output Enable hardware control input and it is pulled down with 300 kΩ resistor.
When SEL pin is high, this pin is serial interface chip select and it is pulled up with 300 kΩ resistor. This is an active-low signal.</td></tr>
<tr><td rowspan="7">11
40</td><td rowspan="7">OUT_TYPE_SEL0/
IC3
OUT_TYPE_SEL1/
IC4</td><td rowspan="7">I_{PD}</td><td>Output Signal Type
When SEL pin is low, these two pins select the type for all outputs.</td></tr>
<tr><td>OUT_TYPE_SEL1 | OUT_TYPE_SEL0 | Output 0 to 4</td></tr>
<tr><td>0 | 0 | LVPECL</td></tr>
<tr><td>0 | 1 | LVDS</td></tr>
<tr><td>1 | 0 | HCSL</td></tr>
<tr><td>1 | 1 | High-Z (Disabled)</td></tr>
<tr><td>When SEL pin is high, these two pins are unused and should be left unconnected.</td></tr>
<tr><td colspan="4">Crystal Oscillator</td></tr>
<tr><td>13</td><td>XIN</td><td>I</td><td>Crystal Oscillator Input or Crystal Bypass Mode or Crystal Overdrive Mode
If a crystal oscillator is not used, pull down to this pin or connect it to ground.</td></tr>
<tr><td>14</td><td>XOUT</td><td>O</td><td>Crystal Oscillator Output</td></tr>
</table>

TABLE 1-1: PIN DESCRIPTION (CONTINUED)

Pin Number	Pin Name	Type	Description
No Connect			
2 3	NC1 NC2	NC	**No Connect (not connected to the die)** Leave unconnected or connect to GND for mechanical support.
Power and Ground			
12 36	VDD	P	**Positive Supply Voltage.** Connect to 3.3V or 2.5V supply.
4 7	VDDO_A	P	**Positive Supply Voltage for Differential Outputs Bank A** Connect to 3.3V or 2.5V power supply. VDDO_A does not have to be connected to the same voltage level as VDD or VDDO_B. These pins power up differential outputs OUT0_p/n and OUT1_p/n..
24 27	VDDO_B	P	**Positive Supply Voltage for Differential Outputs Bank B** Connect to 3.3V or 2.5V power supply. VDDO_B does not have to be connected to the same voltage level as VDD or VDDO_A. These pins power up differential outputs OUT2_p/n, OUT3_p/n and OUT4_p/n.
38	VDD_LVCMOS	P	**Positive Supply Voltage for LVCMOS Output** Connect to 3.3V, 2.5V, 1.8V, or 1.5V power supply.
1 10 20 21 30 31	GND	P	**Ground.** Connect to ground.
ePad	GND	P	**Ground.** Connect to ground.

NOTES:

2.0 FUNCTIONAL DESCRIPTION

The ZL40235 is a programmable or hardware pin controlled low additive jitter, low power 3 x 5 LVPECL/HCSL/LVDS fanout buffer.

Two inputs can accept signal in differential (LVPECL, SSTL, LVDS, HSTL, CML) or single-ended (LVPECL or LVCMOS) format and the third input can accept a single-ended signal or it can be used to build a crystal oscillator by connecting an external crystal resonator between its XIN and XOUT pins. All the other components for building crystal oscillator are built into the device such as load capacitance, series, and shunt resistors.

The ZL40235 has five LVPECL/HCSL/LVDS outputs that can be powered from 3.3V or 2.5V supply. Each output can be independently enabled/disabled via SPI bus. The type of each output driver can be programmed to be LVPECL, HCSL or LVDS. Hence, the device can be configured to support applications where different signal formats are needed.

The device operates from 2.5V±5% or 3.3V±5% supply. Its operation is ensured over the industrial temperature range of –40°C to +85°C.

2.1 Clock Inputs

The following blocks diagram shows how to terminate different signals fed to the ZL40235 inputs.

Figure 2-1 shows how to terminate a single ended output such as LVCMOS. Resistors Ideally, resistors R1 and R2 should be 100Ω each and $R_O + R_S$ should be 50Ω so that the transmission line is terminated at both ends with characteristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor R_S should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (Table 5-4). The source resistors of R_S = 270Ω could be used for standard LVCMOS driver. This will provide 516 mV of voltage swing for 3.3V LVCMOS driver with load current of (3.3V/2) x (1/(270Ω + 50Ω)) = 5.16 mA.

For optimum performance both differential input pins (_p and _n) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.

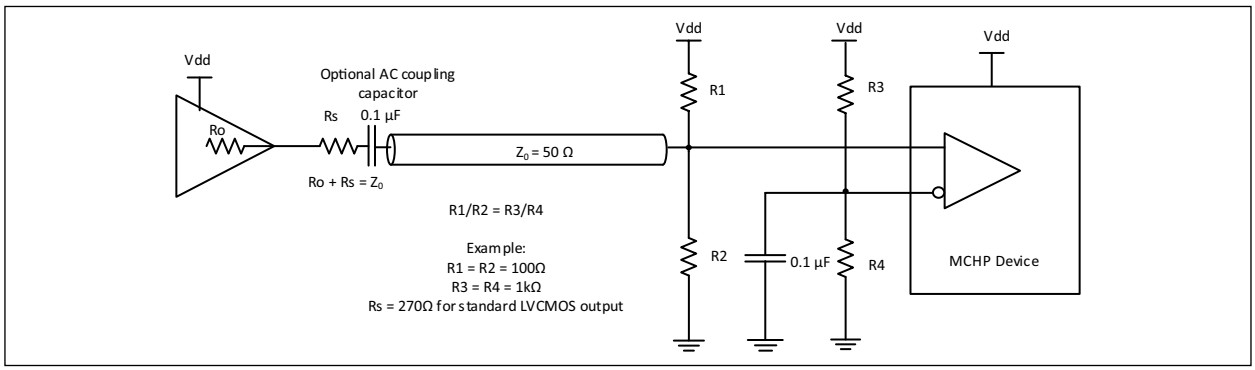


FIGURE 2-1: *Input Driven by a Single-Ended Output.*

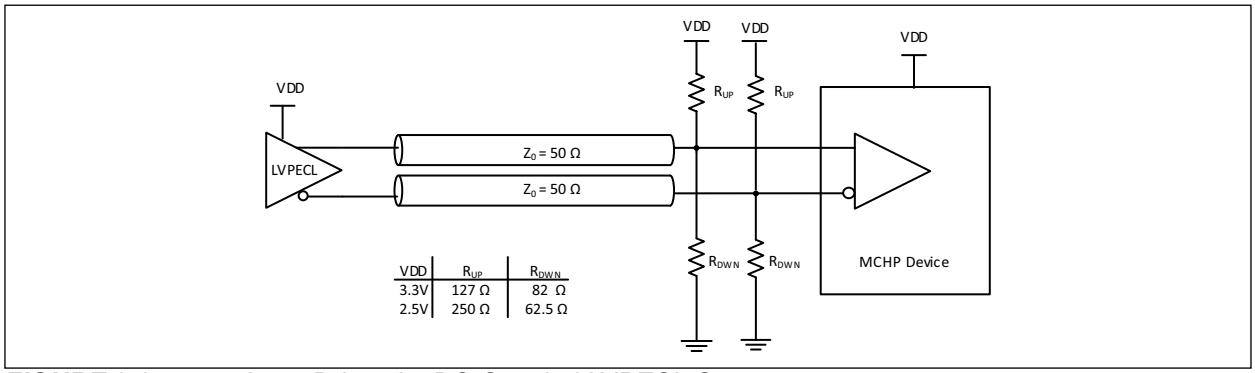


FIGURE 2-2: *Input Driven by DC-Coupled LVPECL Output.*

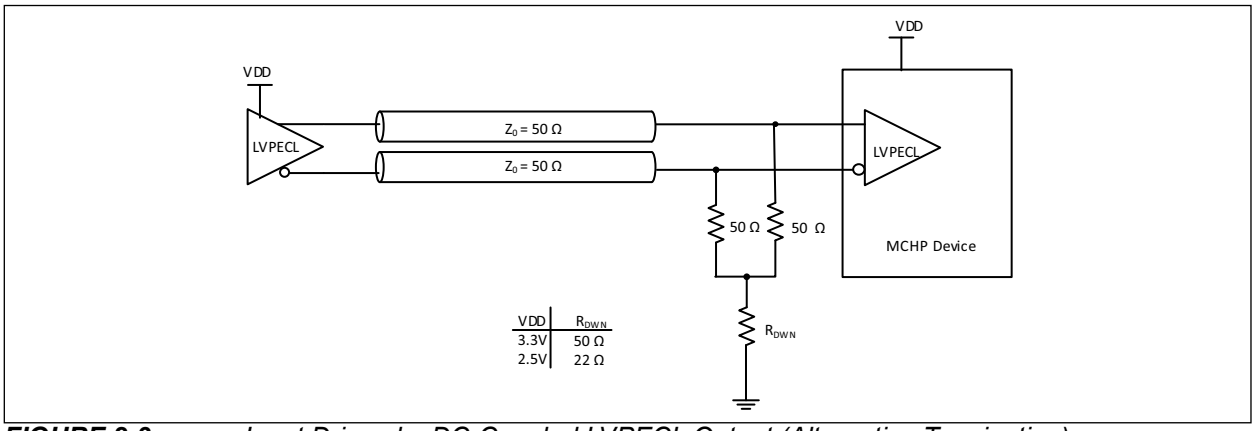


FIGURE 2-3: *Input Driven by DC-Coupled LVPECL Output (Alternative Termination).*

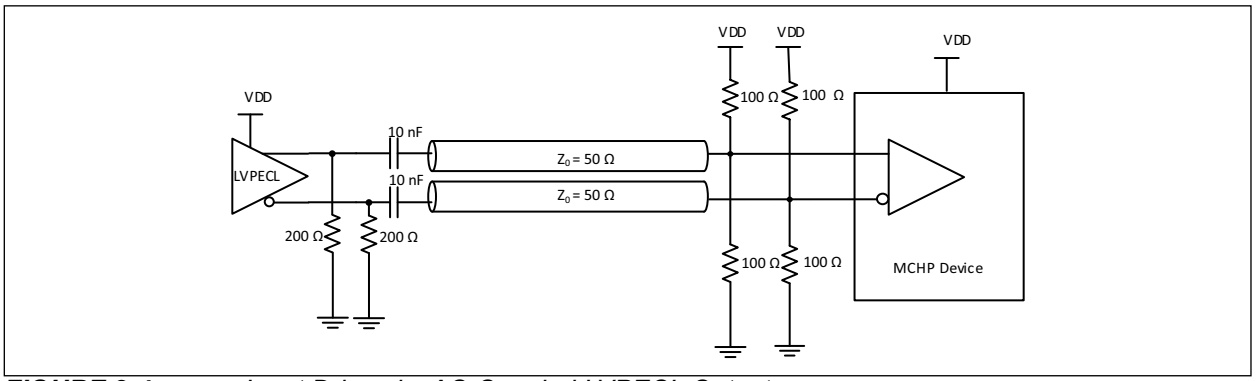


FIGURE 2-4: *Input Driven by AC-Coupled LVPECL Output.*

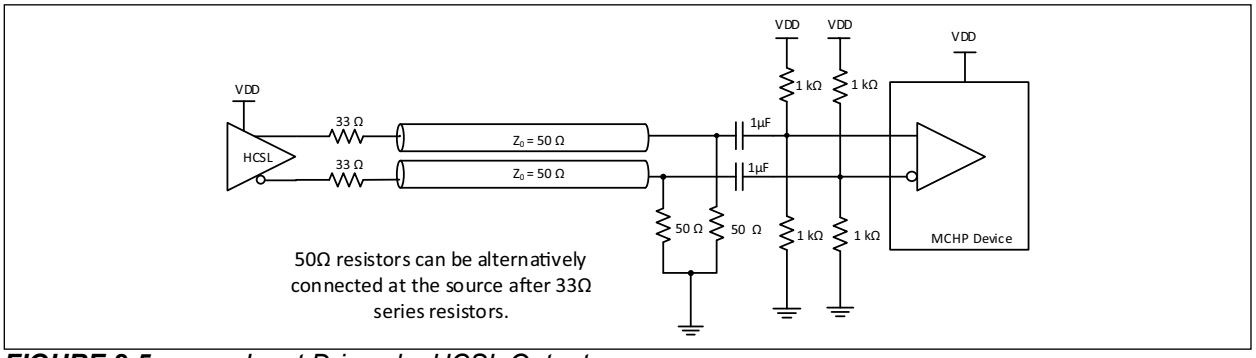


FIGURE 2-5: *Input Driven by HCSL Output.*

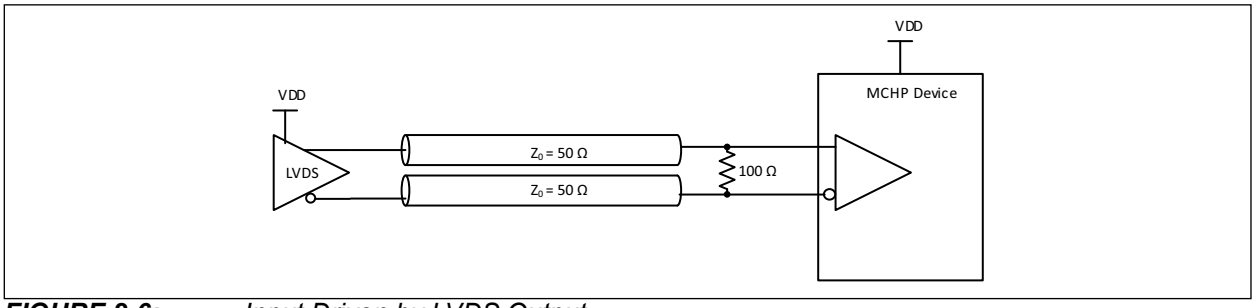


FIGURE 2-6: *Input Driven by LVDS Output.*

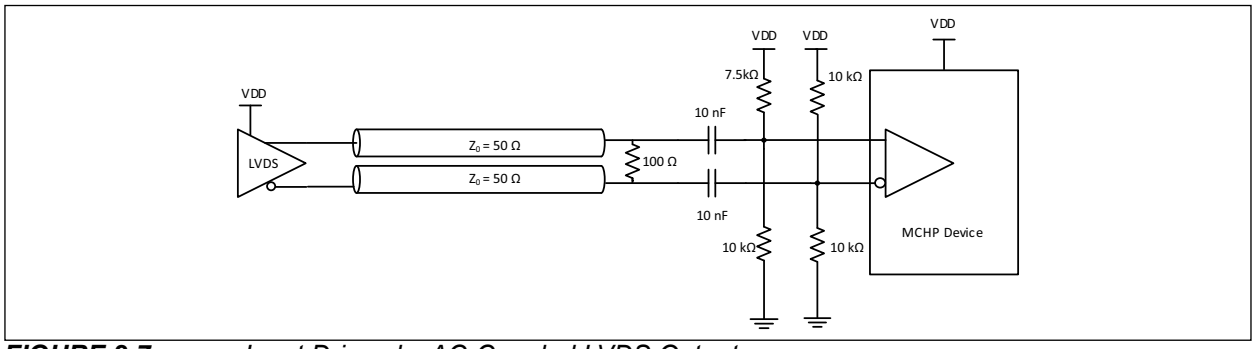


FIGURE 2-7: *Input Driven by AC-Coupled LVDS Output.*

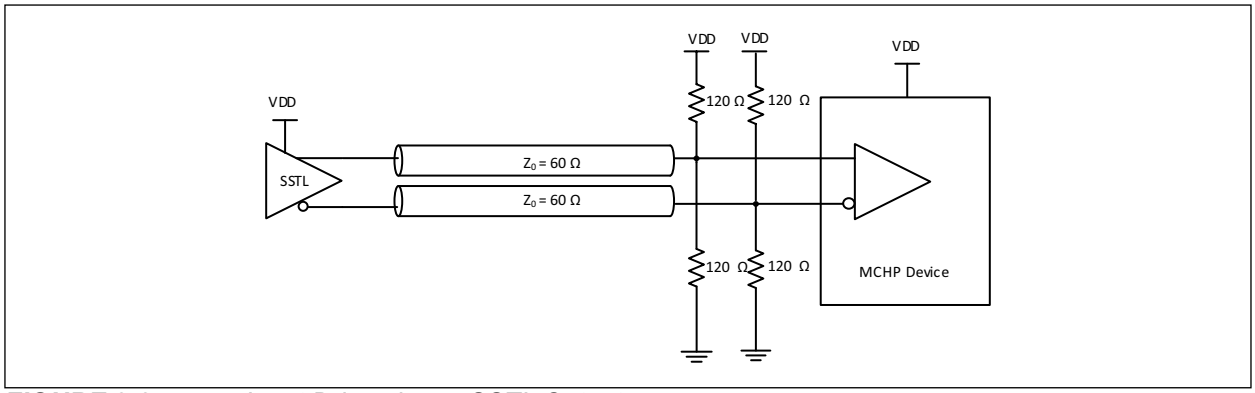


FIGURE 2-8: *Input Driven by an SSTL Output.*

2.2 Clock Outputs

The LVCMOS output (OUT10) requires only a series termination resistor whose value is dependent on the LVCMOS output voltage as shown in Figure 2-9.

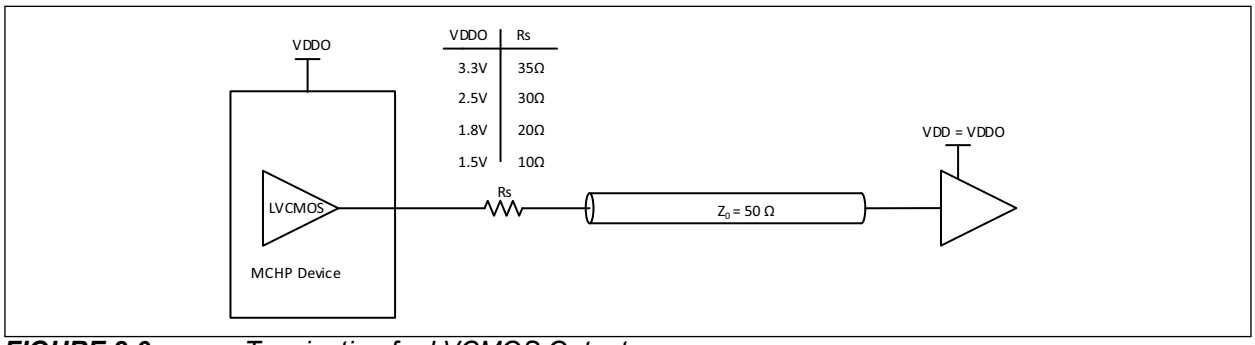


FIGURE 2-9: *Termination for LVCMOS Output.*

Differential outputs LVPECL and LVDS should have the same termination as their corresponding outputs described in the previous section. HCSL outputs should be terminated with 33Ω series resistors at the source and 50Ω shunt resistors at the source or at the end on the transmission line. AC coupling and re-biasing is not required at the outputs when driving native HCSL receivers.

The device is designed to drive the differential input of semiconductor devices. In applications that use a transformer to convert from the differential to the single-ended output (for example, driving an oscilloscope 50Ω input), a resistor larger than 10Ω should be added at the center tap of the primary winding to achieve optimum jitter performance as shown in Figure 2-10. This is to provide a nominal common mode impedance of 10Ω or higher, which is typical for differential terminations.

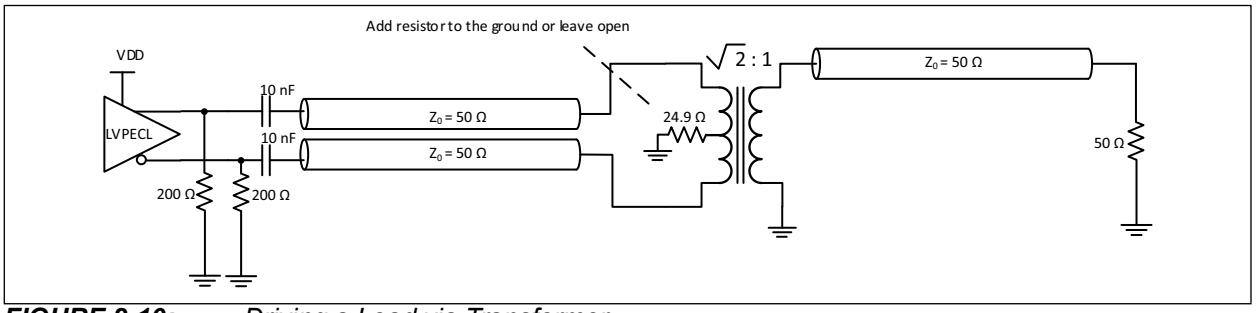


FIGURE 2-10: *Driving a Load via Transformer.*

2.3 Crystal Oscillator Input

The crystal oscillator circuit can work with crystal resonators from 8 MHz to 160 MHz. To be able to support crystal resonators with different characteristics, all internal components are programmable.

The load capacitors can be programmed from 0 pF to 21.75 pF (4 pF default) with a resolution of 0.25 pF, which not only meets load requirement for most crystal resonator but also allows for fine tuning of the crystal resonator frequency. The amplifier gain can be adjusted in five steps and series resistor can be adjusted as parallel combination of seven different resistors: 0Ω, 10.5Ω, 21Ω, 42Ω, 84Ω, 161Ω, and 312Ω (84Ω default). Although the first resistor is 0Ω, the series resistance R_S will be slightly higher than 0Ω due to parasitic resistance of the switch that connects the resistor. Hence, the minimum series resistance is achieved when all seven resistors are connected in parallel. The shunt resistor is fixed and its value is 500 kΩ.

In Hardware Controlled Mode, the capacitive load is set at 4 pF, internal series resistance to 84Ω, and they cannot be changed. For crystals that require higher load or series resistance, additional capacitance and/or series resistance can be added externally as shown in Figure 2-11.

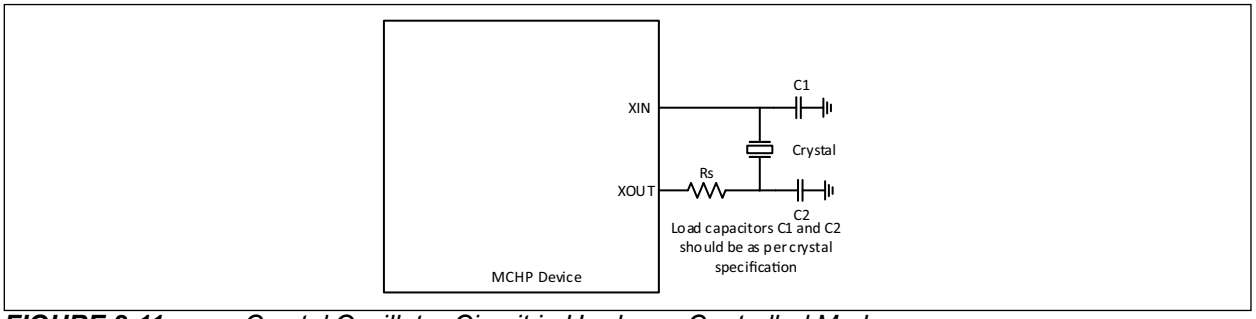


FIGURE 2-11: *Crystal Oscillator Circuit in Hardware Controlled Mode.*

2.4 Termination of Unused Inputs and Outputs

Unused inputs can be left unconnected or, alternatively, IN_0/1 can be pulled down by a 1 kΩ resistor. Unused outputs should be left unconnected.

2.5 Power Consumption

The device's total power consumption can be calculated as:

EQUATION 2-1:

$$P_T = P_S + P_{XTAL} + P_C + P_{O\_DIF} + P_{O\_LVCMOS}$$

Where:

$P_S = V_{DD} \times I_S$ — The core power when the XTAL is not used. The current is specified in Table 5-3. If the XTAL is running, this power should be set to zero.

$P_{XTAL} = V_{DD} \times I_{DD\_XTAL}$ — The core power when the XTAL is used. The current is specified in Table 5-3. If the XTAL is not used, this power should be set to zero.

$P_C = V_{DDO} \times I_{DD\_CM}$ — Common output power shared among all ten outputs. The current I_{DD_CM} is specified Table 5-3.

$P_{O\_DIF} = V_{DDO} \times (I_{DD\_LVDS} \times N_1 + I_{DD\_LVPECL} \times N_2 + I_{DD\_HCSL} \times N_3)$ — Output power where the output currents are specified Table 5-3. N_1, N_2, & N_3 are the number of enabled LVPECL, LVDS, & HSCL outputs, respectively and $N_1+N_2+N_3$ is less than or equal to 5.

$P_{O\_LVCMOS} = V_{DD\_LVCMOS} \times (I_{DD} \times f/100MHz + V_{DD\_LVCMOS} \times C_{LOAD} \times f)$ — Dynamic LVCMOS output power. I_{DD} is specified in Table 5-3. If LVCMOS output is disabled, this term is equal to zero.

Power dissipated inside the device can be calculated by subtracting the power dissipated in termination/biasing resistors from the power consumption.

EQUATION 2-2:

$$P_D = P_T - N_1 \times P_{LVPECL} - N_2 \times P_{LVDS} - N_3 \times P_{HCSL}$$

Where:

N_1, N_2, and N_3 are the number of enabled LVPECL, LVDS, and HSCL outputs, respectively. Because there are five differential outputs, $N_1 + N_2 + N_3$ is less than or equal to 5.

$$P_{LVPECL} = (V_{OH} - V_B)^2/50\Omega + (V_{OL} - V_B)^2/50\Omega + (V_{OH} - V_B) \times V_B/50\Omega + (V_{OL} - V_B) \times V_B/50\Omega$$

V_{OH} and V_{OL} are the output high and low voltages respectively for LVPECL output.

V_B is LVPECL bias voltage equal to V_{DD} – 2V.

$P_{LVDS} = V_{SW}^2/100\Omega$ — V_{SW} is the voltage swing of the LVDS output.

$P_{HCSL} = (V_{SW}/50\Omega)^2 \times (33\Omega + 50\Omega)$ — V_{SW} is the voltage swing of the HCSL output. 50Ω is the termination resistance and 33Ω is the series resistance of the HCSL output.

2.6 Power Supply Filtering

Each power pin (VDD and VDDO) should be decoupled with a 0.1 µF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example, 0402 X5R ceramic capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board, each power supply could be further insulated with a low resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent components from the noise generated by the device. Figure 2-12 shows recommended decoupling for each power pin.

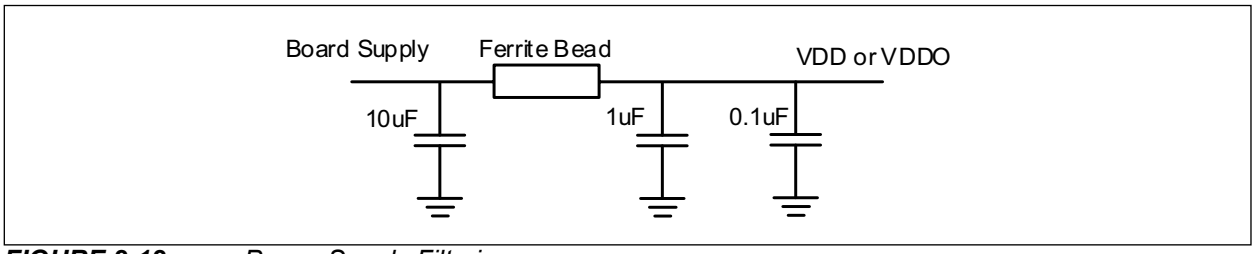


FIGURE 2-12: *Power Supply Filtering.*

2.7 Power Supplies and Power-Up Sequence

The device has four different power supplies: VDD, VDDO_A, VDDO_B, and VDD_LVCMOS which are mutually independent. Voltages supported by each of these power supplies are specified in Table 1-1.

The device is not sensitive to the power-up sequence. For example, a commonly used sequence where higher voltage comes up before or at the same time as the lower voltages can be used (or any other sequence).

2.8 Host Interface

ZL40235 can be controlled via hardware pins (SEL pin tied low) or via SPI port (SEL pin tied high). The mode shall be selected during power up and it cannot be changed on the fly.

2.8.1 HARDWARE CONTROL MODE

In this mode, ZL40235 is controlled via Input Select (IN_SEL0/1) pins that select which one of three inputs is fed to the output and show in Table 2-1 and OUT_TYPE_SEL0/1 pins that select signal level (LVPECL, LVDS, HCSL, or Hi-Z) as shown in Table 2-2.

All input control pins have a low input threshold voltage so they can be driven from the device with low output voltage (FPGA/CPLD). Supported voltages are between 1.2V and V_{DD} (2.5V or 3.3V).

TABLE 2-1: INPUT CLOCK SELECTION

IN_SEL1	IN_SEL0	Selected Input
0	0	IN0_p, IN0_n
0	1	IN1_p, IN1_n
1	X	XIN

TABLE 2-2: OUTPUT TYPE SELECTION

OUT_TYPE_SEL1	OUT_TYPE_SEL0	Output
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	High-Z (Output Disabled)

2.8.2 SPI CONTROL MODE

ZL40235 is controlled via four SPI client interface pins as shown in the following figure.

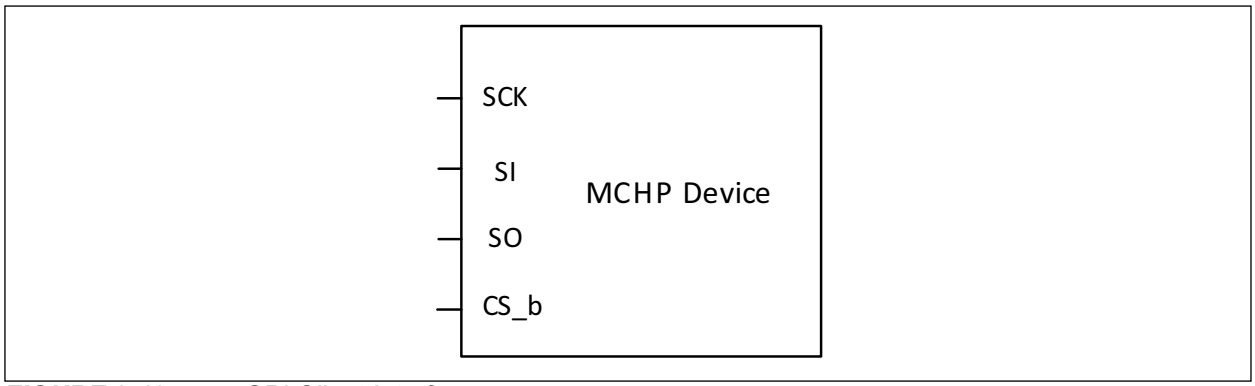


FIGURE 2-13: *SPI Client Interface.*

All SPI input pins have a low threshold voltage so they can be driven by a low output voltage SPI host device. Supported voltages are between 1.2V and V_{DD} (2.5V or 3.3V). This allows device to be controlled from an FPGA with low voltage I/O supply.

The serial peripheral interface supports half-duplex processor mode, which means that during a write cycle to the device, output data from the SO pin must be ignored. Similarly, the input data on the SI pin is ignored by the device during a read cycle.

The SPI interface supports two modes of access: Most Significant bit (MSb) first transmission or Least Significant bit (LSb) first transmission. The mode is automatically selected based on the state of SCK pin when the CS_b pin is active. If the SCK pin is low during CS_b activation, then MSb first timing is selected. If the SCK pin is high during CS_b activation, then LSb first timing is selected.

The SPI port expects 1-bit to differentiate between read and write operation followed by 7-bit addressing and 8-bit data transmission. During SPI access, the CS_b pin must be held low until the operation is complete. Burst read/write mode is also supported by leaving the chip select signal CS_b low after a read or a write. The address will be automatically incremented after each data byte is read or written.

Functional waveforms for the LSb and MSb first mode, and burst mode are shown in Figure 2-14 and Figure 2-15 respectively. Figure 2-16 shows an example of burst mode operation that allows user to read or write consecutive location in the register map.

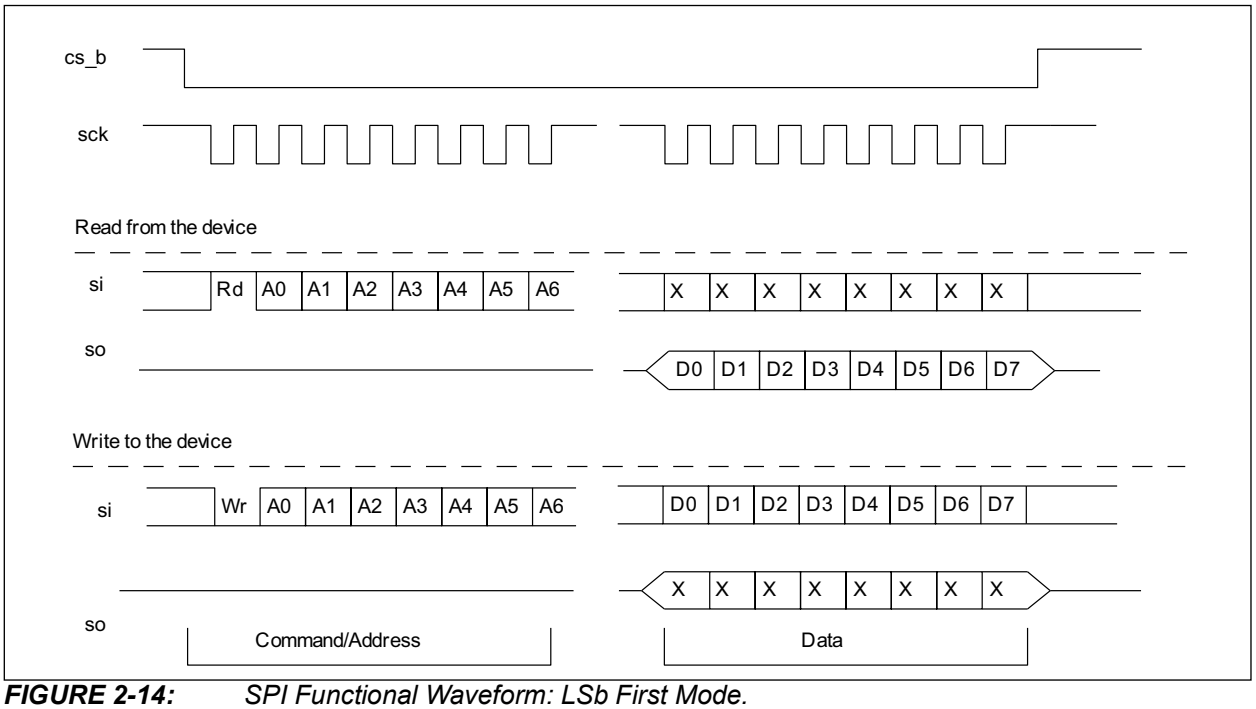


FIGURE 2-14: *SPI Functional Waveform: LSb First Mode.*

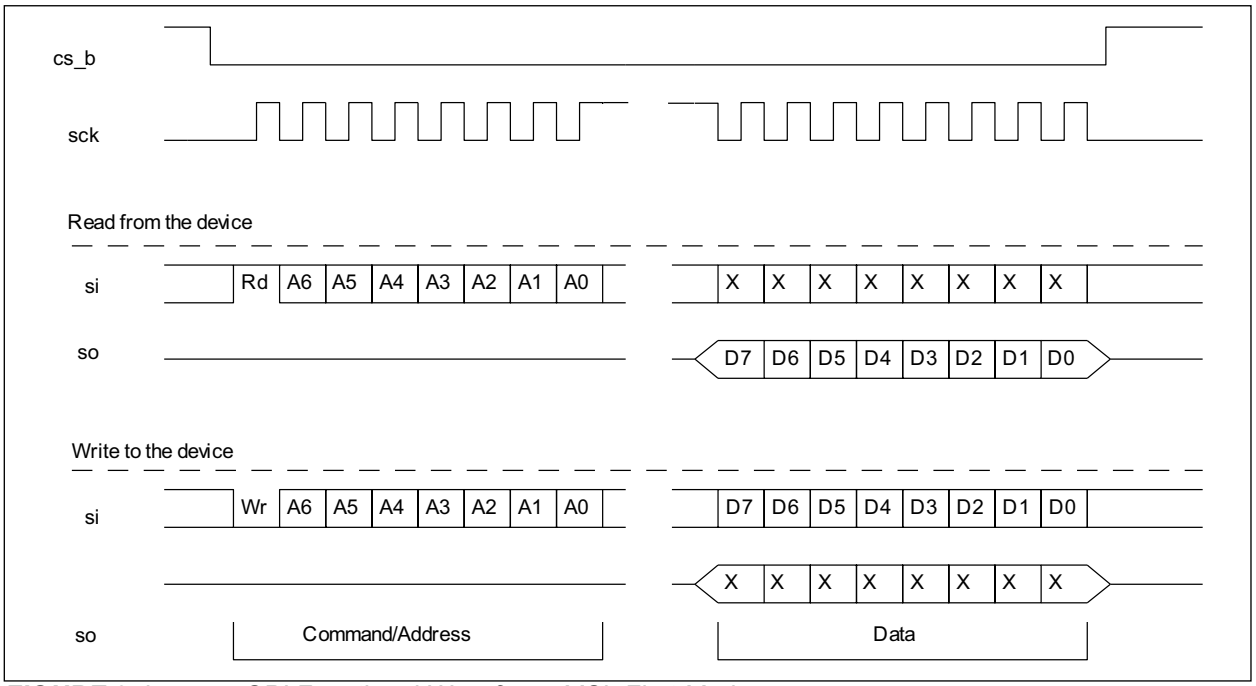


FIGURE 2-15: *SPI Functional Waveform: MSb First Mode.*

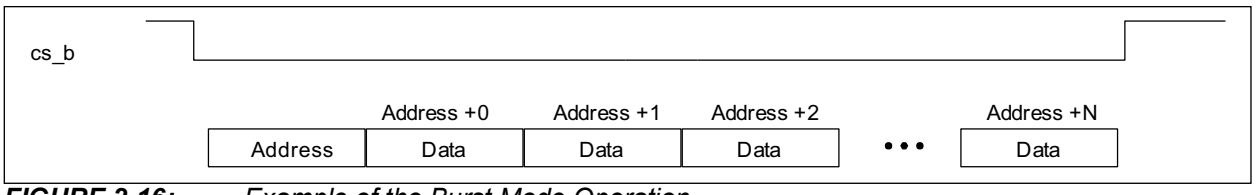


FIGURE 2-16: *Example of the Burst Mode Operation.*

3.0 TYPICAL DEVICE PERFORMANCE

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

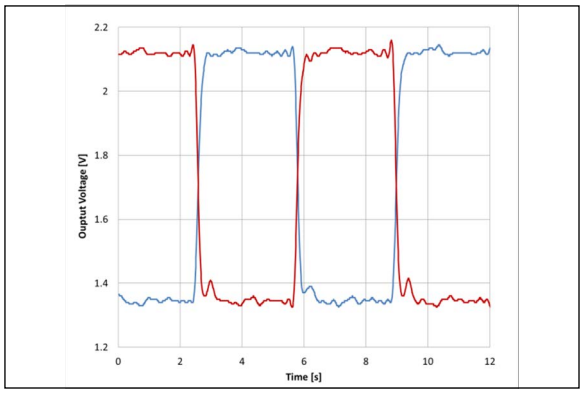


FIGURE 3-1: *156.25 MHz LVPECL.*

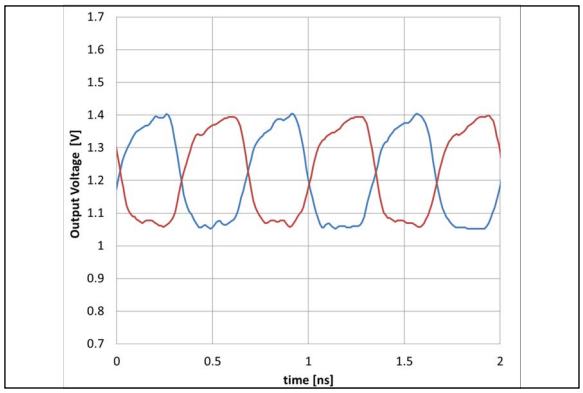


FIGURE 3-4: *1.5 GHz LVDS.*

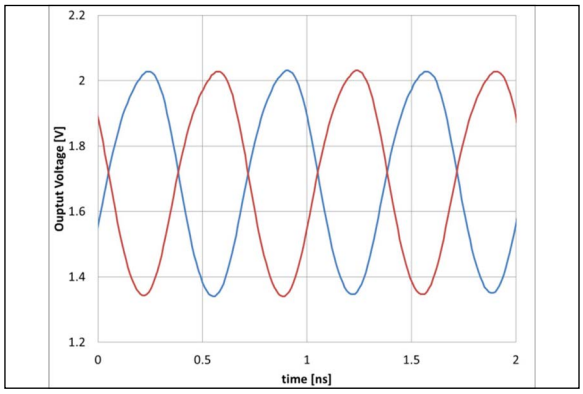


FIGURE 3-2: *1.5 GHz LVPECL.*

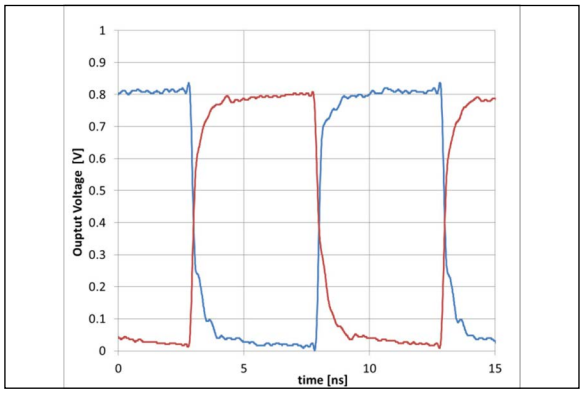


FIGURE 3-5: *100 MHz HCSL.*

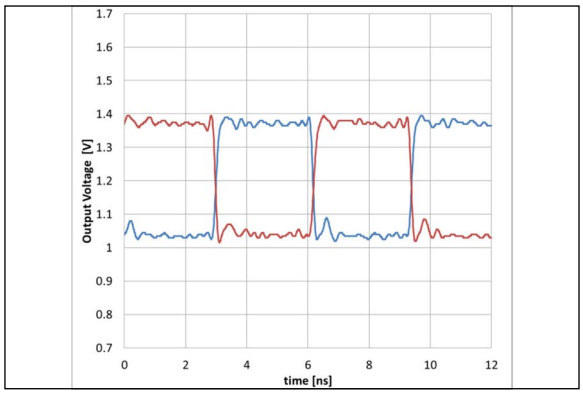


FIGURE 3-3: *156.25 MHz LVDS.*

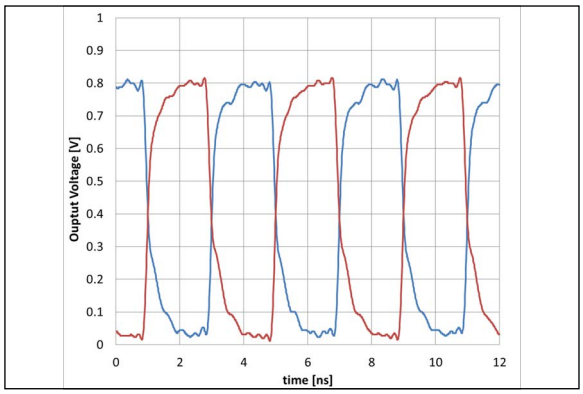


FIGURE 3-6: *250 MHz HCSL.*

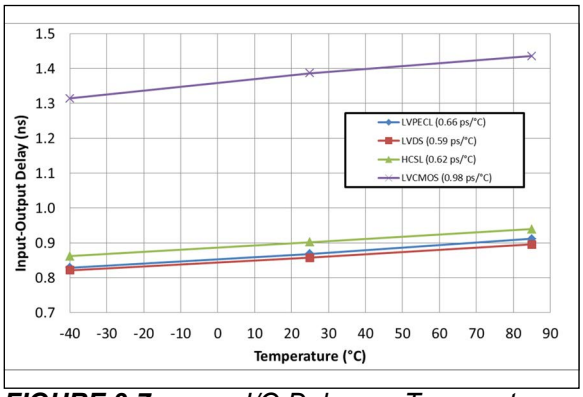


FIGURE 3-7: *I/O Delay vs. Temperature.*

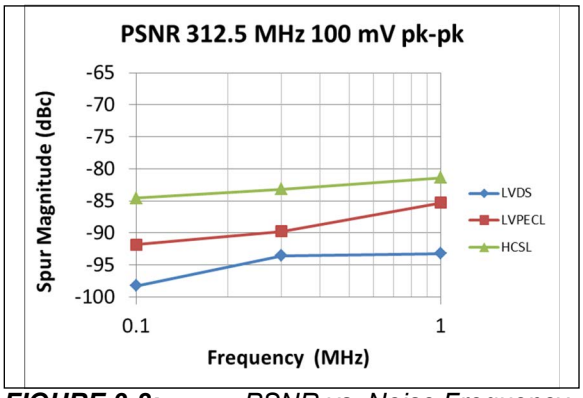


FIGURE 3-8: *PSNR vs. Noise Frequency.*

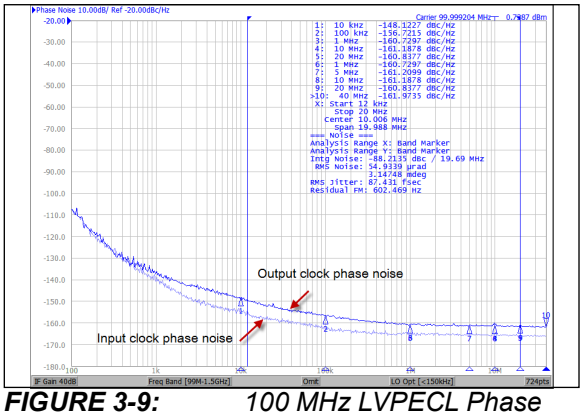


FIGURE 3-9: *100 MHz LVPECL Phase Noise.*

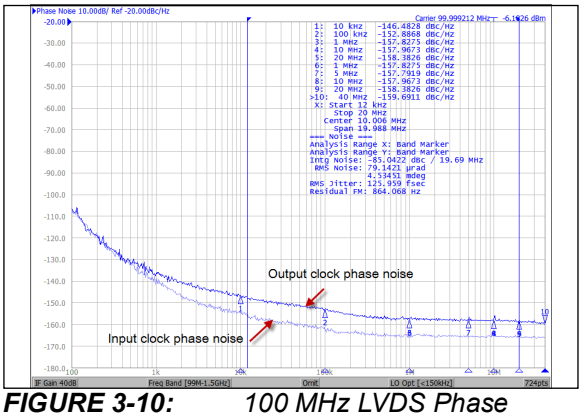


FIGURE 3-10: *100 MHz LVDS Phase Noise.*

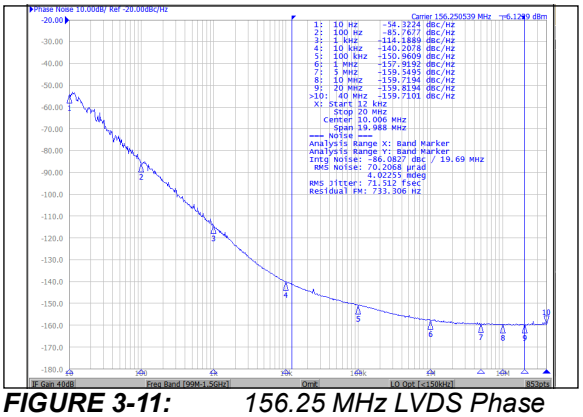


FIGURE 3-11: *156.25 MHz LVDS Phase Noise in XTAL Mode.*

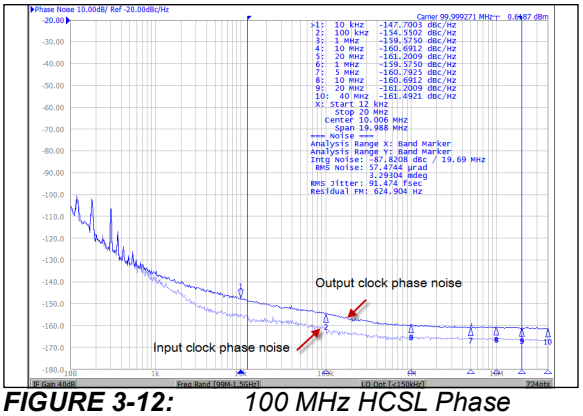


FIGURE 3-12: *100 MHz HCSL Phase Noise.*

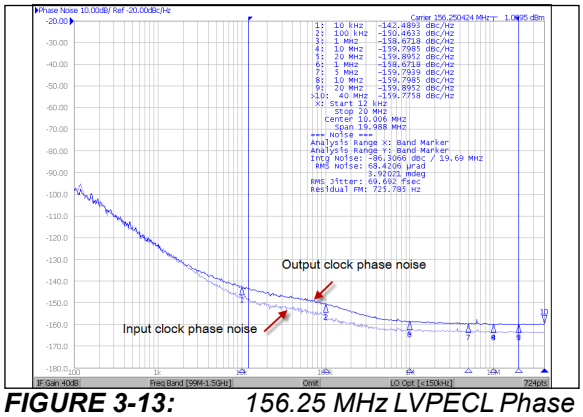


FIGURE 3-13: *156.25 MHz LVPECL Phase Noise.*

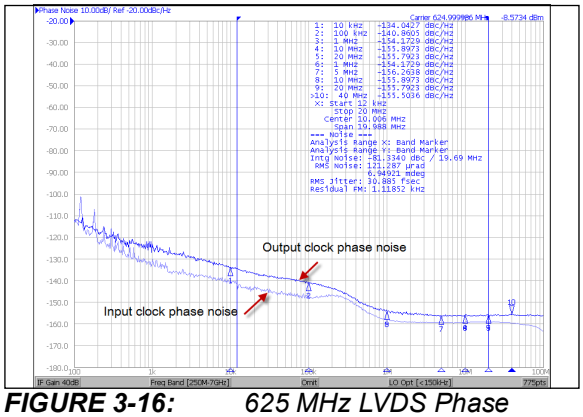


FIGURE 3-16: *625 MHz LVDS Phase Noise.*

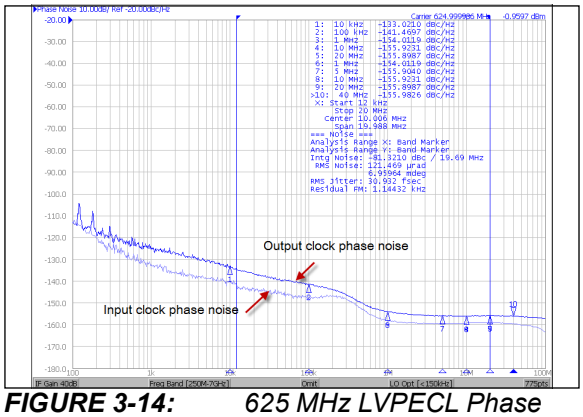


FIGURE 3-14: *625 MHz LVPECL Phase Noise.*

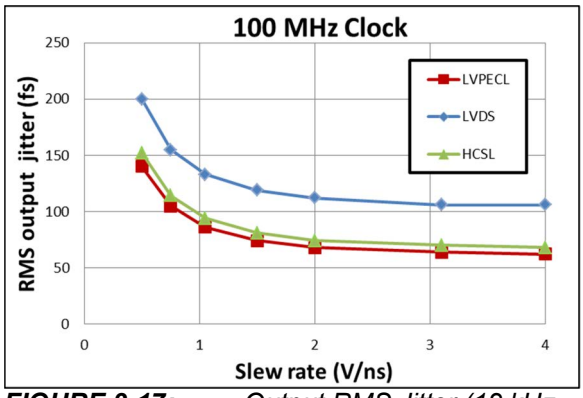


FIGURE 3-17: *Output RMS Jitter (12 kHz to 20 MHz) vs. Input Clock Slew Rate.*

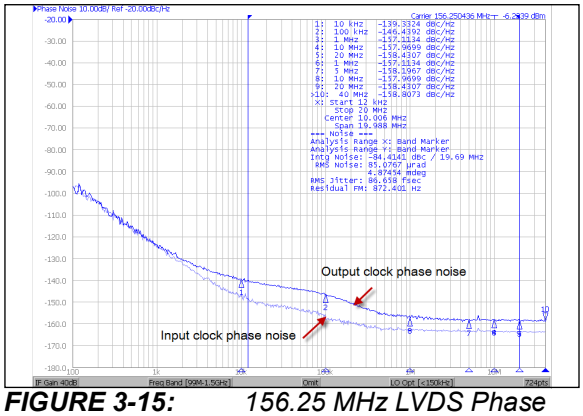


FIGURE 3-15: *156.25 MHz LVDS Phase Noise.*

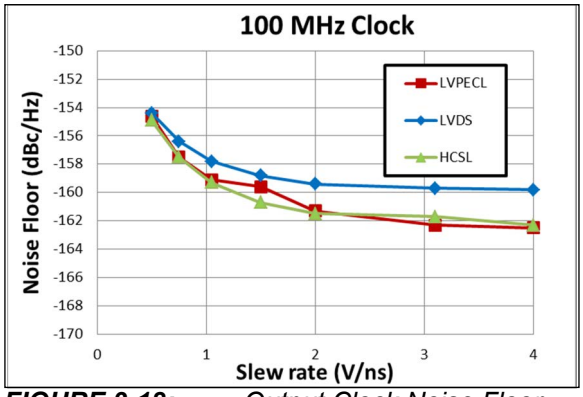


FIGURE 3-18: *Output Clock Noise Floor vs. Input Clock Slew Rate.*

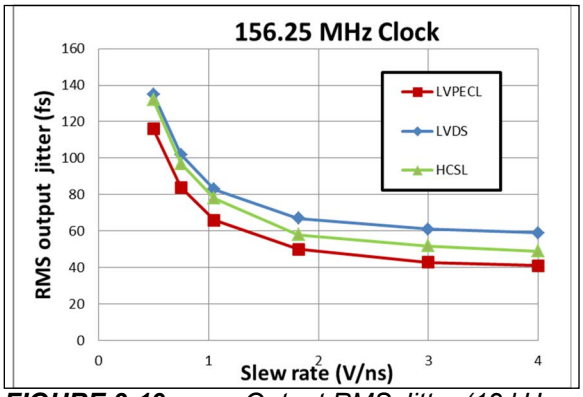


FIGURE 3-19: *Output RMS Jitter (12 kHz to 20 MHz) vs. Input Clock Slew Rate.*

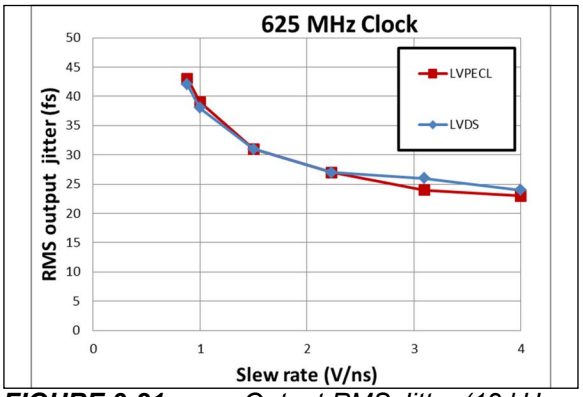


FIGURE 3-21: *Output RMS Jitter (12 kHz to 20 MHz) vs. Input Clock Slew Rate.*

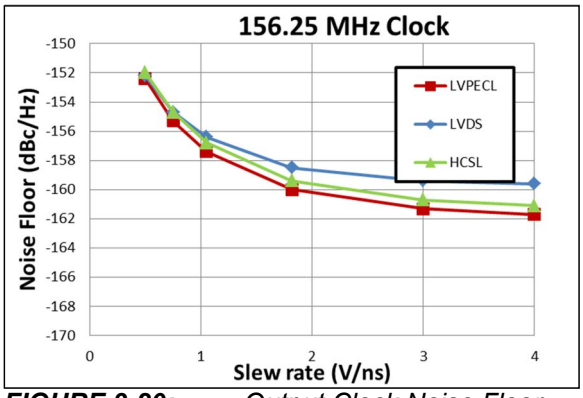


FIGURE 3-20: *Output Clock Noise Floor vs. Input Clock Slew Rate.*

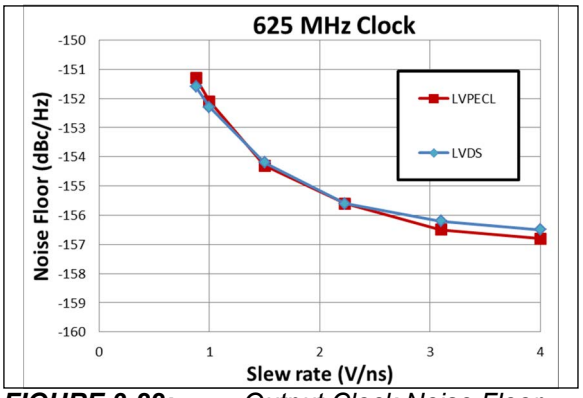


FIGURE 3-22: *Output Clock Noise Floor vs. Input Clock Slew Rate.*

4.0 REGISTER MAP

The device is controlled by accessing registers through the serial interface. Table 4-1 provides a summary of the registers available for the configuration of the device.

TABLE 4-1: REGISTER MAP

Address SPI A[6:0] Hex (0x)	Name	Data D[7:0]
00	XTALBG	xtal_buf_gain[7:0]
01	XTALDL	xtal_drive_level[7:0]
02	XTALLC	xtal_load_cap[7:0]
03	XTALNR	xtal_normal_run
04	—	not used
05	INSEL	input_select[1:0]
06	OUTLOW	output_drive_low
07	DRVTYPEA	{driver_type[5:4], 4'bxxxx} (differential output 1 and 0)
08	—	not used
09	DRVTYPEB	{driver_type[17:12], 2'bxx} (differential output 4, 3, and 2)
0A	—	not used
0B	CMOSDIV	cmos_div[2:0] (cmos)
0C	CMOSOUTEN	output_enable (cmos)
0D	CMOSDRVSTR	driver_strength (cmos)
0E	—	not used
0F/11	Reserved	Leave as default
11	DEVID	Device ID
12 to 1F	Reserved	Leave as default

TABLE 4-2: 0X00 XTALBG - XTAL BUFFER GAIN

Bit	Name	Description	Type	Reset
7:0	xtal_buf_gain[7:0]	Programs crystal buffer (inverting amplifier) gain. Every bit pair (bits: 01, 23, 45, 67) of this register correspond to additional equal gain block which can be added (bits set) or removed (bits cleared). Minimum gain is 0x00 (default) and 0xFF is maximum gain When reference input mode is "bypass XTAL mode" or "differential input modes" with HIGH xtal_normal_run bit, the buffer is disabled and follows "Input Selection". When xtal_normal_run bit is LOW, XTAL buffer is in the "xtal forced run" mode and keep running. **8'b0000_0000: default crystal buffer strength** 8'b0000_0011: enable additional buffer strength 8'b0000_1100: enable additional buffer strength 8'b0011_0000: enable additional buffer strength 8'b1100_0000: enable additional buffer strength	RW	FF

TABLE 4-3: 0X01 XTALDL - XTAL DRIVE LEVEL

Bit	Name	Description	Type	Reset
7:0	xtal_drive_level[7:0]	Internal damping resistance of crystal circuit to limit external crystal's drive level µW. The value of damping resistor is determined by crystal's motion resistance of crystal's equivalent circuit. Drive level should be lower than crystal manufacturer's specification. Crystal's equivalent values should be requested to the manufacturer, (motion resistance and shunt capacitance). The selected resistors are connected to XOUT. Multiple bit combinations available by 7-bit control. Because they use parallel connections, 0xFF is the smallest resistance and 0x01 is the highest resistance. 8'b0000_0000: disable all resistors 8'b0000_0001: 312 Ohm resistor 8'b0000_0010: 161 Ohm resistor 8'b0000_0100: 84 Ohm resistor 8'b0000_1000: 42 Ohm resistor 8'b0001_0000: 21 Ohm resistor 8'b0010_0000: 10.5 Ohm resistor 8'b0100_0000: 0 Ohm connection 8'b1000_0000: not used	RW	04

TABLE 4-4: 0X02 XTALLC - XTAL LOAD CAPACITANCE 0

Bit	Name	Description	Type	Reset
7:0	xtal_load_cap[7:0]	Internal load capacitance of crystal circuit (0 pF to 21.75 pF with the resolution of 0.25 pF). XIN and XOUT have each capacitor connected to GND. Multiple bit combinations available between 8 capacitors. 8'b0000_0000: disable all xtal load capacitors 8'b0000_0001: enable capacitor 0.25 pF 8'b0000_0010: enable capacitor 0.5 pF 8'b0000_0100: enable capacitor 1 pF 8'b0000_1000: enable capacitor 2 pF 8'b0001_0000: enable capacitor 2 pF 8'b0010_0000: enable capacitor 4 pF 8'b0100_0000: enable capacitor 4 pF 8'b1000_0000: enable capacitor 8 pF	RW	40

TABLE 4-5: 0X03 XTALNR - XTAL NORMAL RUN

Bit	Name	Description	Type	Reset
7:1	Reserved	Reserved	R	1111111
0	xtal_normal_run	When this bit is set high crystal oscillator circuit is running only if input_select[1:0] register at address 0x05 selects crystal mode (2'b10). This value is recommended because it provides best jitter performance—XO circuit is running only when it is needed. When this bit is set low the crystal oscillator will keep running even if crystal oscillator is not selected in input_select[1:0] register at address 0x05. This mode should only be used when fast switching between input references and crystal oscillator is required.	RW	1

TABLE 4-6: 0X05 INSEL - INPUT SELECT REGISTER

Bit	Name	Description	Type	Reset
7:2	Reserved	Reserved	R	111111
1:0	input_select[1:0]	Input reference clock selection. Proper external coupling and termination are required. 2'b00: Differential input from IN0_p and IN0_n 2'b01: Differential input from IN1_p and IN1_n 2'b10: Fundamental XTAL mode with XIN and XOUT (Use internal crystal oscillator circuits) or XTAL overdrive mode (single-ended clock signal fed to XIN) 2'b11: XTAL bypass mode (single-ended clock signal with XIN and disabled internal crystal buffer circuit in the analog block)	RW	00

TABLE 4-7: 0X06 OUTLOW - OUTPUT DRIVE LOW

Bit	Name	Description	Type	Reset
7:1	Reserved	Reserved	R	111111
0	output_drive_low	Forces all disabled outputs to drive low in LVPECL mode. 1'b1: All differential outputs that are disabled in DRVTYPE registers (addresses 0x07, 0x08, 0x09 and 0x0A) will drive low in LVPECL mode. Hence, LVPECL biasing/termination resistors are required for proper functionality of this feature. 1'b0: This feature is ignored and all outputs that are disabled in DRVTYPE registers (addresses 0x07, 0x08, 0x09 and 0x0A) will stay in disabled (high-Z) mode.	RW	0

TABLE 4-8: 0X07 DRVTYPEA - OUTPUT TYPE SELECT BANK-A

Bit	Name	Description	Type	Reset
7:6	driver_type[7:6]	Output driver type of differential OUT1. The same description as for OUT0.	RW	11
5:4	driver_type[5:4]	Output driver type of differential OUT0. 2'b00: LVPECL outputs 2'b01: LVDS outputs 2'b10: HCSL outputs 2'b11: outputs disabled (Disabled state is dependent on "out-_drive_low" control bit of register OUTLOW.")	RW	11
3:0	Reserved	Reserved	RO	X

TABLE 4-9: 0X09 DRVTYPEB - OUTPUT TYPE SELECT BANK-B

Bit	Name	Description	Type	Reset
7:6	driver_type[17:16]	Output driver type of differential OUT4. The same description as OUT0.	RW	11
5:4	driver_type[15:14]	Output driver type of differential OUT3. The same description as OUT0.	RW	11
3:2	driver_type[13:12]	Output driver type of differential OUT2. The same description as OUT0.	RW	11
1:0	Reserved	Reserved	RO	X

TABLE 4-10: 0X0B CMOSDIV - CMOS OUTPUT DIVIDER

Bit	Name	Description	Type	Reset
7:3	Reserved	Reserved	R	11111
2:0	cmos_div[2:0]	Integer divider from a selected input reference clock for OUT_LVCMOS (1 to 8). **3'b000: division ratio = 1** 3'b001: division ratio = 2 3'b010: division ratio = 3 3'b011: division ratio = 4 3'b100: division ratio = 5 3'b101: division ratio = 6 3'b110: division ratio = 7 3'b111: division ratio = 8	RW	000

TABLE 4-11: 0X0C CMOSOUTEN - LVCMOS OUTPUT ENABLE

Bit	Name	Description	Type	Reset
7:1	Reserved	Reserved	R	1111111
0	output_enable	Output enable of OUT_LVCMOS. Disabled state is dependent on "out_drive_low" control bit. 1'b0: Disable OUT_LVCMOS output 1'b1: Enable OUT_LVCMOS output	RW	0

TABLE 4-12: 0X0D CMOSDRVSTR - CMOS DRIVER STRENGTH

Bit	Name	Description	Type	Reset
7:1	Reserved	Reserved	R	1111111
0	driver_strength	OUT_LVCMOS output strength. 1'b0: low strength 1'b1: high strength	RW	0

TABLE 4-13: 0X11 DEVID - DEVICE IDENTIFICATION

Bit	Name	Description	Type	Reset
7	Unused	Unused	R	0
6:5	Reserved	Reserved	—	11
4:0	dev_id	Device ID **5'h02: ZL40235**	RO	00010

NOTES:

5.0 ELECTRICAL CHARACTERISTICS

TABLE 5-1: ABSOLUTE MAXIMUM RATINGS

(Note 1, Note 2, Note 3)

Parameter	Symbol	Min.	Max.	Units
Supply Voltage, 3.3V	V_{DD}/V_{DDO}	–0.5	4.6	V
Supply Voltage, 2.5V	V_{DD}/V_{DDO}	–0.5	3.5	V
Storage Temperature Range	T_{ST}	–55	125	°C

Note 1: Exceeding these values may cause permanent damage.

2: Functional operation under these conditions is not implied.

3: Voltages are with respect to ground (GND) unless otherwise stated.

TABLE 5-2: RECOMMENDED OPERATING CONDITIONS

(Note 1, Note 2)

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Voltage, 3.3V	$V_{DD}/V_{DDO}/V_{DD\_LVCMOS}$	3.135	3.30	3.465	V
Supply Voltage, 2.5V	$V_{DD}/V_{DDO}/V_{DD\_LVCMOS}$	2.375	2.50	2.625	V
Supply Voltage, 1.8V	V_{DD_LVCMOS}	1.6	1.8	2.0	V
Supply Voltage, 1.5V	V_{DD_LVCMOS}	1.35	1.5	1.65	V
Operating Temperature	T_A	–40	+25	+85	°C
Input Voltage	V_{DD-IN}	–0.3	—	V_{DD} + 0.3	V

Note 1: Voltages are with respect to ground (GND) unless otherwise stated.

2: The device core supports two power supply modes (3.3V and 2.5V).

TABLE 5-3: CURRENT CONSUMPTION

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Core device current (all outputs and XTAL disabled)	$I_{S\_3.3V}$	—	163	197	mA	V_{DD} = 3.3V+5%
	$I_{S\_2.5V}$	—	153	187	mA	V_{DD} = 2.5V+5%
Core device current (all outputs disabled) XTAL circuit enabled with 25 MHz Crystal connected between XIN and XOUT	$I_{DD\_XTAL\_3.3V}$	—	128	154	mA	V_{DD} = 3.3V+5%
	$I_{DD\_XTAL\_2.5V}$	—	124	150	mA	V_{DD} = 2.5V+5%
Common output current	$I_{DD\_CM\_3.3V}$	—	13.44	15.05	mA	V_{DDO} = 3.3V+5%
	$I_{DD\_CM\_2.5V}$	—	12.18	13.65	mA	V_{DDO} = 2.5V+5%
Dynamic LVCMOS current for high strength output (f = 100 MHz) Needs to be scaled for different frequencies by f/100 MHz	$I_{DD\_3.3V}$	—	4.08	4.74	mA	V_{DDO} = 3.3V+5%
	$I_{DD\_2.5V}$	—	2.90	3.29	mA	V_{DDO} = 2.5V+5%
Dynamic LVCMOS current for low strength output (f = 100 MHz) Needs to be scaled for different frequencies by f/100 MHz	$I_{DD\_3.3V}$	—	2.38	2.68	mA	V_{DDO} = 3.3V+5%
	$I_{DD\_2.5V}$	—	1.74	1.96	mA	V_{DDO} = 2.5V+5%
Current dissipation per LVPECL output	$I_{DD\_LVPECL\_3.3V}$	—	19.36	23.26	mA	V_{DDO} = 3.3V+5%
	$I_{DD\_LVPECL\_2.5V}$	—	19.38	22.17	mA	V_{DDO} = 2.5V+5%
Current dissipation per LVDS output	$I_{DD\_LVDS\_3.3V}$	—	6.73	8.00	mA	V_{DDO} = 3.3V+5%
	$I_{DD\_LVDS\_2.5V}$	—	6.87	7.83	mA	V_{DDO} = 2.5V+5%
Current dissipation per HCSL output	$I_{DD\_HCSL\_3.3V}$	—	16.43	19.87	mA	V_{DDO} = 3.3V+5%
	$I_{DD\_HCSL\_2.5V}$	—	17.14	19.18	mA	V_{DDO} = 2.5V+5%

TABLE 5-4: INPUT CHARACTERISTICS

Note 1, Note 2, Note 3						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**
CMOS high-level input voltage for control inputs	V_{CIH}	1.05	—	—	V	—
CMOS low-level input voltage for control inputs	V_{CIL}	—	—	0.45	V	—
CMOS input leakage current for control inputs (includes current due to pull-down resistors)	I_{IL}	–25	—	50	µA	$V_I = V_{DD}$ or 0V
Differential input common mode voltage for IN0_p/n and IN1_p/n	V_{CM}	1	—	2	V	—
Differential input voltage difference for IN0_p/n and IN1_p/n, f ≤1 GHz (Note 4)	V_{ID}	0.15	—	1.3	V	—
Differential input voltage difference for IN0_p/n and IN1_p/n for 1 GHz < f ≤ 1.6 GHz (Note 4)	V_{ID}	0.35	—	1.3	V	—
Differential input leakage current for IN0_p/n and IN1_p/n (includes current due to pull-up and pull-down resistors)	I_{IL}	–150	—	150	µA	V_I = 2V or 0V
Single-ended input voltage for IN0_p and IN1_p	V_{SI}	–0.3	—	2.7	V	V_{DD} = 3.3V or 2.5V
Single-ended input common mode voltage (IN0_p/n and IN1_p/n)	V_{SIC}	1	—	2	V	V_{DD} = 3.3V or 2.5V
Single-ended input voltage swing for IN0_p and IN1_p	V_{SID}	0.3	—	1.3	V	V_{DD} = 3.3V or 2.5V
Input frequency (differential)	f_{IN}	0	—	1600	MHz	—
Input frequency (LVCMOS)	f_{IN_CMOS}	0	—	250	MHz	—
Input duty cycle	dc	35%	—	65%	—	—
Input slew rate	Slew	—	2	—	V/ns	—
Input pull-up/ pull-down resistance	R_{PU}/R_{PD}	—	60	—	kΩ	—
Input pull-down resistance for INx_p	R_{PD}	—	30	—	kΩ	—
Input multiplexer isolation IN0_p/n to IN1_p/n and vice versa Power on both inputs 0 dBm, f_{OFFSET} > 50 kHz	I_{SO}	—	–84	—	dBc	f_{IN} = 100 MHz
		—	–82	—		f_{IN} = 200 MHz
		—	–71	—		f_{IN} = 400 MHz
		—	–67	—		f_{IN} = 800 MHz

Note 1: Values are over recommended operating conditions.

2: Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V).

3: Input mux isolation is measured as amplitude of f_{OFFSET} spur in dBc on the output clock phase noise plot.

4: Input differential voltage is calculated as $V_{ID} = V_{IH} – V_{IL}$ where V_{IH} and V_{IL} are input voltage high and low respectively. It should not be confused with $V_{ID} = 2 \times (V_{IH} – V_{IL})$ used in some data sheets. Please refer to Figure 5-1.

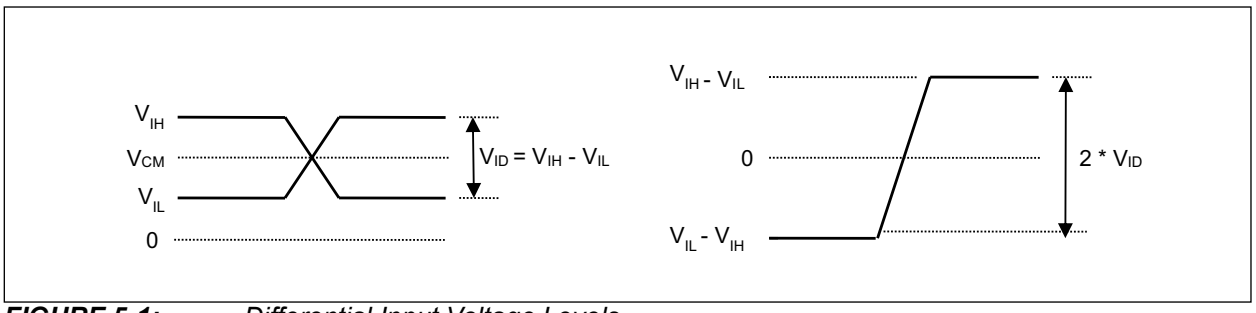


FIGURE 5-1: *Differential Input Voltage Levels.*

TABLE 5-5: CRYSTAL OSCILLATOR CHARACTERISTICS

Note 1, Note 2						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**
Mode of oscillation	Mode	Fundamental			—	—
Frequency	f	8	—	160	MHz	—
On chip load capacitance in SPI controlled mode	C_L	0	—	21.75	pF	Programmable
On chip load capacitance in pin controlled mode		—	4	—	pF	Fixed
On chip series resistor in SPI controlled mode	R_S	0	—	312	Ω	Programmable
		—	84	—	Ω	Fixed
On chip shunt resistor	R	—	500	—	kΩ	—
Frequency in overdrive mode Note 3	f_{OV}	0.1	—	250	MHz	Functional but may not meet AC parameters Minimum depends on AC coupling Capacitor (0.1 µF assumed)
Frequency in bypass mode Note 4	f_{BP}	0	—	250	MHz	Functional but may not meet AC parameters

Note 1: Values are over recommended operating conditions.

2: Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V).

3: Maximum input level is 2V.

4: Maximum output level is V_{DD}.

TABLE 5-6: POWER SUPPLY REJECTION RATIO FOR V_{DD} = V_{DDO} = 3.3V

Note 1, Note 2, Note 3						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**
PSRR for LVPECL output	$PSRR_{LVPECL}$	—	–71.75	—	dBc	f_{IN} = 156.25 MHz
			–84.45			f_{IN} = 312.5 MHz
			–82.11			f_{IN} = 625 MHz
PSRR for LVDS output	$PSRR_{LVDS}$	—	–95.16	—	dBc	f_{IN} = 156.25 MHz
			–97.77			f_{IN} = 312.5 MHz
			–79.23			f_{IN} = 625 MHz
PSRR for HCSL output	$PSRR_{HCSL}$	—	–77.15	—	dBc	f_{IN} = 100 MHz
			–76.75			f_{IN} = 156.25 MHz
			–80.44			f_{IN} = 312.5 MHz

Note 1: Values are over recommended operating conditions.

2: Noise injected to VDDO power supply with frequency 100 kHz and amplitude 100 mVpp.

3: PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot.

TABLE 5-7: POWER SUPPLY REJECTION RATIO FOR V_{DD} = V_{DDO} = 2.5V

Note 1, Note 2, Note 3

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
PSRR for LVPECL output	$PSRR_{LVPECL}$	—	–73.68	—	dBc	f_{IN} = 156.25 MHz
			–78.88			f_{IN} = 312.5 MHz
			–71.82			f_{IN} = 625 MHz
PSRR for LVDS output	$PSRR_{LVDS}$	—	–90.04	—	dBc	f_{IN} = 156.25 MHz
			–79.99			f_{IN} = 312.5 MHz
			–73.45			f_{IN} = 625 MHz
PSRR for HCSL output	$PSRR_{HCSL}$	—	–92.16	—	dBc	f_{IN} = 100 MHz
			–74.08			f_{IN} = 156.25 MHz
			–91.88			f_{IN} = 312.5 MHz

Note 1: Values are over recommended operating conditions.

2: Noise injected to VDDO power supply with frequency 100 kHz and amplitude 100 mVpp.

3: PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot.

TABLE 5-8: LVCMOS OUTPUT CHARACTERISTICS FOR V_{DDO} = 3.3V

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output high voltage (1 mA load)	V_{OH}	V_{DDO} – 0.1	—	—	V	DC measurement
Output low voltage (1 mA load)	V_{OL}	—	—	0.1	V	DC measurement
Output High Current (Load adjusted to V_{OUT} = V_{DDO}/2)	I_{OH}	—	30	—	mA	DC measurement
Output Low Current (Load adjusted to V_{OUT} = V_{DDO}/2)	I_{OL}	—	34	—	mA	DC measurement
Output impedance	R_O	—	15	—	Ω	DC measurement
Rise time (20% to 80%)	t_R	—	220	310	ps	—
Fall time (20% to 80%)	t_F	—	320	365	ps	—
Output frequency	f_O	0	—	250	MHz	—
Input to output delay	t_{IOD}	1.07	1.28	2.07	ns	—
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	3	cycles	—
Additive RMS jitter in 1 MHz to 5 MHz band	$t_{j\_1M\_5M}$	—	46	80	fs	Input Clock 25 MHz
Additive RMS jitter in 12 kHz to 5 MHz band	$t_{j\_12K\_5M}$	—	56	90	fs	Input Clock 25 MHz
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	60	79	fs	Input Clock 125 MHz
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	65	86	fs	Input Clock 125 MHz
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	61	94	fs	Input Clock 156.25 MHz
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	66	100	fs	Input Clock 156.25 MHz

TABLE 5-8: LVCMOS OUTPUT CHARACTERISTICS FOR V_{DDO} = 3.3V

Noise Floor	N_F	—	–165	–162	dBc/Hz	Input clock: 25 MHz
		—	–160	–156		Input clock: 125 MHz
		—	–158	–153		Input clock: 156.25 MHz

Note 1: Values are over recommended operating conditions.

TABLE 5-9: LVCMOS OUTPUT CHARACTERISTICS FOR V_{DDO} = 2.5V

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output high voltage (1 mA load)	V_{OH}	V_{DDO} – 0.1	—	—	V	DC measurement
Output low voltage (1 mA load)	V_{OL}	—	—	0.1	V	DC measurement
Output High Current (Load adjusted to $V_{OUT} = V_{DDO}/2$)	I_{OH}	—	21	—	mA	DC measurement
Output Low Current (Load adjusted to $V_{OUT} = V_{DDO}/2$)	I_{OL}	—	25	—	mA	DC measurement
Output impedance	R_O	—	15	—	Ω	DC measurement
Rise time (20% to 80%)	t_R	—	225	310	ps	—
Fall time (20% to 80%)	t_F	—	320	365	ps	—
Output frequency	f_O	0	—	250	MHz	—
Input to output delay	t_{IOD}	1.10	1.41	2.30	ns	—
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	3	cycles	—
Additive RMS jitter in 1 MHz to 5 MHz band	$t_{j\_1M\_5M}$	—	51	104	fs	Input Clock 25 MHz
Additive RMS jitter in 12 kHz to 5 MHz band	$t_{j\_12K\_5M}$	—	62	111	fs	Input Clock 25 MHz
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	64	81	fs	Input Clock 125 MHz
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	70	88	fs	Input Clock 125 MHz
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	62	94	fs	Input Clock 156.25 MHz
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	68	100	fs	Input Clock 156.25 MHz
Noise Floor	N_F	—	–164	–161	dBc/Hz	Input clock: 25 MHz
		—	–159	–155		Input clock: 125 MHz
		—	–158	–153		Input clock: 156.25 MHz

Note 1: Values are over recommended operating conditions.

TABLE 5-10: LVPECL OUTPUT CHARACTERISTICS FOR V_{DDO} = 3.3V

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output high voltage	V_{LVPECL_OH}	1.9	2.08	2.4	V	DC Measurement
Output low voltage	V_{LVPECL_OL}	1.2	1.36	1.7	V	DC Measurement
Output differential swing (Note 2)	V_{LVPECL_SW}	0.6	0.72	0.9	V	DC Measurement
Variation of V_{LVPECL_SW} for complementary output states	ΔV_{LVPECL_SW}	0	0.02	0.07	V	—
Common mode output	V_{CM}	1.6	1.72	2.1	V	—
Output frequency when $V_{LVPECL\_SW} \geq 0.6V$	$f_{MAX\_0.6VSW}$	—	—	800	MHz	—
Output frequency when $V_{LVPECL\_SW} \geq 0.4V$	$f_{MAX\_0.4VSW}$	—	—	1600	MHz	—
Rise or fall time (20% to 80%)	t_R/t_F	—	110	170	ps	—
Output frequency	f_O	0	—	1600	MHz	—
Output to output skew	t_{OOSK}	—	—	40	ps	—
Device to device output skew	t_{DOOSK}	—	—	120	ps	—
Input to output delay	t_{IOD}	0.73	0.87	1.1	ns	—
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	3	cycles	—
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	68	96	fs	Input clock: 100 MHz
		—	50	64	fs	Input clock: 156.25 MHz
		—	20	32	fs	Input clock: 625 MHz
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	71	101	fs	Input clock: 100 MHz
		—	55	70	fs	Input clock: 156.25 MHz
		—	25	39	fs	Input clock: 625 MHz
Noise floor	N_F	—	–161	–159	dBc/Hz	Input clock: 100 MHz
		—	–160	–155	dBc/Hz	Input clock: 156.25 MHz
		—	–155	–151	dBc/Hz	Input clock: 625 MHz

Note 1: Values are over recommended operating conditions.

2: Output differential swing is calculated as $V_{SW} = V_{OH} – V_{OL}$. It should not be confused with $V_{SW} = 2 \times (V_{OH} – V_{OL})$ used in some data sheets. Please refer to Figure 5-2.

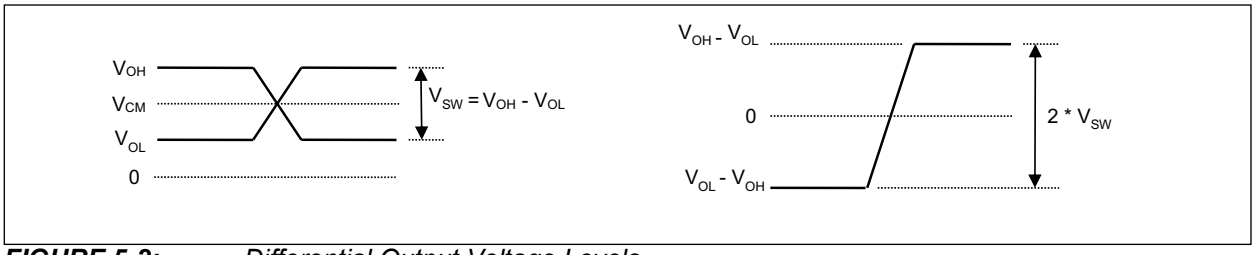


FIGURE 5-2: *Differential Output Voltage Levels.*

TABLE 5-11: LVPECL OUTPUT CHARACTERISTICS FOR V_{DDO} = 2.5V

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output high voltage	V_{LVPECL_OH}	1.1	1.28	1.7	V	DC Measurement
Output low voltage	V_{LVPECL_OL}	0.4	0.57	0.9	V	DC Measurement
Output differential swing (Note 2)	V_{LVPECL_SW}	0.6	0.71	0.9	V	DC Measurement
Variation of V_{LVPECL_SW} for complementary output states	ΔV_{LVPECL_SW}	0	0.02	0.05	V	—
Common mode output	V_{CM}	0.8	0.92	1.2	V	—
Output frequency when $V_{LVPECL\_SW} \geq 0.6V$	$f_{MAX\_0.6VSW}$	—	—	800	MHz	—
Output frequency when $V_{LVPECL\_SW} \geq 0.4V$	$f_{MAX\_0.4VSW}$	—	—	1600	MHz	—
Rise or fall time (20% to 80%)	t_R/t_F	—	120	170	ps	—
Output frequency	f_O	—	—	1600	MHz	—
Output to output skew	t_{OOSK}	—	—	40	ps	—
Device to device output skew	t_{DOOSK}	—	—	120	ps	—
Input to output delay	t_{IOD}	0.75	0.87	1.1	ns	—
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	3	cycles	—
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	65	91	fs	Input clock: 100 MHz
		—	50	64	fs	Input clock: 156.25 MHz
		—	20	30	fs	Input clock: 625 MHz
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	69	99	fs	Input clock: 100 MHz
		—	54	75	fs	Input clock: 156.25 MHz
		—	26	41	fs	Input clock: 625 MHz
Noise floor	N_F	—	–161	–159	dBc/Hz	Input clock: 100 MHz
		—	–160	–156	dBc/Hz	Input clock: 156.25 MHz
		—	–155	–151	dBc/Hz	Input clock: 625 MHz

Note 1: Values are over recommended operating conditions.

2: Output differential swing is calculated as $V_{SW} = V_{OH} – V_{OL}$. It should not be confused with $V_{SW} = 2 \times (V_{OH} – V_{OL})$ used in some data sheets. Please refer to Figure 5-2.

TABLE 5-12: LVDS OUTPUTS FOR V_{DDO} = 3.3V

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output high voltage	V_{LVDS_OH}	1.3	1.39	1.47	V	DC Measurement
Output low voltage	V_{LVDS_OL}	1.0	1.07	1.15	V	DC Measurement
Output differential swing (Note 2)	V_{LVDS_SW}	0.25	0.32	0.39	V	DC Measurement
Variation of V_{LVDS_SW} for complementary output states	ΔV_{LVDS_SW}	0	0.002	0.01	V	—
Common mode output	V_{CM}	1.15	1.23	1.3	V	—
Variation of V_{CM} for complementary output states	ΔV_{CM}	0	0.001	0.01	V	—
Output frequency when $V_{LVDS\_SW} \geq 250$ mV	$f_{MAX\_0.25VSW}$	—	—	800	MHz	—
Output frequency when $V_{LVDS\_SW} \geq 200$ mV	$f_{MAX\_0.2VSW}$	—	—	1600	MHz	—
Rise or fall time (20% to 80%)	t_R/t_F	—	110	170	ps	—
Output frequency	f_O	0	—	1600	MHz	—
Output to output skew	t_{OOSK}	—	—	20	ps	—
Device to device output skew	t_{DOOSK}	—	—	130	ps	—
Input to output delay	t_{IOD}	0.76	0.86	1.1	ns	—
Output Short Circuit Current Single-Ended	I_S	–24	—	24	mA	Single-ended outputs shorted to GND
Output Short Circuit Current Differential	I_{SD}	–24	—	24	mA	Complementary outputs shorted
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	3	cycles	—
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	110	144	fs	Input clock: 100 MHz
		—	63	81	fs	Input clock: 156.25 MHz
		—	21	33	fs	Input clock: 625 MHz
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	115	150	fs	Input clock: 100 MHz
		—	73	102	fs	Input clock: 156.25 MHz
		—	26	40	fs	Input clock: 625 MHz
Noise floor	N_F	—	–158	–156	fs	Input clock: 100 MHz
		—	–158	–155	fs	Input clock: 156.25 MHz
		—	–154	–151	fs	Input clock: 625 MHz

Note 1: Values are over recommended operating conditions.

2: Output differential swing is calculated as $V_{SW} = V_{OH} – V_{OL}$. It should not be confused with $V_{SW} = 2 \times (V_{OH} – V_{OL})$ used in some data sheets. Please refer to Figure 5-2.

TABLE 5-13: LVDS OUTPUTS FOR V_{DDO} = 2.5V

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output high voltage	V_{LVDS_OH}	1.3	1.4	1.5	V	DC Measurement
Output low voltage	V_{LVDS_OL}	0.97	1.05	1.13	V	DC Measurement
Output differential swing (Note 2)	V_{LVDS_SW}	0.25	0.35	0.44	V	DC Measurement
Variation of V_{LVDS_SW} for complementary output states	ΔV_{LVDS_SW}	0	0.001	0.01	V	—

TABLE 5-13: LVDS OUTPUTS FOR V_{DDO} = 2.5V (CONTINUED)

Common mode output	V_{CM}	1.15	1.23	1.3	V	—
Variation of V_{CM} for complementary output states	ΔV_{CM}	0	0.001	0.01	V	—
Output frequency when $V_{LVDS\_SW} \geq 250$ mV	$f_{MAX\_0.25VSW}$	—	—	800	MHz	—
Output frequency when $V_{LVDS\_SW} \geq 200$ mV	$f_{MAX\_0.2VSW}$	—	—	1600	MHz	—
Rise or fall time (20% to 80%)	t_R/t_F	—	110	170	ps	—
Output frequency	f_O	0	—	1600	MHz	—
Output to output skew	t_{OOSK}	—	—	20	ps	—
Device to device output skew	t_{DOOSK}	—	—	130	ps	—
Input to output delay	t_{IOD}	0.78	0.86	1.12	ns	—
Output Short Circuit Current Single-Ended	I_S	–24	—	24	mA	Single-ended outputs shorted to GND
Output Short Circuit Current Differential	I_{SD}	–24	—	24	mA	Complementary outputs shorted
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	3	cycles	—
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	107	140	fs	Input clock: 100 MHz
		—	62	77	fs	Input clock: 156.25 MHz
		—	20	31	fs	Input clock: 625 MHz
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	111	146	fs	Input clock: 100 MHz
		—	66	83	fs	Input clock: 156.25 MHz
		—	24	36	fs	Input clock: 625 MHz
Noise floor	N_F	—	–158	–156	fs	Input clock: 100 MHz
		—	–159	–155	fs	Input clock: 156.25 MHz
		—	–155	–151	fs	Input clock: 625 MHz

Note 1: Values are over recommended operating conditions.

2: Output differential swing is calculated as $V_{SW} = V_{OH} - V_{OL}$. It should not be confused with $V_{SW} = 2 \times (V_{OH} - V_{OL})$ used in some data sheets. Please refer to Figure 5-2.

TABLE 5-14: HCSL OUTPUTS FOR V_{DDO} = 3.3V

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output high voltage	V_{HCSL_OH}	0.6	0.85	1.1	V	DC Measurement
Output low voltage	V_{HCSL_OL}	–0.05	0	0.05	V	DC Measurement
Output differential swing (Note 2)	V_{HCSL_SW}	0.6	0.85	1.1	V	DC Measurement
Variation of V_{HCSL_SW} for complementary output states	ΔV_{HCSL_SW}	0	0.003	0.05	V	—
Common mode output	V_{CM}	0.28	0.43	0.55	V	—
Variation of V_{CM} for complementary output states	ΔV_{CM}	0	0.002	0.05	V	—
Absolute Crossing Voltage	V_{CROSS}	0.320	0.384	0.447	V	—
Total Variation of V_{CROSS}	ΔV_{CROSS}	—	—	0.127	V	—
Output frequency	f_{MAX}	0	—	400	MHz	—
Rise or fall time (20% to 80%)	t_R/t_F	—	143	309	ps	—
Output to output skew	t_{OOSK}	—	—	21	ps	—

TABLE 5-14: HCSL OUTPUTS FOR V_{DDO} = 3.3V (CONTINUED)

Device to device output skew	t_{DOOSK}	—	—	129	ps	—
Input to output delay	t_{IOD}	0.73	0.90	1.08	ns	—
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	3	cycles	—
Additive Jitter as per PCIe 3.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$t_{jPCIe\_3.0}$	—	20	40	fs	Input clock: 100 MHz
Additive Jitter as per PCIe 4.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$t_{jPCIe\_4.0}$	—	20	40	fs	Input clock: 100 MHz
Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 MHz to 1.8 MHz, CDR for 32 GT/s CC)	$t_{jPCIe\_5.0}$	—	13	19	fs	Input clock: 100 MHz
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	73	104	fs	Input clock: 100 MHz
		—	53	69	fs	Input clock: 156.25 MHz
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	77	112	fs	Input clock: 100 MHz
		—	64	100	fs	Input clock: 156.25 MHz
Noise floor	N_F	—	–161	–159	dBc/Hz	Input clock: 100 MHz
		—	–159	–155	dBc/Hz	Input clock: 156.25 MHz

Note 1: Values are over recommended operating conditions.

2: Output differential swing is calculated as $V_{SW} = V_{OH} – V_{OL}$. It should not be confused with $V_{SW} = 2 \times (V_{OH} – V_{OL})$ used in some data sheets. Please refer to Figure 5-2.

TABLE 5-15: HCSL OUTPUTS FOR V_{DDO} = 2.5V

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output high voltage	V_{HCSL_OH}	0.6	0.83	1.1	V	DC Measurement
Output low voltage	V_{HCSL_OL}	–0.05	0	0.05	V	DC Measurement
Output differential swing (Note 2)	V_{HCSL_SW}	0.5	0.83	1.1	V	DC Measurement
Variation of V_{HCSL_SW} for complementary output states	ΔV_{HCSL_SW}	0	0.003	0.05	V	—
Common mode output	V_{CM}	0.28	0.42	0.55	V	—
Variation of V_{CM} for complementary output states	ΔV_{CM}	0	0.002	0.05	V	—
Absolute Crossing Voltage	V_{CROSS}	0.260	0.316	0.372	V	—
Total Variation of V_{CROSS}	ΔV_{CROSS}	—	—	0.108	V	—
Output frequency	f_{MAX}	0	—	400	MHz	—
Rise or fall time (20% to 80%)	t_R/t_F	—	125	162	ps	—
Output to output skew	t_{OOSK}	—	—	21	ps	—
Device to device output skew	t_{DOOSK}	—	—	129	ps	—
Input to output delay	t_{IOD}	0.76	0.92	1.10	ns	—
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	3	cycles	—
Additive Jitter as per PCIe 3.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$t_{jPCIe\_3.0}$	—	20	40	fs	Input clock: 100 MHz

TABLE 5-15: HCSL OUTPUTS FOR V_{DDO} = 2.5V (CONTINUED)

Additive Jitter as per PCIe 4.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$t_{jPCIe\_4.0}$	—	20	40	fs	Input clock: 100 MHz
Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 MHz to 1.8 MHz, CDR for 32 GT/s CC)	$t_{jPCIe\_5.0}$	—	13	19	fs	Input clock: 100 MHz
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	68	95	fs	Input clock: 100 MHz
		—	52	66	fs	Input clock: 156.25 MHz
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	72	102	fs	Input clock: 100 MHz
		—	56	71	fs	Input clock: 156.25 MHz
Noise floor	N_F	—	–161	–158	dBc/Hz	Input clock: 100 MHz
		—	–160	–153	dBc/Hz	Input clock: 156.25 MHz

Note 1: Values are over recommended operating conditions.

2: Output differential swing is calculated as $V_{SW} = V_{OH} – V_{OL}$. It should not be confused with $V_{SW} = 2 \times (V_{OH} – V_{OL})$ used in some data sheets. Please refer to Figure 5-2.

TABLE 5-16: LVCMOS OUTPUT PHASE NOISE WITH 25 MHZ XTAL

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Jitter RMS in 12 kHz to 5 MHz band	$t_{J\_12k\_5M}$	—	103	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	117	—		V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise floor	N_F	—	–75	—	dBc/Hz	V_{DD} = 3.3V, V_{DDO} = 3.3V @10 Hz
		—	–107	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 Hz
		—	–132	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 kHz
		—	–150	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 kHz
		—	–162	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 kHz
		—	–166	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 MHz
		—	–166	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @5 MHz
		—	–70	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 Hz
		—	–102	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 Hz
		—	–130	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 kHz
		—	–149	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 kHz
		—	–161	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 kHz
		—	–165	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 MHz
		—	–165	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @5 MHz

Note 1: Values are over recommended operating conditions.

TABLE 5-17: LVPECL OUTPUT PHASE NOISE WITH 25 MHZ XTAL

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Jitter RMS in 12 kHz to 5 MHz band	$t_{J\_12k\_5M}$	—	265	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	213	—		V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise floor	N_F	—	–75	—	dBc/Hz	V_{DD} = 3.3V, V_{DDO} = 3.3V @10 Hz
		—	–107	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 Hz
		—	–133	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 kHz
		—	–152	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 kHz
		—	–157	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 kHz
		—	–158	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 MHz
		—	–157	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @5 MHz
		—	–71	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 Hz
		—	–103	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 Hz
		—	–130	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 kHz
		—	–151	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 kHz
		—	–158	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 kHz
		—	–160	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 MHz
		—	–159	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @5 MHz

Note 1: Values are over recommended operating conditions.

TABLE 5-18: LVDS OUTPUT PHASE NOISE WITH 25 MHZ XTAL

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Jitter RMS in 12 kHz to 5 MHz band	$t_{J\_12k\_5M}$	—	178	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	190	—		V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise floor	N_F	—	–75	—	dBc/Hz	V_{DD} = 3.3V, V_{DDO} = 3.3V @10 Hz
		—	–107	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 Hz
		—	–133	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 kHz
		—	–154	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 kHz
		—	–161	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 kHz
		—	–161	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 MHz
		—	–160	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @5 MHz
		—	–68	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 Hz
		—	–103	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 Hz
		—	–130	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 kHz
		—	–152	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 kHz
		—	–161	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 kHz
		—	–160	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 MHz
		—	–159	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @5 MHz

Note 1: Values are over recommended operating conditions.

TABLE 5-19: HCSL OUTPUT PHASE NOISE WITH 25 MHZ XTAL

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Jitter RMS in 12 kHz to 5 MHz band	$t_{J\_12k\_5M}$	—	269	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	228	—		V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise floor	N_F	—	–76	—	dBc/Hz	V_{DD} = 3.3V, V_{DDO} = 3.3V @10 Hz
		—	–107	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 Hz
		—	–133	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 kHz
		—	–152	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 kHz
		—	–157	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 kHz
		—	–157	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 MHz
		—	–157	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @5 MHz
		—	–73	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 Hz
		—	–105	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 Hz
		—	–131	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 kHz
		—	–151	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 kHz
		—	–158	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 kHz
		—	–159	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 MHz
		—	–159	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @5 MHz

Note 1: Values are over recommended operating conditions.

TABLE 5-20: LVCMOS OUTPUT PHASE NOISE WITH 125 MHZ XTAL

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Jitter RMS in 12 kHz to 5 MHz band	$t_{J\_12k\_5M}$	—	92	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	105	—		V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise floor	N_F	—	–58	—	dBc/Hz	V_{DD} = 3.3V, V_{DDO} = 3.3V @10 Hz
		—	–90	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 Hz
		—	–118	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 kHz
		—	–136	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 kHz
		—	–150	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 kHz
		—	–158	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 MHz
		—	–159	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 MHz
		—	–53	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 Hz
		—	–86	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 Hz
		—	–113	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 kHz
		—	–134	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 kHz
		—	–148	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 kHz
		—	–157	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 MHz
		—	–158	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 MHz

Note 1: Values are over recommended operating conditions.

TABLE 5-21: LVPECL OUTPUT PHASE NOISE WITH 125 MHZ XTAL

Note 1

Parameter	Symbol	Min	Typ.	Max	Units	Condition
Jitter RMS in 12 kHz to 5 MHz band	$t_{J\_12k\_5M}$	—	76	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	86	—		V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise floor	N_F	—	–58	—	dBc/Hz	V_{DD} = 3.3V, V_{DDO} = 3.3V @10 Hz
		—	–90	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 Hz
		—	–118	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 kHz
		—	–140	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 kHz
		—	–154	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 kHz
		—	–159	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 MHz
		—	–161	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 MHz
		—	–54	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 Hz
		—	–86	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 Hz
		—	–114	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 kHz
		—	–137	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 kHz
		—	–152	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 kHz
		—	–158	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 MHz
		—	–160	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 MHz

Note 1: Values are over recommended operating conditions.

TABLE 5-22: LVDS OUTPUT PHASE NOISE WITH 125 MHZ XTAL

Note 1

Parameter	Symbol	Min	Typ.	Max	Units	Condition
Jitter RMS in 12 kHz to 5 MHz band	$t_{J\_12k\_5M}$	—	98	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	100	—		V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise floor	N_F	—	–57	—	dBc/Hz	V_{DD} = 3.3V, V_{DDO} = 3.3V @10 Hz
		—	–90	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 Hz
		—	–118	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 kHz
		—	–140	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 kHz
		—	–152	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 kHz
		—	–157	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 MHz
		—	–158	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 MHz
		—	–54	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 Hz
		—	–86	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 Hz
		—	–114	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 kHz
		—	–137	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 kHz
		—	–153	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 kHz
		—	–157	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 MHz
		—	–158	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 MHz

Note 1: Values are over recommended operating conditions.

TABLE 5-23: HCSL OUTPUT PHASE NOISE WITH 125 MHZ XTAL

Note 1

Parameter	Symbol	Min	Typ.	Max	Units	Condition
Jitter RMS in 12 kHz to 5 MHz band	$t_{J\_12k\_5M}$	—	83	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	85	—		V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise floor	N_F	—	–58	—	dBc/Hz	V_{DD} = 3.3V, V_{DDO} = 3.3V @10 Hz
		—	–90	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 Hz
		—	–118	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 kHz
		—	–140	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 kHz
		—	–152	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 kHz
		—	–158	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 MHz
		—	–160	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 MHz
		—	–54	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 Hz
		—	–86	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 Hz
		—	–114	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 kHz
		—	–137	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 kHz
		—	–153	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 kHz
		—	–158	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 MHz
		—	–159	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 MHz

Note 1: Values are over recommended operating conditions.

TABLE 5-24: LVCMOS OUTPUT PHASE NOISE WITH 156.25 MHZ XTAL

Note 1

Parameter	Symbol	Min	Typ.	Max	Units	Condition
Jitter RMS in 12 kHz to 5 MHz band	$t_{J\_12k\_5M}$	—	79	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	88	—		V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise floor	N_F	—	–53	—	dBc/Hz	V_{DD} = 3.3V, V_{DDO} = 3.3V @10 Hz
		—	–81	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 Hz
		—	–111	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 kHz
		—	–135	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 kHz
		—	–149	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 kHz
		—	–157	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 MHz
		—	–159	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 MHz
		—	–53	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 Hz
		—	–82	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 Hz
		—	–113	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 kHz
		—	–135	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 kHz
		—	–148	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 kHz
		—	–156	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 MHz
		—	–158	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 MHz

Note 1: Values are over recommended operating conditions.

TABLE 5-25: LVPECL OUTPUT PHASE NOISE WITH 156.25 MHZ XTAL

Note 1

Parameter	Symbol	Min	Typ.	Max	Units	Condition
Jitter RMS in 12 kHz to 5 MHz band	$t_{J\_12k\_5M}$	—	61	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	68	—		V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise floor	N_F	—	–52	—	dBc/Hz	V_{DD} = 3.3V, V_{DDO} = 3.3V @10 Hz
		—	–80	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 Hz
		—	–111	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 kHz
		—	–140	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 kHz
		—	–153	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 kHz
		—	–159	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 MHz
		—	–161	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 MHz
		—	–53	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 Hz
		—	–81	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 Hz
		—	–114	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 kHz
		—	–140	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 kHz
		—	–151	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 kHz
		—	–158	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 MHz
		—	–160	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 MHz

Note 1: Values are over recommended operating conditions.

TABLE 5-26: LVDS OUTPUT PHASE NOISE WITH 156.25 MHZ XTAL

Note 1

Parameter	Symbol	Min	Typ.	Max	Units	Condition
Jitter RMS in 12 kHz to 5 MHz band	$t_{J\_12k\_5M}$	—	79	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	76	—		V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise floor	N_F	—	–52	—	dBc/Hz	V_{DD} = 3.3V, V_{DDO} = 3.3V @10 Hz
		—	–81	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 Hz
		—	–111	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 kHz
		—	–138	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 kHz
		—	–148	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 kHz
		—	–157	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 MHz
		—	–159	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 MHz
		—	–52	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 Hz
		—	–82	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 Hz
		—	–113	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 kHz
		—	–140	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 kHz
		—	–151	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 kHz
		—	–157	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 MHz
		—	–159	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 MHz

Note 1: Values are over recommended operating conditions.

TABLE 5-27: HCSL OUTPUT PHASE NOISE WITH 156.25 MHZ XTAL

Note 1

Parameter	Symbol	Min	Typ.	Max	Units	Condition
Jitter RMS in 12 kHz to 5 MHz band	$t_{J\_12k\_5M}$	—	72	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	72	—		V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise floor	N_F	—	–53	—	dBc/Hz	V_{DD} = 3.3V, V_{DDO} = 3.3V @10 Hz
		—	–86	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 Hz
		—	–114	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 kHz
		—	–139	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 kHz
		—	–148	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 kHz
		—	–157	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 MHz
		—	–160	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 MHz
		—	–53	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 Hz
		—	–86	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 Hz
		—	–115	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 kHz
		—	–140	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 kHz
		—	–151	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 kHz
		—	–157	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 MHz
		—	–160	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 MHz

Note 1: Values are over recommended operating conditions.

TABLE 5-28: SERIAL PERIPHERAL INTERFACE (SPI) TIMING

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
sck period	tcyc	124	—	—	ns	See Figure 5-3 and Figure 5-4
sck pulse width low	tclkl	62	—	—	ns	
sck pulse width high	tclkh	62	—	—	ns	
si setup (write) from sck rising edge	trxs	10	—	—	ns	
si hold (write) from sck falling edge	trxh	10	—	—	ns	
so delay (read) from sck falling edge	txd	—	—	25	ns	
cs_b to output high impedance	tohz	—	—	60	ns	
cs_b setup from sck falling edge (LSB first)	tcssi	20	—	—	ns	See Figure 5-3
cs_b hold from sck falling edge (LSB first)	tcshi	10	—	—	ns	
cs_b setup from sck falling edge (MSB first)	tcssm	20	—	—	ns	See Figure 5-4
cs_b hold from sck falling edge (MSB first)	tcshm	10	—	—	ns	

Note 1: Values are over Recommended Operating Conditions. For LSB first mode timing diagram, refer to Figure 5-3. For MSB first mode timing diagram, refer to Figure 5-4. Values shown are proposed for the data sheet, these values are to be confirmed.

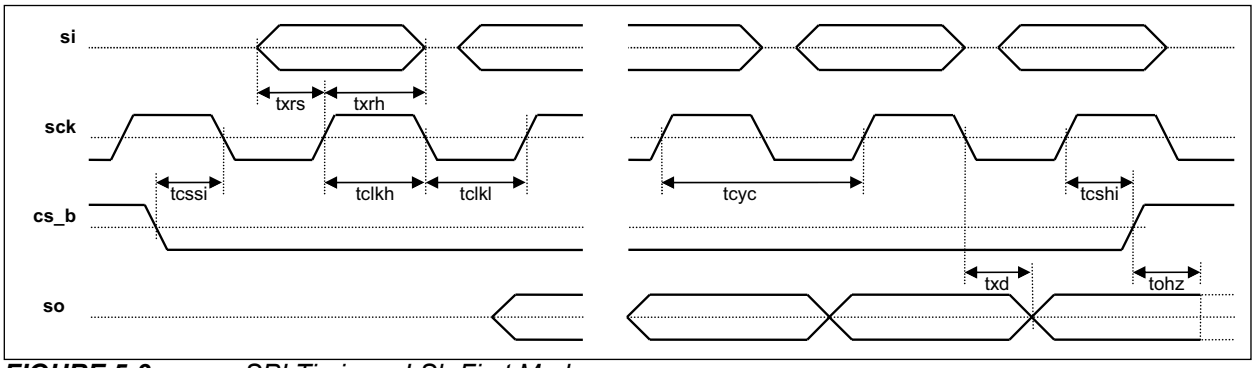


FIGURE 5-3: *SPI Timing – LSb First Mode.*

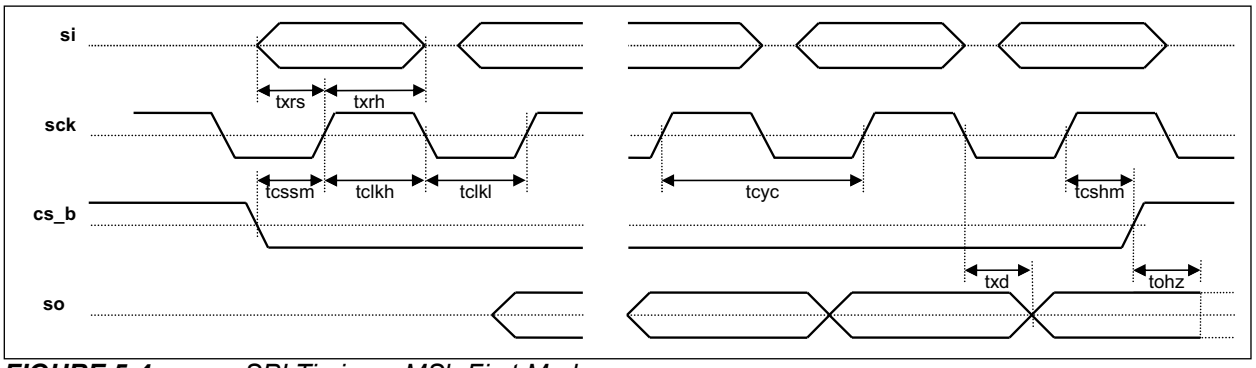


FIGURE 5-4: *SPI Timing – MSb First Mode.*

THERMAL SPECIFICATIONS

Parameter	Symbol	Condition	Value	Units
Maximum Ambient Temperature	T_A	—	85	°C
Maximum Junction Temperature	$T_{J(MAX)}$	—	125	°C
Package Thermal Resistance, 6x6 VQFN 40-Lead				
Junction to Ambient Thermal Resistance Note 1	θ_{JA}	Still air	22.2	°C/W
		1m/s airflow	17.6	°C/W
		2.5 m/s airflow	15.8	°C/W
Junction to Board Thermal Resistance	θ_{JB}	—	7.2	°C/W
Junction to Case Thermal Resistance	θ_{JC}	—	14.3	°C/W
Junction to Pad Thermal Resistance Note 2	θ_{JP}	Still air	3.9	°C/W
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	Still air	0.2	°C/W

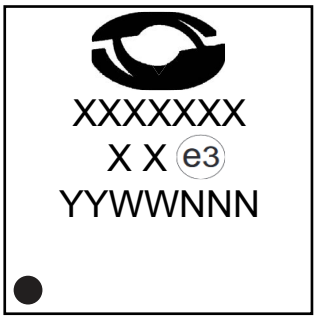
Note 1: Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on an 4-layer JEDEC standard test board and dissipating maximum power.

2: Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package).

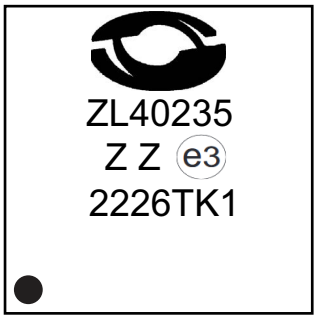
6.0 PACKAGE OUTLINE

6.1 Package Marking Information

40-Lead VQFN*



Example



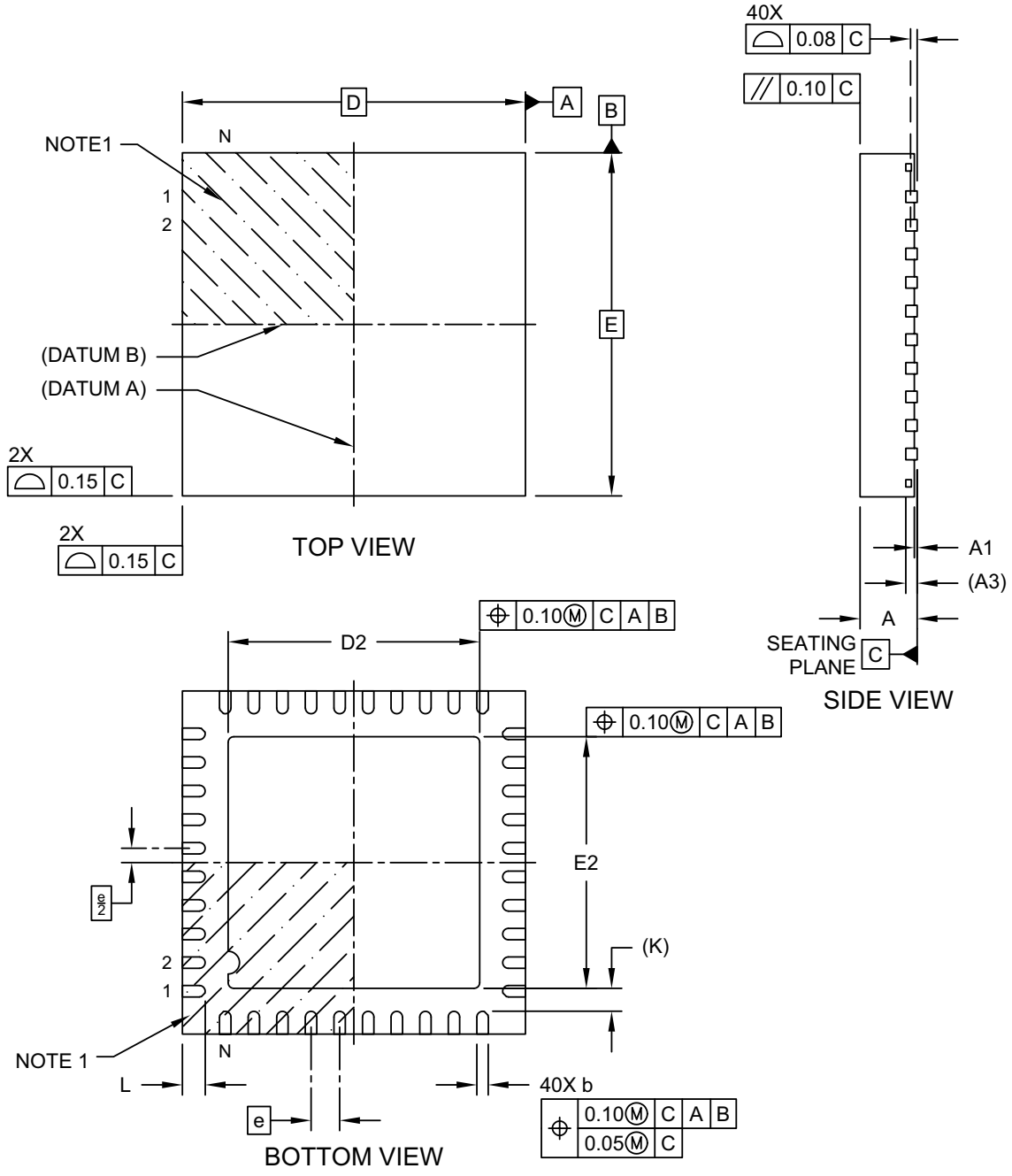
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

40-Lead Very Thin Plastic Quad Flat, No Lead Package (M6C) - 6x6x1 mm Body [VQFN] With 4.3 mm Exposed Pad; Microsemi Legacy Package

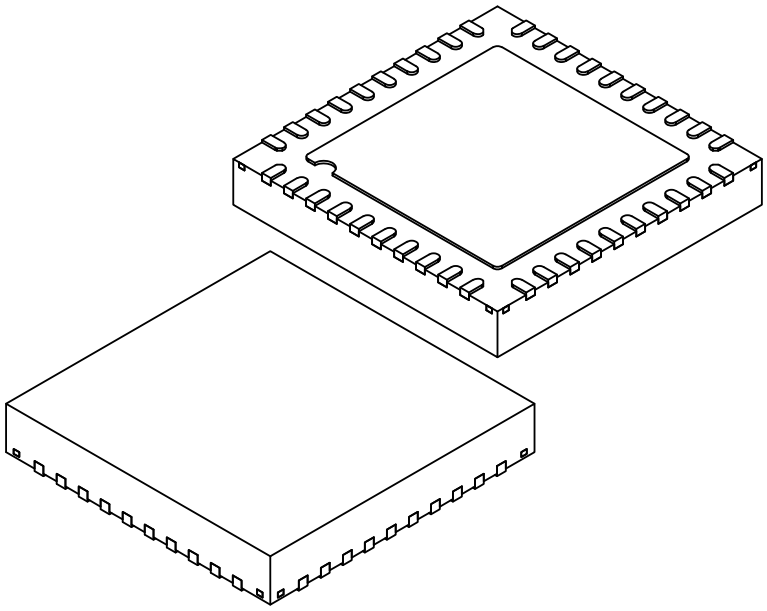
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-25403 Rev A Sheet 1 of 2

40-Lead Very Thin Plastic Quad Flat, No Lead Package (M6C) - 6x6x1 mm Body [VQFN] With 4.3 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		40	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.20	4.30	4.40
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.20	4.30	4.40
Terminal Width	b	0.18	0.23	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K		0.50 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

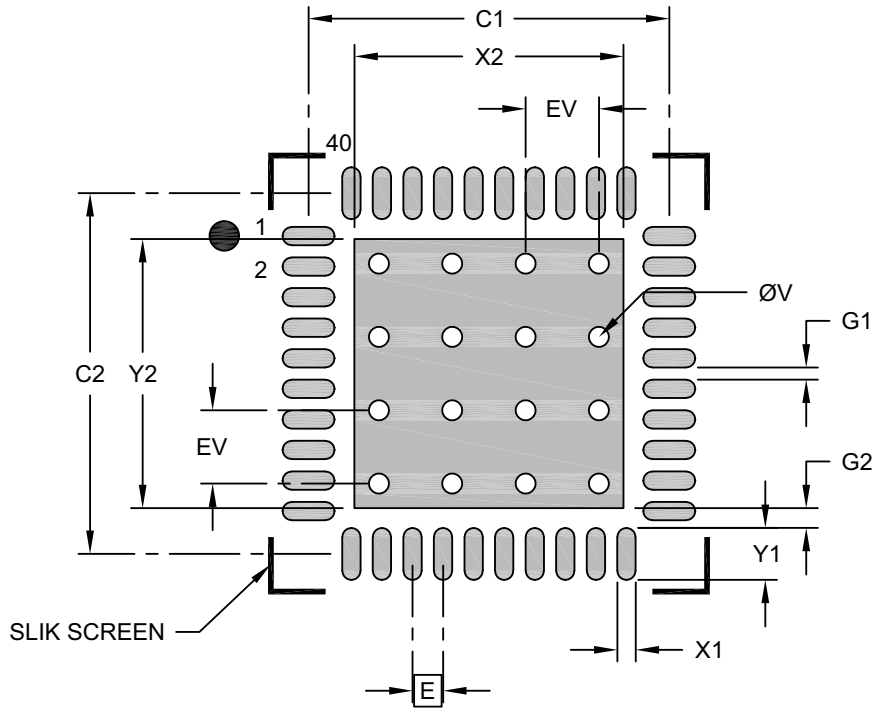
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25403 Rev A Sheet 2 of 2

40-Lead Very Thin Plastic Quad Flat, No Lead Package (M6C) - 6x6x1 mm Body [VQFN] With 4.3 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			4.40
Center Pad Length	Y2			4.40
Contact Pad Spacing	C1		5.90	
Contact Pad Spacing	C2		5.90	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.85
Contact Pad to Center Pad (Xnn)	G1	0.33		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-27403 Rev A

NOTES:

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS20006807A (12-14-23)	—	Converted Microsemi data sheet ZL40235 to Microchip DS20006807A. Minor text changes throughout.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	X	X
Device	Chip Carrier Type	Package	Media Type	Finish

Device:	ZL40235: Low Skew, Low Additive Jitter 3 x 5 Output LVPECL/ LVDS/HCSL Fanout Buffer with One LVCMOS Output
Chip Carrier Type:	L = Leadless Chip Carrier
Package:	D = 40-Lead VQFN Package
Media Type:	G = 490/Tray F = 4,000/Reel
Finish:	1 = Pb Free with Matte Sn Lead Finish Equating to RoHS e3

Examples:

a) ZL40235LDG1: ZL40235, Leadless Chip Carrier, 40-Lead VQFN Package, 490/ Tray, Pb Free with Matte Sn Lead Finish Equating to RoHS e3

b) ZL40235LDF1: ZL40235, Leadless Chip Carrier, 40-Lead VQFN Package, 4,000/ Reel, Pb Free with Matte Sn Lead Finish Equating to RoHS e3

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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