TC8020

Six-Pair N-Channel and P-Channel Enhancement-Mode MOSFET

Features

- High-voltage Vertical DMOS Technology
- Integrated Gate-to-Source Resistor
- Integrated Gate-to-Source Zener Diode
- +/–3.5A at 50V Typical Peak Output
- Low Threshold, Low On-resistance
- Low Input and Output Capacitance
- Fast Switching Speeds
- Electrically Isolated N-channel and P-channel MOSFET Pairs

Applications

- High-voltage Pulsers
- Amplifiers
- Buffers
- Piezoelectric Transducer Drivers
- General Purpose Line Drivers
- Logic-level Interfaces

General Description

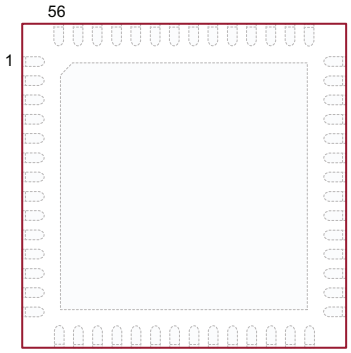
The TC8020 consists of six pairs of high-voltage, low-threshold N-channel and P-channel MOSFETs in a 56-lead VQFN package. All MOSFETs have integrated the output drain high-voltage diodes, gate-to-source resistors, and gate-to-source Zener diode clamps which are desired for high-voltage pulser applications. The complimentary, high-speed, high-voltage, gate-clamped N-channel and P-channel MOSFET pairs utilize an advanced vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input and output capacitance, and fast switching speeds are desired.

Package Type

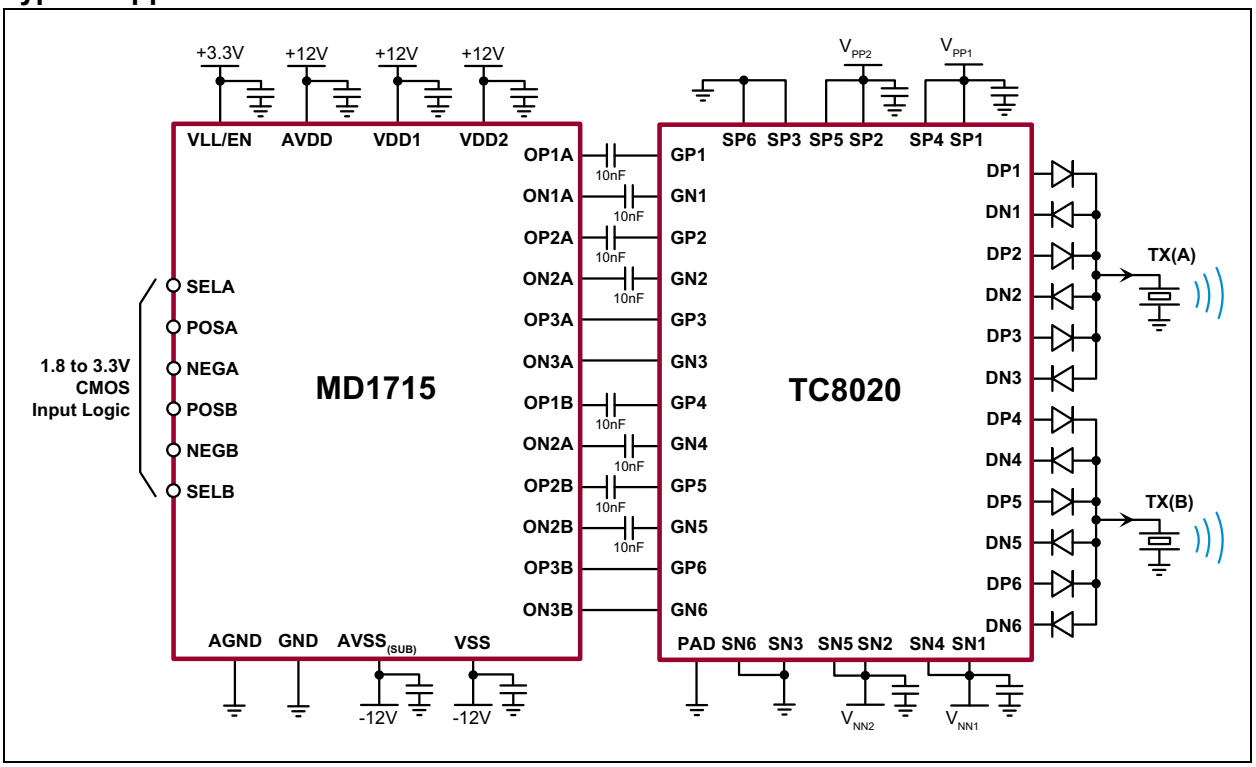
56-lead VQFN

(Top view)

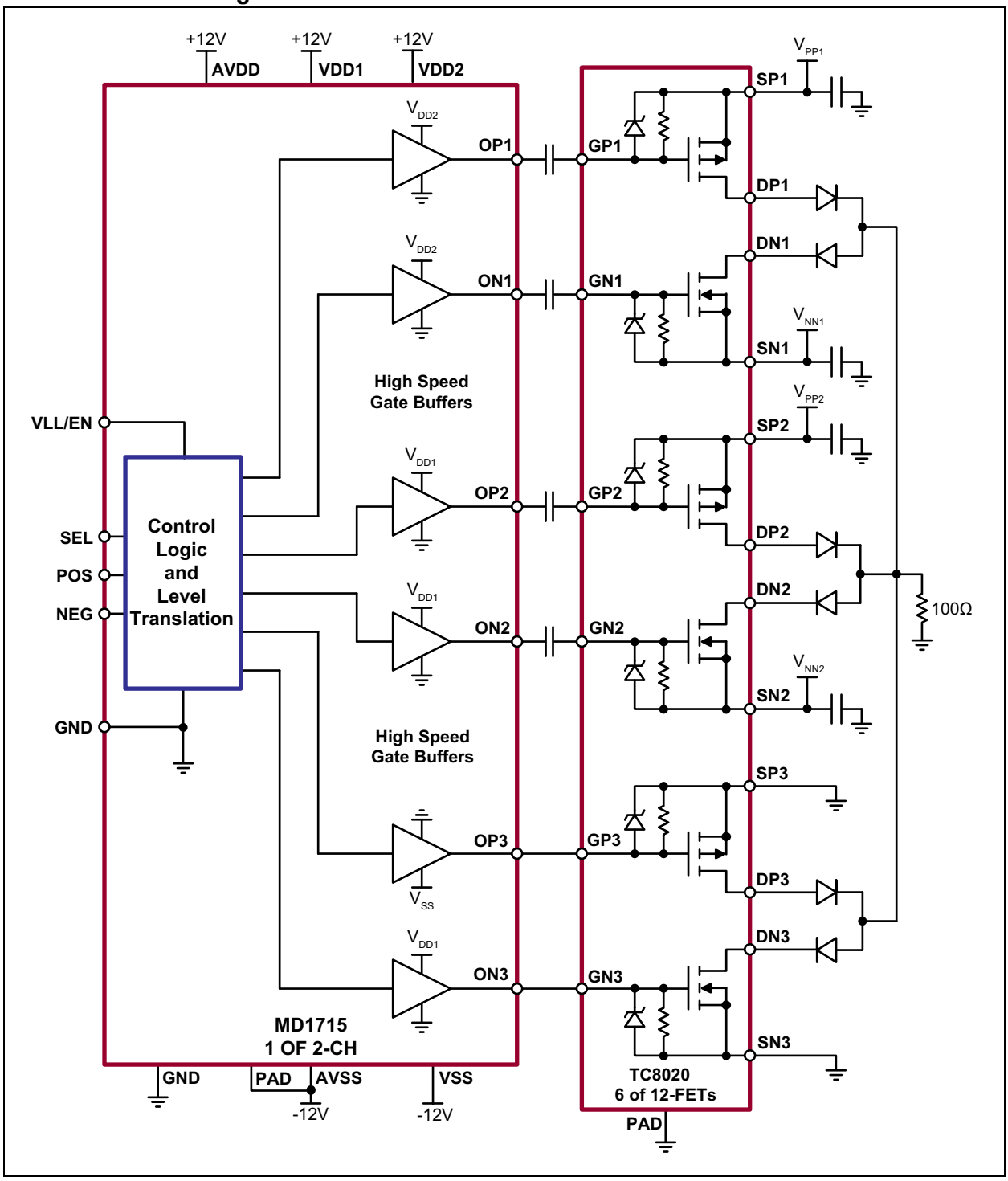


See Table 2-1 for pin information.

Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Drain-to-Source Voltage ..... BV_{DSS}
Drain-to-Gate Voltage ..... BV_{DGS}
Operating Ambient Temperature, T_A ..... –55°C to +150°C
Storage Temperature, T_S ..... –55°C to +150°C

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

N-CHANNEL ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = 25°C.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
DC PARAMETER (Note 1)						
Drain-to-Source Breakdown Voltage	BV_{DSS}	200	—	—	V	V_{GS} = 0V, I_D = 1 mA
Gate Threshold Voltage	$V_{GS(th)}$	1	—	2.4	V	V_{GS} = V_{DS}, I_D = 1 mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	–4.5	mV/°C	V_{GS} = V_{DS}, I_D = 1 mA (Note 2)
Gate-to-Source Shunt Resistor	R_{GS}	5	—	26	kΩ	I_{GS} = 100 µA
Gate-to-Source Zener voltage	VZ_{GS}	13.2	—	25	V	I_{GS} = 2 mA
Zero-gate Voltage Drain Current	I_{DSS}	—	—	10	µA	V_{DS} = Maximum rating, V_{GS} = 0V
		—	—	1	mA	V_{DS} = 0.8 Maximum rating, V_{GS} = 0V, T_A = 125°C (Note 2)
On-state Drain Current	$I_{D(ON)}$	1.2	1.8	—	A	V_{GS} = 4.5V, V_{DS} = 25V
		2	3.2	—		V_{GS} = 10V, V_{DS} = 25V
Static Drain-to-Source On-state Resistance	$R_{DS(ON)}$	—	6	9	Ω	V_{GS} = 4.5V, I_D = 150 mA
		—	5.3	8		V_{GS} = 10V, I_D = 1A
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	1	%/°C	V_{GS} = 10V, I_D = 1A (Note 2)
AC PARAMETER (Note 2)						
Forward Transconductance	G_{FS}	400	—	—	mmho	V_{DS} = 25V, I_D = 500 mA
Input Capacitance	C_{ISS}	—	50	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1 MHz
Common-source Output Capacitance	C_{OSS}	—	18	—		
Reverse Transfer Capacitance	C_{RSS}	—	7	—		
Turn-on Delay Time	$t_{d(ON)}$	—	—	10	ns	V_{DD} = 25V, I_D = 500 mA, R_{GEN} = 25Ω
Rise Time	t_r	—	—	15		
Turn-off Delay Time	$t_{d(OFF)}$	—	—	20		
Fall Time	t_f	—	—	15		
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	1.8	V	V_{GS} = 0V, I_{SD} = 500 mA (Note 1)
Reverse Recovery Time	t_{rr}	—	300	—	ns	V_{GS} = 0V, I_{SD} = 500 mA (Note 2)

Note 1: Unless otherwise stated, all DC parameters are 100% tested at +25°C. Pulse test: 300 µs pulse, 2% duty cycle.

2: Specification is obtained by characterization and is not 100% tested.

P-CHANNEL ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = 25°C.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
DC PARAMETER (Note 1)						
Drain-to-Source Breakdown Voltage	BV_{DSS}	–200	—	—	V	V_{GS} = 0V, I_D = –1 mA
Gate Threshold Voltage	$V_{GS(th)}$	–1	—	–2.4	V	V_{GS} = V_{DS}, I_D = –1 mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	4.5	mV/°C	V_{GS} = V_{DS}, I_D = –1 mA (Note 2)
Gate-to-Source Shunt Resistor	R_{GS}	5	—	26	kΩ	I_{GS} = –100 µA
Gate-to-Source Zener Voltage	VZ_{GS}	–13.2	—	–24	V	I_{GS} = –2 mA
Zero-gate Voltage Drain Current	I_{DSS}	—	—	–10	µA	V_{DS} = Maximum rating, V_{GS} = 0V
		—	—	–1	mA	V_{DS} = 0.8 Maximum rating, V_{GS} = 0V, T_A = 125°C (Note 2)
On-state Drain Current	$I_{D(ON)}$	–0.8	–1.25	—	A	V_{GS} = –4.5V, V_{DS} = –25V
		–2	–2.8	—		V_{GS} = –10V, V_{DS} = –25V
Static Drain-to-Source On-state Resistance	$R_{DS(ON)}$	—	7	10	Ω	V_{GS} = –4.5V, I_D = –150 mA
		—	6.5	9.5		V_{GS} = –10V, I_D = –1A
Change in $R_{DS(ON)}$ with Temperature	$\Delta_{RDS(ON)}$	—	—	1	%/°C	V_{GS} = –10V, I_D = –1A (Note 2)
AC PARAMETER (Note 2)						
Forward Transconductance	G_{FS}	400	—	—	mmho	V_{DS} = –25V, I_D = –500 mA
Input Capacitance	C_{ISS}	—	55	—	pF	V_{GS} = 0V, V_{DS} = –25V, f = 1 MHz
Common-source Output Capacitance	C_{OSS}	—	20	—		
Reverse Transfer Capacitance	C_{RSS}	—	8	—		
Turn-on Delay Time	$t_{d(ON)}$	—	—	10	ns	V_{DD} = –25V, I_D = –1A, R_{GEN} = 25Ω
Rise Time	t_r	—	—	15		
Turn-on Delay Time	$t_{d(OFF)}$	—	—	20		
Fall Time	t_f	—	—	15		
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	–1.8	V	V_{GS} = 0V, I_{SD} = –500 mA (Note 1)
Reverse Recovery Time	t_{rr}	—	300	—	ns	V_{GS} = 0V, I_{SD} = –500 mA (Note 2)

Note 1: Unless otherwise stated, all DC parameters are 100% tested and at +25°C. Pulse test: 300 µs pulse, 2% duty cycle.

2: Specification is obtained by characterization and is not 100% tested.

TEMPERATURE SPECIFICATIONS

Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–55	—	+150	°C	
Storage Temperature	T_S	–55	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
56-lead VQFN	θ_{JA}	—	27	—	°C/W	Note 1

Note 1: 1 oz, 4-layer, 3” x 4” PCB

2.0 PIN DESCRIPTION

Table 2-1 shows the description of pins in TC8020.
Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	GN1	Gate of N-MOSFET 1
2	GN2	Gate of N-MOSFET 2
3	NC	No Connection
4	GN3	Gate of N-MOSFET 3
5	GP3	Gate of P-MOSFET 3
6	NC	No Connection
7	SN3	Source of N-MOSFET 3
8	SN6	Source of N-MOSFET 6
9	NC	No Connection
10	GP6	Gate of P-MOSFET 6
11	GN6	Gate of N-MOSFET 6
12	NC	No Connection
13	GN5	Gate of N-MOSFET 5
14	GN4	Gate of N-MOSFET 4
15	GP5	Gate of P-MOSFET 5
16	GP4	Gate of P-MOSFET 4
17	NC	No Connection
18	SN5	Source of N-MOSFET 5
19	NC	No Connection
20	SN4	Source of N-MOSFET 4
21	NC	No Connection
22	VSUB	Die attachment substrate, must be grounded externally.
23	NC	No Connection
24	SP4	Source of P-MOSFET 4
25	NC	No Connection
26	SP5	Source of P-MOSFET 5
27	NC	No Connection
28	NC	No Connection
29	DP4	Drain of P-MOSFET 4
30	DN4	Drain of N-MOSFET 4
31	DP5	Drain of P-MOSFET 5
32	DN5	Drain of N-MOSFET 5
33	DP6	Drain of P-MOSFET 6
34	DN6	Drain of N-MOSFET 6
35	SP6	Source of P-MOSFET 6
36	SP3	Source of P-MOSFET 3
37	DP3	Drain of P-MOSFET 3
38	DN3	Drain of N-MOSFET 3
39	DP2	Drain of P-MOSFET 2
40	DN2	Drain of N-MOSFET 2

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
41	DP1	Drain of P-MOSFET 1
42	DN1	Drain of N-MOSFET 1
43	NC	No Connection
44	NC	No Connection
45	SP2	Source of P-MOSFET 2
46	NC	No Connection
47	SP1	Source of P-MOSFET 1
48	NC	No Connection
49	VSUB	Die attachment substrate, must be grounded externally.
50	NC	No Connection
51	SN1	Source of N-MOSFET 1
52	NC	No Connection
53	SN2	Source of N-MOSFET 2
54	NC	No Connection
55	GP1	Gate of P-MOSFET 1
56	GP2	Gate of P-MOSFET 2
Thermal pad		Must be grounded externally.

3.0 FUNCTIONAL DESCRIPTION

Figure 3-1 and Figure 3-2 illustrate the switching waveforms and test circuits for TC8020. See Figure 3-3 for the circuit pin layout.

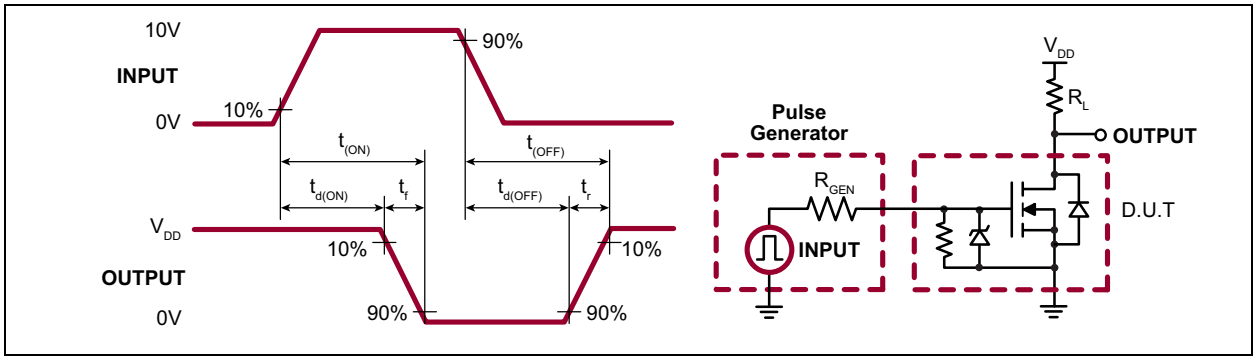


FIGURE 3-1: *N-channel Switching Waveforms and Test Circuit.*

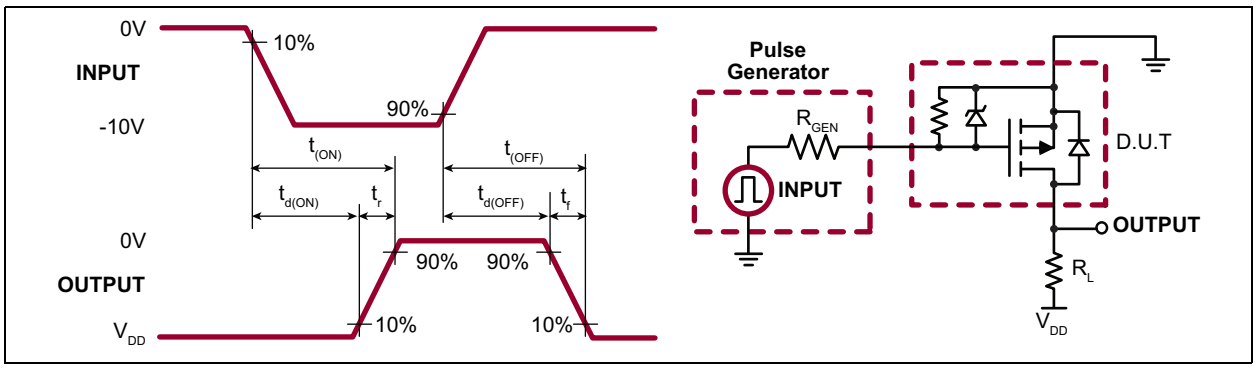


FIGURE 3-2: *P-channel Switching Waveforms and Test Circuit.*

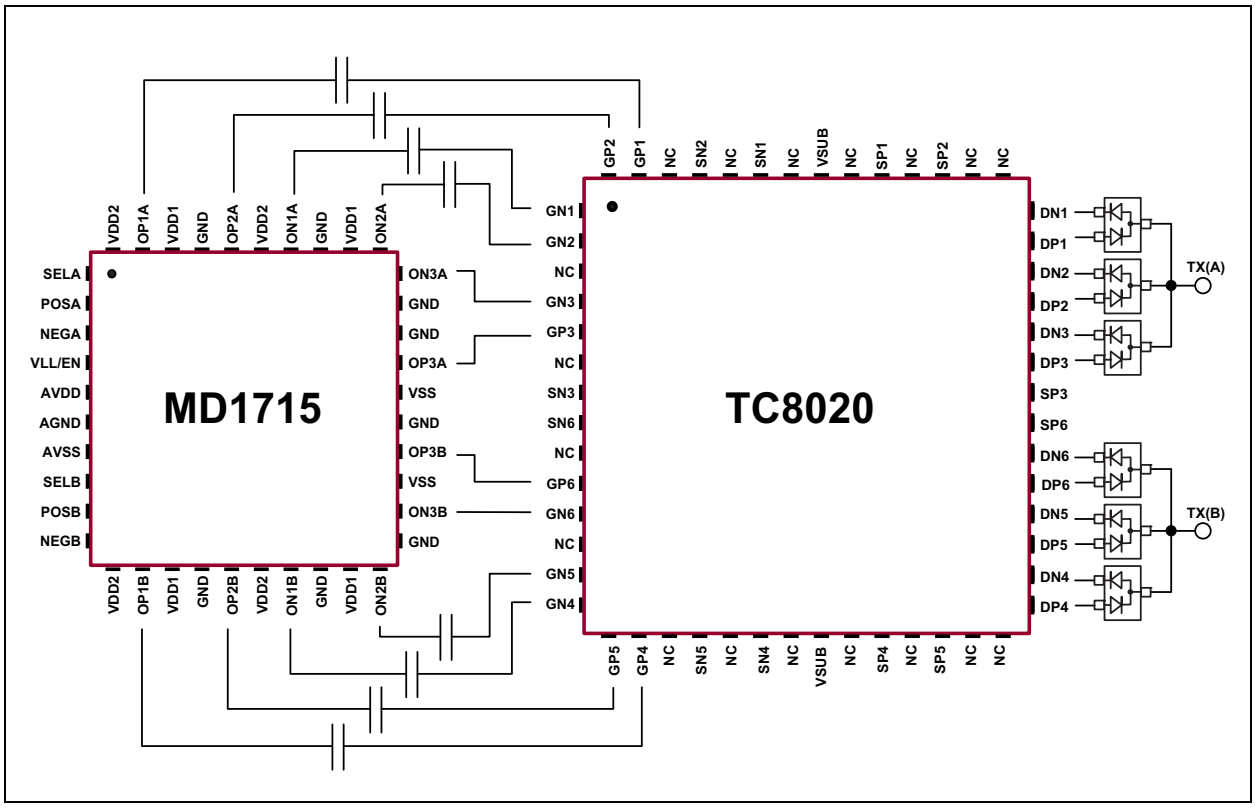


FIGURE 3-3: *Circuit Pin Layout.*

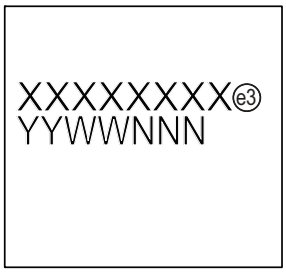
TABLE 3-1: PRODUCT SUMMARY

BV_{DSS}/BV_{DGS} (V)		$R_{DS(ON)}$ (Maximum) (Ω)	
N-Channel	**P-Channel**	**N-Channel**	**P-Channel**
200	–200	8	9.5

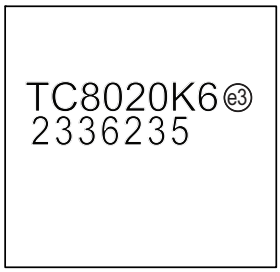
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

56-lead VQFN



Example

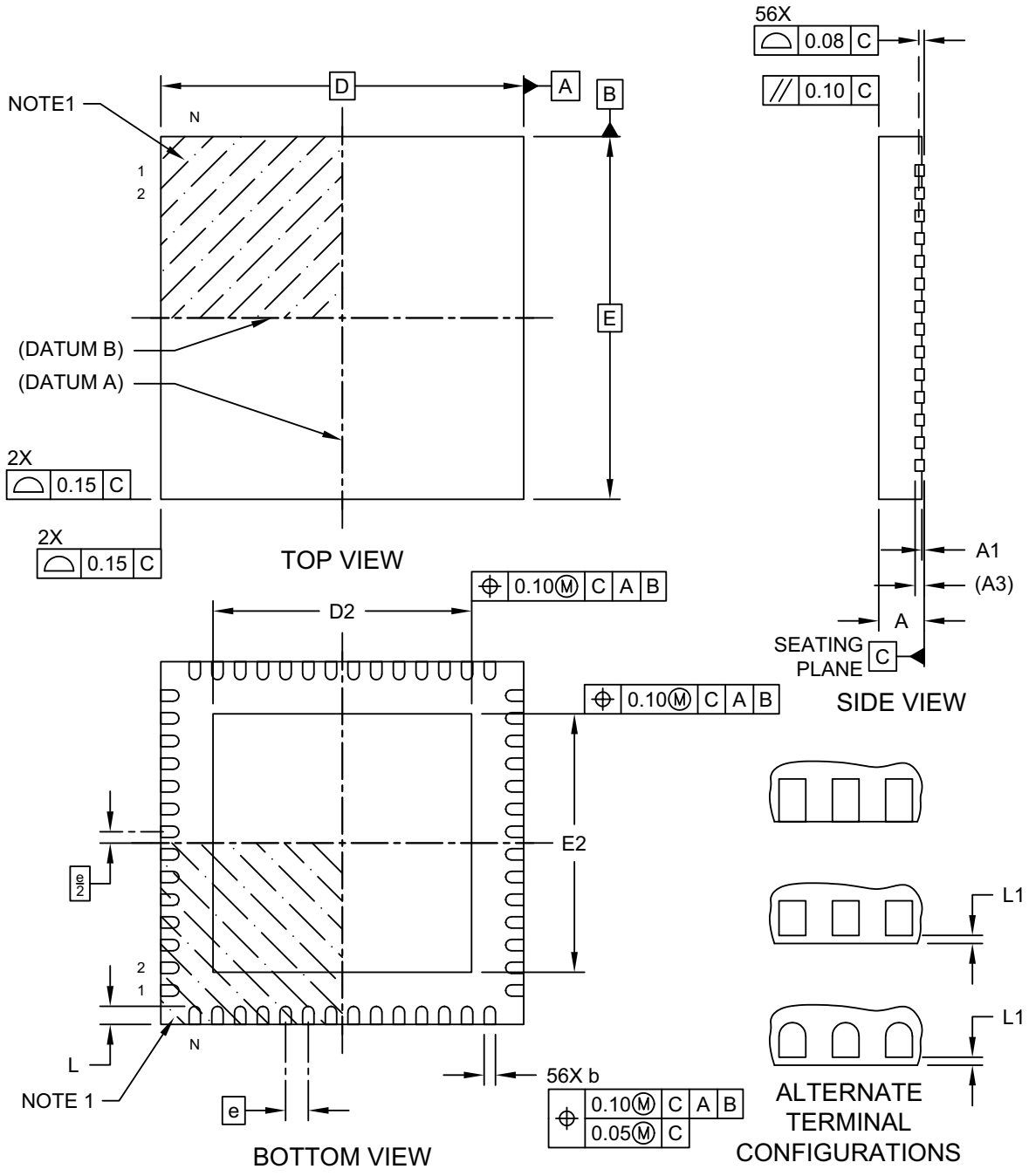


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

56-Lead Very Thin Quad Flat, No Lead Package (5XF) - 8x8x1.0 mm Body [VQFN]
Supertex Legacy Package K6

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-299-5XF Rev A Sheet 1 of 2

56-Lead Very Thin Quad Flat, No Lead Package (5XF) - 8x8x1.0 mm Body [VQFN]
Supertex Legacy Package K6

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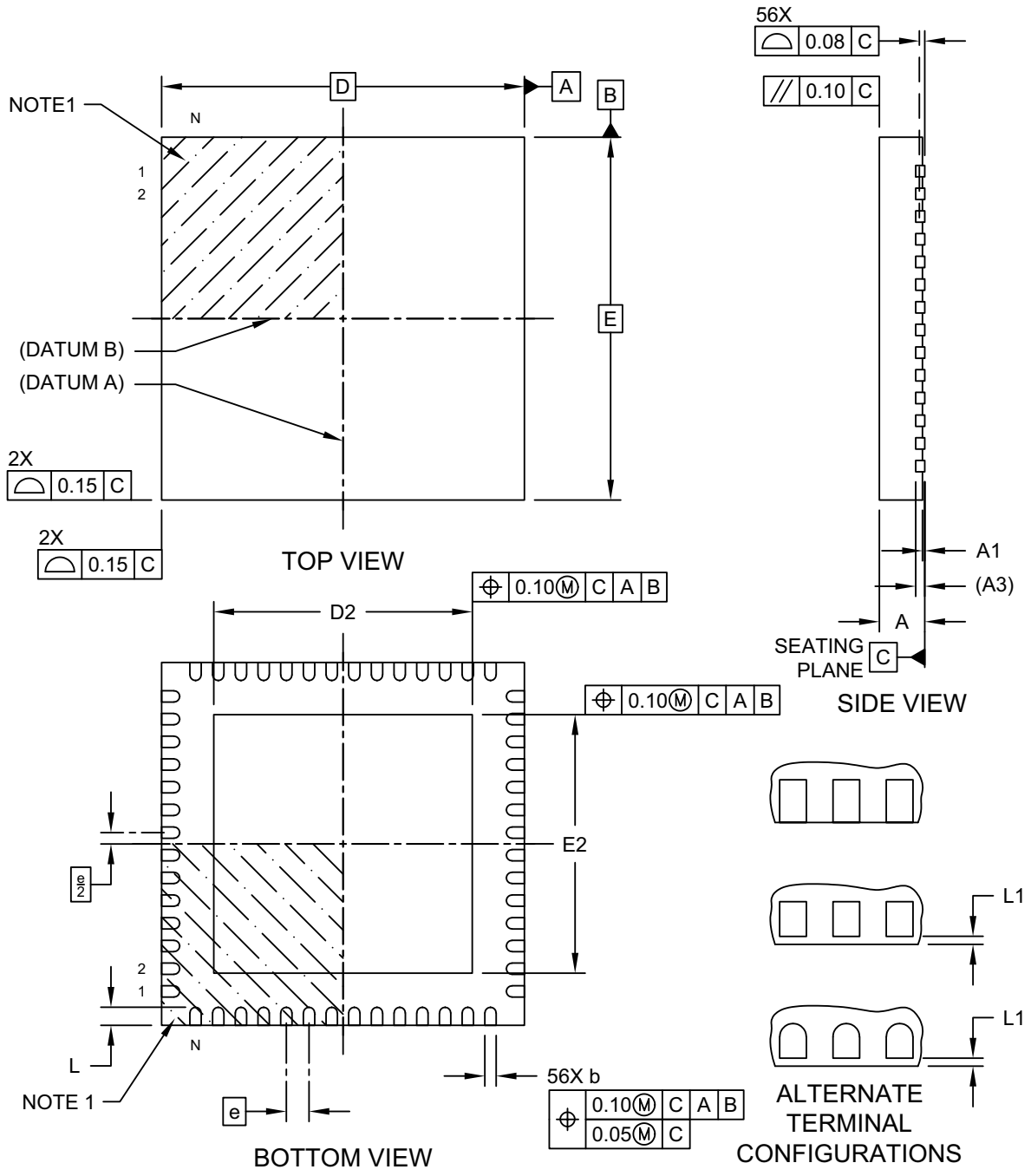

Microchip Technology Drawing C04-299-5XF Rev A Sheet 1 of 2

56-Lead Very Thin Quad Flat, No Lead Package (5XF) - 8x8x1.0 mm Body [VQFN] Supertex Legacy Package K6

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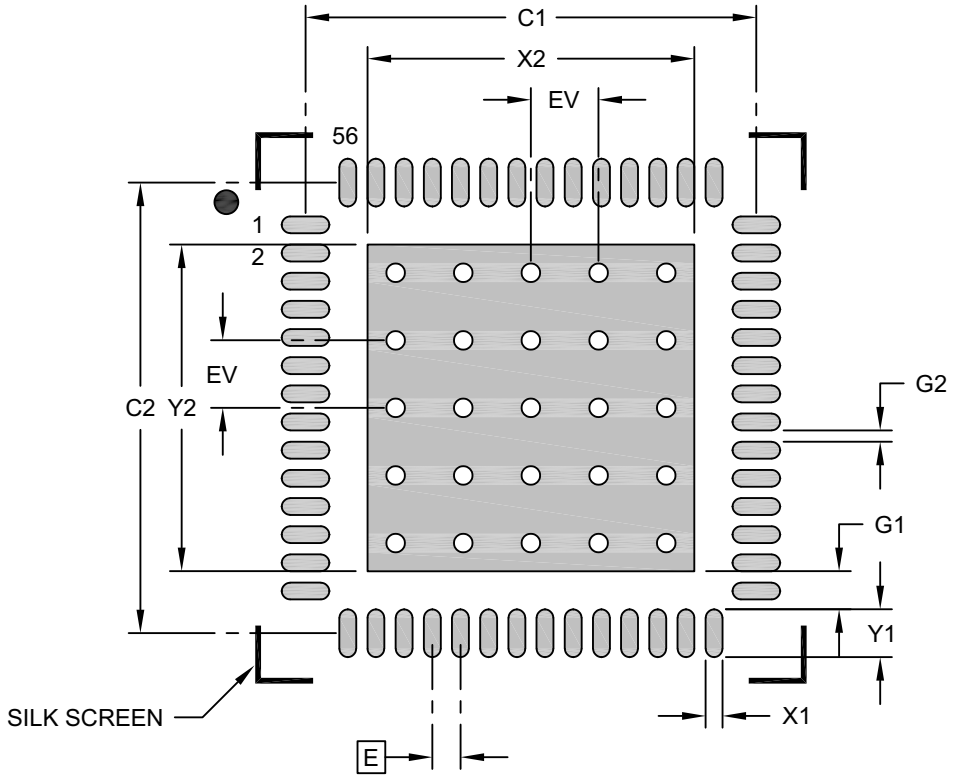

RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Center Pad Width	X2			5.80
Center Pad Length	Y2			5.80
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.85
Contact Pad to Center Pad (Xnn)	G1	0.68		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2299-5FX Rev A

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (July 2023)

- Updated package outline drawings
- Changed “56-lead QFN” to “56-lead VQFN” to align packaging specifications with the actual BQM
- Made minor text changes throughout the document

Revision A (June 2022)

- Converted Supertex Doc# DSFP-TC8020 to Microchip DS20005781A
- Changed the package marking format
- Changed the quantity of the 56-lead QFN K6 M937 media type from 2000/Reel to 3000/Reel to align packaging specification with the actual BQM
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	TC8020	=	Six-Pair N-Channel and P-Channel Enhancement-Mode MOSFET
Package:	K6	=	56-lead VQFN
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Types:	(blank)	=	250/Tray for a K6 Package
	M937	=	3000/Reel for a K6 Package

Examples:

a) TC8020K6-G:	Six-Pair N-Channel and P-Channel Enhancement-Mode MOSFET, 56-lead VQFN, 250/Tray
b) TC8020TK6-G-M937:	Six-Pair N-Channel and P-Channel Enhancement-Mode MOSFET, 56-lead VQFN, 3000/Reel

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