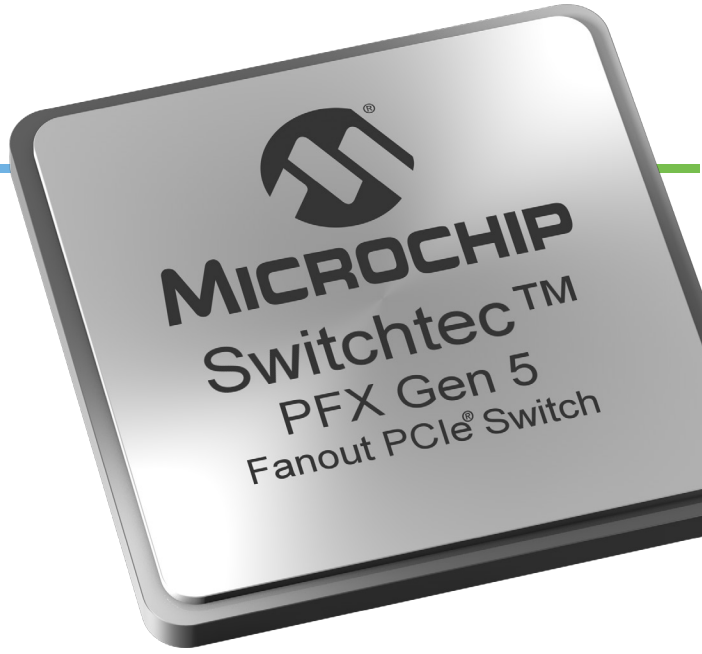
Switchtec™ PFX Gen 5 Fanout PCIe® Switch Family

PM50100, PM50084, PM50068, PM50052, PM50036, PM50028



Summary

The Switchtec PFX Gen 5 Fanout PCIe Switch Family comprises high-reliability PCIe switches supporting up to 100 lanes, 52 ports, 26 virtual switch partitions, 48 non-transparent bridges (NTBs), hot- and surprise-plug controllers for each port, advanced error containment and comprehensive diagnostics and debug capabilities, a wide breadth of I/O interfaces and an integrated MIPS processor.

Typical applications for the PFX family include data center equipment, defense and industrial servers, workstations, test equipment, video production and broadcasting equipment, cellular infrastructure, access networks, metro networks and core networking.

Features

High-Performance Non-Blocking Gen 5 Switches

- 100-lane, 84-lane, 68-lane, 52-lane, 36-lane and 28-lane variants
- Up to 48 NTBs assignable to any port
- Logical non-transparent (NT) interconnect allows for larger topologies
- Supports 1+1 and N+1 failover mechanisms
- NT address translation using direct windows and multiple sub-windows per BAR

DMA Controller

- High-performance, ultra-low latency cut-through DMA engine
- Up to 64 DMA channels

Error Containment

- Advanced Error Reporting (AER) on all ports
- Downstream Port Containment (DPC) on all downstream ports
- Completion Timeout Synthesis (CTS) to prevent an error state in an upstream host due to incomplete non-posted transactions
- Hot- and surprise-plug controllers per port
- GPIOs configurable for different cable/connector standards

PCIe Interfaces

- Passive, managed and optical cables
- SFF-8644, SFF-8643, SFF-8639, OCuLink and other connectors
- SHPC-enabled slot and edge connectors

Diagnostics and Debug

- Real-time eye capture
- External loopback capability
- Errors, statistics, performance and TLP latency counters

Highlights

- High-reliability PCIe: robust error containment, hot- and surprise-plug controllers per port, end-to-end data integrity protection, ECC protection on RAMs, high-quality, low-power SERDES
- Comprehensive diagnostics and debugging
- Secure system solution with boot image authentication

Peripheral I/O Interfaces

- Two-Wire Interfaces (TWIs) with SMBus support
- SFF-8485-compliant SGPIO ports
- Parallel GPIO pins
- UARTs
- 100/GE MAC ports (RMII/GMII)
- JTAG and EJTAG interface

High-Speed I/O

- PCIe Gen 5 32 GT/s
- Supports PCIe-compliant link training and manual PHY configuration

Power Management

- Active State Power Management (ASPM)
- Software-controlled power management

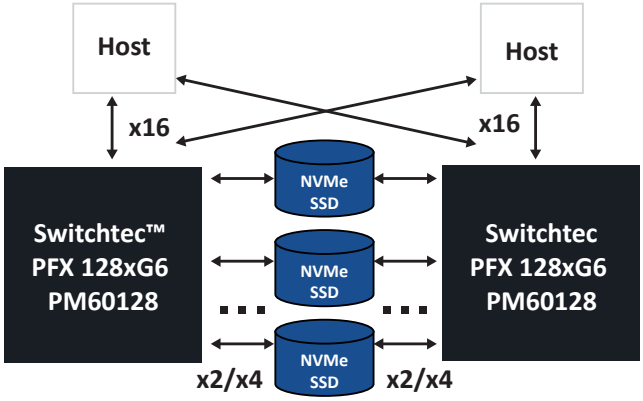
ChipLink Diagnostic Tools

- Extensive debug, diagnostics, configuration and analysis tools with an intuitive GUI
- Access to configuration data, management capabilities and signal integrity analysis tools (such as real-time eye capture)
- Connects to device over in-band PCIe or sideband signals (UART, TWI and EJTAG)

Evaluation Kit

The PM52100-KIT Switchtec Gen 5 PCIe Switch Evaluation Kit is a device evaluation environment that supports multiple interfaces.

Example Application



Ordering Information

Product	Part Numbers	Lanes	Partitions	Hot-Plug Controllers
PFX 100xG5 Gen 5 Fanout PCIe® Switch	PM50100B-FEI	100	26	52
PFX 84xG5 Gen 5 Fanout PCIe Switch	PM50084B-FEI	84	22	44
PFX 68xG5 Gen 5 Fanout PCIe Switch	PM50068B-FEI	68	18	36
PFX 52xG5 Gen 5 Fanout PCIe Switch	PM50052B-FEI	52	14	28
PFX 36xG5 Gen 5 Fanout PCIe Switch	PM50036B-FEI	36	10	20
PFX 28xG5 Gen 5 Fanout PCIe Switch	PM50028B-FEI	28	8	16