SY89854U

Precision Low Power 1:4 LVPECL Fanout Buffer/ Translator with Internal Termination

Features

- Precision 1:4, LVPECL fanout buffer
- Low power: 137 mW (2.5V typ.)
- Guaranteed AC performance over temperature and supply voltage:
  - DC- to > 2GHz Clock f_{MAX}
  - <340 ps t_{pd}
  - <180 ps t_r/t_f time
  - <20 ps max. skew
- Ultra-low jitter design:
  - <1 ps_{RMS} random jitter
  - <10 ps_{PP} deterministic jitter
  - <10 ps_{PP} total jitter (clock)
- Unique patent pending input termination and VT pin accepts DC-coupled and AC-coupled inputs (CML, PECL, LVDS)
- Typical 800 mV (100k) LVPECL output swing
- Power supply 2.5V ±5% or 3.3V ±10%
- Industrial temperature range –40°C to +85°C
- Available in ultra-small 3 mm × 3 mm 16-lead VQFN Package

Applications

- SONET and All GigE clock distribution
- Fibre Channel clock and data distribution
- Backplane distribution

General Description

The SY89854U is a 2.5V/3.3V precision, high-speed, fully differential 1:4 LVPECL fanout buffer. Optimized to provide four identical output copies with less than 20 ps of skew and less than 10 ps_{PP} total jitter, the SY89854U can process clock signals as fast as 2 GHz.

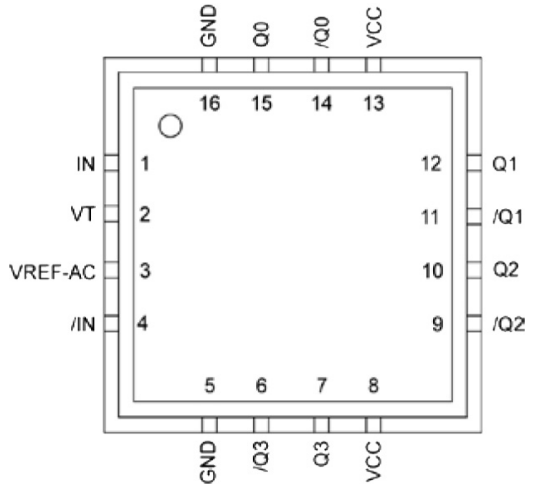
The differential input includes Microchip's unique, patent pending 3-lead input termination architecture that interfaces to any differential signal (AC or DC-coupled) as small as 100 mV (200 mVpp) without any level shifting or termination resistor networks in the signal path.

For AC-coupled input interface applications, an on-board output reference voltage (VREF-AC) is provided to bias the center-tap (VT) pin. The outputs are 800 mV LVPECL, with fast rise/fall times guaranteed to be less than 180 ps.

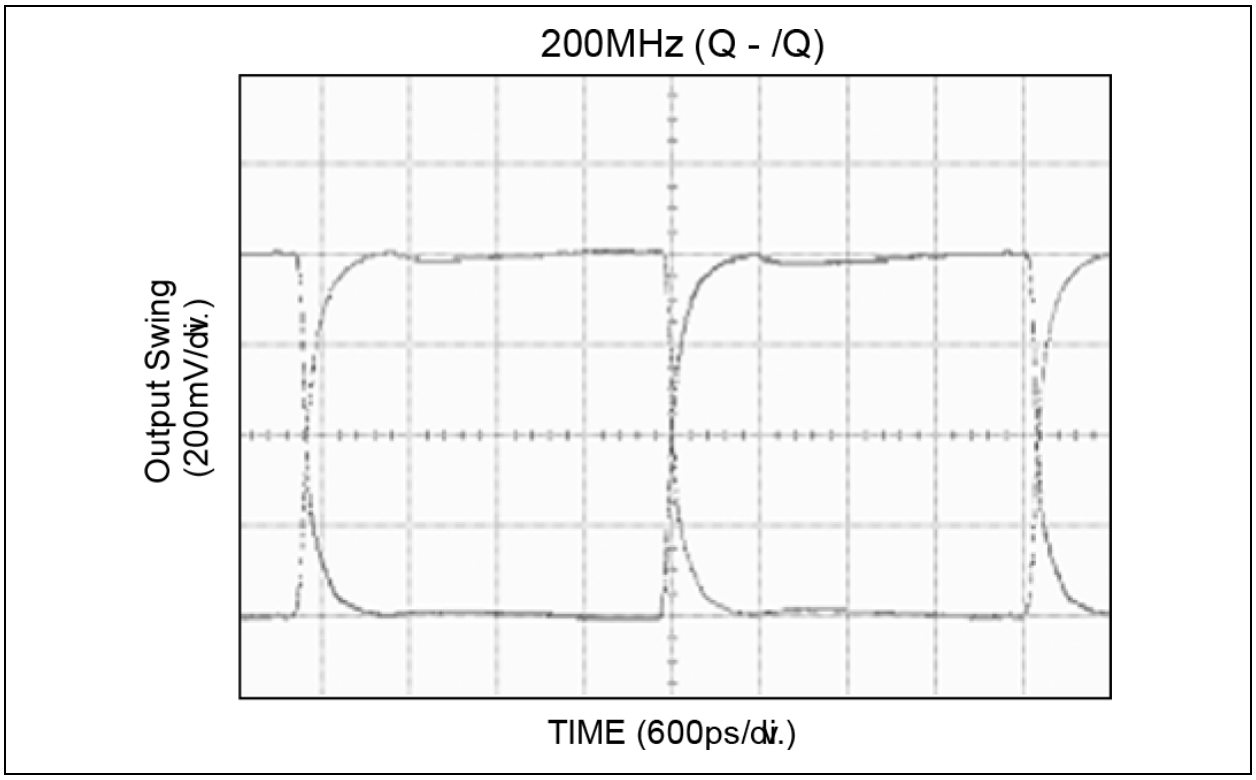
The SY89854U operates from a 2.5V ±5% supply or a 3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. The SY89854U is part of Microchip's high-speed, Precision Edge® product line.

Package Type

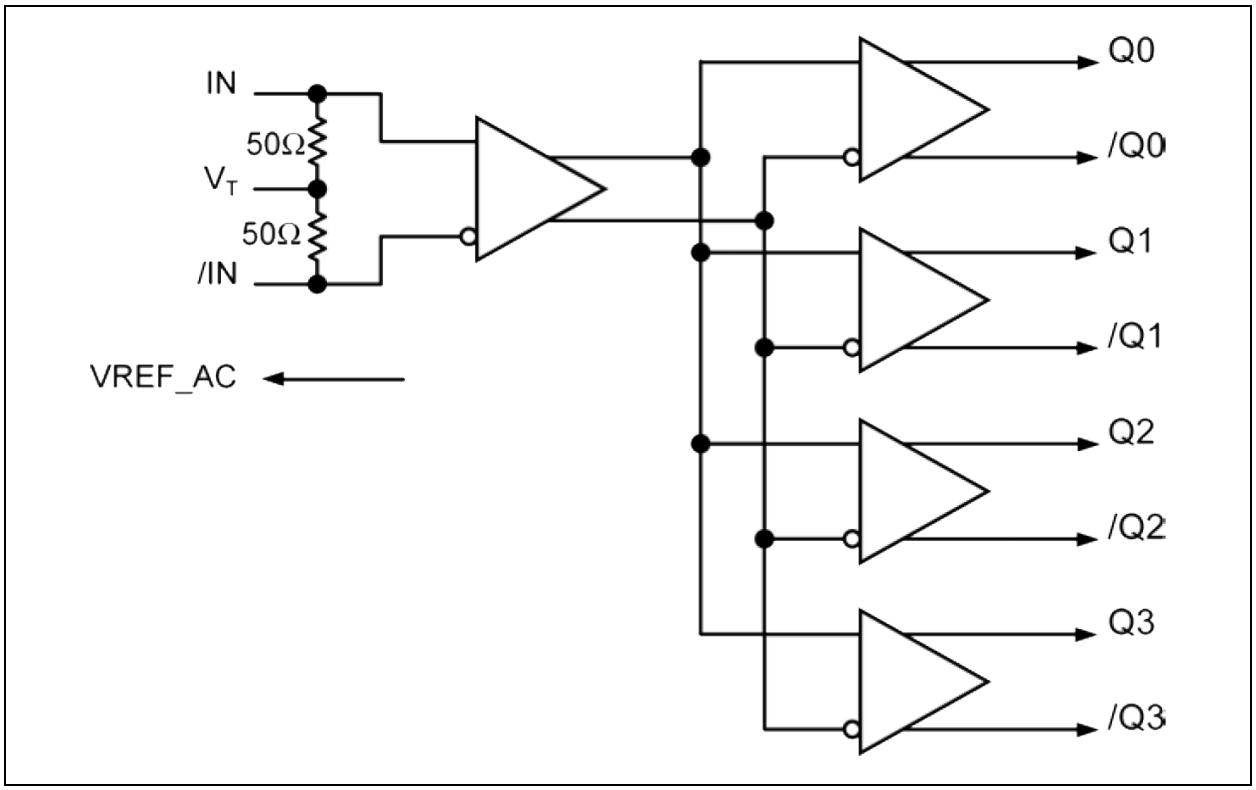
SY89854U
16-Lead VQFN



Typical Application



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (VIN) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT}) Continuous ..... 50 mA
LVPECL Output Current (I_{OUT}) Surge ..... 100 mA
Termination Current (Note 1), Source or sink current on VT ..... ±50 mA
Input Current, Source or sink current on IN, /IN ..... ±50 mA
VREF-AC Current (Note 1), Source or sink current ..... ±2 mA

Operating Ratings††

Supply Voltage (V_{CC}) ..... +2.375V to +2.625V
Supply Voltage (V_{CC}) ..... +3.0V to +3.6V

† **Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

†† **Notice:** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 1: Due to the limited drive capability use for input of the same package only.

TABLE 1-1: DC ELECTRICAL CHARACTERISTICS

All values applicable for when T_A = –40°C to +85°C unless otherwise noted. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power Supply	V_{CC}	2.375	2.5	2.625	V	—
		3.0	3.3	3.6		
Power Supply Current	I_{CC}	—	55	78	mA	No load, max. V_{CC}
Input Resistance (IN to VT)	R_{IN}	45	50	55	Ω	—
Differential Input Resistance (IN to /IN)	$R_{DIFF-IN}$	90	100	110	Ω	—
Input HIGH Voltage (IN, /IN)	V_{IH}	V_{CC} – 1.6	—	V_{CC}	V	Note 2
Input LOW Voltage (IN, /IN)	V_{IL}	0	—	V_{IH} – 0.1	V	—
Input Voltage Swing (IN, /IN)	V_{IN}	0.1	—	1.7	V	See Figure 5-1
Differential Input Voltage Swing |IN – /IN|	V_{DIFF_IN}	0.2	—	—	V	See Figure 5-2
IN-to-V_T	$V_{T\ IN}$	—	—	1.28	V	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.\

2: V_{IH} (min) not lower than 1.2V.

TABLE 1-2: LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 50Ω to V_{CC} – 2V; T_A = –40°C to +85°C, unless otherwise noted. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Output HIGH Voltage (Q, /Q)	V_{OH}	V_{CC} – 1.145	—	V_{CC} – 0.895	V	—
Output LOW Voltage (Q, /Q)	V_{OL}	V_{CC} – 1.945	—	V_{CC} – 1.695	V	—
Output Voltage Swing (Q, /Q)	V_{OUT}	550	800	—	mV	See Figure 5-1
Differential Output Voltage Swing (Q, /Q)	V_{DIFF_OUT}	1100	1600	—	mV	See Figure 5-2

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

TABLE 1-3: AC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 50Ω to V_{CC} − 2V; T_A = –40°C to + 85°C, unless otherwise noted. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Maximum Frequency	f_{MAX}	2.0	3.5	—		Clock, V_{OUT} ≥ 400 mV
		—	2.5	—		NRZ Data
Propagation Delay IN-to-Q	t_{pd}	140	220	340		V_{IN} ≥ 100 mV_{pk}
Differential Propagation Delay Temperature Coefficient	t_{pd} Tempco	—	100	—		—
Within-Device Skew	t_{SKEW}	—	4	20		Note 2
Part-to-Part Skew	t_{SKEW}	—	—	150		Note 3
Random Jitter (RJ)	t_{JITTER}	—	—	1		Note 4
Deterministic Jitter (DJ)		—	—	10		Note 5
Cycle-to-Cycle Jitter		—	—	1		Note 6
Total Jitter		—	—	10		Note 7
Output Rise/Fall Times (20% to 80%)	t_r, t_f	50	100	180		At full output swing

Note 1: High-frequency AC-parameters are guaranteed by design and characterization.

2: Output-to-output skew is measured between outputs under identical conditions.

3: Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs. Part-to-part skew includes variation in t_{pd}.

4: Random jitter is measured with a K28.7 character pattern, measured at 2.5 Gbps.

5: DJ is measured at 2.5 Gbps, with both K28.5 and 223 – 1 PRBS pattern.

6: Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.

7: Total jitter definition: with an ideal clock input of frequency <f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

TABLE 1-4: TEMPERATURE SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Range						
Operating Temperature	T_A	–40	—	+85	°C	—
Lead Temperature	T_{LEAD}	—	+260	—	°C	Soldering, 20 sec.
Storage Temperature	T_S	–65	—	+150	°C	—
Package Thermal Resistance (Note 1)						
VQFN, Still Air	θ_{JA}	—	+60	—	°C/W	—
VQFN, Junction-to-Board	ψ_{JB}	—	+38	—	°C/W	—

Note 1: Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and ψ_{JB} are calculated based on a 4-layer board in still air, unless otherwise stated.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 4	IN, /IN	**Differential Input:** This input pair is the signal to be buffered. These inputs accept AC- or DC-coupled differential signals as small as 100 mV (200 mV_{PP}). Each pin of this pair internally terminates to a VT pin through 50Ω. Note that this input will default to an indeterminate state if left open. Please refer to the “Input Interface Applications” section for more details.
2	VT	**Input Termination Center-Tap:** Each side of the differential input pair terminates to this pin. The VT pin provides a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.
8, 13	VCC	**Positive Power Supply.** Bypass with 0.1 µF||0.01 µF low ESR capacitors as close to the VCC pin as possible.
15, 14 12, 11 10, 9 7, 6	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	**Differential 100K LVPECL Output:** These LVPECL outputs are the precision, low skew copies of the input signal. Terminate with 50Ω to V_{CC} – 2V. Unused output pairs may be left floating with no impact on jitter. See “Output Interface Applications” section.
5, 16	GND, Exposed Pad	**Ground:** Ground pin and exposed pad must be connected to the same ground plane.
3	VREF-AC	**Reference Voltage:** This output biases to V_{CC} – 1.2V. It is used when AC coupling the inputs (IN, /IN). Connect VREF-AC to the VT pin. Bypass VREF-AF pin with a 0.01 µF low ESR capacitor to VCC. Maximum sink/source capability is 1.5 mA. See “Input Interface Applications” section for more details.

3.0 TYPICAL CHARACTERISTICS

V_{CC} = 2.5V; V_{IN} = 100 mV_{pk}, T_A = 25°C, unless otherwise noted.

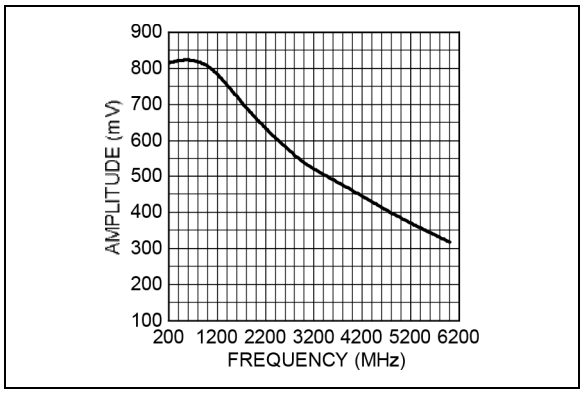


FIGURE 3-1: AMPLITUDE VS. FREQUENCY.

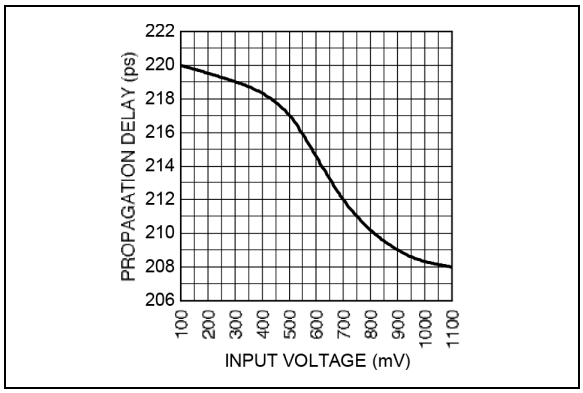


FIGURE 3-3: PROPAGATION DELAY VS. INPUT VOLTAGE.

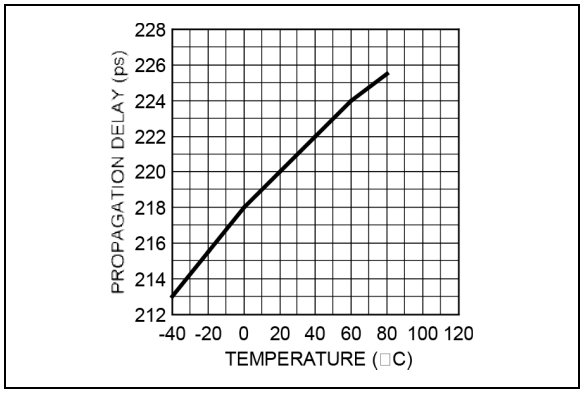


FIGURE 3-2: PROPAGATION DELAY VS. TEMPERATURE.

4.0 TYPICAL OUTPUT WAVEFORMS

V_{CC} = 2.5V; V_{IN} = 100 mV, T_A = 25°C, unless otherwise noted.

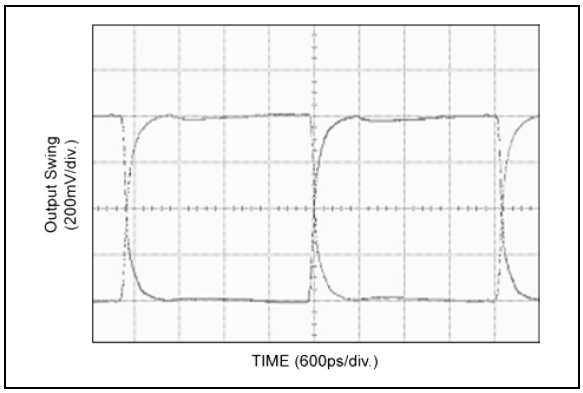


FIGURE 4-1: 200 MHZ (Q – /Q) OUTPUT.

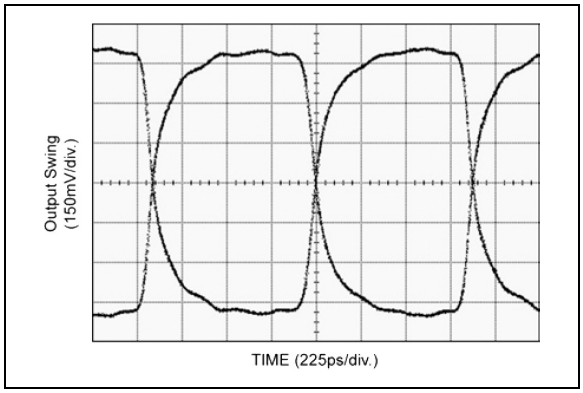


FIGURE 4-2: 622 MHZ (Q – /Q) OUTPUT.

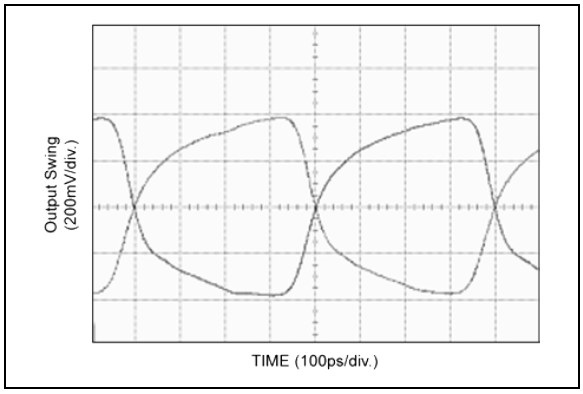


FIGURE 4-3: 1.25 GHZ (Q – /Q) OUTPUT.

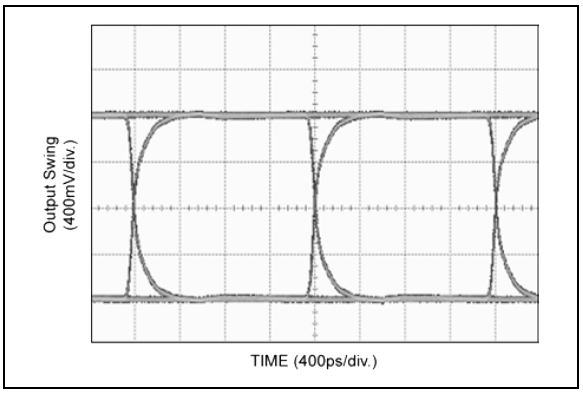


FIGURE 4-4: 622 MBPS (Q – /Q) OUTPUT.

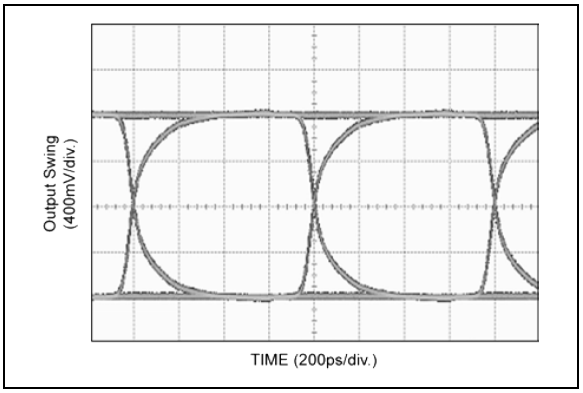


FIGURE 4-5: 1.25 GBPS (Q – /Q) OUTPUT.

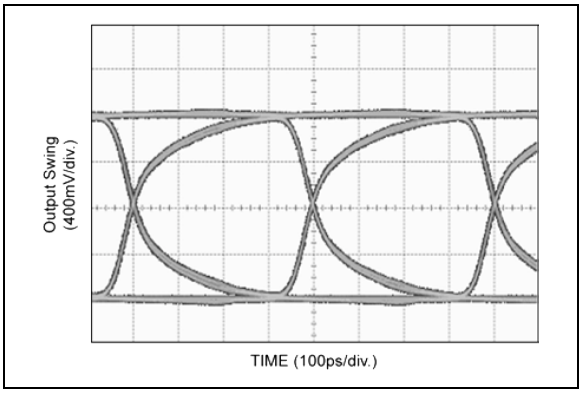


FIGURE 4-6: 2.5 GBPS (Q – /Q) OUTPUT.

5.0 SINGLE-ENDED AND DIFFERENTIAL SWINGS

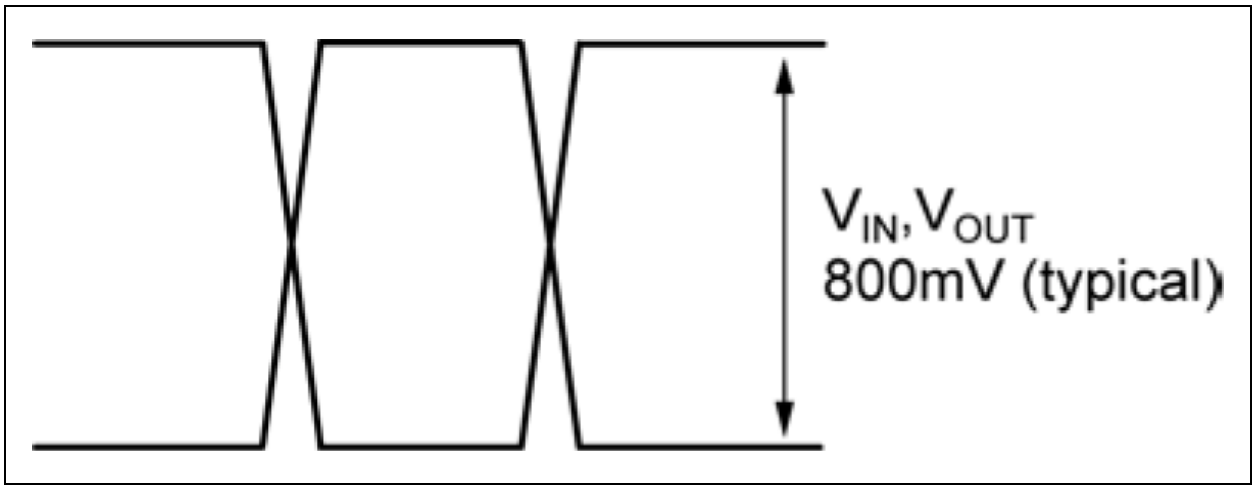


FIGURE 5-1: SINGLE-ENDED VOLTAGE SWING.

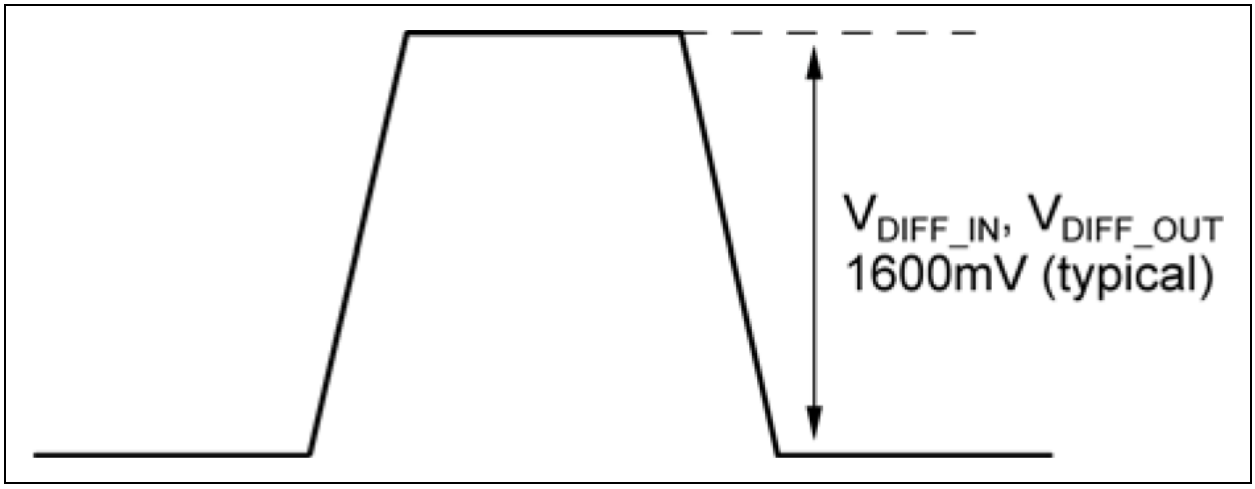


FIGURE 5-2: DIFFERENTIAL VOLTAGE SWING.

6.0 TIMING DIAGRAM

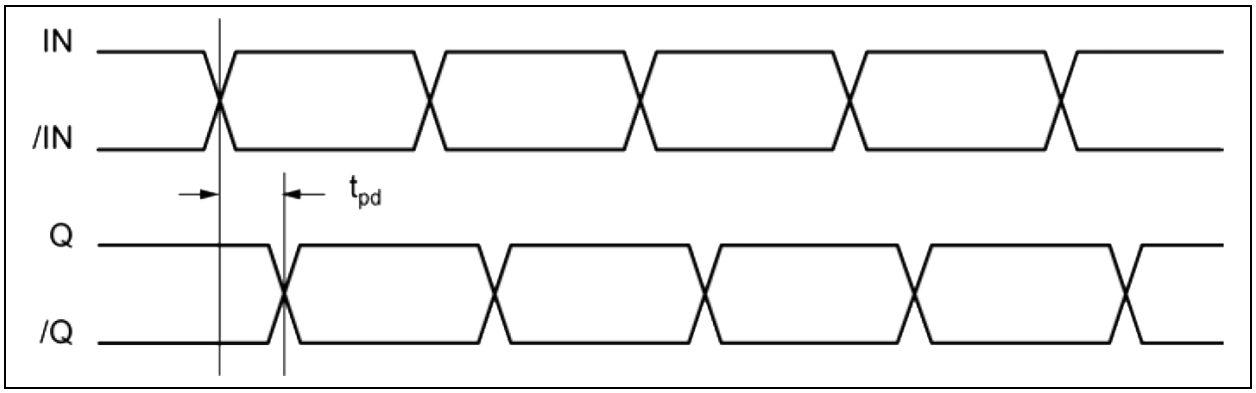


FIGURE 6-1: TIMING DIAGRAM.

7.0 INPUT AND OUTPUT STAGES

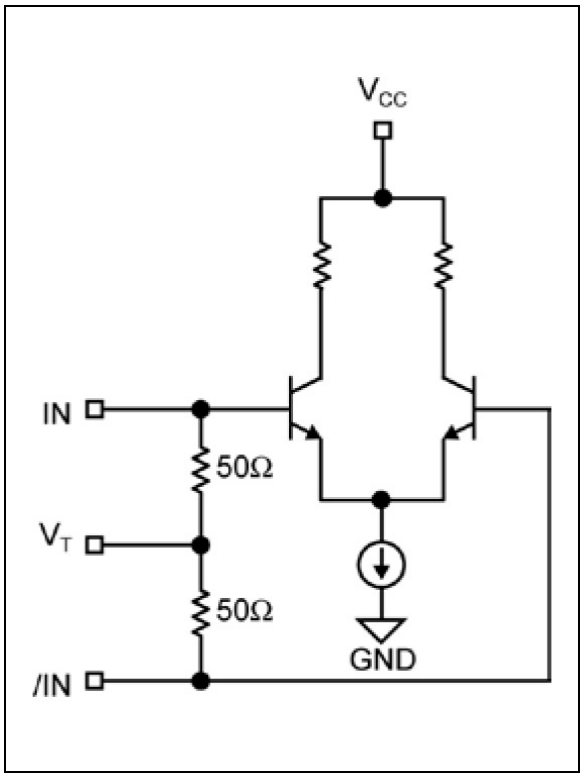


FIGURE 7-1: SIMPLIFIED DIFFERENTIAL INPUT STAGE.

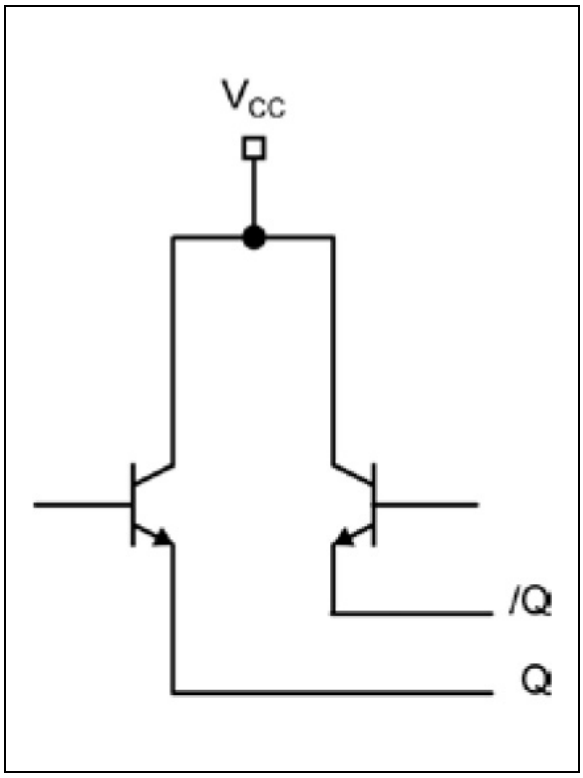


FIGURE 7-2: SIMPLIFIED LVPECL OUTPUT STAGE.

8.0 INPUT INTERFACE APPLICATIONS

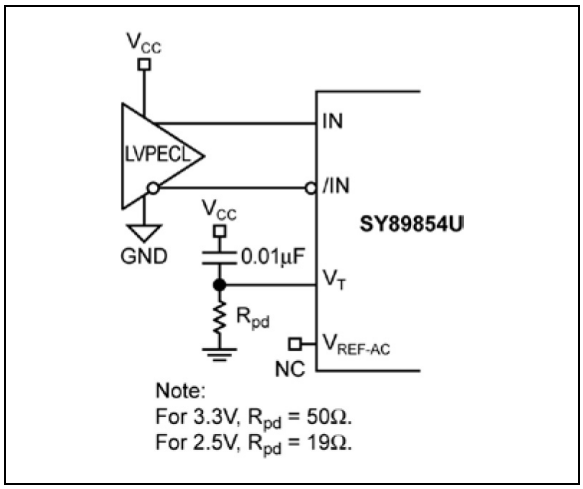


FIGURE 8-1: DC-COUPLED LVPECL INPUT INTERFACE.

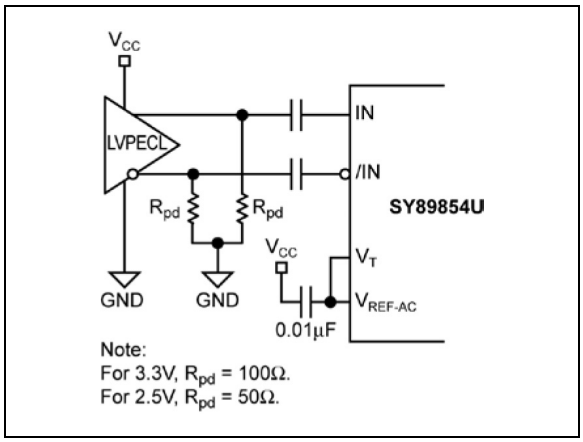


FIGURE 8-2: AC-COUPLED LVPECL INPUT INTERFACE.

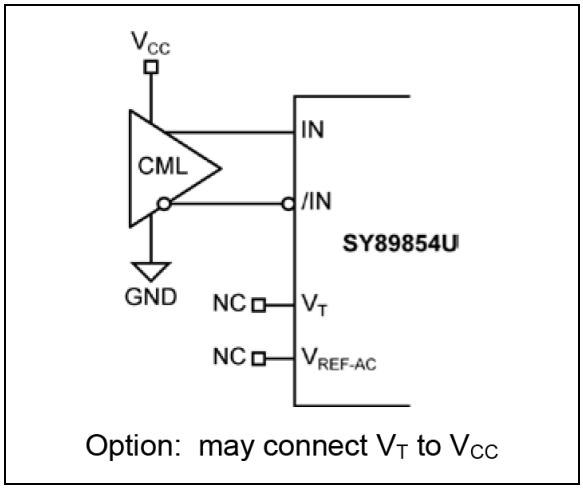


FIGURE 8-3: DC-COUPLED CML INPUT INTERFACE.

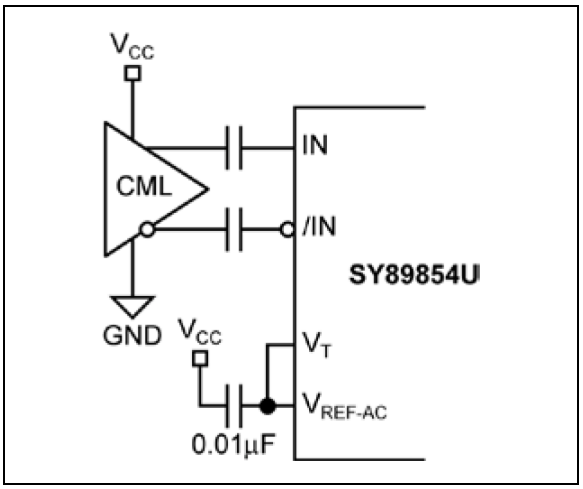


FIGURE 8-4: AC-COUPLED CML INPUT INTERFACE.

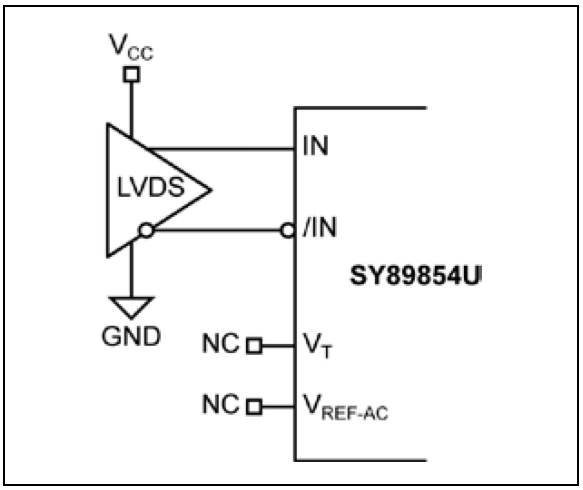


FIGURE 8-5: DC-COUPLED LVDS INPUT INTERFACE.

9.0 OUTPUT TERMINATION RECOMMENDATIONS

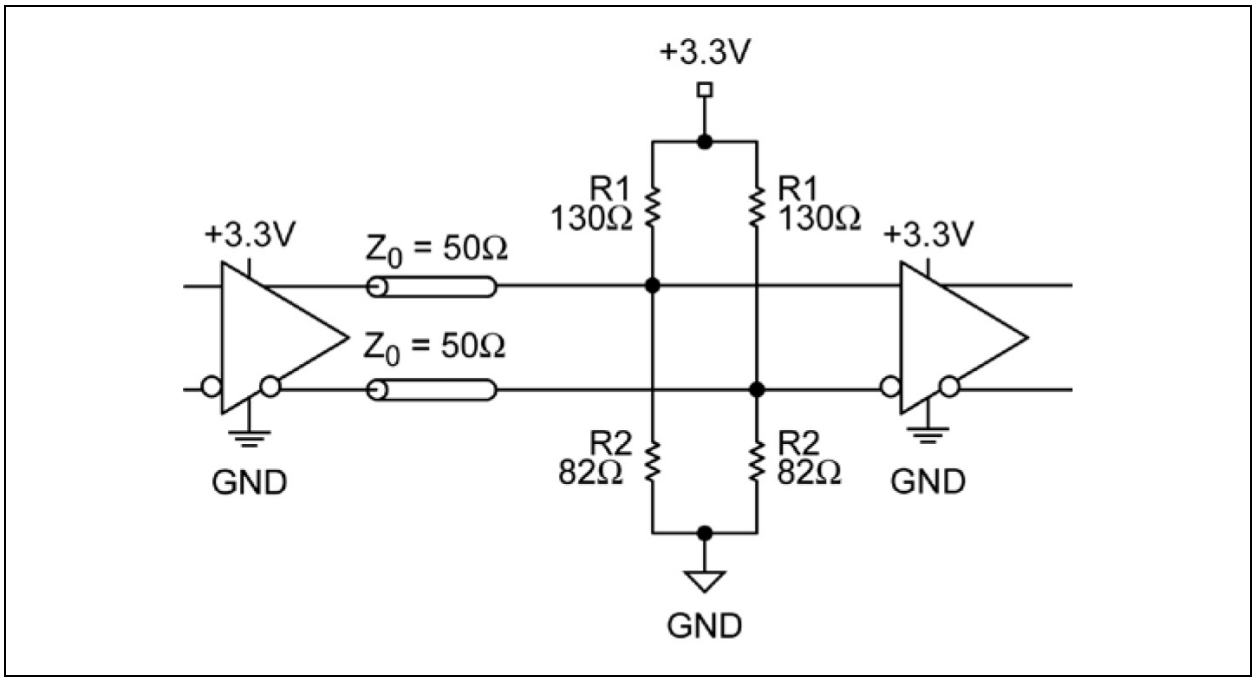


FIGURE 9-1: PARALLEL THEVENIN EQUIVALENT TERMINATION.

Note 1: For +2.5V systems: R1 = 250Ω, R2 = 82.5Ω.

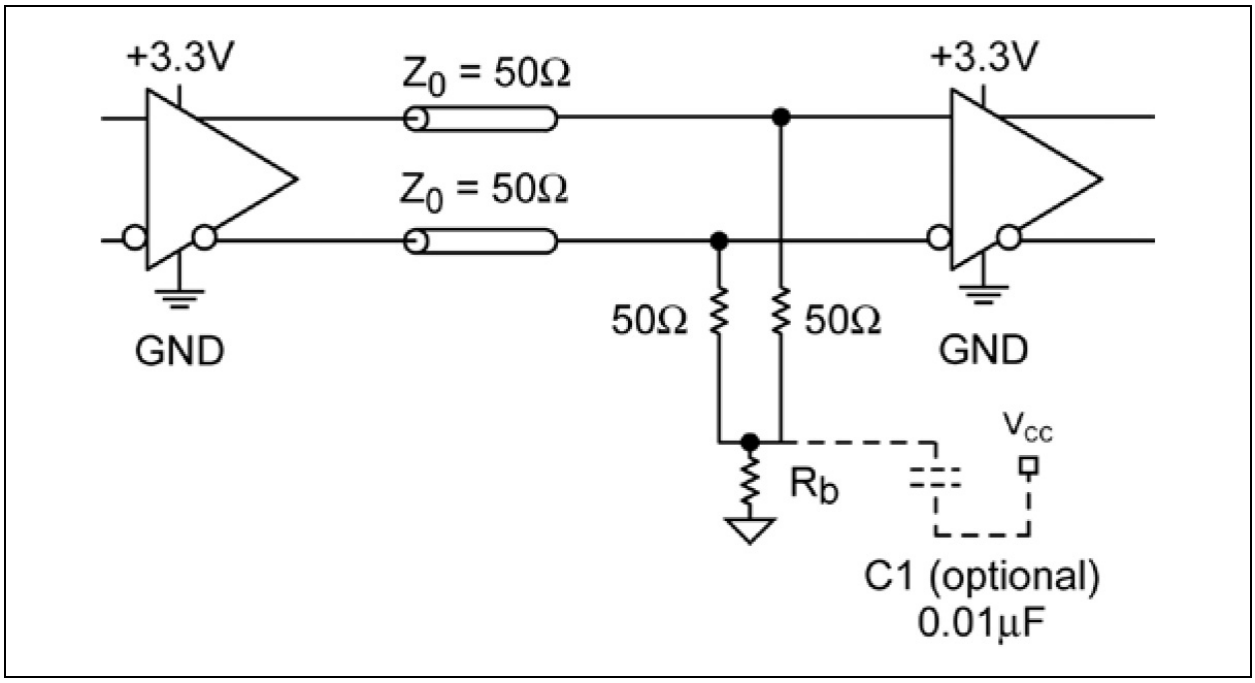


FIGURE 9-2: PARALLEL TERMINATION (THREE-RESISTOR).

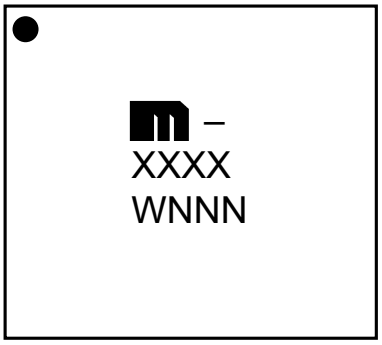
Note 1: For +2.5V systems, Rb = 19Ω.

2: For +3.3V systems, Rb = 50Ω.

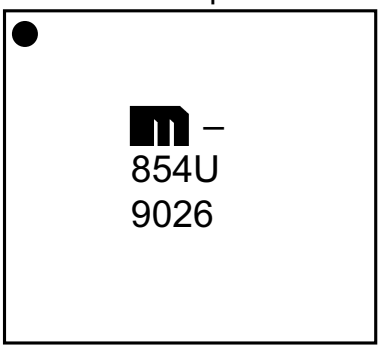
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

16-Lead VQFN*



Example*



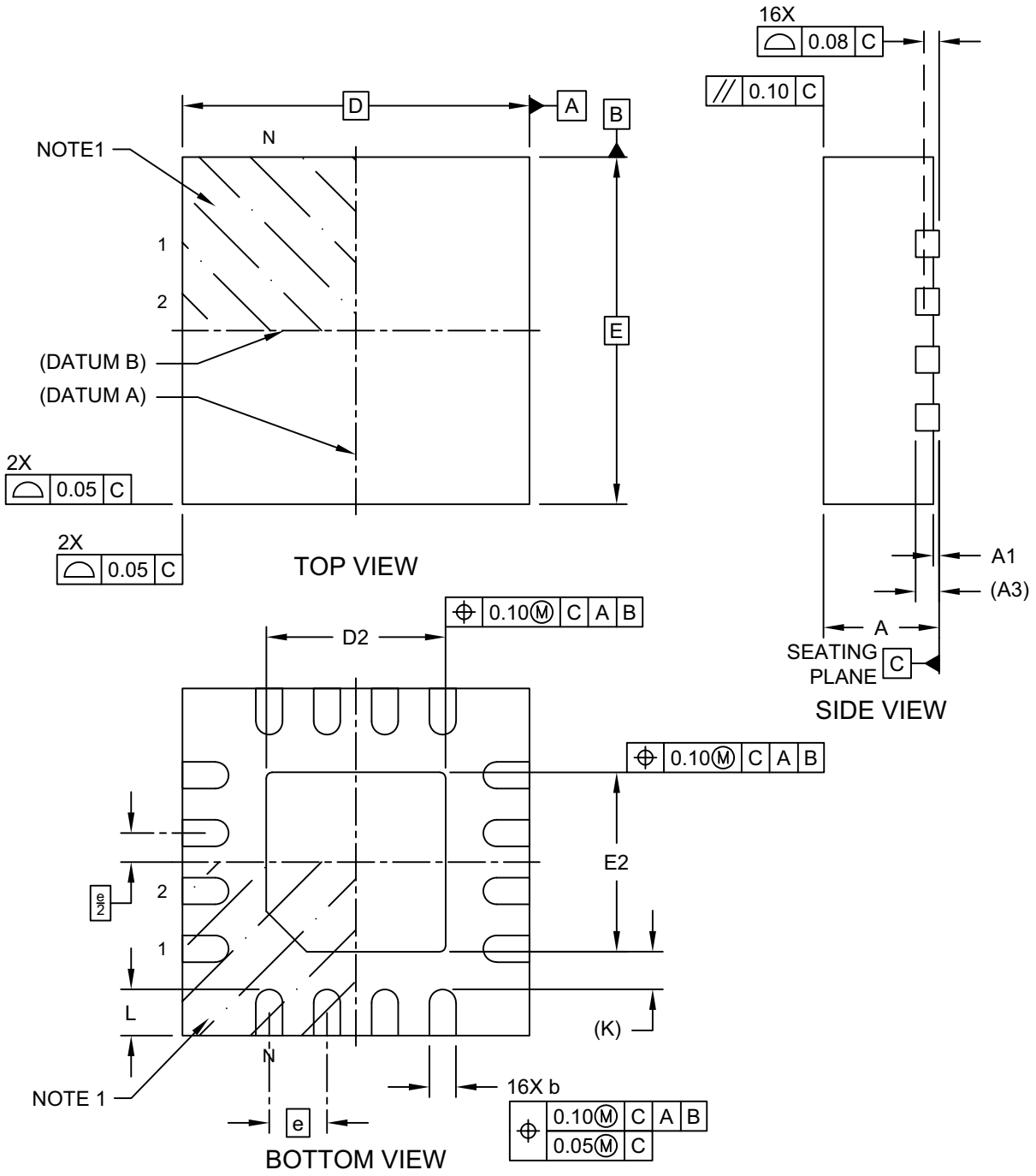
Legend:	XX...X	Product code or customer-specific information
	W	Week code
	NNN	Alphanumeric traceability code (week)
	*	This package is Pb-free. The Pb-free JEDEC designator can be found on the outer packaging for this package.
	●	Pin one index is identified by a dot

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

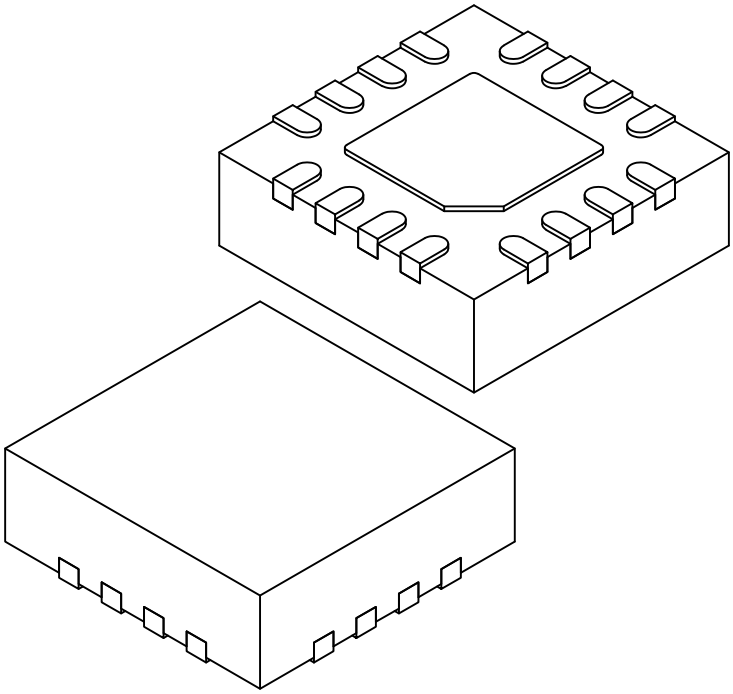
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1103-NCA Rev C Sheet 1 of 2

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	1.50	1.55	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.55	1.60
Terminal Width	b	0.18	0.23	0.28
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.33 REF	

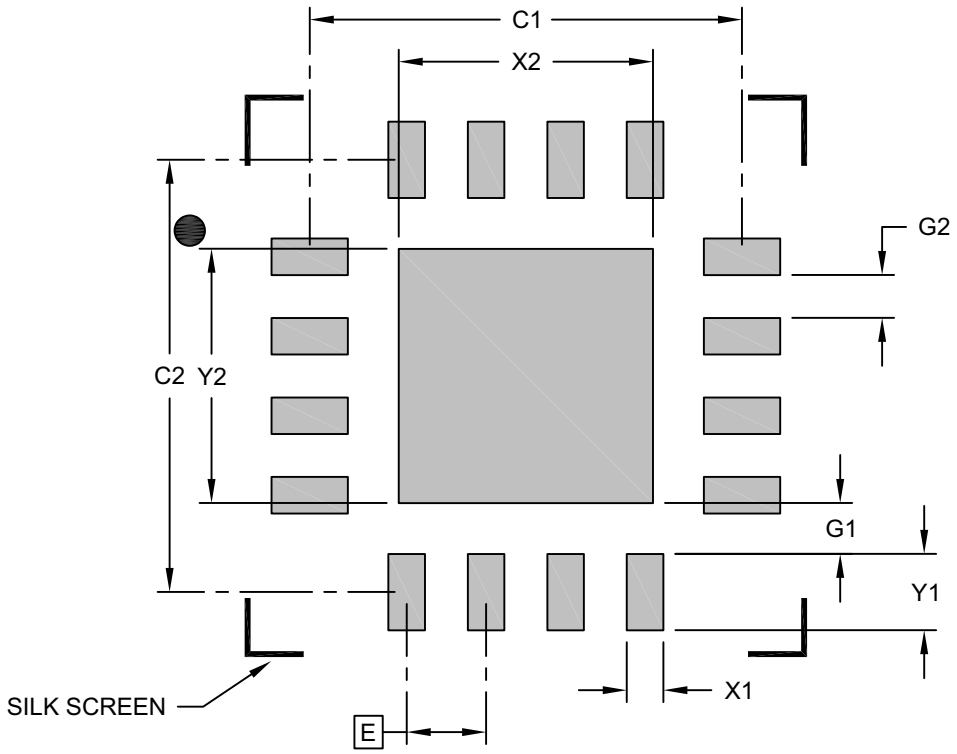
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1103-NCA Rev C Sheet 2 of 2

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			1.60
Center Pad Length	Y2			1.60
Contact Pad Spacing	C1		2.72	
Contact Pad Spacing	C2		2.72	
Contact Pad Width (Xnn)	X1			0.23
Contact Pad Length (Xnn)	Y1			0.48
Contact Pad to Center Pad (Xnn)	G1	0.32		
Contact Pad to Contact Pad (Xnn)	G2	0.27		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3103-NCA Rev C

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (May 2024)

- Converted Micrel data sheet for SY89854U to Microchip format as DS20006867A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XX
Device	Supply Voltage Range	Package	Temperature Range	Special Processing

Device:	SY89854	=	Precision Low Power 1:4 LVPECL Fanout Buffer/ Translator with Internal Termination
Voltage Option:	U	=	3.3V
Package:	M	=	16-Lead VQFN
Temperature Range:	G	=	–40°C to 85°C
Special Processing:	<blank>	=	100/Tube
	TR	=	1,000/Reel

Examples:

a) **SY89854UMG**

2.5V/3.3, 16-Lead VQFN, –40°C to 85°C, 100/Tube

b) **SY89854UMG-TR**

2.5V/3.3, 16-Lead VQFN, –40°C to 85°C, 1000/Reel

NOTES:

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