SY89544U

2.5V, 3.2 Gbps, Differential 4:1 LVDS Multiplexer with Internal Input Termination

Features

- Selects Among Four Differential Inputs
- Guaranteed AC Performance over Temperature and Voltage:
  - DC-to >3.2 Gbps Data Rate Throughput
  - <510 ps In-to-Q t_{PD}
  - <150 ps t_r/t_f
- Ultra Low-Jitter Design:
  - <1 ps_{RMS} Random Jitter
  - <10 ps_{PP} Deterministic Jitter
  - <10 ps_{PP} Total Jitter (Clock)
  - <0.7 ps_{RMS} Crosstalk-Induced Jitter
- Unique Input Isolation Design Minimizes Crosstalk
- Internal Input Termination
- Unique Input Termination and VT Pin Accepts DC-Coupled and AC-Coupled Inputs (LVDS, LVPECL, CML)
- 350 mV LVDS Output Swing
- CMOS/TTL-Compatible MUX Select
- Power Supply 2.5V ±5%
- –40°C to +85°C Temperature Range
- Available in 32-Lead (5 mm x 5 mm) QFN Package

Applications

- SONET/SDH Channel Select
- Fibre Channel Multi-Channel Select
- Gigabit Ethernet Multi-Channel Select

General Description

The SY89544U is a fast, low-jitter, 4:1 differential MUX with an LVDS-compatible (350 mV) output with guaranteed data rate throughput of 3.2 Gbps over temperature and voltage.

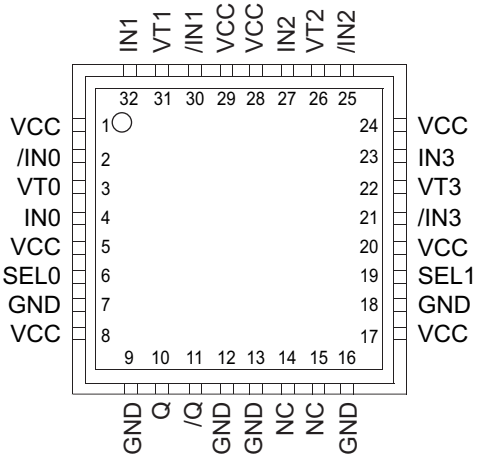
The SY89544U differential inputs include a unique, 3-pin internal termination that allows access to the termination network through a VT pin. This feature allows the device to easily interface to different logic standards, both AC- and DC-coupled without external resistor-bias and termination networks. The result is a clean, stub-free, low-jitter interface solution.

The SY89544U operates from a single 2.5V supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require a 3.3V supply, consider the SY89545L. For applications that require two differential outputs, consider the SY89546U or SY89547L. The SY89544U is part of Microchip's Precision Edge® product family.

Package Type

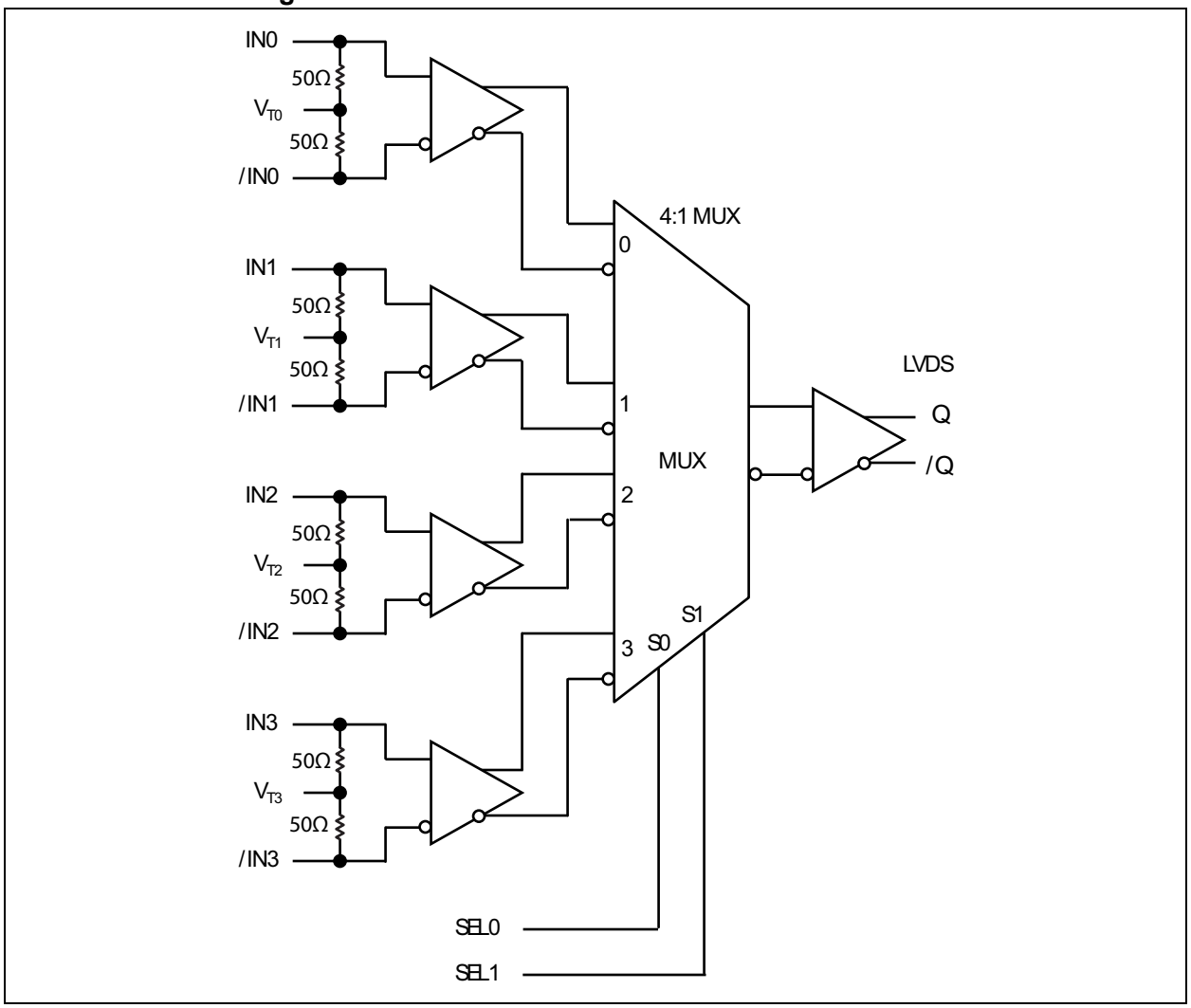
SY89544U

32-Lead 5x5 QFN (M)



United States Patent No. RE44,134

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVDS Output Current (I_{OUT}) ..... ±10 mA
Termination Current (Source or Sink Current on VT) (I_{VT}) ..... ±100 mA

Operating Ratings ‡

Supply Voltage Range (V_{CC}) ..... +2.375V to +2.675V

† Notice: Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 2.5V ±5%; T_A = –40°C to +85°C, unless otherwise stated. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Current	I_{CC}	—	50	70	mA	No load.
Input Resistance (IN-to-VT)	R_{IN}	45	50	55	Ω	—
Differential Input Resistance (IN-to-/IN)	R_{DIFF_IN}	90	100	110	Ω	—
Input High Voltage (IN, /IN)	V_{IH}	1.2	—	V_{CC}	V	—
Input Low Voltage (IN, /IN)	V_{IL}	0	—	V_{IH} - 0.1	V	—
Input Voltage Swing (IN, /IN)	V_{IN}	0.1	—	V_{CC}	V	Note 2
Differential Input Voltage Swing |IN – /IN|	V_{DIFF_IN}	0.2	—	—	V	Note 2
Voltage from IN or /IN to VT	IN-to-VT	—	—	1.8	V	—

Note 1: The circuit is designed to meet the DC specifications show in the table above after thermal equilibrium has been established.

2: See Figure 5-1 and Figure 5-2 for V_{IN} and V_{DIFF_IN} definitions.

LVDS OUTPUTS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 2.5V ±5%; T_A = –40°C to +85°C; R_L = 100Ω across Q and /Q, unless otherwise stated. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output High Voltage (Q, /Q)	V_{OH}	—	—	1.475	V	Note 3
Output Low Voltage (Q, /Q)	V_{OL}	0.925	—	—	V	Note 3
Output Voltage Swing (Q, /Q)	V_{OUT}	250	350	—	mV	Note 2
Differential Output Voltage Swing |Q – /Q|	V_{DIFF_OUT}	500	700	—	mV	Note 2
Output Common Mode Voltage	V_{OCM}	1.125	—	1.275	V	Note 4
Change in Output Common Mode Voltage	ΔV_{OCM}	–50	—	50	mV	Note 4

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

2: See Figure 5-1 and Figure 5-2 for V_{OUT} and V_{DIFF_OUT} definitions.

3: See Figure 8-1.

4: See Figure 8-2.

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 2.5V ±5%; T_A = –40°C to +85°C; unless otherwise stated. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V	—
Input Low Voltage	V_{IL}	0	—	0.8	V	—
Input High Current	I_{IH}	–125	—	40	µA	—
Input Low Current	I_{IL}	–300	—	—	µA	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 2.5V ±5%; T_A = –40°C to +85°C; R_L = 100Ω across Q and /Q, unless otherwise stated. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Operating Frequency	f_{MAX}	3.2	—	—	Gbps	NRZ Data
		—	4	—	GHz	Clock, V_{OUT} ≥ 200 mV
Differential Propagation Delay	t_{pd}	310	410	510	ps	IN-to-Q
		200	400	700	ps	SEL-to-Q
Input-to-Input Skew	t_{SKEW}	—	5	20	ps	Note 2
Part-to-Part Skew		—	—	200	ps	Note 3
Data, Random Jitter	t_{JITTER}	—	—	1	ps_{RMS}	Note 4
Data, Deterministic Jitter		—	—	10	ps_{PP}	Note 5
Clock, Total Jitter		—	—	10	ps_{PP}	Note 6
Clock, Cycle-to-Cycle Jitter		—	—	1	ps_{RMS}	Note 7
Crosstalk-Induced Jitter Adjacent Channel		—	—	0.7	ps_{RMS}	Note 8
Output Rise/Fall Time (20% to 80%)	t_r/t_f	35	80	150	ps	At full output swing.

Note 1: Measured with 100 mV input swing. See Figure 4-1 for definition of propagation delay parameters. High-frequency AC parameters are guaranteed by design and characterization.

2: Input-to-input skew is the difference in propagation delay between any two inputs to the output under identical conditions.

3: Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

4: Random jitter is measured with a K28.7 comma detect character pattern, measured at 1.25 Gbps and 3.2 Gbps.

5: Deterministic jitter is measured at 1.25 Gbps and 3.2 Gbps, with both K28.5 and 2^{23}–1 PRBS pattern.

6: Total jitter definition: with an ideal clock input of frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

7: Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, T_n–T_{n-1} where T is the time between rising edges of the output signal.

8: Crosstalk is measured at the output while applying two similar frequencies to adjacent inputs that are asynchronous with respect to each other at the inputs.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Temperature Range	T_A	–40	—	+85	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Maximum Junction Temperature	T_J	—	—	+125	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20s
Package Thermal Resistances (Note 2)						
Thermal Resistance QFN-32	θ_{JA}	—	35	—	°C/W	Still-Air
	θ_{JA}	—	28	—	°C/W	500 lfpm
	Ψ_{JB}	—	20	—	°C/W	Junction-to-Board

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2: Package thermal resistance assumed exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. Ψ_{JB} uses 4-layer θ_{JA} in still-air unless otherwise stated.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

V_{CC} = 2.5V, T_A = +25°C, R_L = 100Ω across Q and /Q, unless otherwise stated.

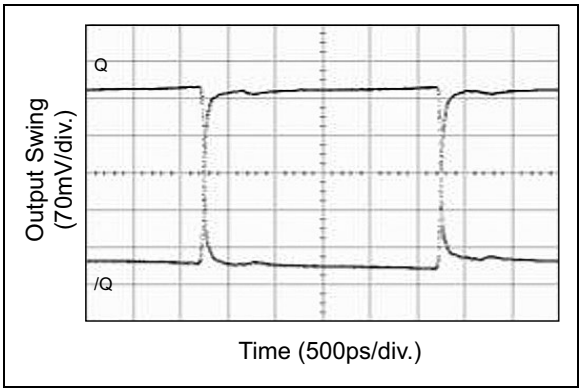


FIGURE 2-1: *200 MHz Output.*

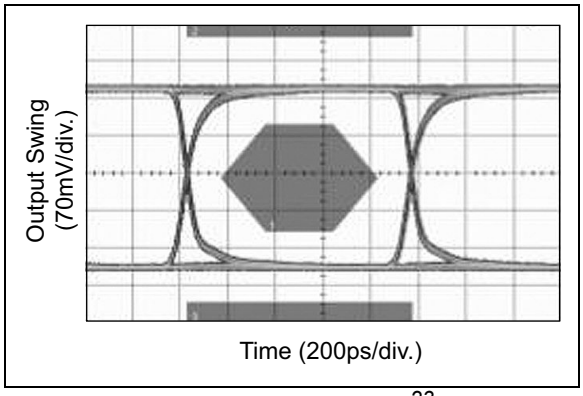


FIGURE 2-4: *1xFC Mask (2^{23}–1 PRBS).*

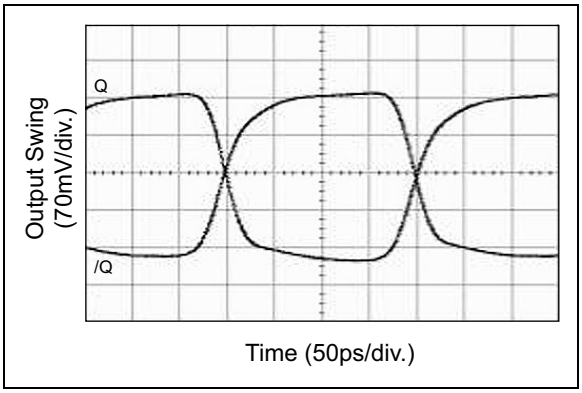


FIGURE 2-2: *2.5 GHz Output.*

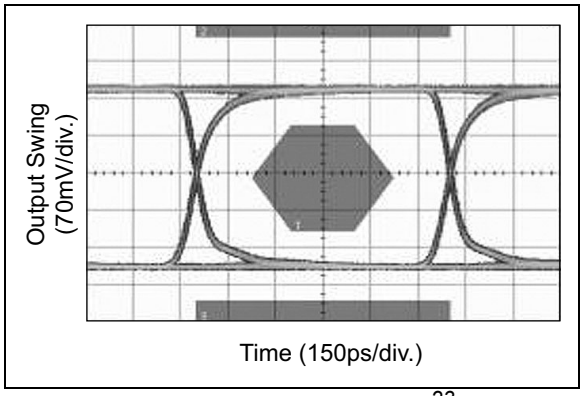


FIGURE 2-5: *1xGBE Mask (2^{23}–1 PRBS).*

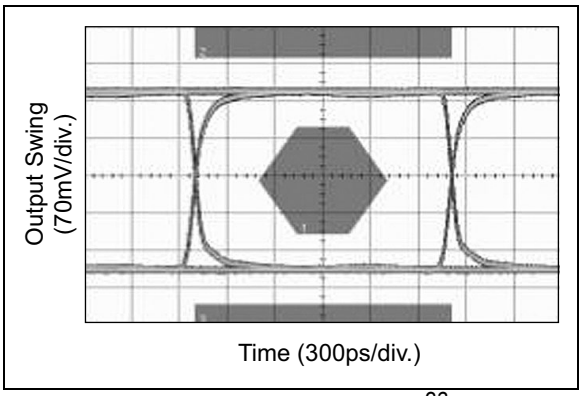


FIGURE 2-3: *OC-12 Mask (2^{23}–1 PRBS).*

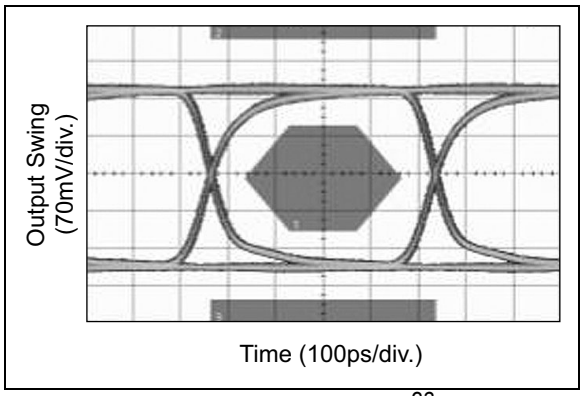


FIGURE 2-6: *2xFC Mask (2^{23}–1 PRBS).*

V_{CC} = 2.5V, T_A = +25°C, R_L = 100Ω across Q and /Q, unless otherwise stated.

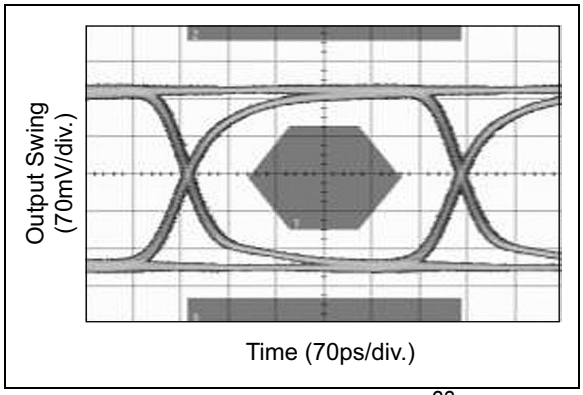


FIGURE 2-7: *2xGBE Mask (2^{23}–1 PRBS).*

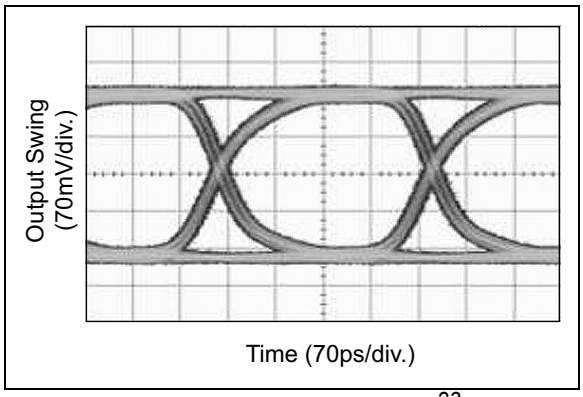


FIGURE 2-8: *3.2 Gbps Eye (2^{23}–1 PRBS).*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
4, 2, 32, 30, 27, 25, 23, 21	IN0, /IN0 IN1, /IN1 IN2, /IN2 IN3, /IN3	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-coupled signals as small as 100 mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Unused differential input pairs can be terminated by connecting one input to VCC and the complementary input to GND through a 1 kΩ resistor. The VT pin is to be left open in this configuration. Please refer to the Input Interface Applications section for more details.
3, 31 26, 22	VT0, VT1, VT2, VT3	Input Termination Center-Tap: Each side of the differential input pair, terminates to a VT pin. The VT0, VT1, VT2, VT3 pins provide a center-tap to a termination network for maximum interface flexibility. See the Input Interface Applications section for more details.
6, 19	SEL0, SEL1	These single-ended TTL-/CMOS-compatible inputs select the inputs to the multiplexers. Note that these inputs are internally connected to a 25 kΩ pull-up resistor and will default to a logic HIGH state if left open. Input switching threshold is $V_{CC}/2$.
1, 5, 8, 17, 20, 24, 28, 29	VCC	Positive Power Supply: Bypass with 0.1 µF||0.01 µF low ESR capacitors. The 0.01 µF capacitor should be as close to a VCC pin as possible.
10, 11	Q, /Q	Differential Outputs: This LVDS output pair is the output of the device. It is a logic function of the IN0, IN1, IN2, IN3, SEL0, and SEL1 inputs. Please refer to Table 3-2 for details.
7, 9, 12, 13, 16, 18	GND, Exposed Pad	Ground: Ground pin and exposed pad must be connected to the same ground plane.
14,15	NC	No connect (unused pins).

TABLE 3-2: TRUTH TABLE

IN0	IN1	IN2	IN3	SEL0	SEL1	Q	/Q
0	X	X	X	0	0	0	1
1	X	X	X	0	0	1	0
X	0	X	X	1	0	0	1
X	1	X	X	1	0	1	0
X	X	0	X	0	1	0	1
X	X	1	X	0	1	1	0
X	X	X	0	1	1	0	1
X	X	X	1	1	1	1	0

4.0 TIMING DIAGRAM

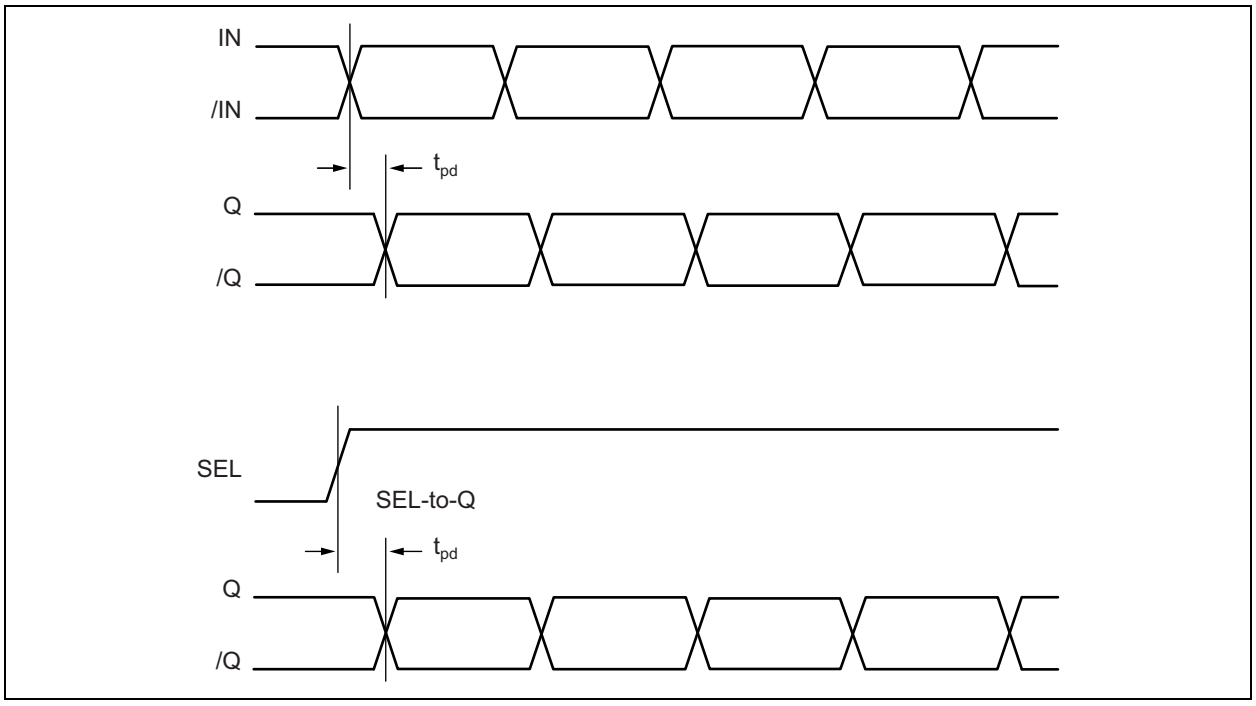


FIGURE 4-1: *Timing Diagram.*

5.0 SINGLE-ENDED AND DIFFERENTIAL SWINGS

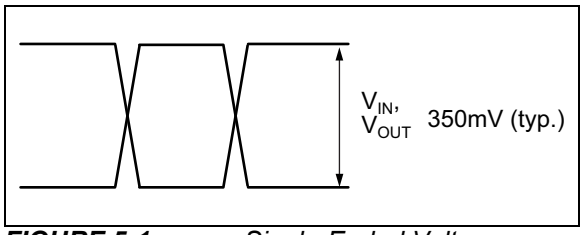


FIGURE 5-1: *Single-Ended Voltage Swing.*

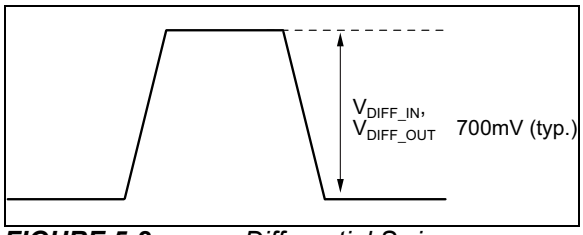


FIGURE 5-2: *Differential Swing.*

6.0 INPUT STAGE

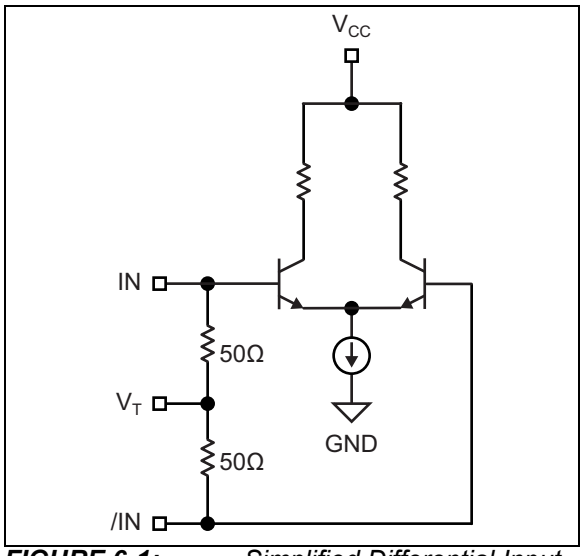


FIGURE 6-1: *Simplified Differential Input Stage.*

7.0 INPUT INTERFACE APPLICATIONS

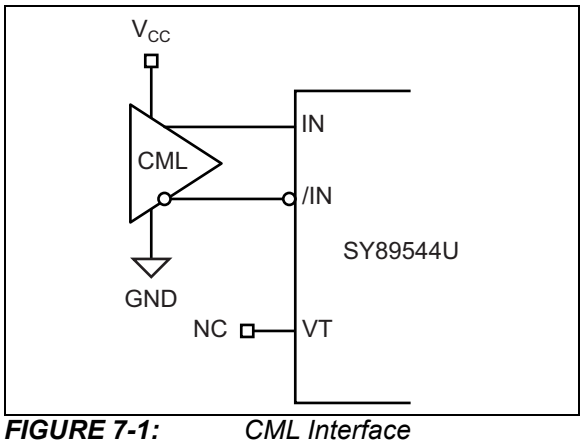


FIGURE 7-1: *CML Interface (DC-Coupled).*

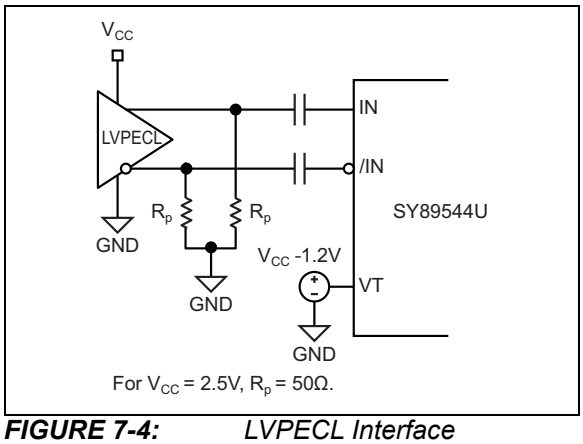


FIGURE 7-4: *LVPECL Interface (AC-Coupled).*

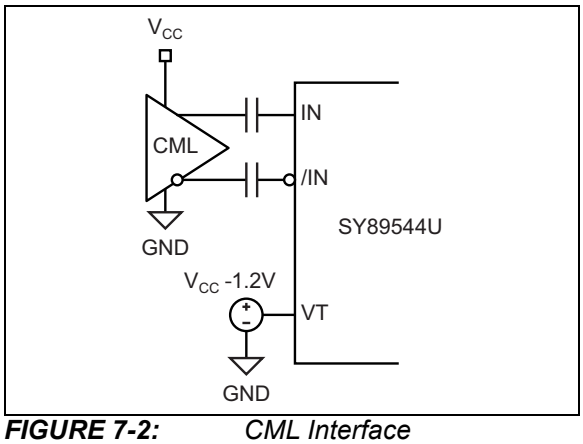


FIGURE 7-2: *CML Interface (AC-Coupled).*

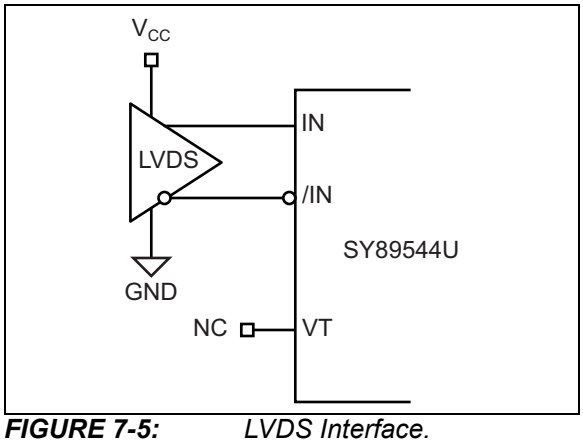


FIGURE 7-5: *LVDS Interface.*

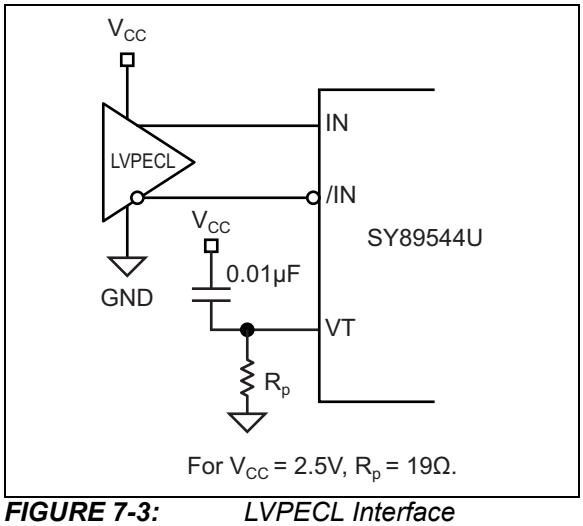


FIGURE 7-3: *LVPECL Interface (DC-Coupled).*

8.0 LVDS OUTPUTS

LVDS specifies a small swing of 350 mV typical, on a nominal 1.2V common mode above ground. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum, to keep EMI low.

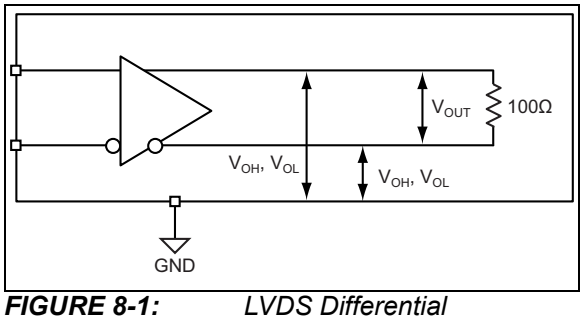


FIGURE 8-1: *LVDS Differential Measurement.*

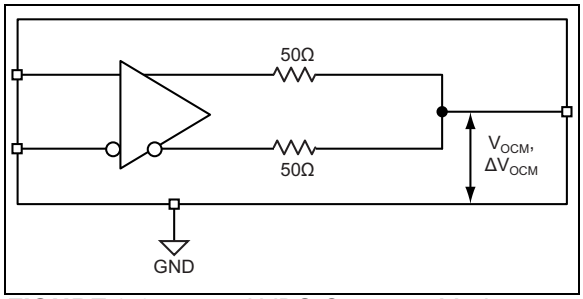
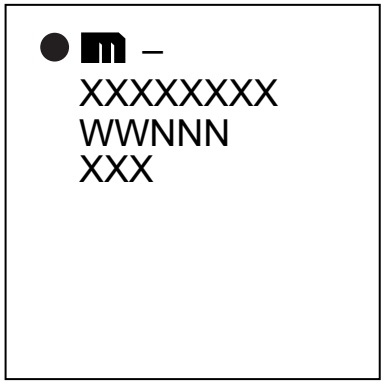


FIGURE 8-2: *LVDS Common Mode Measurement.*

9.0 PACKAGING INFORMATION

9.1 Package Marking Information

32-Pin QFN*



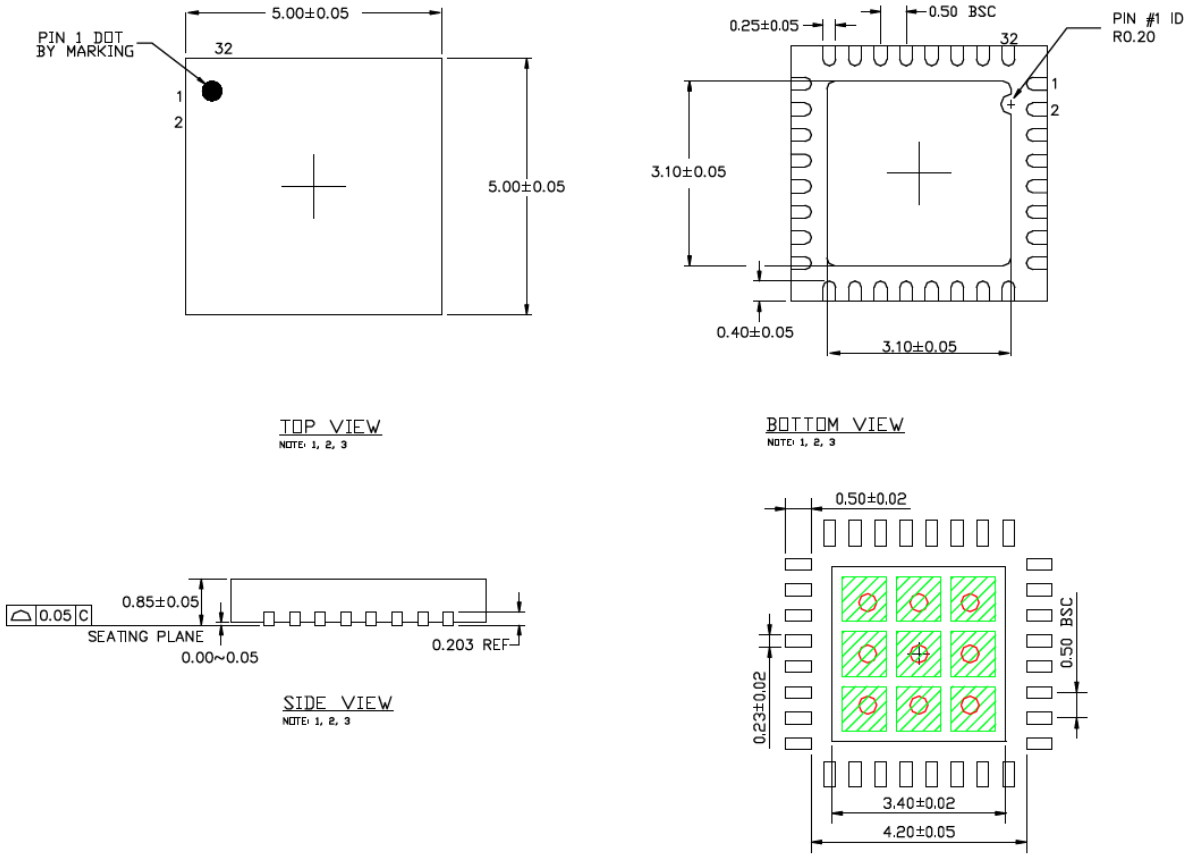
Example

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

TITLE

32 LEAD QFN 5x5mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	QFN55-32LD-PL-1	UNIT	MM



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) INDICATE SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.87x0.87 MM IN SIZE, 1.07 MM PITCH.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: REVISION HISTORY

Revision A (March 2019)

- Converted Micrel document SY89544U to Microchip data sheet DS20006174A.
- Fixed an error in the Package Type image where Pin 2 and Pin 4 were swapped.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XX
Device	Voltage Option	Package	Temperature Range	Special Processing

Device:	SY89544:		2.5V, 3.2 Gbps, Differential 4:1 LVDS Multiplexer with Internal Termination
Voltage Option:	U	=	2.5V
Package:	M	=	32-Lead 5 mm x 5 mm QFN
Temperature Range:	G	=	–40°C to +85°C (Pb-Free NiPdAu)
Special Processing:	<blank>=		60/Tube
	TR	=	1,000/Reel

Examples:

a) SY89544UMG: 2.5V, 3.2 Gbps, Differential 4:1 LVDS Multiplexer with Internal Termination, 2.5V, 32-Lead 5 mm x 5 mm QFN, –40°C to +85°C (Pb-Free NiPdAu), 60/Tube

b) SY89544UMG-TR: 2.5V, 3.2 Gbps, Differential 4:1 LVDS Multiplexer with Internal Termination, 2.5V, 32-Lead 5 mm x 5 mm QFN, –40°C to +85°C (Pb-Free NiPdAu), 1,000/Tube

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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