



SY58052AU

Ultra-Precision CML Data and Clock
Synchronizer with Internal Input and Output
Termination

Precision Edge®

General Description

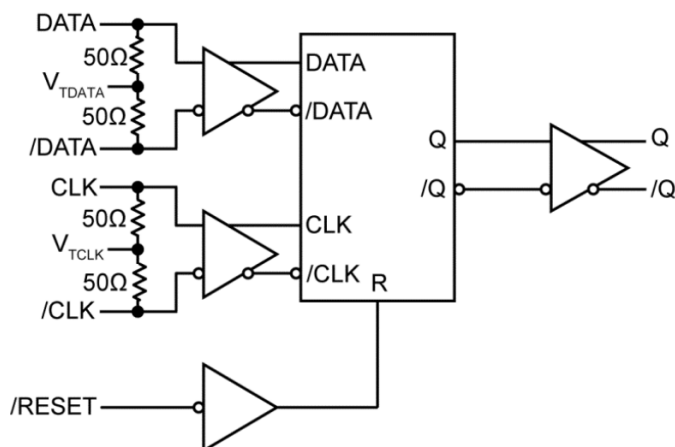
The SY58052AU is an ultra-fast, precision, low jitter data-to-clock resynchronizer with a guaranteed maximum data throughput of 10.7Gbps and a maximum clock of 10.7GHz. The SY58052AU is an ideal solution for backplane retiming or retiming after the data passes through long trace lengths. Serial data comes into the data input, and the CML output is synchronous to the input reference clock's rising edge.

The SY58052AU differential inputs include a unique, internal termination design that allows access to the termination network through a V_T pin. This feature allows the device to easily interface to different logic standards, both AC- and DC-coupled, without external resistor-bias and termination networks. The result is a clean, stub-free, low-jitter interface solution. The differential CML output is optimized for 50 Ω environments with internal 50 Ω source termination and a 400mV output swing.

The SY58052AU operates from a 2.5V or 3.3V supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). The SY58052AU is part of a Micrel's Precision Edge® product family.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Functional Block Diagram



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Revision 1.0

FOMhelp@micrel.com or (408) 955-1690

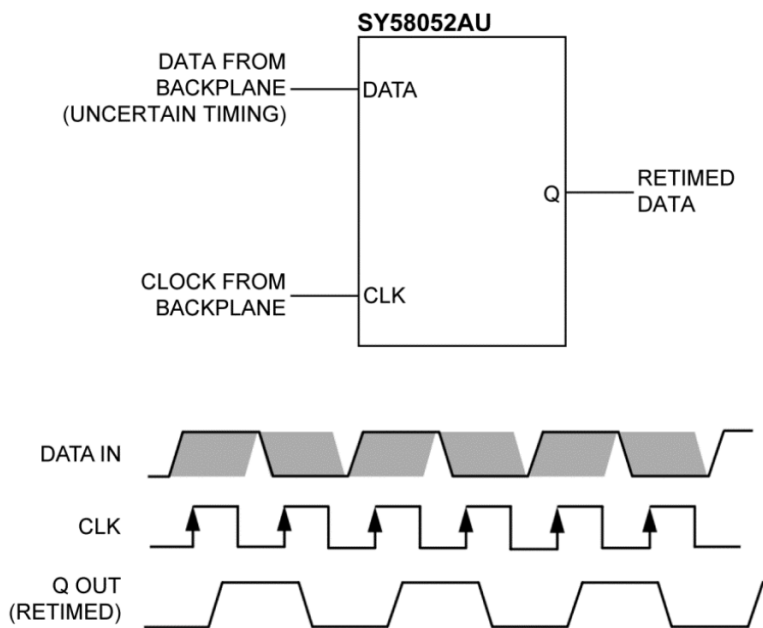
Features

- Resynchronize data to a reference clock
- Guaranteed AC performance over temperature and voltage:
 - DC-to > 10.7Gbps data rate throughput
 - DC-to > 10.7GHz clock f_{MAX}
 - 160ps any in-to-out t_{PD}
 - 30ps typical Rise/Fall time
- Ultra low-jitter design:
 - 0.3ps_{RMS} typical random jitter
 - 3ps_{PP} typical deterministic jitter (data)
 - < 10ps_{PP} total jitter (clock)
- Internal 50 Ω input termination
- Unique input termination and V_T pin accepts DC- and AC-coupled inputs (CML, PECL)
- Internal 50 Ω output source termination
- 400mV CML output swing
- Power supply: 2.5V \pm 5% or 3.3V \pm 10%
- –40°C to +85°C industrial temperature range
- Available in a 3mm \times 3mm 16-pin QFN package

Applications

- Data communications systems
- Serial OC-192, OC192+FEC data-to-clock realignment
- Parallel 10Gbps for OC-768
- All SONET OC-3 – OC-768 applications
- Fiber channel
- Gigabit Ethernet
- ATE
- Test and measurement

Typical Application

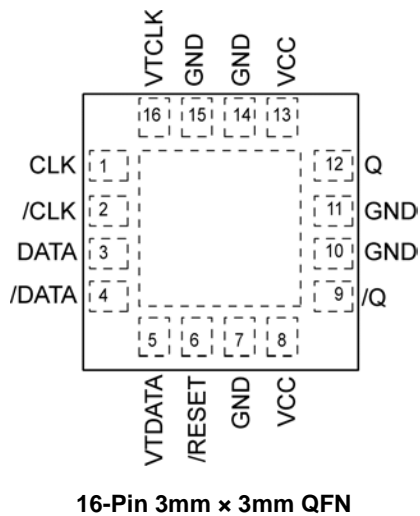


Ordering Information⁽¹⁾

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|-------------------------------|------------------|-----------------|--------------------------------------|----------------|
| SY58052AUMG | 3mm × 3mm QFN-16 | Industrial | 052A with Pb-Free Bar Line Indicator | NiPdAu Pb-Free |
| SY58052AUMG TR ⁽²⁾ | 3mm × 3mm QFN-16 | Industrial | 052A with Pb-Free Bar Line Indicator | NiPdAu Pb-Free |

- Notes:
- 1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
 - 2. Tape and reel.





Pin Configuration



Pin Description

| Pin Number | Pin Name | Pin Function |
|-------------------|----------------------|--|
| 1, 2 | CLK, /CLK | Differential Input: This input pair is the clock signal that re-times the data signal at DATA, /DATA. Each pin of this pair internally terminates to the VTCLK pin to 50Ω. Note that this input will default to an indeterminate state if left open (see Input Interface Applications). |
| 3, 4 | DATA, /DATA | Differential Input: This input pair is the signal to be synchronized by the CLK, /CLK signal. Each pin of this pair internally terminates to the VTDATA pin to 50Ω. Note that this input will default to an indeterminate state if left open (see Input Interface Applications). |
| 5 | VTDATA | Input Termination Center-Tap: Each of the two inputs, DATA, /DATA terminates to this pin. The VTDATA pin provides a center-tap to a termination network for maximum interface flexibility (see Input Interface Applications). |
| 6 | /RESET | TTL/CMOS-Compatible Input: The /RESET input asynchronously forces the Q output to a logic "0" state whenever it is active low. Possible state changes due to rising edges on CLK, /CLK are ignored until /RESET goes inactive high. |
| 7, 10, 11, 14, 15 | GND (Exposed Pad) | Ground. Exposed pad must be connected to the same potential as the GND pin. |
| 8, 13 | VCC | Positive Power Supply. Bypass with 0.1μF 0.01μF low-ESR capacitors. |
| 12, 9 | Q, /Q | Differential Output: This CML output pair is the output of the flip-flop. The data input is transferred to the Q output at the rising edge of CLK (falling edge of /CLK) (see Input Interface Applications). |
| 16 | VTCLK | Input Termination Center-Tap: Each of the two inputs, CLK, /CLK terminates to this pin. The VTCLK pin provides a center-tap to a termination network for maximum interface flexibility (see Input Interface Applications). |

Truth Table

| DATA | /DATA | CLK | /CLK | /RESET | Q | /Q |
|------|-------|---|---|--------|-----------|------------|
| X | X | X | X | 0 | 0 | 1 |
| X | X | 0 | 1 | 1 | Q_{N-1} | $/Q_{N-1}$ |
| X | X | 1 | 0 | 1 | Q_{N-1} | $/Q_{N-1}$ |
| 0 | 1 |  |  | 1 | 0 | 1 |
| 1 | 0 |  |  | 1 | 1 | 0 |

Absolute Maximum Ratings⁽³⁾

Supply Voltage (V_{CC}) -0.5V to +4.0V
 Input Voltage (V_{IN}) -0.5V to V_{CC}
 CML Output Voltage (V_{OUT}) $V_{CC} - 1.0V$ to $V_{CC} + 0.5V$
 Termination Current⁽⁶⁾
 Source or Sink Current on VTDATA, VCLK $\pm 60mA$
 Input Current
 Source or Sink Current on DATA, /DATA, CLK, /CLK
 $\pm 30mA$
 Lead Temperature (soldering, 20s) +260°C
 Storage Temperature (T_S) -65°C to +150°C

Operating Ratings⁽⁴⁾

Supply Voltage
 (V_{CC}) +2.375V to +2.625V / +2.97V to 3.63V
 Ambient Temperature (T_A) -40°C to +85°C
 Package Thermal Resistance⁽⁵⁾
 QFN (θ_{JA})
 Still-Air 61°C/W
 QFN (ψ_{JB})
 Junction-to-Board 38°C/W

DC Electrical Characteristics⁽⁷⁾

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|----------------|--|---|-------|------|----------------|----------|
| V_{CC} | Power Supply | | 2.375 | | 2.625 | V |
| | | | 2.97 | | 3.63 | |
| I_{CC} | Power Supply Current | With load, for either 2.5V or 3.3V supply | | 42 | 60 | mA |
| R_{IN} | Differential Input Resistance (DATA, /DATA or CLK, /CLK) | | 90 | 100 | 110 | Ω |
| V_{IH} | Input HIGH Voltage (DATA, /DATA or CLK, /CLK) | Note 8 | 1.2 | | V_{CC} | V |
| V_{IL} | Input LOW Voltage (DATA, /DATA or CLK, /CLK) | Note 8 | 0 | | $V_{IH} - 0.1$ | V |
| V_{IN} | Input Voltage Swing (DATA, /DATA or CLK, /CLK) | Note 8, see Figure 4 | 100 | | | mV |
| V_{DIFF_IN} | Differential Input Voltage Swing (DATA, /DATA) or (CLK, /CLK) | Note 8, see Figure 5 | 200 | | | mV |
| $ I_{IN} $ | Input Current (DATA, /DATA) or (CLK, /CLK) | Note 8 | | | 21 | mA |

Notes:

- Permanent device damage may occur if the ratings in the Absolute Maximum Ratings are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
- The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
- Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} uses 4-layer θ_{JA} in still-air, unless otherwise stated.
- Due to the limited drive capability use for input of the same package only.
- The circuit is designed to meet the DC specifications shown in the DC Electrical Characteristics chart after thermal equilibrium has been established.
- Due to the internal termination (see [Input and Output Stage Internal Termination](#)) the input current depends on the applied voltages at DATA, /DATA and VTDATA inputs, or the CLK, /CLK and VTCLK inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit.

LVTTTL/CMOS DC Electrical Characteristics⁽⁹⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|----------|--------------------|-----------|------|------|------|---------|
| V_{IH} | Input HIGH Voltage | | 2.0 | | | V |
| V_{IL} | Input LOW Voltage | | | | 0.8 | mV |
| I_{IH} | Input HIGH Current | | -50 | | 20 | μA |
| I_{IL} | Input LOW Current | | -100 | | | μA |

CML Outputs DC Electrical Characteristics⁽⁹⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $R_L = 100\Omega$ across output pair or equivalent; $T_A = -40^\circ C$ to $+120^\circ C$, unless otherwise noted.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|-----------------|---|------------------------------|------------------|------|----------|----------|
| V_{OH} | Output HIGH Voltage (Q, /Q) | $R_L = 50\Omega$ to V_{CC} | $V_{CC} - 0.020$ | | V_{CC} | V |
| V_{OUT} | Output Voltage Swing (Q, /Q) | See Figure 4 | 325 | 400 | | mV |
| V_{DIFF_OUT} | Differential Output Voltage Swing (Q, /Q) | See Figure 5 | 650 | 800 | | mV |
| R_{OUT} | Output Source Impedance (Q, /Q) | | 45 | 50 | 55 | Ω |

AC Electrical Characteristics⁽¹⁰⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $R_L = 100\Omega$ across output pair or equivalent; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.

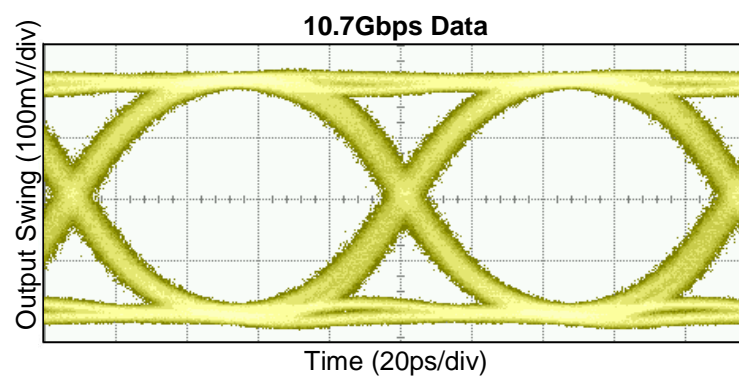
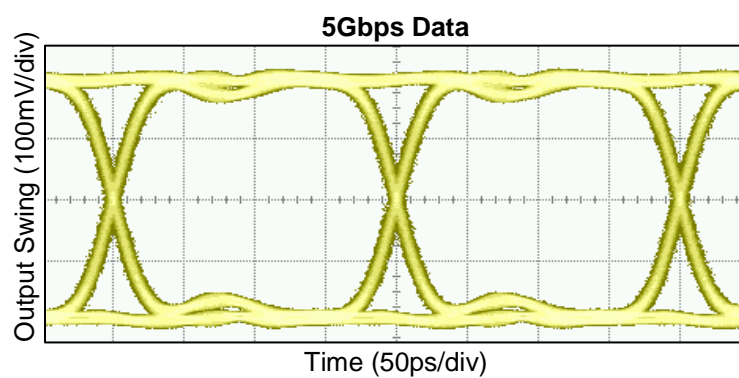
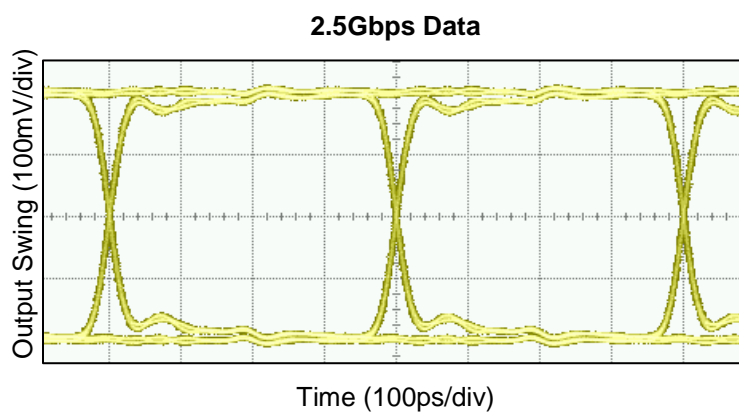
| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|--------------|--------------------------------|---|------|------|------|------------|
| f_{MAX} | Maximum Operating Frequency | Clock | 10.7 | | | GHz |
| | | Data | 10.7 | | | Gbps |
| t_{PD} | Propagation Delay (CLK-to-Q) | | 70 | | 160 | ps |
| t_{RESET} | Propagation Delay (Reset-to-Q) | | | | 300 | ps |
| t_S | Set-Up Time | | 20 | | | ps |
| t_H | Hold Time | | 20 | | | ps |
| t_{RR} | Reset Recovery Time | $V_{TH} = V_{CC}/2$ | 250 | | | ps |
| t_{JITTER} | Random Jitter (R_J) | Typical values at ambient temperature ⁽¹¹⁾ . | | 0.3 | 1 | ps_{RMS} |
| | Deterministic Jitter (D_J) | Typical values at ambient temperature ⁽¹²⁾ . | | 3 | 10 | |
| | Total Jitter (T_J) | Clock ⁽¹³⁾ | | | 10 | ps_{PP} |
| | | Data ⁽¹³⁾ | | | 14 | |
| t_r, t_f | Rise/Fall Times (20% to 80%) | At full output swing | | 30 | 50 | ps |

Notes:

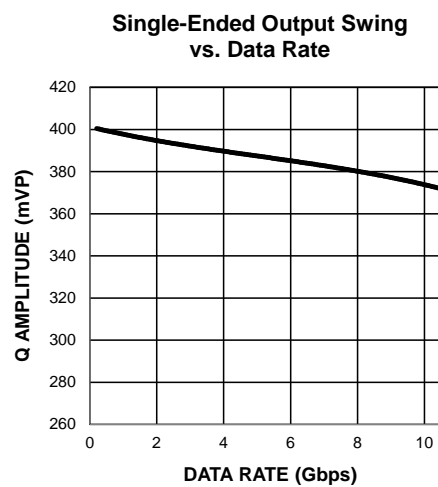
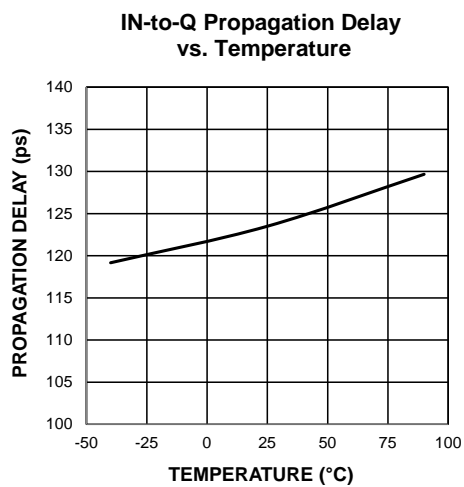
9. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
10. Measured with 100mV input swing (see Timing Diagrams for definition of parameters). High-frequency AC-parameters are guaranteed by design and characterization.
11. R_J is measured with a K28.7 comma detect character pattern, measured at 10.7Gbps and 2.5Gbps.
12. D_J is measured at 10.7Gbps and 2.5Gbps, with both K28.5 and $2^{23}-1$ PRBS pattern.
13. Total jitter definition: with an ideal clock input frequency of $\leq f_{MAX}$, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

Typical Operating Characteristics

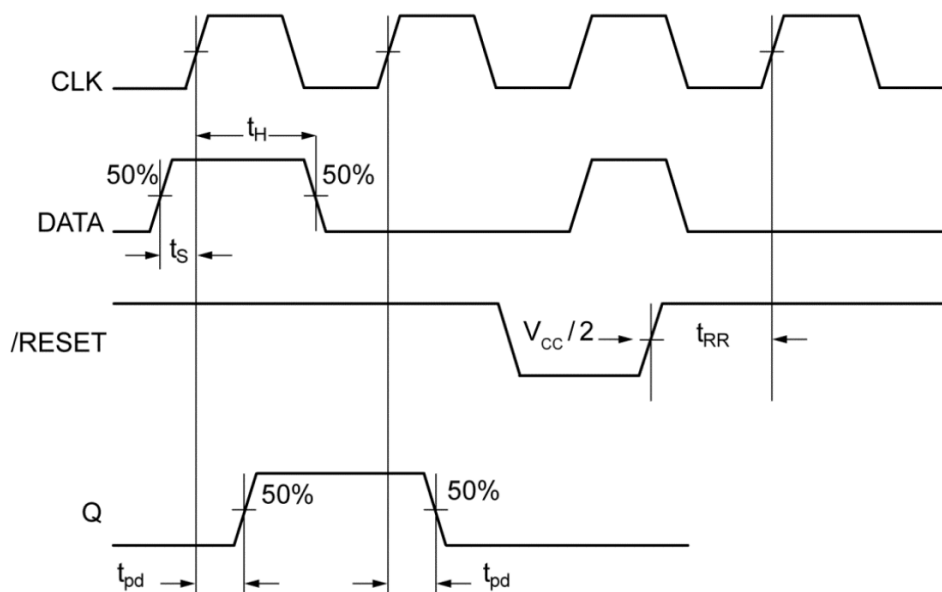
$V_{CC} = 3.3V$, $GND = 0V$, $CLK = 400mV$, $DATA = 400mV$, $T_A = +25^{\circ}C$



Typical Operating Characteristics (Continued)



Timing Diagram



Input and Output Stage Internal Termination

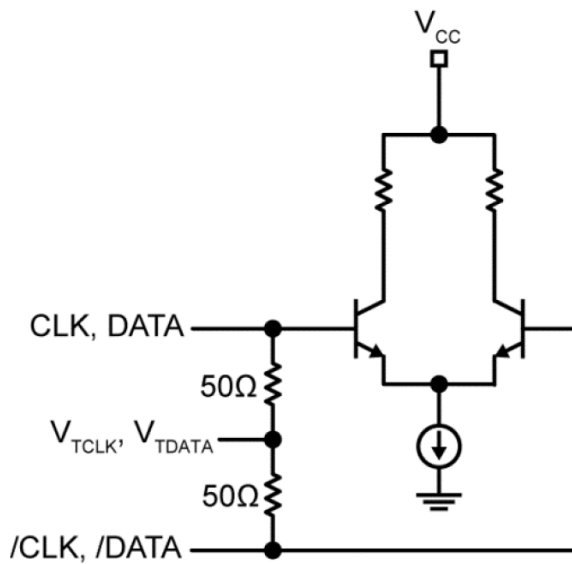


Figure 1. Simplified Differential Input Stage

Input and Output Stage Internal Termination (Continued)

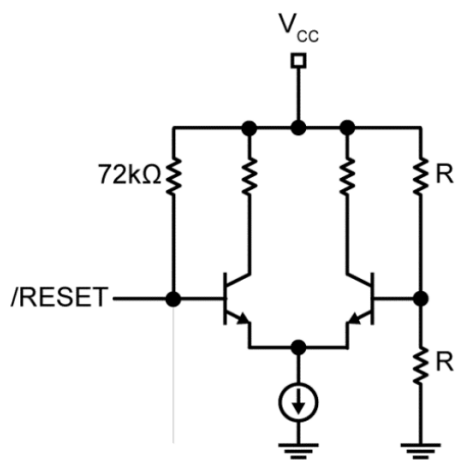


Figure 2. Simplified TTL/CMOS Input

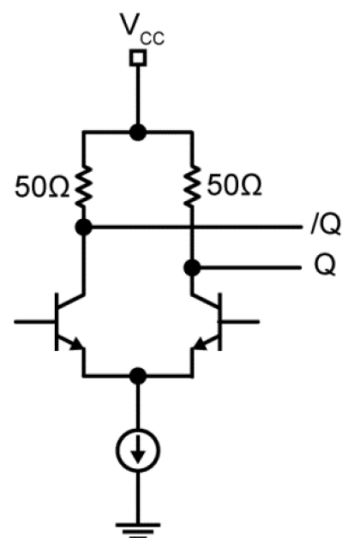


Figure 3. Simplified Differential Output Stage

Operating Characteristics

Definition of single-ended and differential swings.



Figure 4. Single-Ended Swing

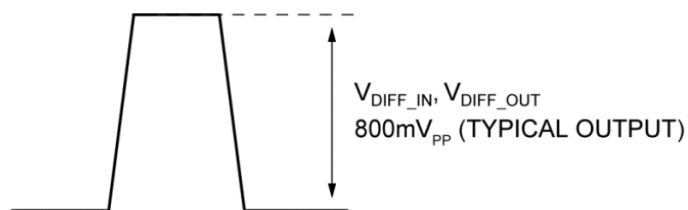
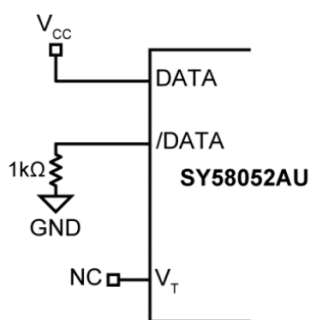


Figure 5. Differential Swing

Input Interface Applications



NOTE: INPUT HIGH LEVEL SHOWN

Figure 6. Static Input Level

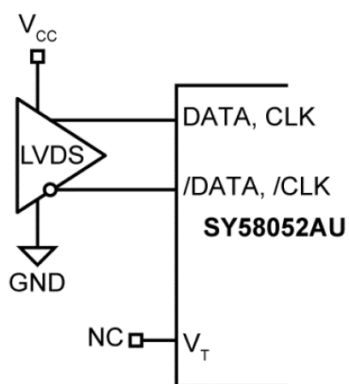
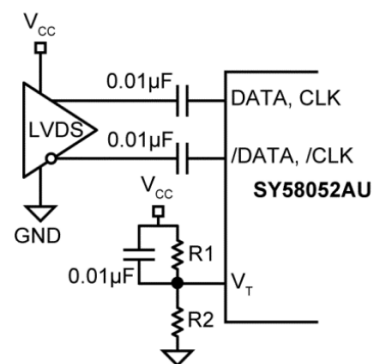


Figure 7. LVDS Interface (DC-Coupled)



NOTE: $R_1 = 1\text{k}\Omega$, $R_2 = 1.4\text{k}\Omega$

Figure 8. LVDS Interface (AC-Coupled)
Note: Be certain that the LVDS driver can be AC-coupled.

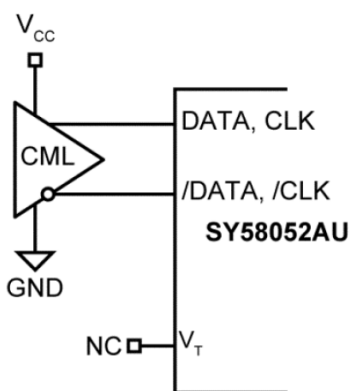
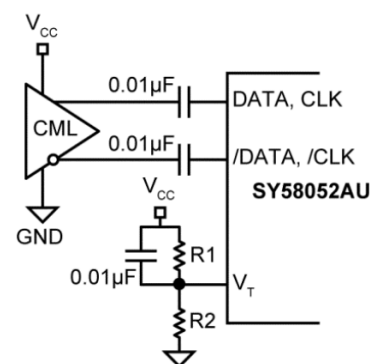


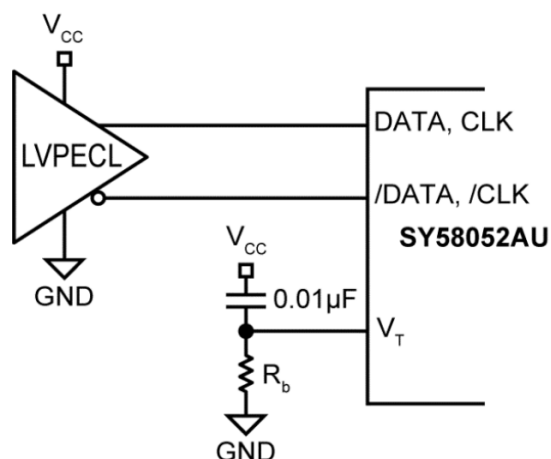
Figure 9. CML Interface (DC-Coupled)
(OPTION: V_T may be connected to V_{CC})



NOTE: $R_1 = 1\text{k}\Omega$, $R_2 = 1.4\text{k}\Omega$

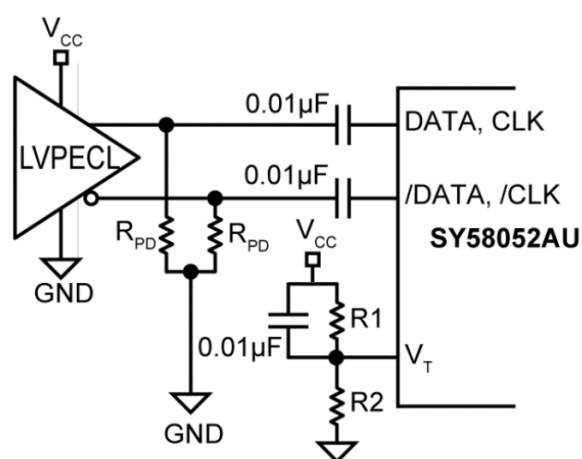
Figure 10. CML Interface (AC-Coupled)

Input Interface Applications (Continued)



NOTE: FOR 3.3V SUPPLY, $R_b = 50\Omega$
FOR 2.5V SUPPLY, $R_b = 19\Omega$

Figure 11. LVPECL Interface (DC-Coupled)



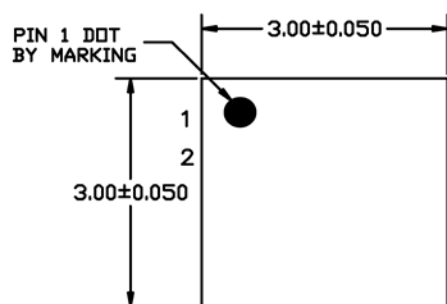
NOTE: FOR 2.5V, $R_{PD} = 50\Omega$, $R_1 = 1k\Omega$, $R_2 = 1.4k\Omega$.
FOR 3.3V, $R_{PD} = 100\Omega$, $R_1 = 1k\Omega$, $R_2 = 1.4k\Omega$

Figure 12. LVPECL Interface (AC-Coupled)

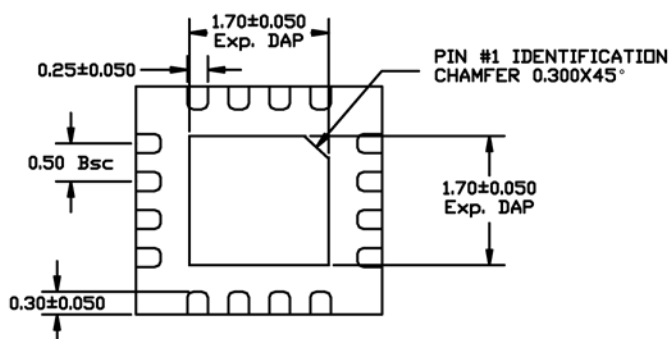
Related Product and Support Documentation

| Part Number | Function | Data Sheet Link |
|---------------|---|--|
| SY58016L | 3.3V 10Gbps Differential CML Line Driver/Receiver with Internal Termination | www.micrel.com/product-info/products/sy58061l.shtml |
| SY58051AU | 10.7Gbps AnyGate® with Internal Input and Output Termination | www.micrel.com/_PDF/HBW/SY58051AU.pdf |
| HBW Solutions | New Products and Applications | www.micrel.com/product-info/products/solutions.shtml |

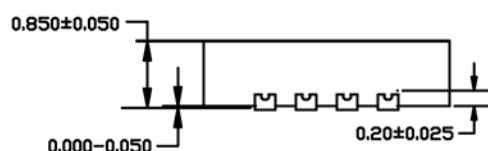
Package Information⁽¹⁴⁾



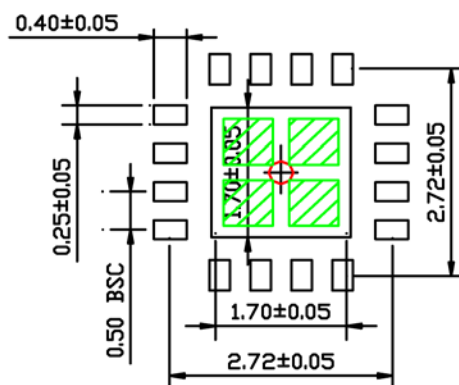
TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



SIDE VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN
NOTE: 4, 5

NOTE:

1. MAXIMUM PACKAGE WARPAGE IS 0.05mm.
2. MAXIMUM ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS
3. PIN #1 IS ON TOP AND WILL BE LASER MARKED.
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAXIMUM THERMAL PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) INDICATE SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60mmx0.60mm IN SIZE, 0.20mm SPACING.

16-Pin 3mm x 3mm QFN Package (MM)

Note:

14. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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