



# SST39LF010/SST39LF020/SST39LF040/ SST39VF010/SST39VF020/SST39VF040

## 1-Mbit/2-Mbit/4-Mbit (x8) Multi-Purpose Flash

### Features

- Organized as 128K x 8/256K x 8/512K x 8
- Single Voltage Read and Write Operations:
  - 3.0V-3.6V for SST39LF010/020/040
  - 2.7V-3.6V for SST39VF010/020/040
- Superior Reliability:
  - Endurance: 100,000 cycles (typical)
  - Greater than 100 years data retention
- Low-Power Consumption (typical values at 14 MHz):
  - Active current: 5 mA (typical)
  - Standby current: 1  $\mu$ A (typical)
- Sector Erase Capability:
  - Uniform 4-Kbyte sectors
- Fast Read Access Time:
  - 55 ns for SST39LF010/020/040
  - 70 ns for SST39VF010/020/040
- Latched Address and Data
- Fast Erase and Byte Program:
  - Sector Erase time: 18 ms (typical)
  - Chip Erase time: 70 ms (typical)
  - Byte Program time: 14  $\mu$ s (typical)
  - Chip Rewrite time:
    - 2 seconds (typical) for SST39LF/VF010
    - 4 seconds (typical) for SST39LF/VF020
    - 8 seconds (typical) for SST39LF/VF040
- Automatic Write Timing:
  - Internal VPP Generation
- End-of-Write Detection:
  - Toggle Bit
  - Data# Polling
- CMOS I/O Compatibility
- JEDEC<sup>®</sup> Standard:
  - Flash EEPROM pinouts and command sets
- All Devices are RoHS Compliant

### Packages

- 32-Lead PLCC
- 32-Lead TSOP

### Product Description

The SST39LF010/020/040 and SST39VF010/020/040 devices are 128K x8, 256K x8 and 5,124K x8 CMOS Multi-Purpose Flash (MPF) manufactured with Microchip's proprietary, high-performance CMOS SuperFlash<sup>®</sup> technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39LF010/020/040 devices write (Program or Erase) with a 3.0V-3.6V power supply while the SST39VF010/020/040 devices write (Program or Erase) with a 2.7V-3.6V power supply. The SST39LF010/020/040/SST39VF010/020/040 devices conform to JEDEC<sup>®</sup> standard pin assignments for x8 memories.

Featuring a high-performance Byte Program, the SST39LF010/020/040 and SST39VF010/020/040 devices provide a maximum Byte Program time of 20  $\mu$ sec. These devices use Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent writes, they have on-chip hardware and software data protection schemes. Designed, manufactured and tested for a broad range of applications, the SST39LF010/020/040 and SST39VF010/020/040 devices are offered with a typical endurance of 100,000 cycles and data retention exceeding 100 years.

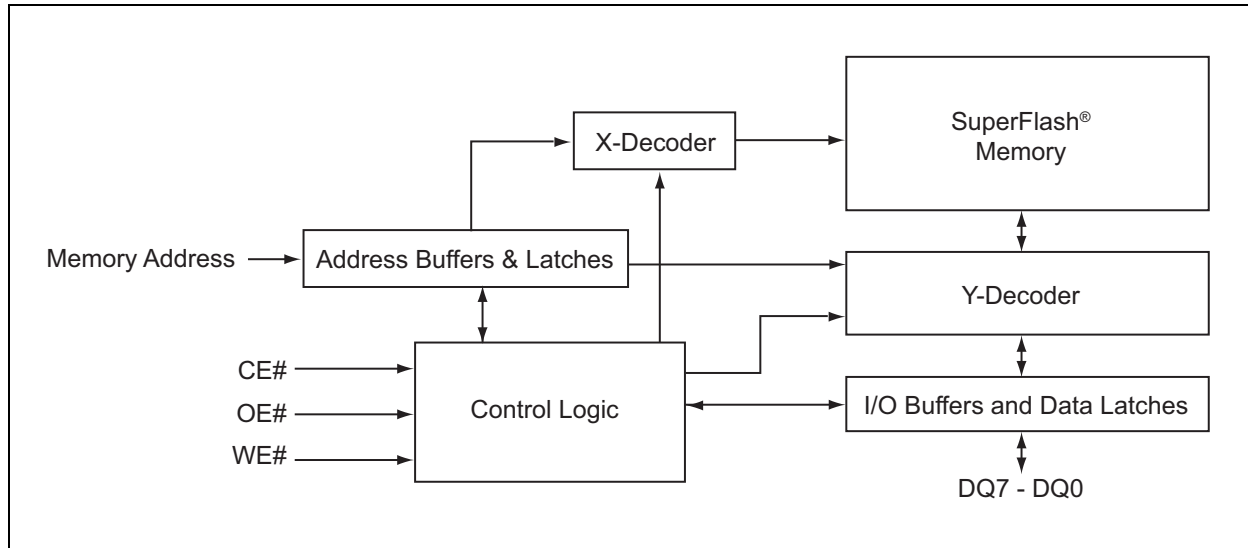
These devices are suited for applications that require convenient and economical updating of program, configuration or data memory. For all system applications, they significantly improve performance and reliability while lowering power consumption. They inherently use less energy during Erase and Program times than alternative Flash technologies. The total energy consumed is a function of the applied voltage, current and time of application. Since, for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative Flash technologies. These devices also improve flexibility while lowering the cost for program, data and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore, the system software or hardware does not have to be modified or derated as is necessary with alternative Flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

See [Figure 2-1](#) for pin assignments and [Table 2-1](#) for pin descriptions.

## 1.0 BLOCK DIAGRAM

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



# SST39LF010/020/040/SST39VF010/020/040

## 2.0 PIN DESCRIPTION

FIGURE 2-1: PIN ASSIGNMENTS

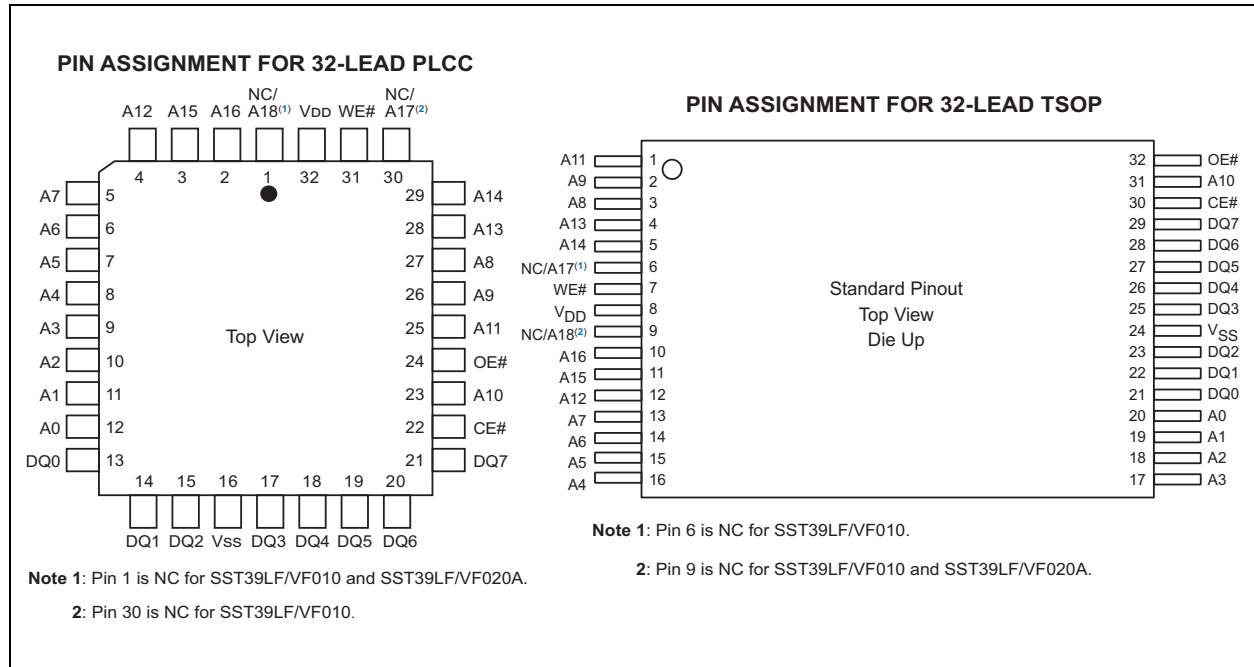


TABLE 2-1: PIN DESCRIPTION

Symbol	Pin Name	Functions
$A_{MS}^{(1)}$ -A0	Address Inputs	Provide memory addresses. During Sector Erase $A_{MS}$ -A12 address lines will select the sector. During Block Erase $A_{MS}$ -A16 address lines will select the block.
DQ7-DQ0	Data Input/Output	Output data during Read cycles and receive input data during Write cycles. Data are internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	Activate the device when CE# is low.
OE#	Output Enable	Gate the data output buffers.
WE#	Write Enable	Control the Write operations.
VDD	Power Supply	Provide power supply voltage: 3.0V-3.6V for SST39LF010/020/040 3.0V-3.6V for SST39VF010/020/040
VSS	Ground	
NC	No Connection	Unconnected pins.

**Note 1:**  $A_{MS}$  = Most significant address  
 $A_{MS}$  = A16 for SST39LF/VF010, A17 for SST39LF/VF020 and A18 for SST39LF/VF040

## 3.0 DEVICE OPERATION

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

### 3.1 Read

The Read operation of the SST39LF010/020/040 and SST39VF010/020/040 devices is controlled by CE# and OE#, and both must be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in a high-impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram (Figure 7-1) for further details.

### 3.2 Byte Program Operation

The SST39LF010/020/040 and SST39VF010/020/040 devices are programmed on a byte-by-byte basis. Before programming, the sector containing the byte must be completely erased. The Program operation is accomplished in three steps.

1. The first step is the three-byte load sequence for Software Data Protection.
2. The second step is to load byte address and byte data. During the Byte Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data are latched on the rising edge of either CE# or WE#, whichever occurs first.
3. The third step is the internal Program operation, which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first.

Once initiated, the Program operation, will be completed within 20  $\mu$ s. See Figure 7-2 and Figure 7-3 for WE# and CE# controlled Program operation timing diagrams and Figure 7-12 for a flowchart. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

### 3.3 Sector Erase Operation

The Sector Erase operation allows the system to erase the device on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 Kbytes. The Sector Erase operation is initiated by executing a six-byte command load sequence for Software Data Protection with Sector Erase command (30H) and Sector Address (SA) in the last bus cycle. The sector address is latched on the falling edge of the sixth WE# pulse, while the command (30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 7-6 for timing waveforms. Any commands written during the Sector Erase operation will be ignored.

### 3.4 Chip Erase Operation

The SST39LF010/020/040 and SST39VF010/020/040 devices provide Chip Erase operation, which allows the user to erase the entire memory array to the '1's state. This is useful when the entire device must be quickly erased.

The Chip Erase operation is initiated by executing a six-byte Software Data Protection command sequence with Chip Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the internal Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4-2 for the command sequence, Figure 7-7 for the timing diagram and Figure 7-15 for the flowchart. Any commands written during the Chip Erase operation will be ignored.

### 3.5 Write Operation Status Detection

The SST39LF010/020/040 and SST39VF010/020/040 devices offer two software methods to detect the completion of a Write (Program or Erase) cycle, thereby optimizing the system's Write cycle time. The software detection includes two status bits: Data# Polling (DQ7) and Toggle Bit (DQ6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system. Therefore, Data# Polling or Toggle Bit maybe be read concurrently with the completion of the write cycle. If this occurs, the system may receive incorrect results from the status detection process. For example, valid data may appear to conflict with either DQ7 or DQ6. To prevent false results upon detection of failures, the software routine should loop to read the accessed location an additional two times. If both reads are valid, then the device has completed the Write cycle; otherwise the failure is valid.

### 3.6 Data# Polling (DQ7)

When the SST39LF010/020/040/SST39VF010/020/040 devices are undergoing internal Program operation, any attempt to read DQ7 will produce the complement of the true data. Once the Program operation is completed, DQ7 will produce true data. Note that even though DQ7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid. Valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1  $\mu$ s. During an internal Erase operation, any attempt to read DQ7 will produce a '0'. Once the internal Erase operation is completed, DQ7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector or Chip Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See [Figure 7-4](#) for the Data# Polling timing diagram and [Figure 7-13](#) for a flowchart.

### 3.7 Toggle Bit (DQ6)

During the internal Program or Erase operation, consecutive attempts to read DQ6 will produce alternating '0's and '1's, i.e., toggling between '0' and '1'. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector or Chip Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See [Figure 7-5](#) for the Toggle Bit timing diagram and [Figure 7-13](#) for a flowchart.

### 3.8 Data Protection

The SST39LF010/020/040/SST39VF010/020/040 devices provide both hardware and software features to protect nonvolatile data from inadvertent writes.

### 3.9 Hardware Data Protection

*Noise/Glitch Protection:* A WE# or CE# pulse of less than 5 ns will not initiate a Write cycle.

*VDD Power-Up/Down Detection:* The Write operation is inhibited when VDD is less than 1.5V.

*Write Inhibit Mode:* Forcing OE# low, CE# high, or WE# high will inhibit the Write operation, preventing inadvertent writes during power-up or power-down.

### 3.10 Software Data Protection (SDP)

The SST39LF010/020/040/SST39VF010/020/040 devices provide the JEDEC<sup>®</sup>-approved Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte load sequence.

The SST39LF010/020/040/SST39VF010/020/040 devices are shipped with the Software Data Protection permanently enabled. See [Table 4-2](#) for the specific software command codes. During the SDP command sequence, invalid commands will abort the device to Read mode, within TRC.

### 3.11 Product Identification

The Product Identification mode identifies the device as the SST39LF/VF010, SST39LF/VF020 or SST39LF/VF040 and the manufacturer as Microchip. This mode may be accessed through software operations. Users may wish to utilize the software Product Identification operation to identify the part (i.e., using the device ID) when multiple manufacturers are used in the same socket. For further details, see [Table 4-2](#) for software operation, [Figure 7-8](#) for the software ID Entry and Read timing diagram and [Figure 7-14](#) for the ID Entry command sequence flowchart.

**TABLE 3-1: PRODUCT IDENTIFICATION**

		Address	Data
Manufacturer's ID		0000H	BFH
Device ID:	SST39LF/VF010	0001H	D5H
	SST39LF/VF020	0001H	D6H
	SST39LF/VF040	0001H	D7H

## 3.12 Product Identification Mode Exit/Reset

To return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the software ID Exit command sequence, which returns the device to the Read operation. Please note that the software ID Exit command is ignored during an internal Program or Erase operation. See [Table 4-2](#) for the software command codes, [Figure 7-9](#) for the timing waveform and [Figure 7-14](#) for a flowchart.

# SST39LF010/020/040/SST39VF010/020/040

## 4.0 OPERATIONS

**TABLE 4-1: OPERATION MODES SELECTION**

Mode	CE#	OE#	WE#	DQ	Address
Read	VIL	VIL	VIH	DOUT	AIN
Program	VIL	VIH	VIL	DIN	AIN
Erase	VIL	VIH	VIL	X <sup>(1)</sup>	Sector address, XXH for Chip Erase
Standby	VIH	X	X	High-Z	X
Write Inhibit	X	VIL	X	High-Z/DOUT	X
	X	X	VIH	High-Z/DOUT	X
Product Identification					
Software Mode	VIL	VIH	VIL		see Table 4-2

**Note 1:** X can be VIL or VIH, but no other value.

**TABLE 4-2: SOFTWARE COMMAND SEQUENCE**

Command Sequence	1 <sup>st</sup> Bus Write Cycle		2 <sup>nd</sup> Bus Write Cycle		3 <sup>rd</sup> Bus Write Cycle		4 <sup>th</sup> Bus Write Cycle		5 <sup>th</sup> Bus Write Cycle		6 <sup>th</sup> Bus Write Cycle	
	Addr <sup>(1)</sup>	Data <sup>(2)</sup>	Addr <sup>(1)</sup>	Data <sup>(2)</sup>	Addr <sup>(1)</sup>	Data <sup>(2)</sup>	Addr <sup>(1)</sup>	Data <sup>(2)</sup>	Addr <sup>(1)</sup>	Data <sup>(2)</sup>	Addr <sup>(1)</sup>	Data <sup>(2)</sup>
Byte Program	5555H	AAH	2AAAH	55H	5555H	A0H	BA <sup>(2)</sup>					
Sector Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA <sub>X</sub> <sup>(3)</sup>	30H
Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry <sup>(4,5)</sup>	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit <sup>(6)</sup>	XXH	F0H										
Software ID Exit <sup>(6)</sup>	5555H	AAH	2AAAH	55H	5555H	F0H						

**Note 1:** Address format A14-A0 (Hex), Addresses AMS- A15 can be VIL or VIH, but no other value, for the command sequence.

AMS = Most significant address

AMS = A16 for SST39LF/VF010, A17 for SST39LF/VF020 and A18 for SST39LF/VF040.

**2:** BA = Program Byte address.

**3:** SA<sub>X</sub> for Sector Erase; uses AMS = A12 address lines.

**4:** The device does not remain in Software Product ID mode if powered down.

**5:** With AMS-A1 = 0; SST Manufacturer's ID = BFH, is read with A0 = 0,  
 SST39LF/VF010 Device ID = D5H, is read with A0 = 1.  
 SST39LF/VF020 Device ID = D6H, is read with A0 = 1.  
 SST39LF/VF040 Device ID = D7H, is read with A0 = 1.

**6:** Both Software ID Exit operations are equivalent.

# SST39LF010/020/040/SST39VF010/020/040

## 5.0 ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings (†)

Temperature under bias .....	-55°C to +125°C
Storage temperature .....	-65°C to +150°C
DC voltage on any pin to ground potential .....	-0.5V to V <sub>DD</sub> +0.5V
Transient voltage (<20 ns) on any pin to ground potential .....	-2.0V to V <sub>DD</sub> +2.0V
Voltage on A9 pin to ground potential .....	-0.5V to 13.2V
Package power dissipation capability (T <sub>A</sub> = +25°C).....	1.0W
Surface mount solder reflow temperature (10 seconds) <sup>(1)</sup> .....	+260°C
Output short circuit current <sup>(2)</sup> .....	50 mA

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Note 1:** Excluding certain with-Pb 32-PLCC units, all packages are +260°C capable in both non-Pb and with-Pb solder versions. Certain with-Pb 32-PLCC package types are capable of +240°C for 10 seconds; please consult the factory for the latest information.

**2:** Output shorted for no more than one second. No more than one output shorted at a time.

**TABLE 5-1: OPERATING RANGE FOR SST39LF010/020/040**

Range	Ambient Temperature	V <sub>DD</sub>
Commercial	0°C to +70°C	3.0V-3.6V

**TABLE 5-2: OPERATING RANGE FOR SST39VF010/020/040**

Range	Ambient Temperature	V <sub>DD</sub>
Commercial	0°C to +70°C	2.7V-3.6V
Industrial	-40°C to +85°C	2.7V-3.6V

**TABLE 5-3: AC CONDITIONS OF TEST<sup>(1)</sup>**

Input Rise/Fall Time	Output Load
5 ns	CL = 30 pF for SST39LF010/020/040
	CL = 100 pF for SST39VF010/020/040

**Note 1:** See [Figure 7-10](#) and [Figure 7-11](#).



# SST39LF010/020/040/SST39VF010/020/040

## 6.0 DC CHARACTERISTICS

**TABLE 6-1: DC OPERATING CHARACTERISTICS (V<sub>DD</sub> = 3.0V-3.6V FOR SST39LF010/020/040 AND 2.7V-3.6V FOR SST39VF010/020/040)<sup>(1)</sup>**

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
IDD	Power Supply Current	—	—		Address Input = V <sub>ILT</sub> /V <sub>IHT</sub> , @ f = 1/TRC minimum V <sub>DD</sub> = V <sub>DD</sub> maximum
	Read <sup>(2)</sup>	—	20	mA	CE# = V <sub>IL</sub> , OE# = WE# = V <sub>IH</sub> all I/Os open
	Program and Erase <sup>(2)</sup>	—	30	mA	CE# = WE# = V <sub>IL</sub> , OE# = V <sub>IH</sub>
ISB	Standby Current V <sub>DD</sub>	—	15	μA	CE# = V <sub>IH</sub> , V <sub>DD</sub> = V <sub>DD</sub> maximum
ILI	Input Leakage Current	—	1	μA	V <sub>IN</sub> = GND to V <sub>DD</sub> , V <sub>DD</sub> = V <sub>DD</sub> maximum
ILO	Output Leakage Current	—	10	μA	V <sub>OUT</sub> = GND to V <sub>DD</sub> , V <sub>DD</sub> = V <sub>DD</sub> maximum
V <sub>IL</sub>	Input Low Voltage	—	0.8	V	V <sub>DD</sub> = V <sub>DD</sub> minimum
V <sub>IH</sub>	Input High Voltage	0.7V <sub>DD</sub>	—	V	V <sub>DD</sub> = V <sub>DD</sub> maximum
V <sub>IHC</sub>	Input High Voltage (CMOS)	V <sub>DD</sub> -0.3	—	V	V <sub>DD</sub> = V <sub>DD</sub> maximum
V <sub>OL</sub>	Output Low Voltage	—	0.2	V	I <sub>OL</sub> = 100 μA, V <sub>DD</sub> = V <sub>DD</sub> minimum
V <sub>OH</sub>	Output High Voltage	V <sub>DD</sub> -0.2	—	V	I <sub>OH</sub> = 100 μA, V <sub>DD</sub> = V <sub>DD</sub> minimum

**Note 1:** Typical conditions for the Active Current shown on the front page of the data sheet are average values at +25°C (room temperature) and V<sub>DD</sub> = 3V for VF devices. Not 100% tested.

**2:** Values are for 70 ns conditions. See the *Multi-Purpose Flash Power Rating* application note for further information.

**3:** 30 mA maximum for Erase operations in the industrial temperature range.

**TABLE 6-2: RECOMMENDED SYSTEM POWER-UP TIMINGS**

Symbol	Parameter	Minimum	Units
TPU-READ <sup>(1)</sup>	Power-Up to Read Operation	100	μs
TPU-WRITE <sup>(1)</sup>	Power-Up to Erase/Program Operation	100	μs

**Note 1:** This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 6-3: CAPACITANCE (T<sub>A</sub> = +25°C, F = 1 MHZ, OTHER PINS OPEN)**

Parameter	Description	Test Condition	Maximum
C <sub>I/O</sub> <sup>(1)</sup>	I/O Pin Capacitance	V <sub>I/O</sub> = 0V	12 pF
C <sub>IN</sub> <sup>(1)</sup>	Input Capacitance	V <sub>IN</sub> = 0V	6 pF

**Note 1:** This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 6-4: RELIABILITY CHARACTERISTICS**

Symbol	Parameter	Minimum Specification	Unit	Test Method
NEND <sup>(1,2)</sup>	Endurance	10,000	Cycles	JEDEC <sup>®</sup> Standard A117
TDR <sup>(1)</sup>	Data Retention	100	Years	JEDEC <sup>®</sup> Standard A103
ILTH <sup>(1)</sup>	Latch Up	100 + IDD	mA	JEDEC <sup>®</sup> Standard A78

**Note 1:** This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**2:** NEND endurance rating is qualified as 10,000 cycles minimum for the whole device. A sector or block level rating would result in a higher minimum specification.

# SST39LF010/020/040/SST39VF010/020/040

## 7.0 AC CHARACTERISTICS

**TABLE 7-1: READ CYCLE TIMING PARAMETERS (V<sub>DD</sub> = 3.0V-3.6V FOR SST39LF010/020/040 AND 2.7V-3.6V FOR SST39VF010/020/040)<sup>(1)</sup>**

Symbol	Parameter	SST39LF010/020/040-55		SST39VF010/020/040-70		Unit
		Minimum	Maximum	Minimum	Maximum	
TRC	Read Cycle Time	55	—	70	—	ns
TCE	Chip Enable Access Time	—	55	—	70	ns
TAA	Address Access Time	—	55	—	70	ns
TOE	Output Enable Access Time	—	30	—	35	ns
TCLZ <sup>(1)</sup>	CE# Low to Active Output	0	—	0	—	ns
TOLZ <sup>(1)</sup>	OE# Low to Active Output	0	—	0	—	ns
TCHZ <sup>(1)</sup>	CE# High to High-Z Output	—	15	—	25	ns
TOHZ <sup>(1)</sup>	OE# High to High-Z Output	—	15	—	25	ns
ToH <sup>(1)</sup>	Output Hold from Address Change	0	—	0	—	ns

**Note 1:** This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

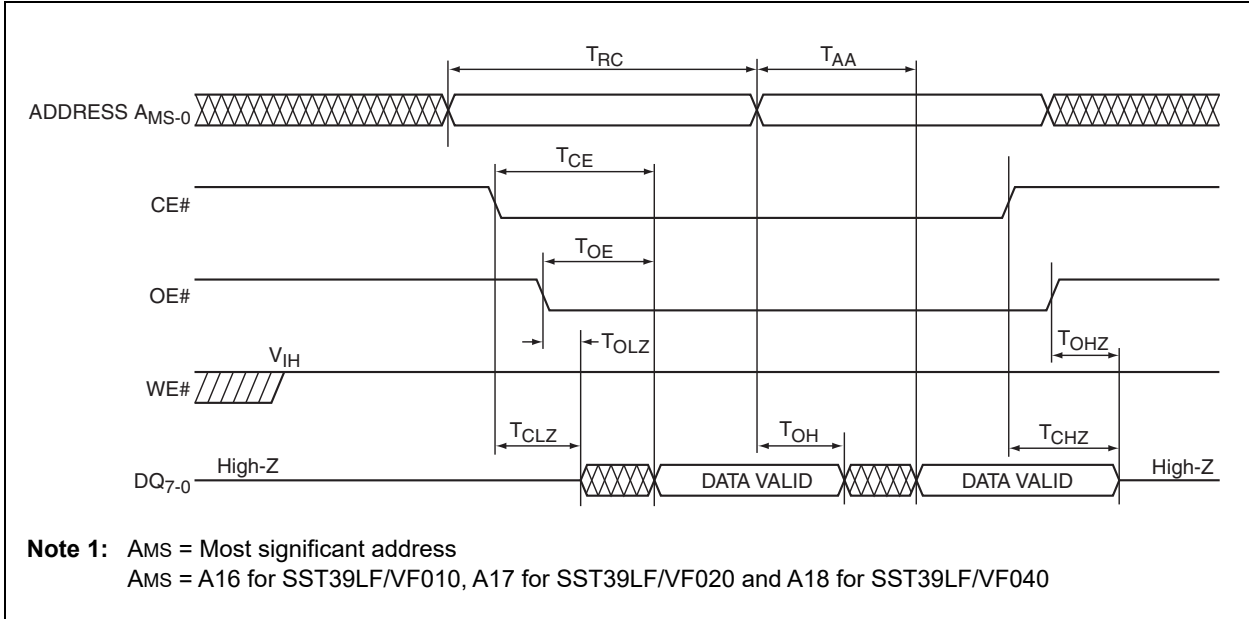
**TABLE 7-2: PROGRAM/ERASE CYCLE TIMING PARAMETERS**

Symbol	Parameter	Minimum	Maximum	Unit
TBP	Byte Program Time	—	20	μs
TAS	Address Setup Time	0	—	ns
TAH	Address Hold Time	30	—	ns
TCS	WE# and CE# Setup Time	0	—	ns
TCH	WE# and CE# Hold Time	0	—	ns
TOES	OE# High Setup Time	0	—	ns
TOEH	OE# High Hold Time	10	—	ns
TCP	CE# Pulse Width	40	—	ns
TWP	WE# Pulse Width	40	—	ns
TWPH <sup>(1)</sup>	WE# Pulse Width High	30	—	ns
TCPH <sup>(1)</sup>	CE# Pulse Width High	30	—	ns
TDS	Data Setup Time	40	—	ns
TDH <sup>(1)</sup>	Data Hold Time	0	—	ns
TIDA <sup>(1)</sup>	Software ID Access and Exit Time	—	150	ns
TSE	Sector Erase	—	25	ms
TSCE	Chip Erase	—	100	ms

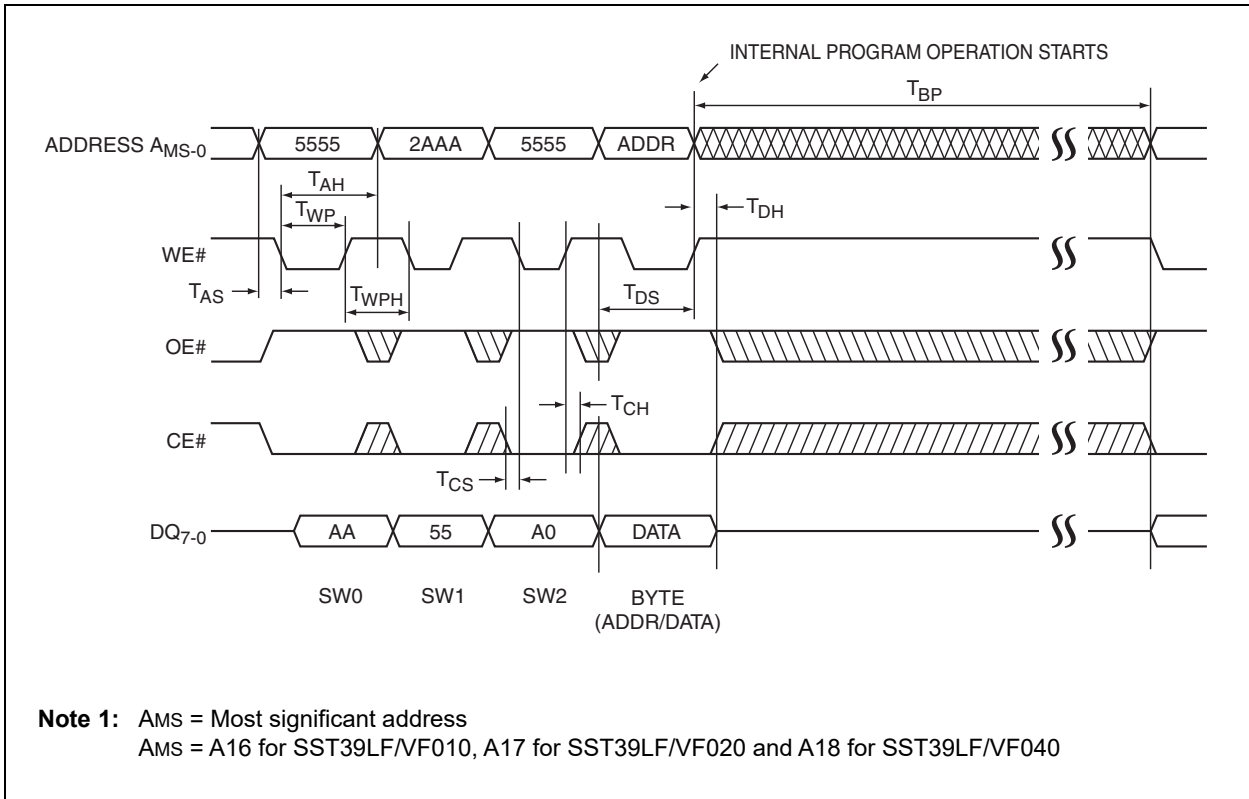
**Note 1:** This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

# SST39LF010/020/040/SST39VF010/020/040

**FIGURE 7-1: READ CYCLE TIMING DIAGRAM**

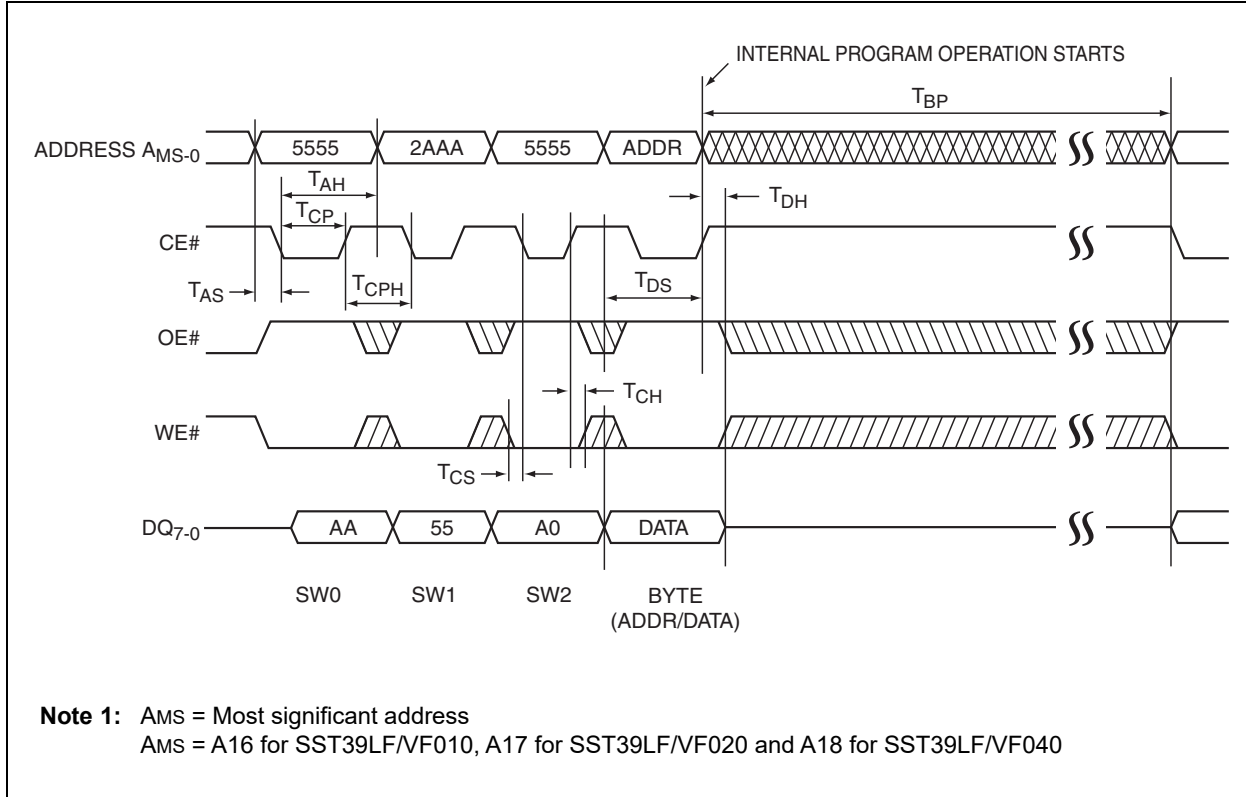


**FIGURE 7-2: WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM**

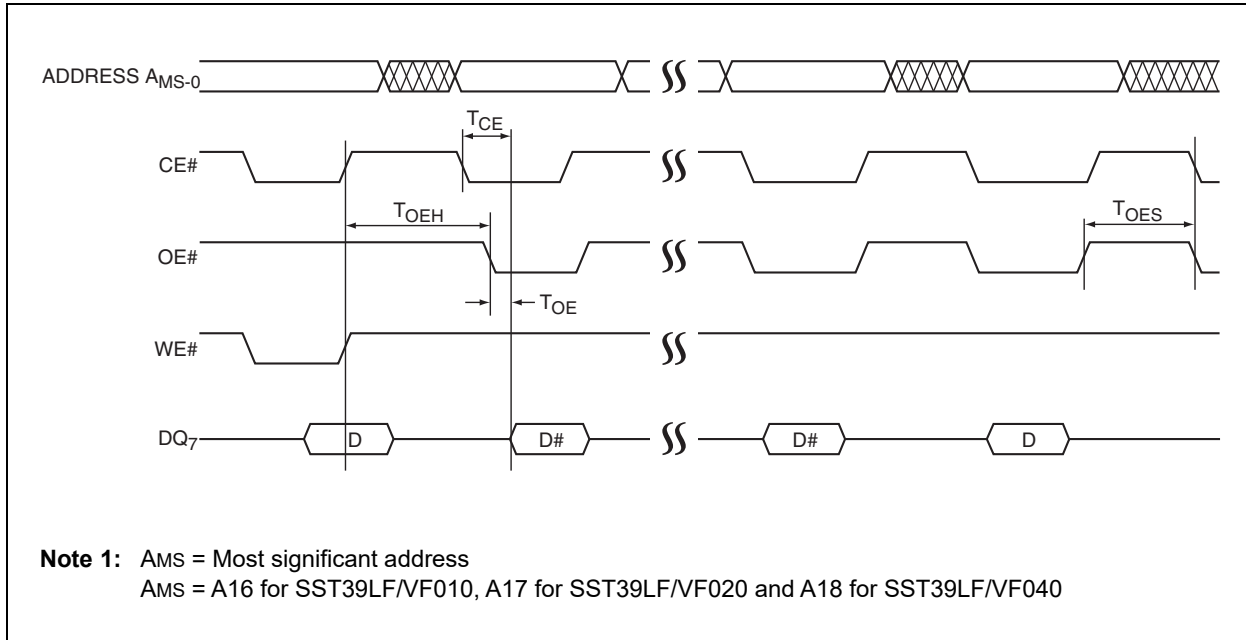


# SST39LF010/020/040/SST39VF010/020/040

**FIGURE 7-3: CE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM**

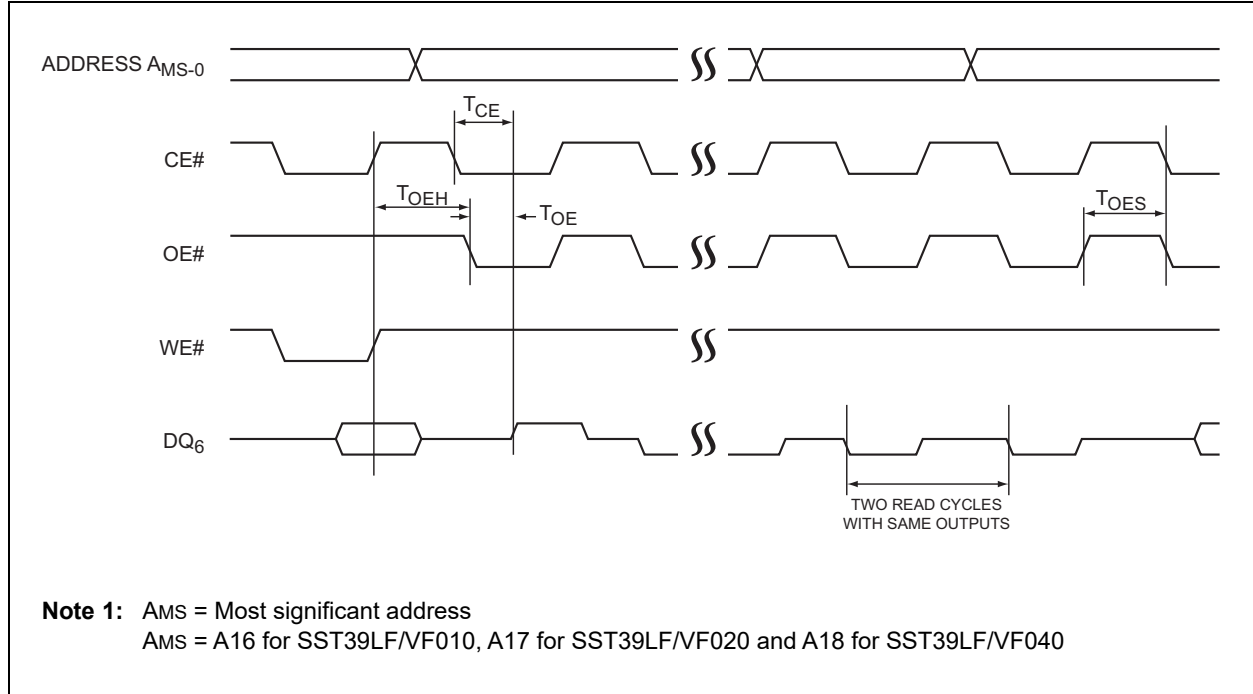


**FIGURE 7-4: DATA# POLLING TIMING DIAGRAM**

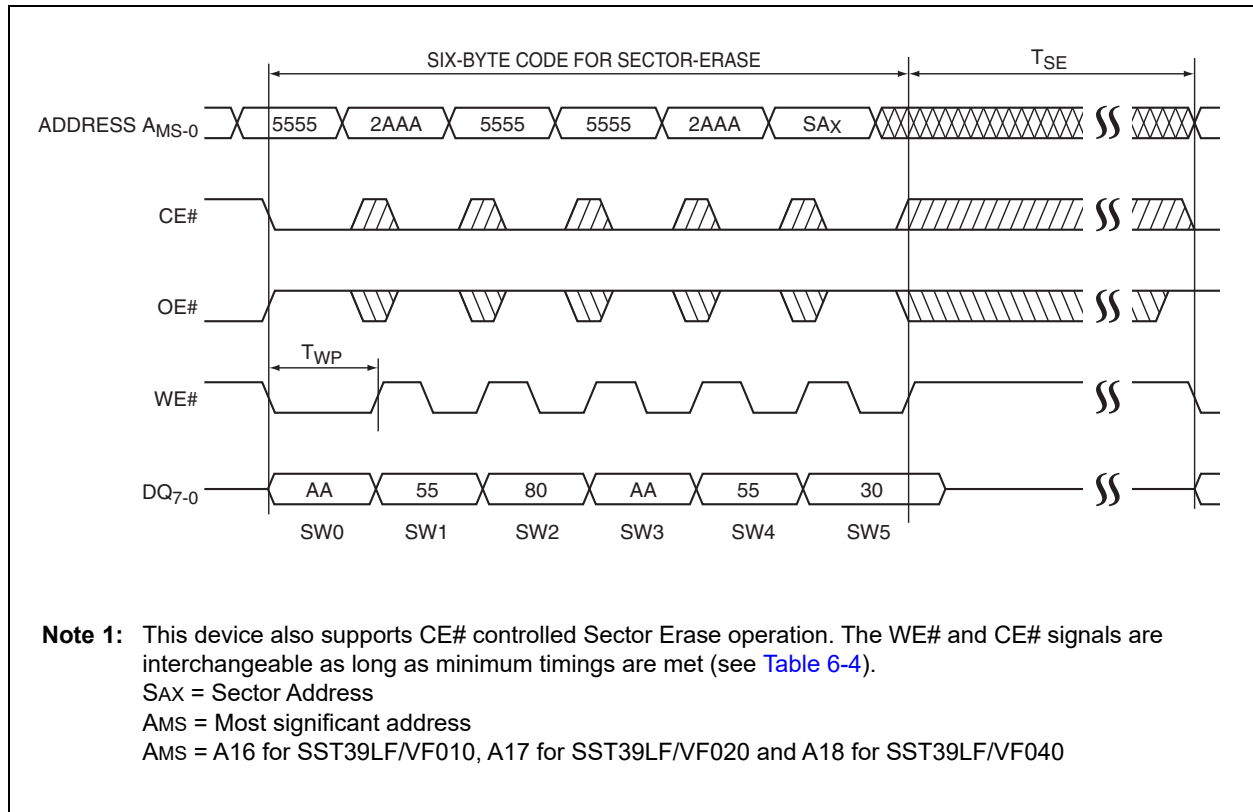


# SST39LF010/020/040/SST39VF010/020/040

**FIGURE 7-5: TOGGLE BIT TIMING DIAGRAM**

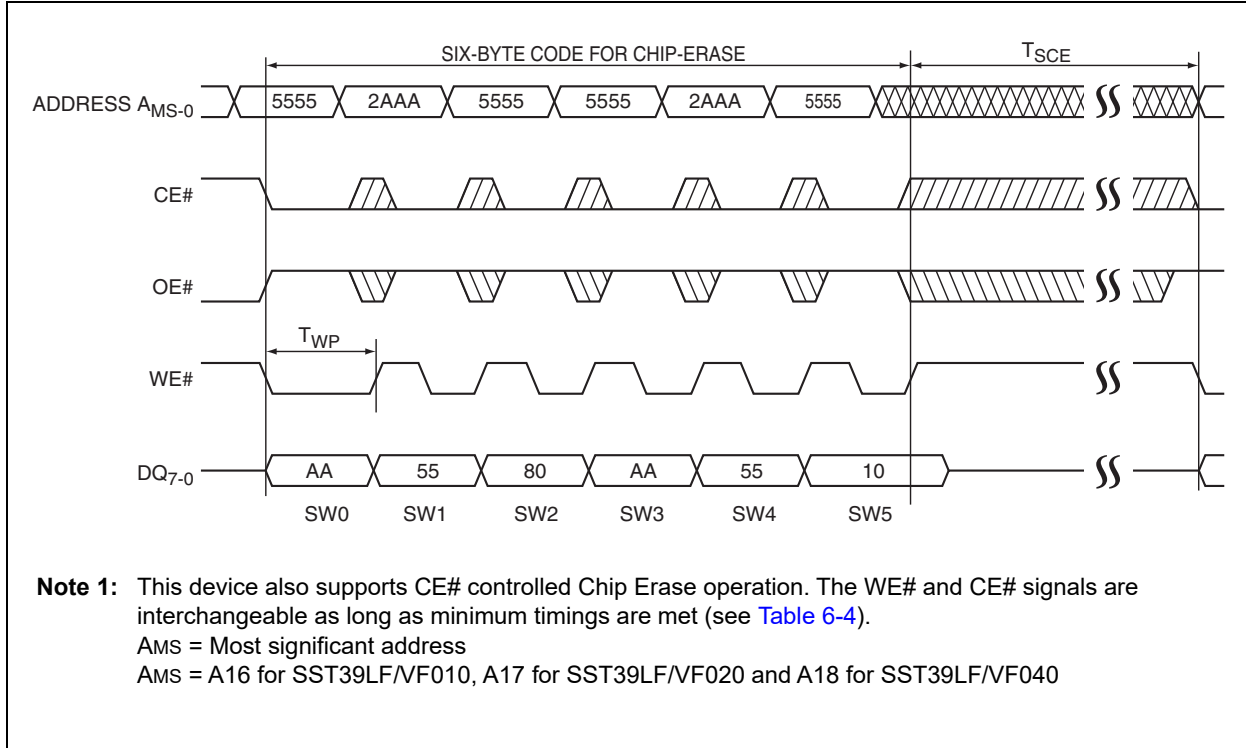


**FIGURE 7-6: WE# CONTROLLED SECTOR ERASE TIMING DIAGRAM**

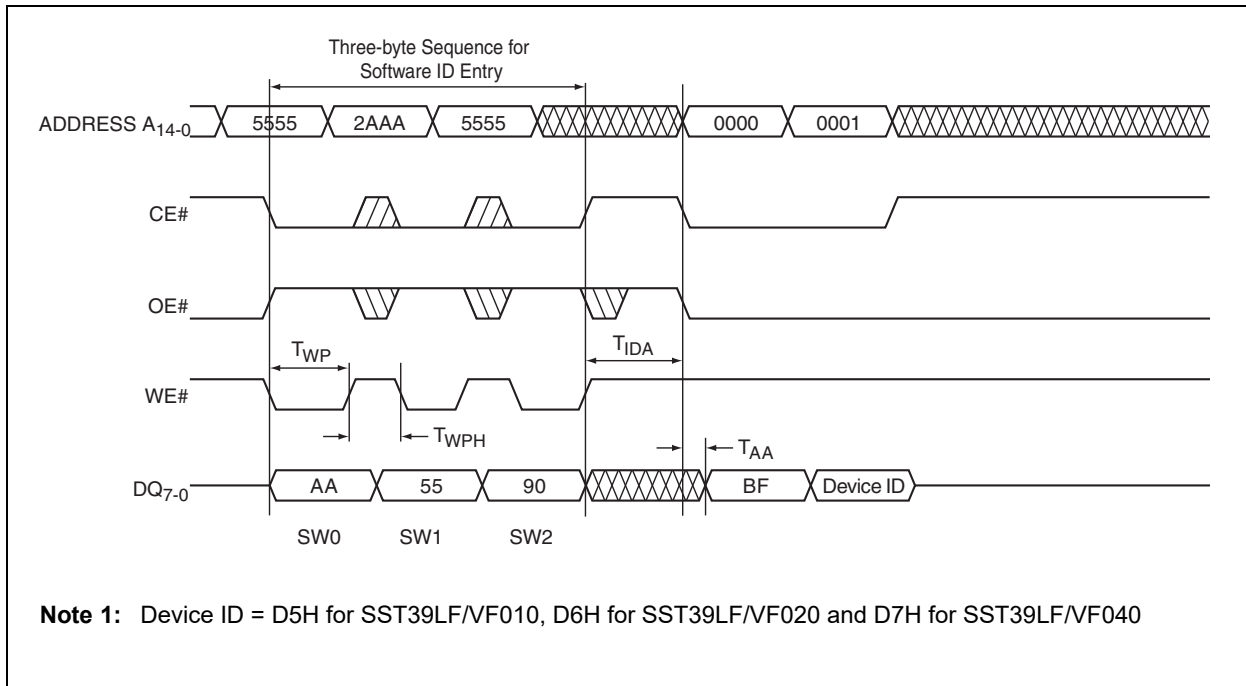


# SST39LF010/020/040/SST39VF010/020/040

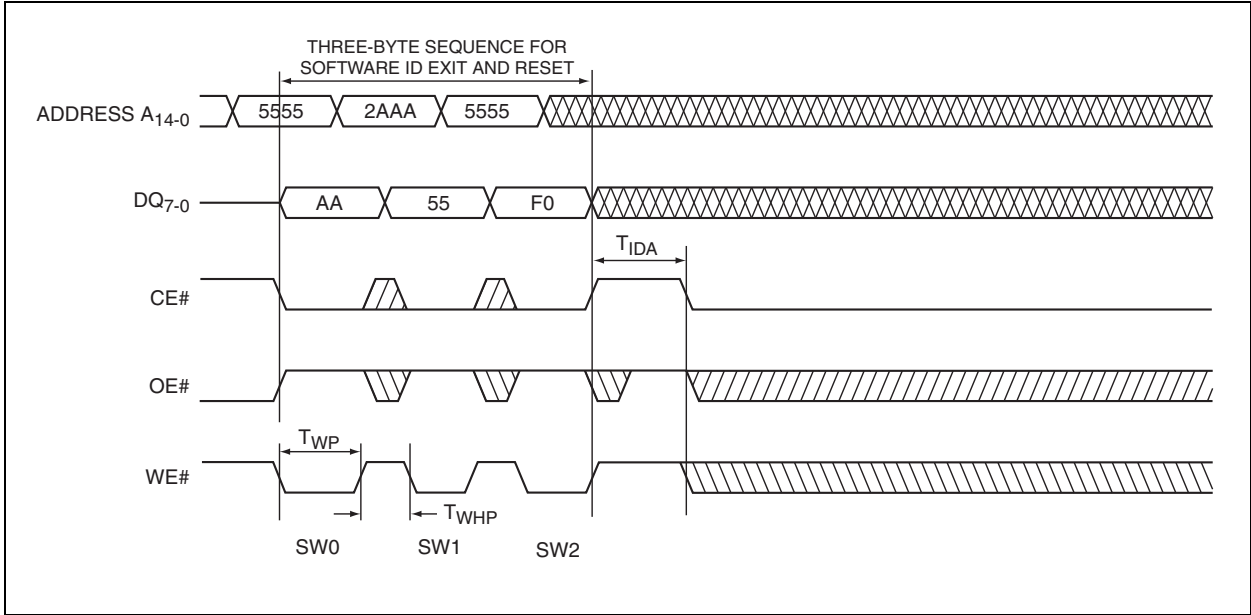
**FIGURE 7-7: WE# CONTROLLED CHIP ERASE TIMING DIAGRAM**



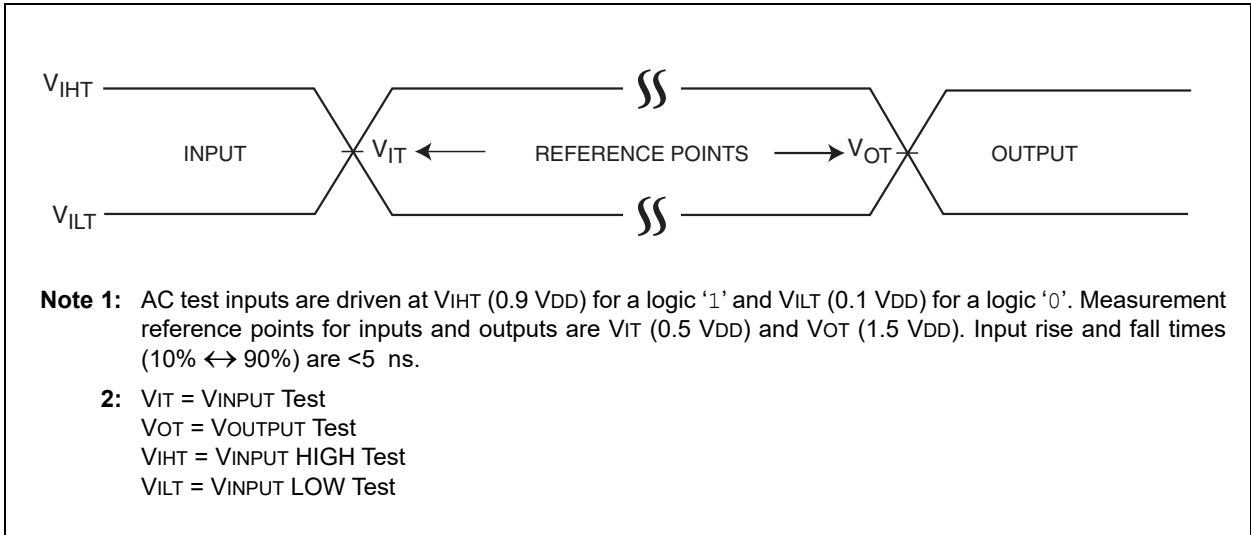
**FIGURE 7-8: SOFTWARE ID ENTRY AND READ**



**FIGURE 7-9: SOFTWARE ID EXIT AND RESET**



**FIGURE 7-10: AC INPUT/OUTPUT REFERENCE WAVEFORMS**



**FIGURE 7-11: A TEST LOAD EXAMPLE**

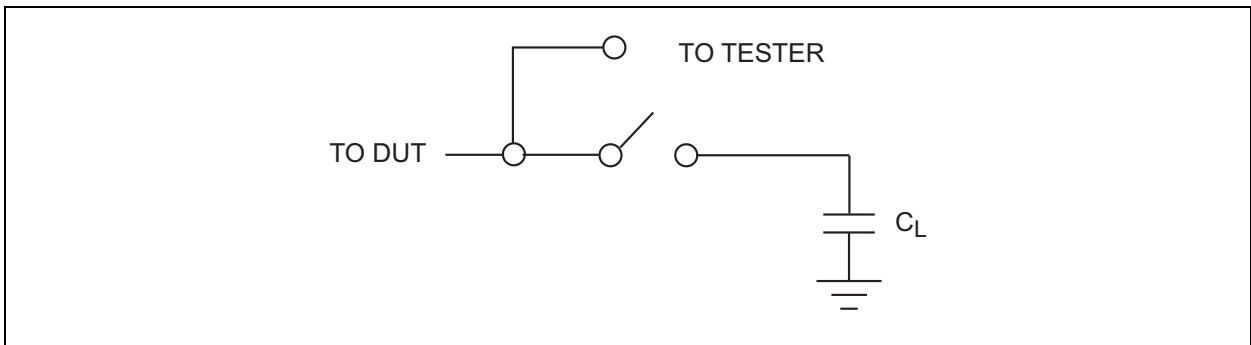


FIGURE 7-12: BYTE PROGRAM ALGORITHM

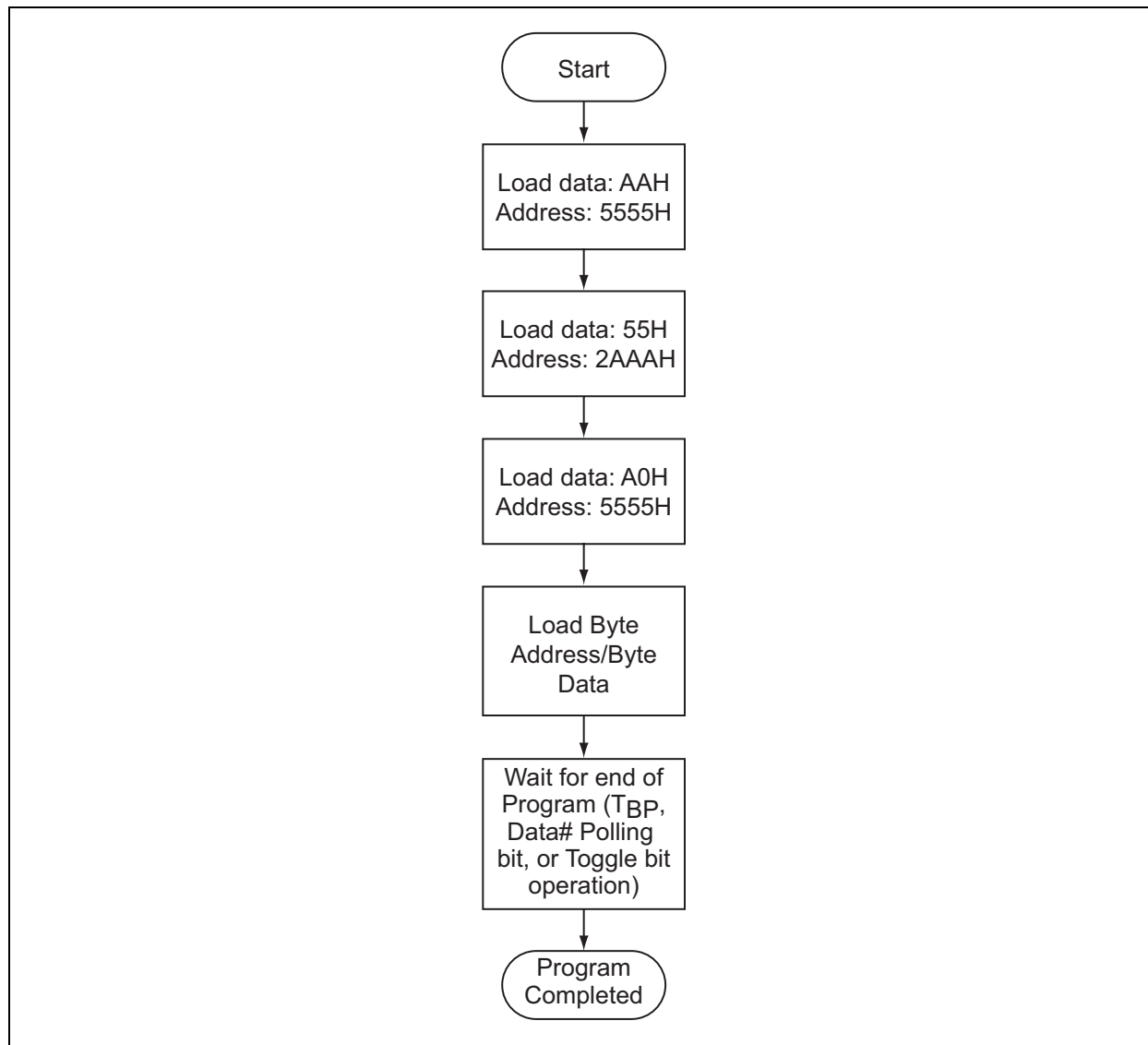




FIGURE 7-13: WAIT OPTIONS

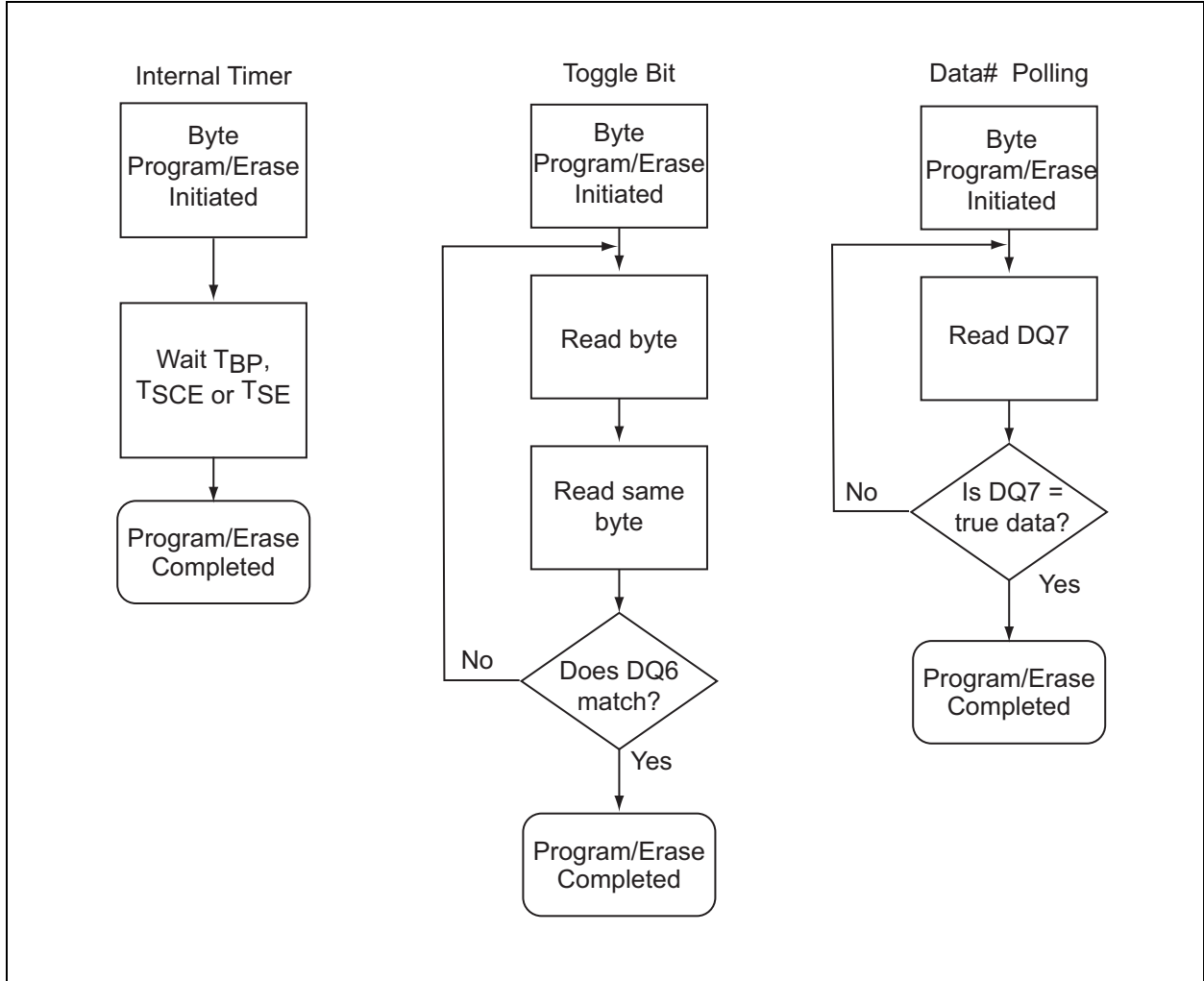


FIGURE 7-14: SOFTWARE ID COMMAND FLOWCHARTS

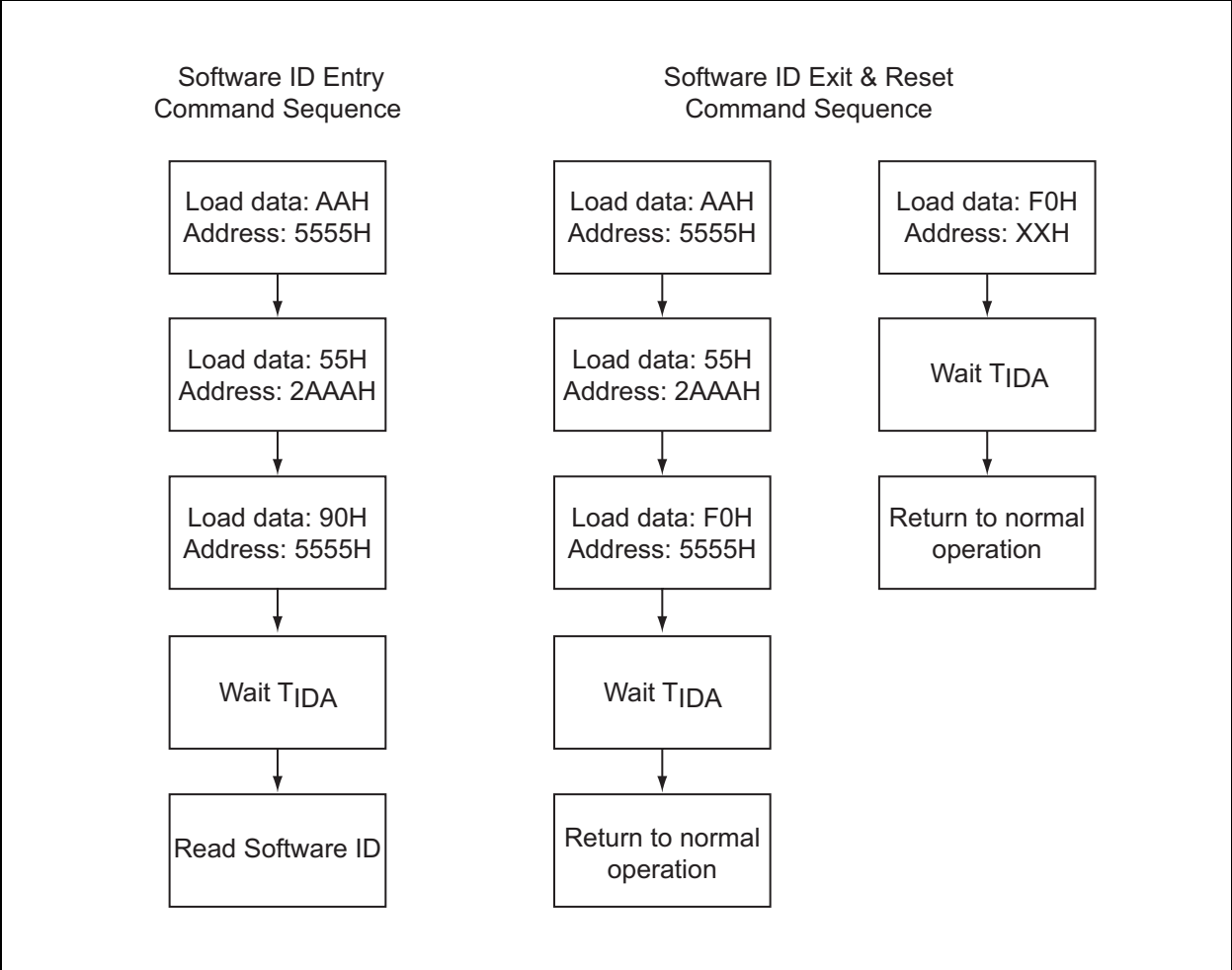
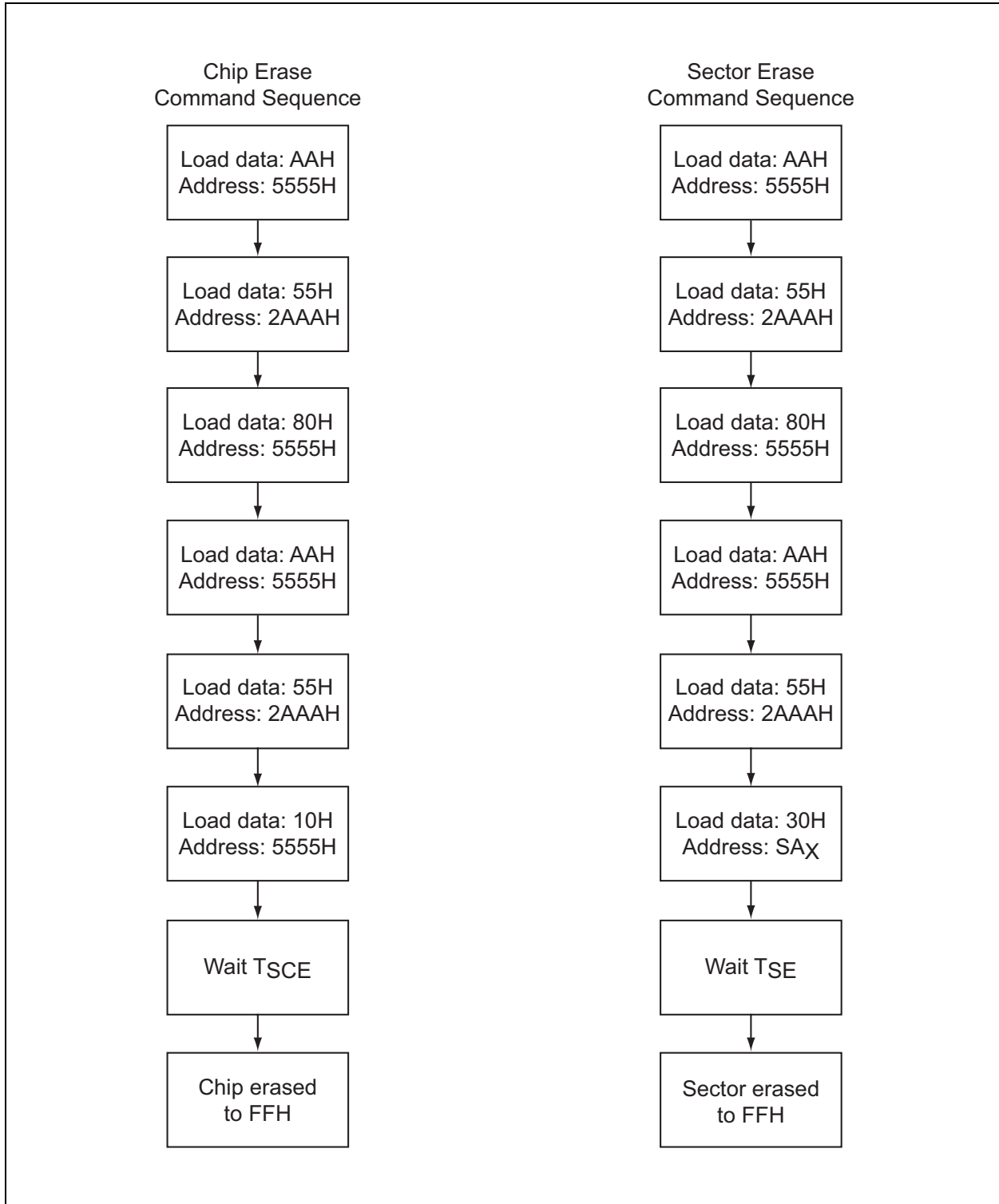


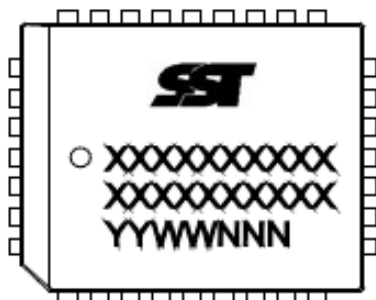
FIGURE 7-15: ERASE COMMAND SEQUENCE



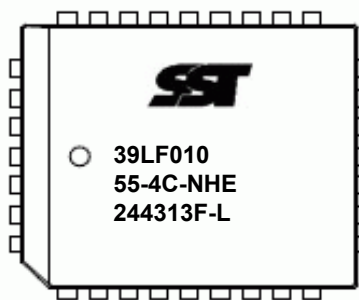
## 8.0 PACKAGING INFORMATION

### 8.1 Package Marking

32-Lead PLCC



Example



32-Lead TSOP



Example



<b>Legend:</b>	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

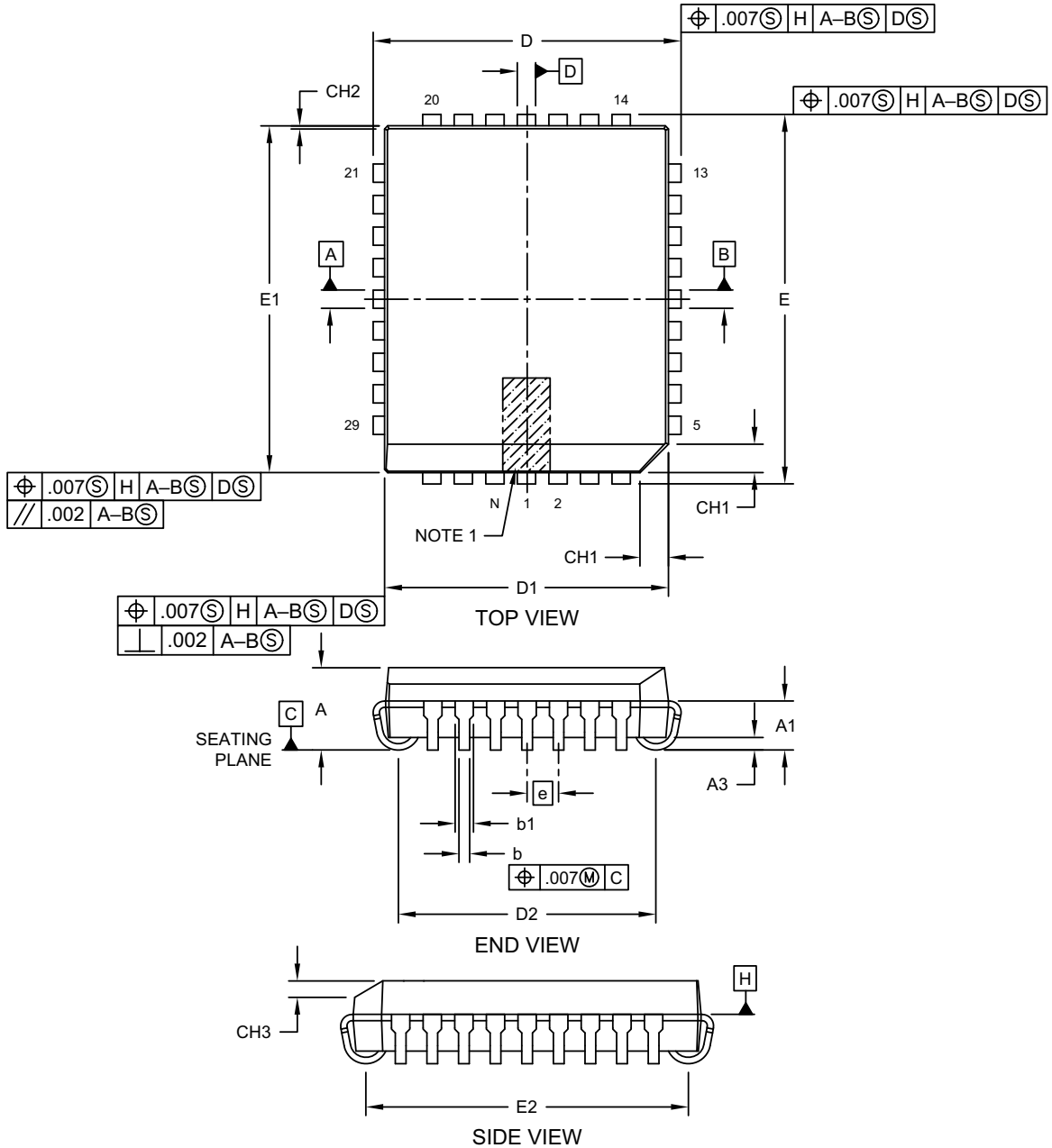
**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

# SST39LF010/020/040/SST39VF010/020/040

## 9.0 PACKAGING DIAGRAMS

### 32-Lead Plastic Leaded Chip Carrier (L) - Rectangle [PLCC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

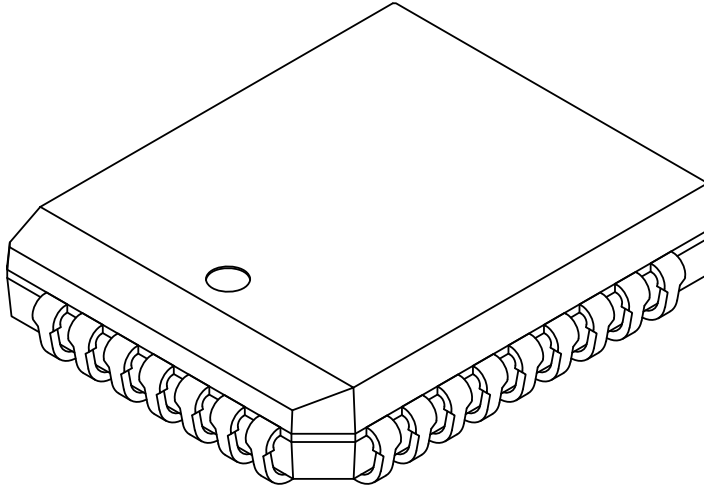


Microchip Technology Drawing C04-023 Rev C Sheet 1 of 2

# SST39LF010/020/040/SST39VF010/020/040

## 32-Lead Plastic Leaded Chip Carrier (L) - Rectangle [PLCC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	32		
Pitch	e	.050 BSC		
Pins along Length	ND	7		
Pins along Width	NE	9		
Overall Height	A	.125	.132	.140
Contact Height	A1	.060	.0775	.095
Standoff §	A3	.015	-	-
Corner Chamfer	CH1	.042	.045	.048
Chamfers	CH2	-	-	.020
Side Chamfer Height	CH3	.023	.026	.029
Overall Length	D	.485	.490	.495
Overall Width	E	.585	.590	.595
Molded Package Length	D1	.447	.450	.453
Molded Package Width	E1	.547	.550	.553
Footprint Length	D2	.376	.411	.446
Footprint Width	E2	.476	.511	.546
Lead Thickness	c	.008	.010	.013
Upper Lead Width	b1	.026	.029	.032
Lower Lead Width	b	.013	.017	.021

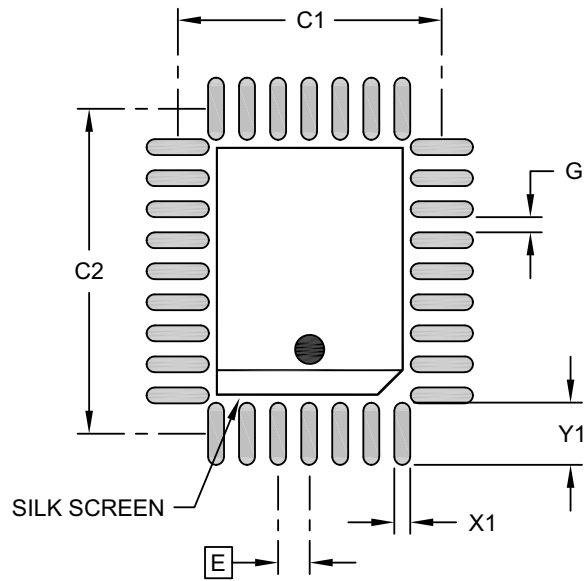
**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-023 Rev C Sheet 2 of 2

## 32-Lead Plastic Leaded Chip Carrier (L) - Rectangle [PLCC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Units		INCHES		
		MIN	NOM	MAX
Dimension Limits				
Contact Pitch	E	.050 BSC		
Contact Pad Spacing	C1		.425	
Contact Pad Spacing	C2		.524	
Contact Pad Width (X32)	X1			.026
Contact Pad Length (X32)	Y1			.100
Contact Pad to Center Pad (X28)	G	.008		

**Notes:**

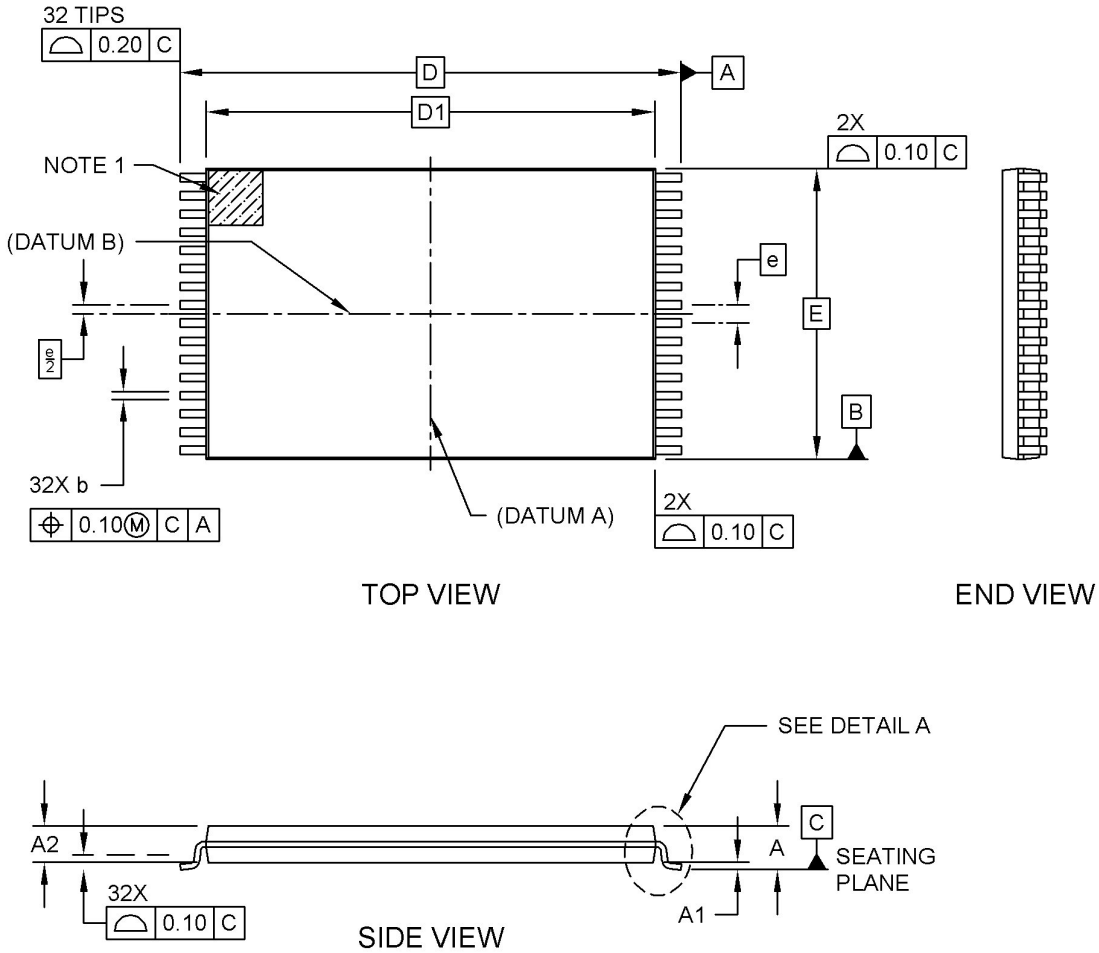
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2023 Rev C

# SST39LF010/020/040/SST39VF010/020/040

## 32-Lead Plastic Thin Small Outline Package (6JW) - 8x13.4 mm Body [TSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



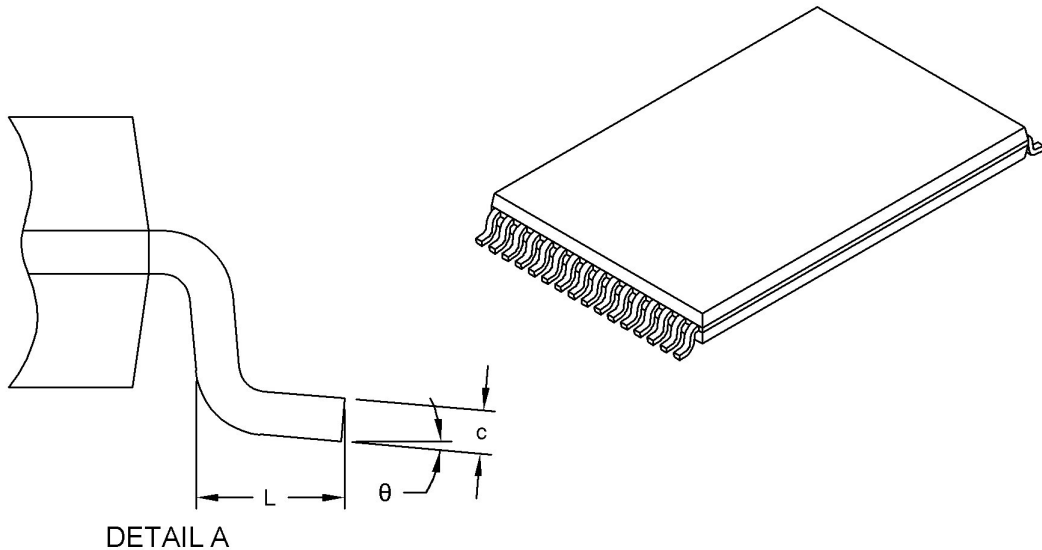
Microchip Technology Drawing C04-628 Rev A Sheet 1 of 2



# SST39LF010/020/040/SST39VF010/020/040

## 32-Lead Plastic Thin Small Outline Package (6JW) - 8x13.4 mm Body [TSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	32		
Pitch	e	0.50 BSC		
Overall Height	A	-	-	1.20
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Length	D	13.40 BSC		
Molded Package Length	D1	11.80 BSC		
Overall Width	E	8.00 BSC		
Terminal Thickness	c	-	-	0.21
Terminal Width	b	0.17	-	0.23
Terminal Length	L	0.30	-	0.70
Foot Angle	θ	0°	-	5°

**Notes:**

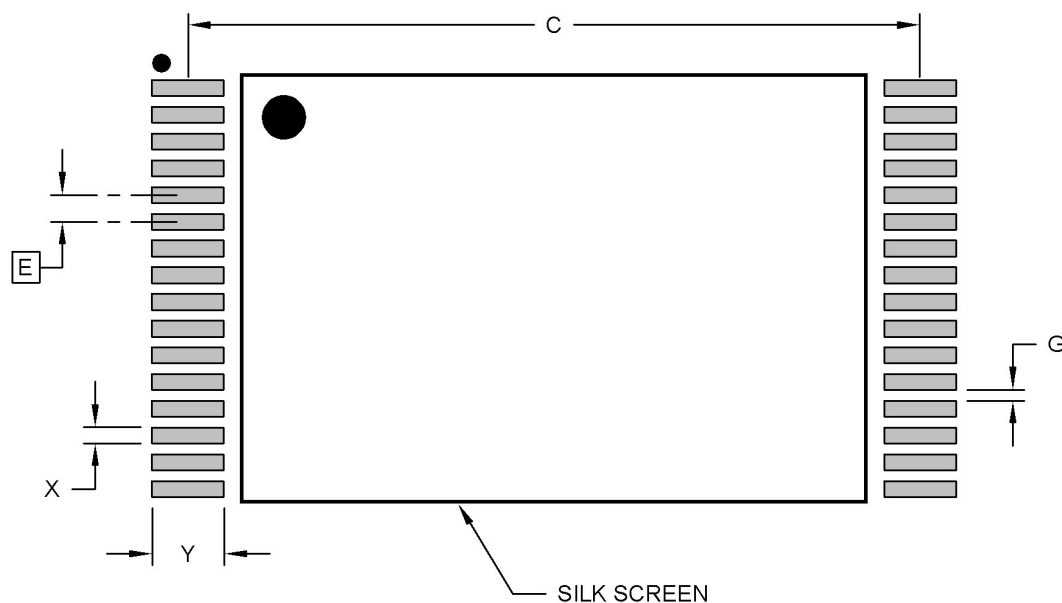
- Pin 1 visual index feature may vary but must be located within the hatched area.
- Dimensions D1 and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-628 Rev A Sheet 2 of 2

# SST39LF010/020/040/SST39VF010/020/040

## 32-Lead Plastic Thin Small Outline Package (6JW) - 8x13.4 mm Body [TSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C		12.90	
Contact Pad Width (X32)	X			0.30
Contact Pad Length (X32)	Y			1.30
Contact Pad to Contact Pad (X30)	G1	0.20		

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2628 Rev A

## APPENDIX A: REVISION HISTORY

### Revision D (November 2024)

Updated Package Marking section.

### Revision C (September 2024)

Replaced WHE package type with TU package type.

### Revision B (June 2013)

EOL of 45 ns parts. Removed all 45 ns parts; Updated Table 12 on page 13 to reflect this change; EOL of B3KE; Removed the B3KE package; EOL of MME; Removed the MME package; Added 55 ns for SST39LF010 and SST39VF010 parts.

### Revision A (August 2011)

EOL of SST39LF512 and SST39VF512 parts; Replacement parts are SST39LF010 and SST39VF010; Applied new document format; Released document under letter revision system; Updated spec number S71150 to DS25023.

### Revision 14 (January 2010)

EOL of SST39LF010-45-4C-YME; Replacement part is SST39LF010-45-4C-MME in this document; Removed all references to the YME package.

### Revision 13 (September 2009)

Changed endurance from 10,000 to 100,000 in Product Description, page 1.

### Revision 12 (April 2009)

Revised "Product Ordering Information" on page 23.

### Revision 11 (February 2009)

Added package YME.

### Revision 10 (November 2008)

Removed leaded parts.

### Revision 09 (January 2006)

Edited page Valid Combinations on page 21; Changed 39LF040-70-4CB3KE to 39LF040-45-4C-B3KE.

### Revision 08 (December 2005)

Added RoHS Compliant statement; Added 4 MBit to Figure 4; Revised Absolute Max Stress Ratings for Surface Mount Solder Reflow Temperature; Removed SST39VFxxx-90 Timing Parameters from Figure 12;

Added Footnote and removed Read Access Speed 90 = 90 to Product Ordering Information; Removed 90 part numbers Valid Combinations lists.

### Revision 07 (November 2003)

2004 Data Book; Added non-Pb MPNs and removed footnote (See page 23); Updated B3K and MM package diagrams.

### Revision 06 (October 2003)

Added new "MM" Micro-Package MPNs for 1M and 2M LF parts - see page 23.

### Revision 05 (March 2003)

Changes to Table 8 on page 12; Added footnote for MPF power usage and Typical conditions; Clarified the Test Conditions for Power Supply Current and Read parameters; Clarified IDD Write to be Program and Erase; Corrected IDD Program and Erase from 20 mA to 30 mA; Part number changes - see page 23 for additional information.

### Revision 04 (October 2002)

Added the B3K package for the 2-Mbit devices; Added footnote in Table 8 to indicate IDD Write is 30 mA max for Erase operations in the Industrial temperature range.

### Revision 03 (February 2002)

2002 Data Book: Reintroduced the 45 ns parts for the SST39LF020 and SST39LF040.

### Revision 02 (August 2000)

Changed speed from 45 ns to 55 ns for the SST39LF020 and SST39LF040.

### Revision 01 (February 2000)

2000 Data Book.

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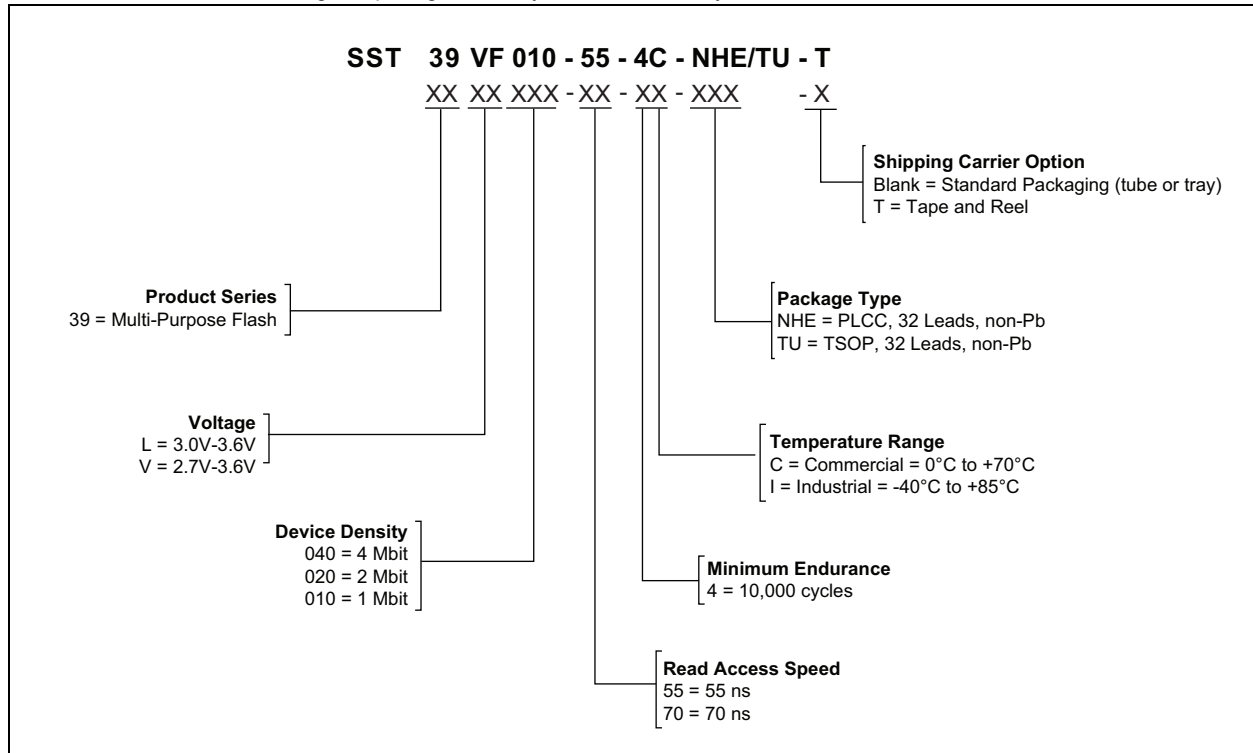
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# SST39LF010/020/040/SST39VF010/020/040

## PRODUCT IDENTIFICATION SYSTEM

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Valid Combinations for SST39LF010 <sup>(1,2)</sup>	
SST39LF010-55-4C-NHE	SST39LF010-55-4C-TU
Valid Combinations for SST39VF010 <sup>(1,2)</sup>	
SST39VF010-70-4C-NHE	SST39VF010-70-4C-TU
SST39VF010-70-4I-NHE	SST39VF010-70-4I-TU
Valid Combinations for SST39LF020 <sup>(1,2)</sup>	
SST39LF020-55-4C-NHE	SST39LF020-55-4C-TU
Valid Combinations for SST39VF020 <sup>(1,2)</sup>	
SST39VF020-70-4C-NHE	SST39VF020-70-4C-TU
SST39VF020-70-4I-NHE	SST39VF020-70-4I-TU
Valid Combinations for SST39LF040 <sup>(1,2)</sup>	
SST39LF040-55-4C-NHE	SST39LF040-55-4C-TU
Valid Combinations for SST39VF040 <sup>(1,2)</sup>	
SST39VF040-70-4C-NHE	SST39VF040-70-4C-TU
SST39VF040-70-4I-NHE	SST39VF040-70-4I-TU

**Note 1:** Valid combinations are those products in mass production or will be in mass production. Consult Microchip sales representative to confirm availability of valid combinations and to determine availability of new combinations.

**2:** For Tape and Reel options add "-T" to part number suffix.

# SST39LF010/020/040/SST39VF010/020/040

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