# MMA041PP5

## DC – 25 GHz GaAs MMIC Distributed LNA

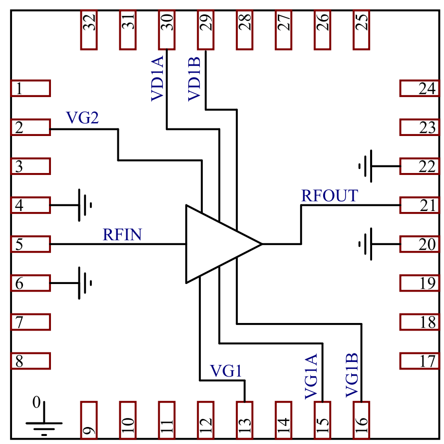
## Product Overview

MMA041PP5 is a gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) pseudomorphic high-electron-mobility transistor (pHEMT) distributed low noise amplifier in a leadless 5 mm × 5 mm surface-mount package that operates between DC and 25 GHz. It is ideal for test instrumentation, wideband military and space applications. The amplifier provides a flat gain of 17 dB, 2.5 dB noise figure, and 21 dBm of output power at 1 dBm gain compression while requiring only 150 mA from a 7 V supply. Output IP3 is typically 35 dBm. The MMA041PP5 amplifier features RF I/Os that are internally matched to 50 Ω. It is also available in die form as the MMA041AA.

### *Key Features*

- Broadband performance: DC to 26 GHz
- High gain: 18.5 dB
- Low noise figure: 3.2 dB
- High output IP3: + 36 dBm
- Positive supply : + 7V @ 150 mA
- 50Ω matched I/O
- Compact die size: 3 mm × 1.3 mm × 0.1 mm

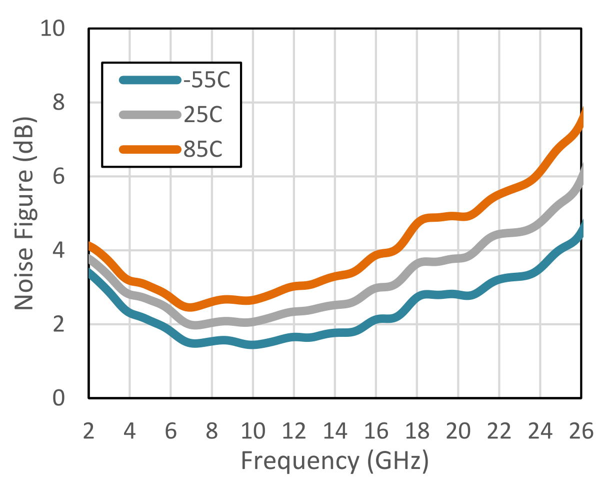
### *Amplifier Functional Diagram*




### *Applications*

- Test and measurement instrumentation
- Military and space
- Wideband microwave radios
- Microwave and mm-Wave communication systems

### *NF Performances*




### *Performance Overview*

| Parameter | Typ. | Units |
|---|---|---|
| Frequency range | DC – 26 | GHz |
| Gain | 18.5 | dB |
| NF | 2 | dB |
| Output IP3 | + 36 | dBm |
| P1dB | + 22 | dBm |

**Export Classification: EAR99**

# Table of Contents

# 1. Electrical Specifications

## 1.1 Typical Electrical Performance

**Table 1-1. Typical Electrical Performance at 25 °C, $V_{DD}$ = + 7V/150 mA and $V_{GG}$ = – 0.4V (Unless otherwise mentioned)**

| Parameter | Frequency Range | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Frequency range | | DC | | 25 | GHz |
| Gain | DC – 6 GHz | 17 | 18 | | dB |
| | 6 – 12 GHz | 16 | 17.5 | | dB |
| | 12 – 20 GHz | 15 | 17 | | dB |
| Gain flatness | 4 – 12 GHz | | ± 0.5 | | dB |
| | 12 – 20 GHz | | ± 0.5 | | dB |
| Noise Figure @ 5V / 150 mA | 2 – 6 GHz | | 2.7 | | dB |
| | 6 –12 GHz | | 2.0 | | dB |
| | 12 – 20 GHz | | 2.5 | | dB |
| OIP3 | DC – 6 GHz | | 35 | | dBm |
| | 6 – 12 GHz | | 36 | | dBm |
| | 12 – 20 GHz | | 34 | | dBm |
| P1dB | DC – 6 GHz | | 21 | | dBm |
| | 6 – 12 GHz | 21 | 22 | | dBm |
| | 12 – 20 GHz | 17 | 19 | | dBm |
| Psat | DC – 6 GHz | | 24 | | dBm |
| | 6 – 12 GHz | | 24 | | dBm |
| | 12 – 20 GHz | | 21 | | dBm |
| Input Return Loss | DC – 6 GHz | | 15 | | dB |
| | 6 – 12 GHz | | 18 | | dB |
| | 12 – 20 GHz | | 13 | | dB |
| Output Return Loss | DC – 6 GHz | | 13 | | dB |
| | 6 – 12 GHz | | 18 | | dB |
| | 12 – 20 GHz | | 16 | | dB |
| $V_{DD}$ (Drain Voltage Supply) | | | + 7 | | V |
| $I_{DD}$ (Drain Current) | | | 150 | | mA |
| $V_{GG}$ (Gate Voltage Bias) | | – 1.0 | – 0.4 | 0 | V |

## 1.2 Typical Performance Curves

The following graphs show the typical performance curves of the MMA041PP5 device at + 25 °C and + 7V/150 mA unless otherwise indicated.

**Figure 1-1. Gain vs. Temperature**

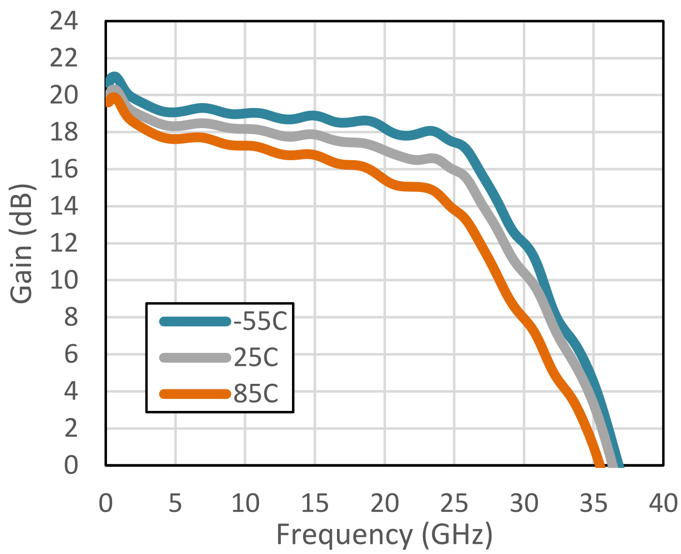



**Figure 1-2. NF vs. Temperature**

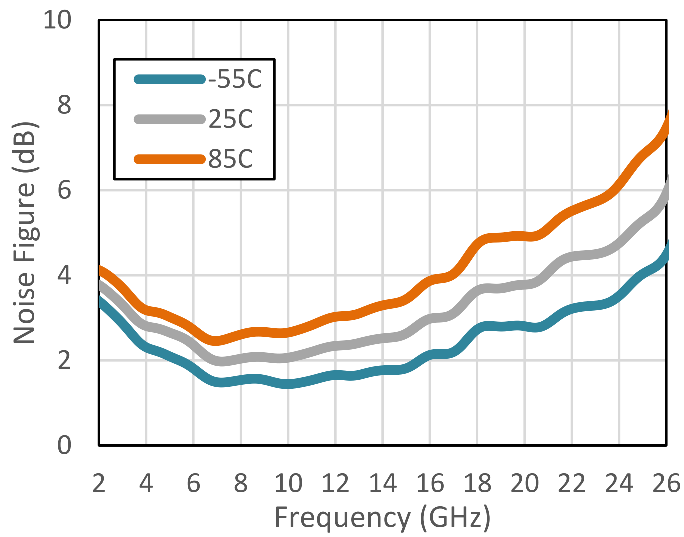



**Figure 1-3. OIP3 vs. Temperature**

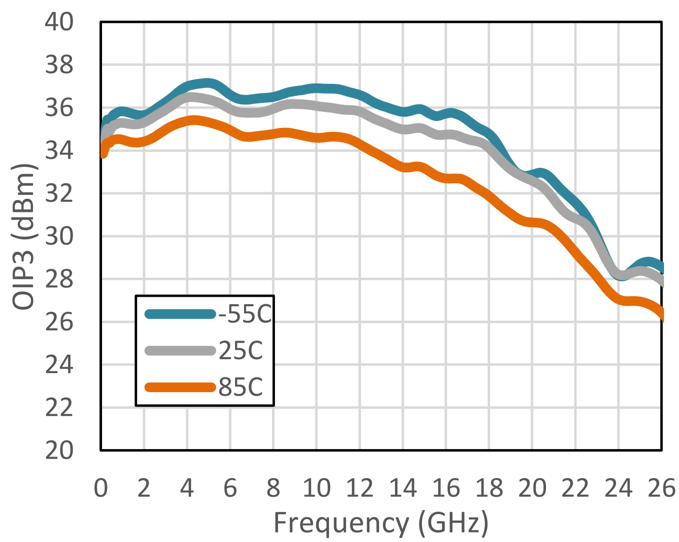



**Figure 1-4. P1dB vs. Temperature**

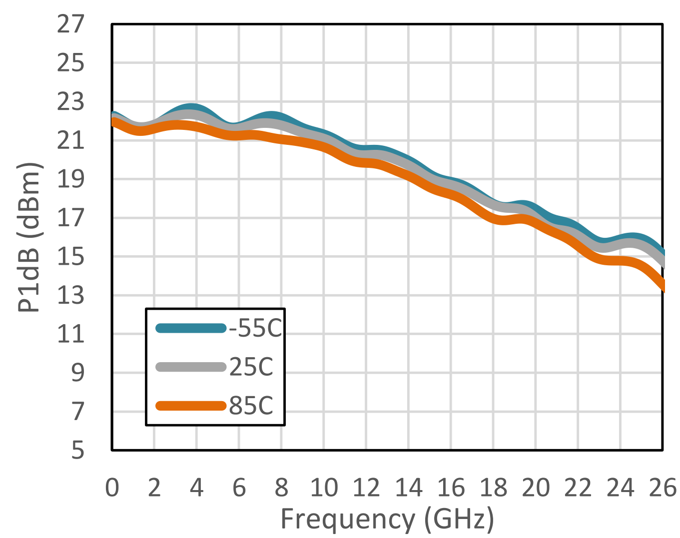


**Figure 1-5. P3dB vs. Temperature**

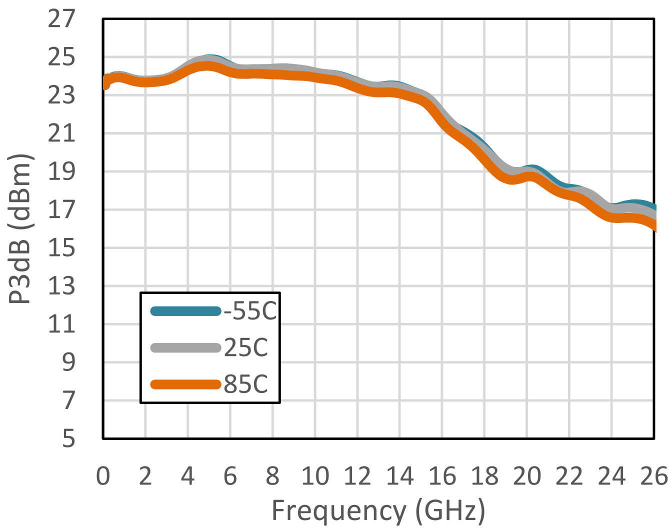



**Figure 1-6. S11 vs. Temperature**

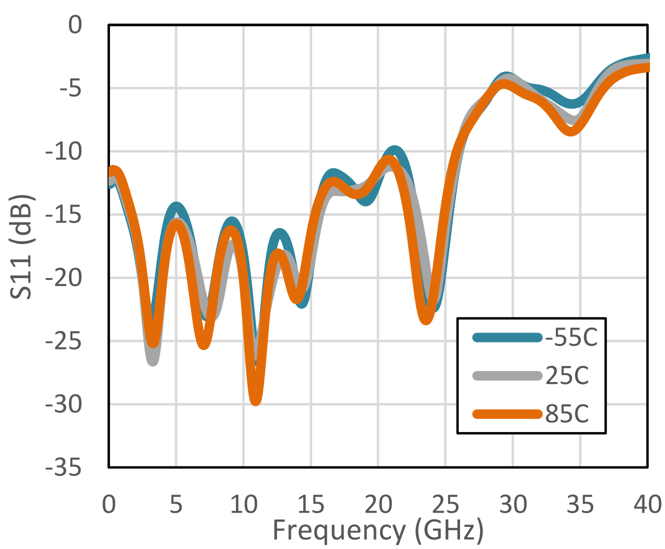



**Figure 1-7. S22 vs. Temperature**

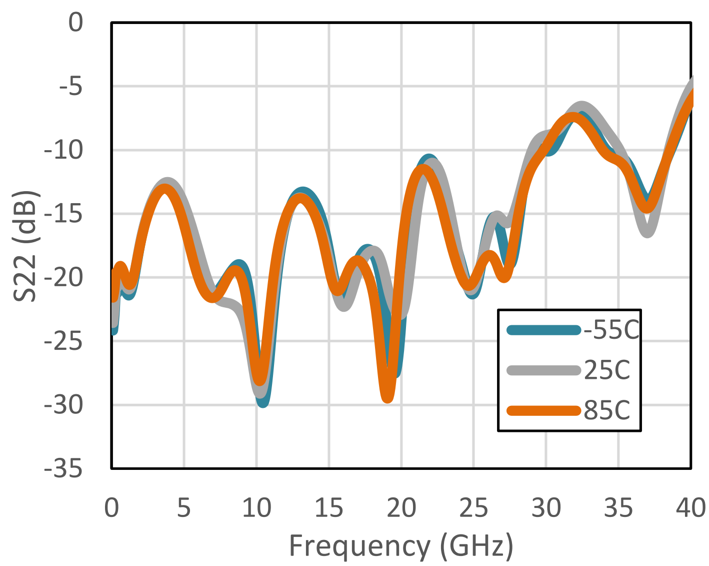


**Figure 1-8. Gain vs. VDD**

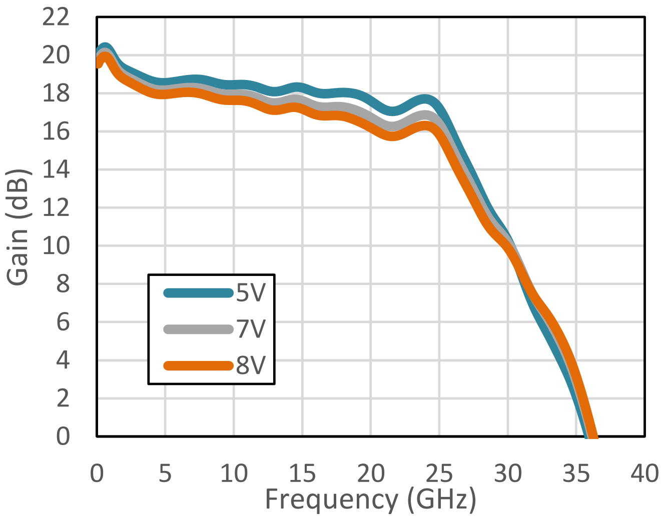



**Figure 1-9. NF. vs. VDD**

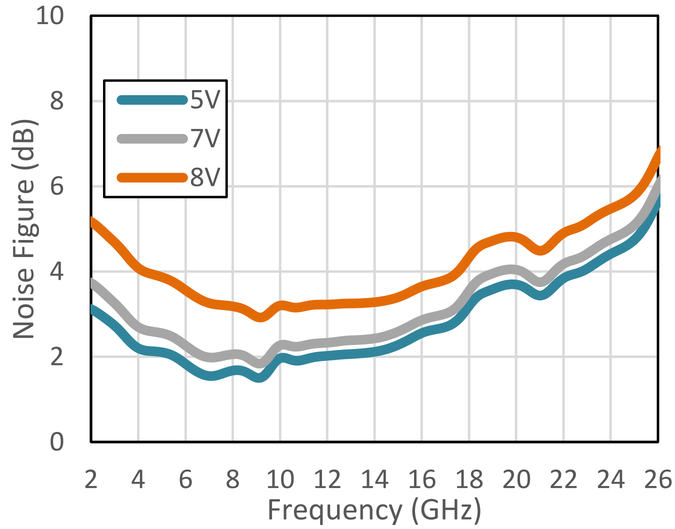



**Figure 1-10. OIP3 vs. VDD**

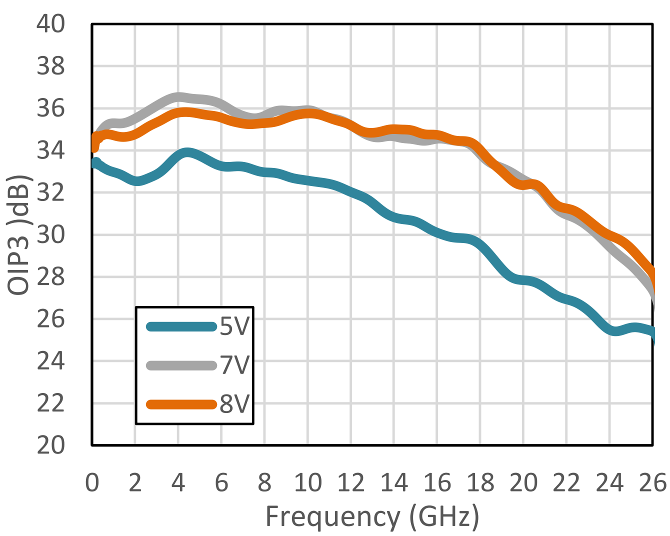



**Figure 1-11. P1dB vs. VDD**

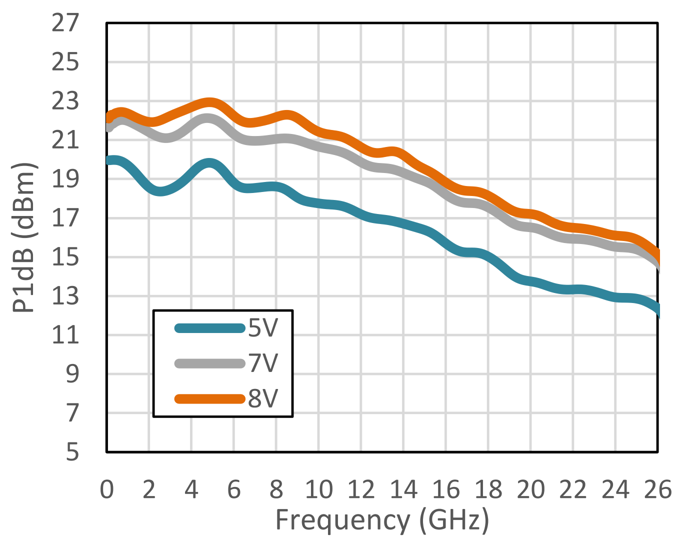


**Figure 1-12. Gain vs. IDD**

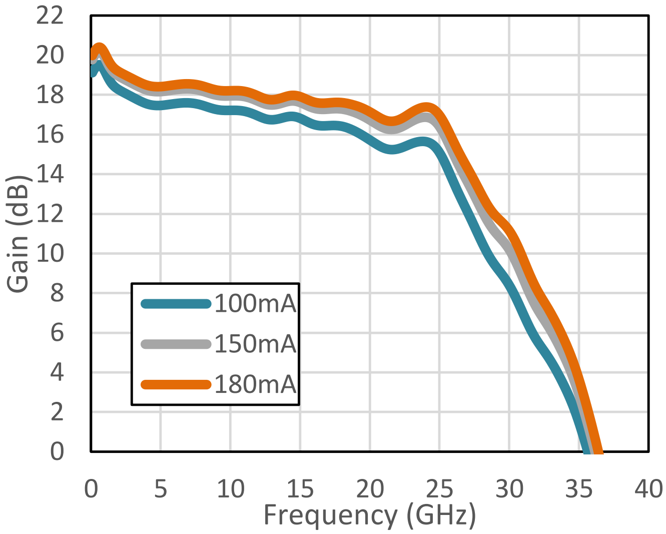



**Figure 1-13. NF vs. IDD**

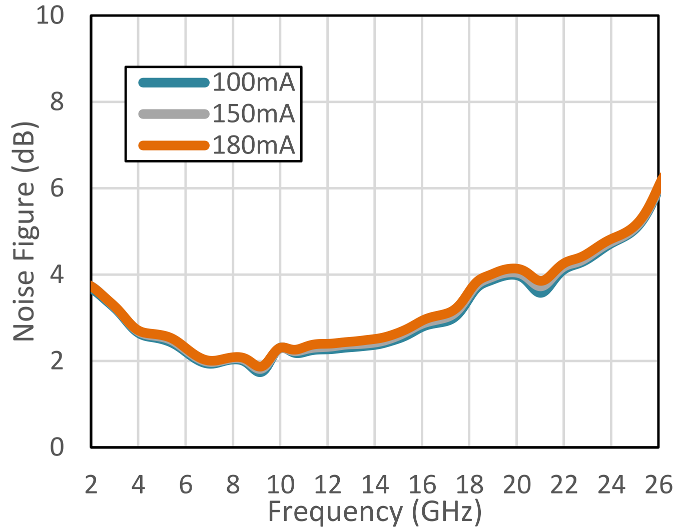
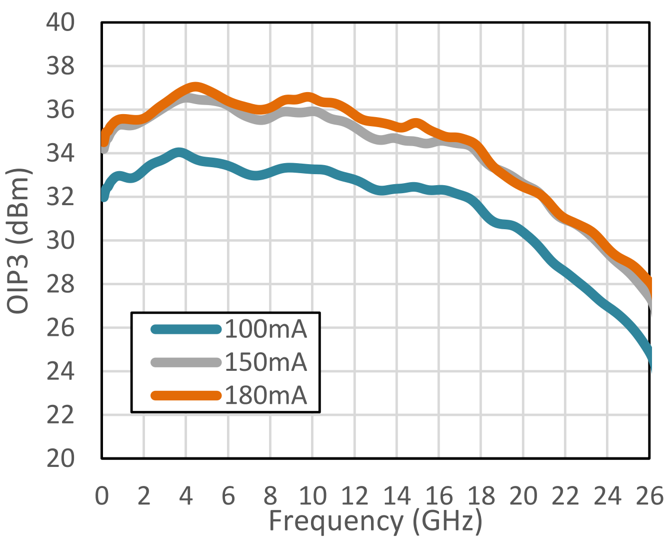



**Figure 1-14. OIP3 vs. IDD**




## 1.3 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the MMA041PP5 device at 25 °C, unless otherwise specified. Exceeding one or any of the maximum ratings potentially could cause damage or latent defects to the device.

**Table 1-2. Absolute Maximum Ratings**

| Parameter | Rating |
|---|---|
| Drain bias voltage ($V_{DD}$) | + 8V |
| $V_D$ Current ($I_{DD}$) | 300 mA |
| DC Power Dissipation (T = + 85 °C) | 2.4W |
| RF Input Power (Pin) | + 19 dBm |
| First Gate bias voltage ($V_{G1}$) | – 2V to + 0.5V |
| Second Gate bias voltage ($V_{G2}$) | $V_D$ +/– 20% |
| Channel Temperature | 150 °C |
| Thermal Resistance | 18 °C/W |
| Operating Temperature | – 55 °C to + 85 °C |
| Storage Temperature | – 65 °C to + 150 °C |


ESD Sensitive Device

# 2. Package Specifications

The following illustration shows the package outline of the MMA041PP5 device. Dimensions are in millimeters [inches].

**Figure 2-1. Package Outline Drawing (mm[Inches])**

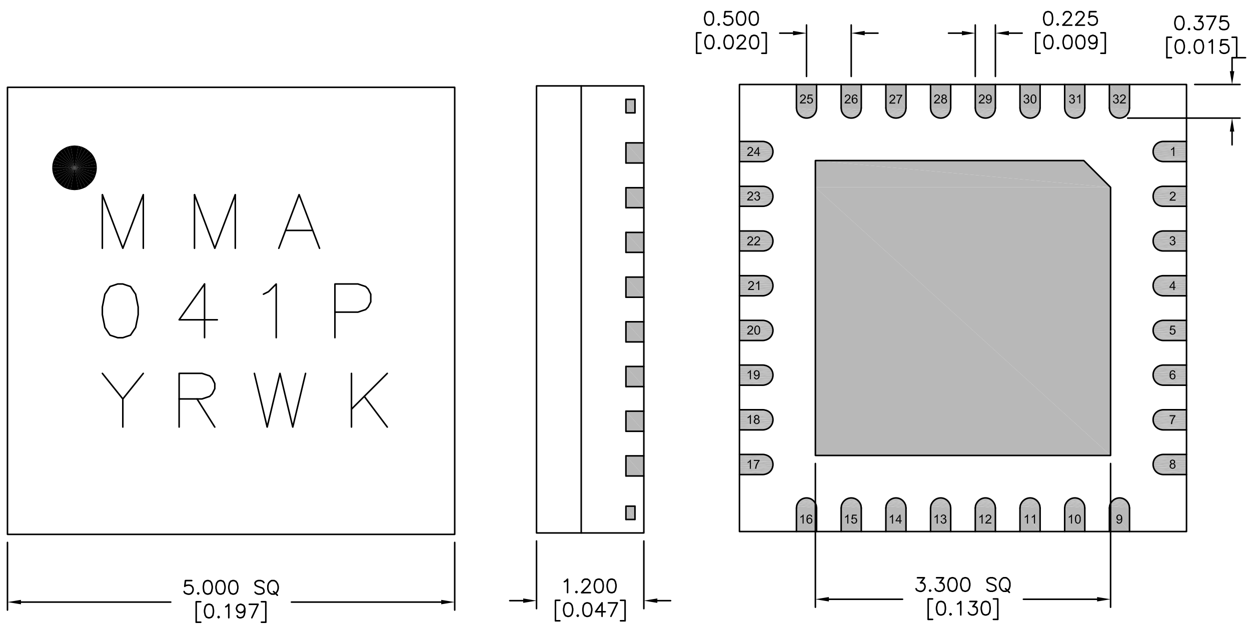



**Table 2-1. Package Information**

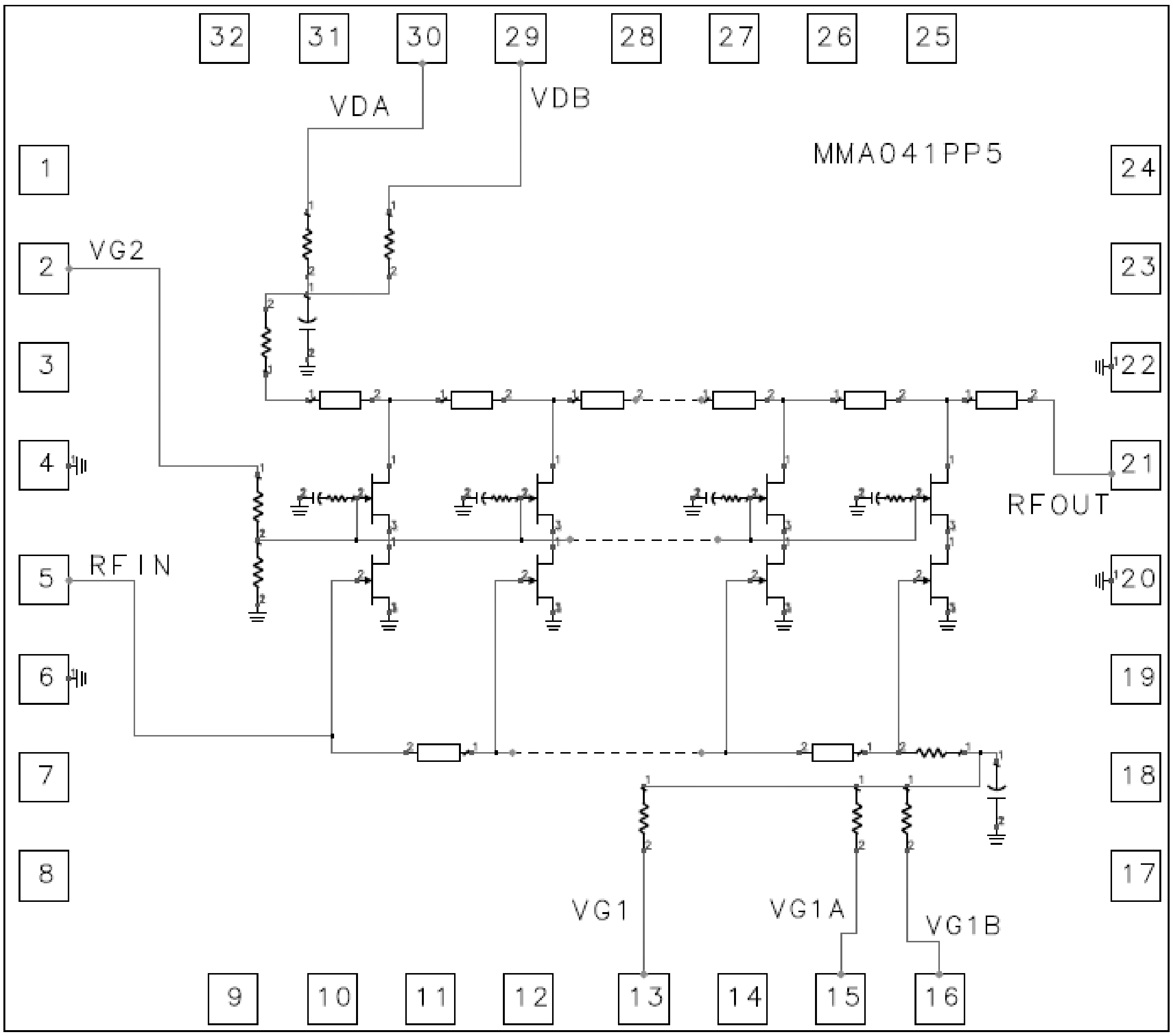
| | |
|---|---|
| Package | 5X5mm 32L Plastic QFN |
| Lead Frame | C194 Cu |
| Plating | Ni: 0.50 um min<br>Pd: 0.02 um min<br>Au: 0.05 um max |
| Package Body Material | RoHS Compliant Low-stress injection molded plastic |
| | |

**Table 2-2. PIN Description**

| PIN Number | Pad Name | Pad Description |
|---|---|---|
| 5 | $RF_{IN}$ | DC – Coupled and matched to 50Ω. (Optional VG1 can be biased on this line.) |
| 21 | $RF_{OUT}$ + $V_{DD}$ | DC – Coupled and matched to 50Ω. (Used to bias $V_{DD}$ ) |
| 13 | $V_{G1}$ | First Gate bias. Adjust to achieve specified $I_{DD}$ |
| 15, 16 | $V_{G1A}$, $V_{G1B}$ | Low-frequency termination. Connect bypass capacitors per application circuit. (No bias required) |
| 2 | $V_{G2}$ | DC couple to VDA externally for nominal operation. |
| 29, 30 | $V_{DB}$, $V_{DA}$ | Low-frequency termination. Connect bypass capacitors per application circuit. (No bias required) |
| 4, 6, 20, 22 | RF/DC GND | Should be connected to PCB RF/DC Ground |

| ...........continued | | |
|---|---|---|
| PIN Number | Pad Name | Pad Description |
| 1, 3, 7, 8, 9, 10, 11, 12, 14, 17, 18, 19, 23, 24, 25, 26, 27, 28, 31, 32 | N/C | These pins are not connected internally.<br>All data was measured with these pins connected to RF/DC ground externally. |
| Backside Paddle | RF/DC GND | Must be connected to RF/DC Ground |

Amplifier Functional Schematic



# 3. Evaluation PCB

**Figure 3-1. MMA041PP5E: Eval PCB**

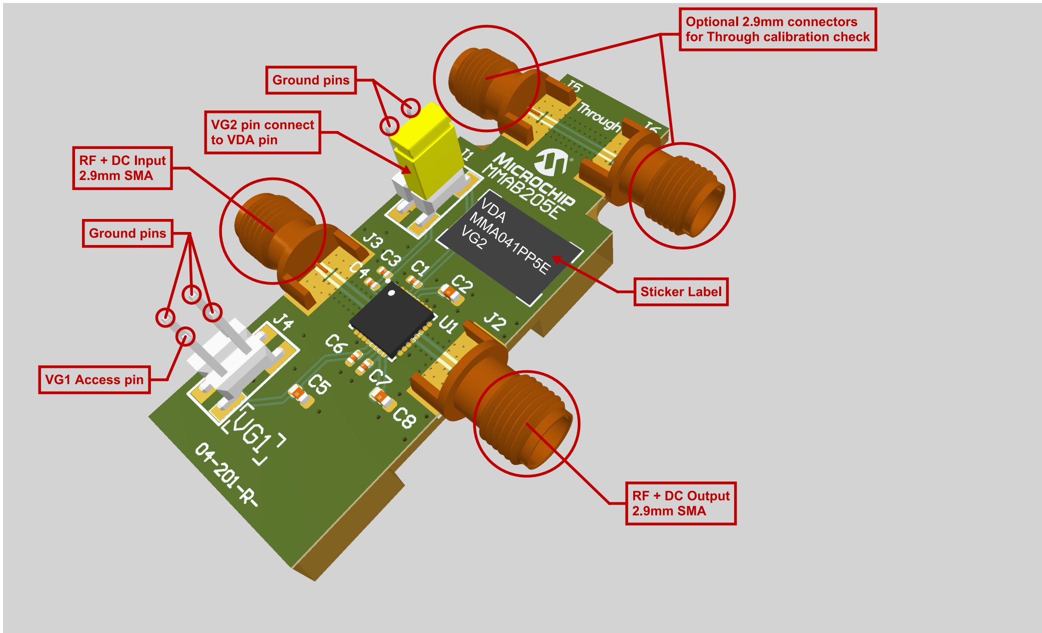



**Figure 3-2. MMA041PP5E: Eval PCB Schematic**

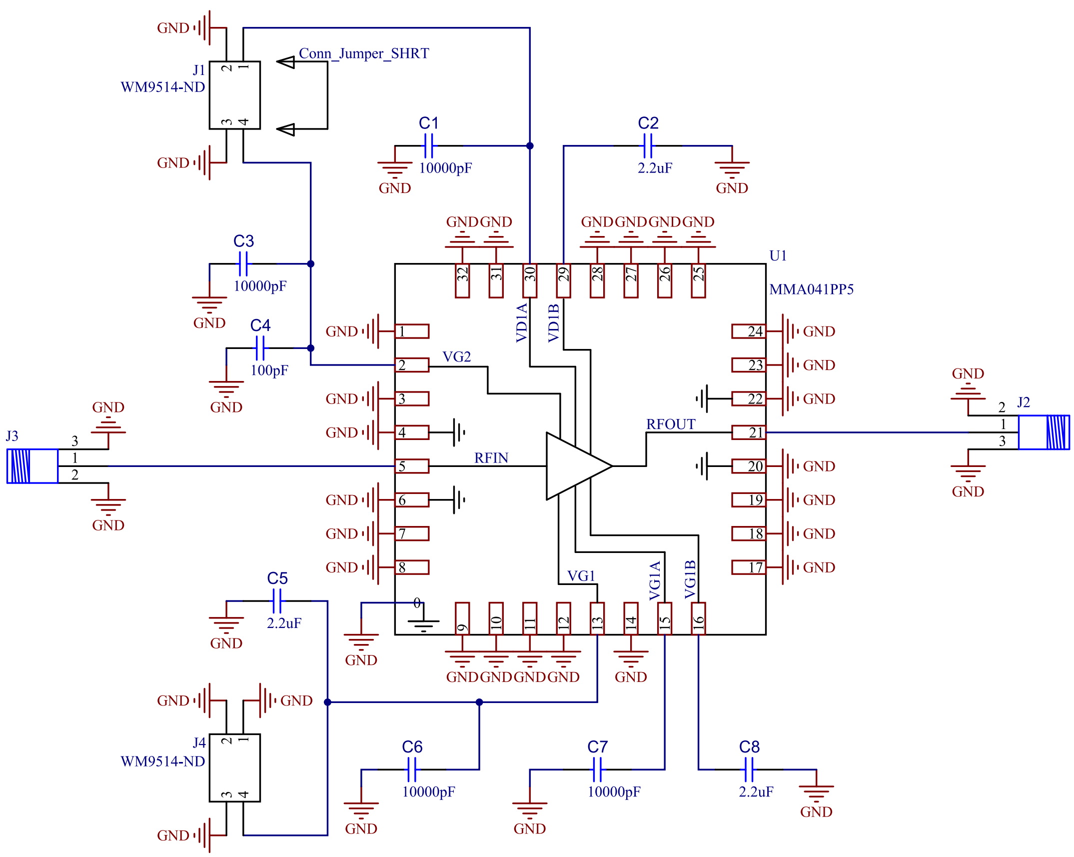


**Table 3-1. Bias Sequence**

| Setp | Bias Sequence |
|---|---|
| 1 | Make sure VG2 to VDA jumper is in place on J1 or, if using external power supply, VG2 power supply is connected to VG2 pin. |
| 2 | Make sure ESD precaution jumper from VG1 to GND on J4 header is removed. |
| 3 | Make sure all DC and RF connections are attached before activating any DC voltage power supplies. |
| | Note: DC supply for VG1 could be attached either through an external bias-T on the RF + DC input port (J3) or through the marked pin on J4. DC supply for VDD should be fed through an external bias-T on the RF + DC output port (J2). |
| 4 | Set VG1 at -1.0V |
| | Note: If using VG2 externally, it should be on soon after VG1. The range of VG2 should be at VDD +/-20% |
| 5 | Set VDD according to your applications plan with current compliance at 200mA |
| | Note: VG2 should be on |
| 6 | Power supply sequencing should always be VG1, (VG2 if used externally), then VDD (VDD is always last on and first off) |
| 7 | Adjust VG1 gradually increasing voltage by 0.01V steps until IDD reaches desired application range. |
| | Note: If external bias-T, used on the RF + DC Output (J2), is showing a very low cut-off frequency, precautions should be made to avoid fast changes of the IDD current otherwise DC spikes, caused by transitions, could exceed the VDD maximum level and damage the part. |

**Table 3-2. Bill of Material**

| Item Num. | Component designator | Description | Mnf. Part Num. | Mnf. | Qty. |
|---|---|---|---|---|---|
| 1 | U1 | 5 X 5 32 Leads QFN | MMA041PP5 | Microchip | 1 |
| 2 | C4 | 100 pF ±10% 25V Ceramic Capacitor X7R 0402 | C0402C101K3GACTU | KEMET | 1 |
| 3 | C2, C5, C8 | 2.2 µF ±10% 16V Ceramic Capacitor X5R 0603 | C1608X5R1C225K080AB | TDK | 3 |
| 4 | C1, C3, C6, C7 | 10000 pF ±10% 50V Ceramic Capacitor X7R 0402 | CC0402KRX7R9BB103 | Yageo | 4 |
| 5 | J2, J3, J5, J6 | Connector, 2.9mm Jack PCB Edge Mount .012 pin | 25-146-1000-90 | Winchester Interconnect | 4 |

| ...........continued | | | | | |
|---|---|---|---|---|---|
| **Item Num.** | **Component designator** | **Description** | **Mnf. Part Num.** | **Mnf.** | **Qty.** |
| 6 | J1, J4 | Connector Unshrouded Header, 2x2, 2.54mm | 15-91-2040 | Molex | 2 |
| 7 | JUMP1 | Connector, 2 Position Shunt, Black, Closed Top 2.54mm | SPC02SYAN | Sullins | 1 |

# 4. Ordering, Shipping and Handling

## 4.1 Ordering Information

For additional ordering information, contact your Microchip sales representative.

| Part Number | Package | Note |
|---|---|---|
| MMA041PP5 | 5 mm × 5 mm, 32L Plastic QFN | |
| MMA041AA | Die | Refer to corresponding MMA041AA Datasheet |
| MMA041PP5E | Eval PCB | |

## 4.2 Packing Information

| Part Number | Description |
|---|---|
| MMA041PP5-TR | Tape and Reel |

**Note:** Contact your Microchip sales representative for the minimum quantity order

# 5. Revision History

**Table 5-1. Revision History**

| Revision | Date | Description |
|---|---|---|
| B | 03/2022 | Document created. |

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