



Low-Jitter, Precision Clock Generator with Two Outputs

MAX3622

General Description

The MAX3622 is a low-jitter precision clock generator optimized for networking applications. The device integrates a crystal oscillator and a phase-locked loop (PLL) clock multiplier to generate high-frequency clock outputs for Ethernet and other networking applications. The proprietary PLL design features ultra-low jitter (0.36psRMS) and excellent power-supply noise rejection, minimizing design risk for network equipment.

The MAX3622 has one LVPECL output and one LVCMOS output. It is available in a 16-pin TSSOP package and operates over the 0°C to +70°C temperature range.

Applications

Ethernet Networking Equipment

Typical Application Circuit and Pin Configuration appear at end of data sheet.

Features

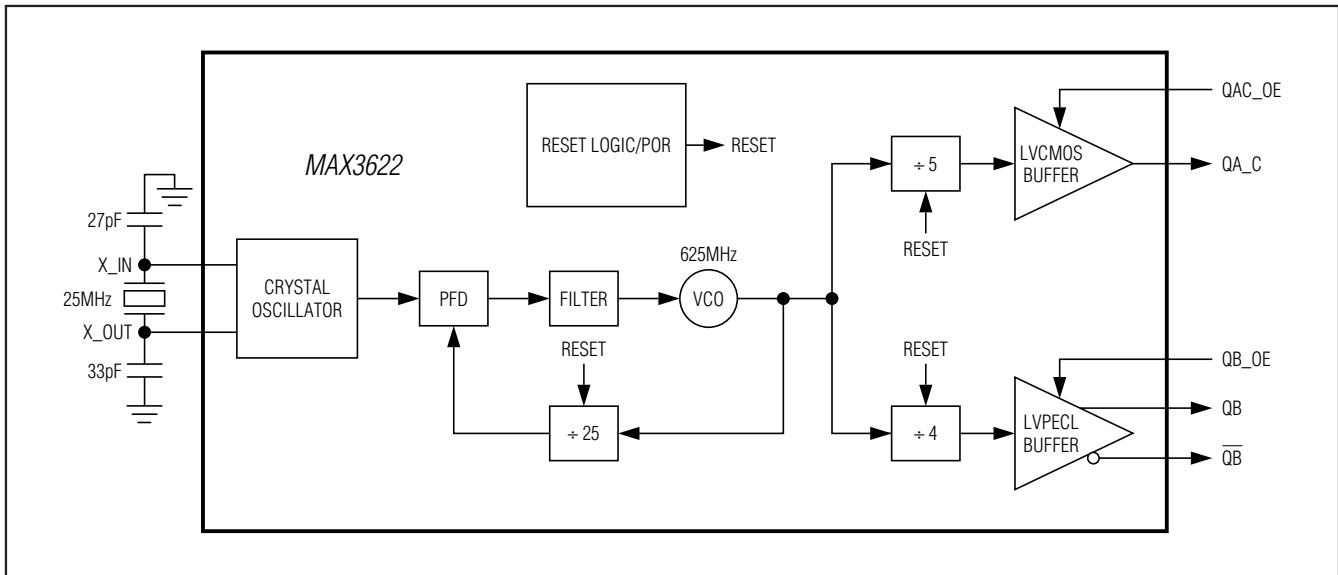
- ◆ Crystal Oscillator Interface: 25MHz Typical
- ◆ Output Frequencies: 125MHz and 156.25MHz
- ◆ Low Jitter
 - 0.14psRMS (1.875MHz to 20MHz)
 - 0.36psRMS (12kHz to 20MHz)
- ◆ Excellent Power-Supply Noise Rejection
- ◆ No External Loop Filter Capacitor Required

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3622CUE+	0°C to +70°C	16 TSSOP	U16-2

+Denotes a lead-free package.

Block Diagram



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range V_{CC} , V_{CCA} , V_{DDO_A} , V_{CCO_B}	-0.3V to +4.0V	Current into QA_C	± 50 mA
Voltage Range at QAC_OE, QB_OE, RES1, RES2	-0.3V to ($V_{CC} + 0.3$ V)	Current into QB, \overline{QB}	-56mA
Voltage Range at X_IN Pin	-0.3V to +1.2V	Continuous Power Dissipation ($T_A = +70^\circ\text{C}$) 16-Pin TSSOP (derate 11.1mW/ $^\circ\text{C}$ above +70 $^\circ\text{C}$)	889mW
Voltage Range at GND0_A	-0.3V to +0.3V	Operating Junction Temperature Range	-55 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Voltage Range at X_OUT Pin	-0.3V to ($V_{CC} - 0.6$ V)	Storage Temperature Range	-65 $^\circ\text{C}$ to +160 $^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{CC} = +3.0\text{V}$ to +3.6V, $T_A = 0^\circ\text{C}$ to +70 $^\circ\text{C}$, unless otherwise noted. Typical values are at $V_{CC} = +3.3\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Current	I_{CC}	(Note 3)		70	90	mA
CONTROL INPUT CHARACTERISTICS (QAC_OE, QB_OE PINS)						
Input Capacitance	C_{IN}			2		pF
Input Logic Bias Resistor	R_{BIAS}			50		k Ω
LVPECL OUTPUT SPECIFICATIONS (QB, \overline{QB} PINS)						
Output High Voltage	V_{OH}		$V_{CC} - 1.13$	$V_{CC} - 0.98$	$V_{CC} - 0.83$	V
Output Low Voltage	V_{OL}		$V_{CC} - 1.85$	$V_{CC} - 1.7$	$V_{CC} - 1.55$	V
Peak-to-Peak Output-Voltage Swing (Single-Ended)			0.6	0.72	0.9	V_{P-P}
Output Rise/Fall Time		20% to 80%	200	350	600	ps
Output Duty-Cycle Distortion			48	50	52	%
LVC MOS/LVTTL INPUT SPECIFICATIONS (QAC_OE, QB_OE PINS)						
Input-Voltage High	V_{IH}		2.0			V
Input-Voltage Low	V_{IL}				0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{CC}$			80	μA
Input Low Current	I_{IL}	$V_{IN} = 0\text{V}$	-80			μA
LVC MOS OUTPUT SPECIFICATIONS (QA_C PIN)						
Output High Voltage	V_{OH}	QA_C sourcing 12mA	2.6			V
Output Low Voltage	V_{OL}	QA_C sinking 12mA			0.4	V
Output Rise/Fall Time		(Note 4)	250	500	1000	ps
Output Duty-Cycle Distortion		(Note 4)	42	50	58	%
Output Impedance				14		Ω

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +3.0V$ to $+3.6V$, $T_A = 0^\circ C$ to $+70^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK OUTPUT AC SPECIFICATIONS						
VCO Frequency Range			620	625	648	MHz
Random Jitter	RJ _{RMS}	12kHz to 20MHz		0.36	1.0	pSRMS
		1.875MHz to 20MHz		0.14		
Deterministic Jitter Induced by Power-Supply Noise (Notes 5, 6)		LVPECL output		4		pSP-P
		LVC MOS output		19		
Spurs Induced by Power-Supply Noise (Note 6)		LVPECL output		-57		dBc
		LVC MOS output		-47		
Nonharmonic and Subharmonic Spurs				-70		dBc
Clock Output SSB Phase Noise at 125MHz		f = 1kHz		-124		dBc/Hz
		f = 10kHz		-126		
		f = 100kHz		-130		
		f = 1MHz		-145		
		f > 10MHz		-153		

Note 1: A series resistor of up to 10.5Ω is allowed between V_{CC} and V_{CCA} for filtering supply noise when system power-supply tolerance is $V_{CC} = 3.3V \pm 5\%$. See Figure 2.

Note 2: LVPECL terminated with 50Ω load connected to $V_{TT} = V_{CC} - 2V$.

Note 3: Both outputs enabled and unloaded.

Note 4: Measured using setup shown in Figure 1 with $V_{CC} = 3.3V \pm 5\%$.

Note 5: Measured with Agilent DSO81304A 40GS/s real-time oscilloscope.

Note 6: Measured with $40mV_{P-P}$, 100kHz sinusoidal signal on the supply with V_{CCA} connected as shown in Figure 2.

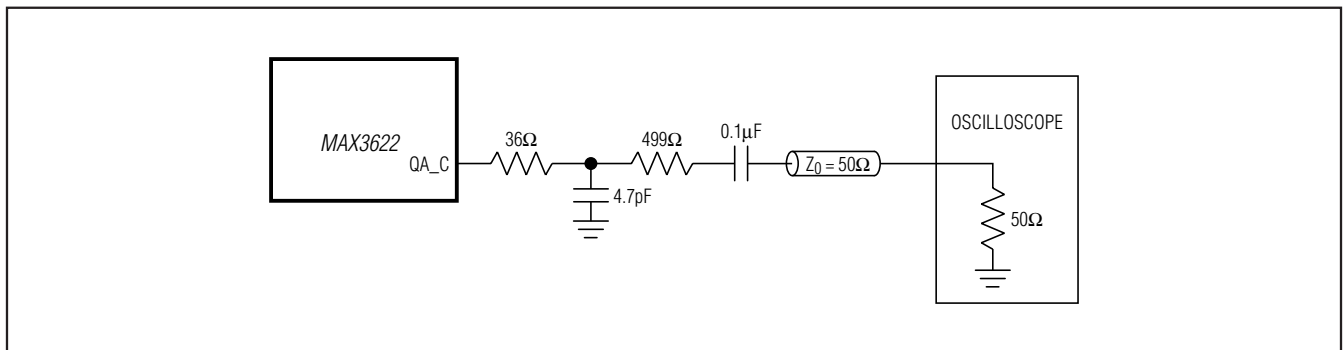
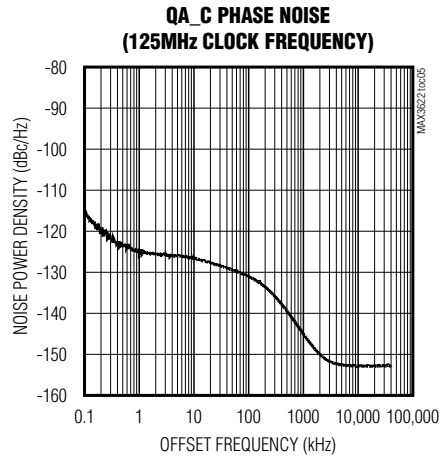
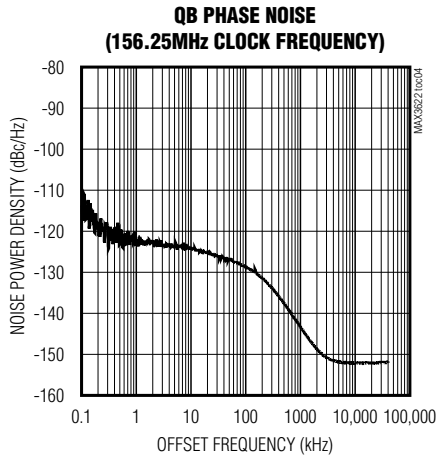
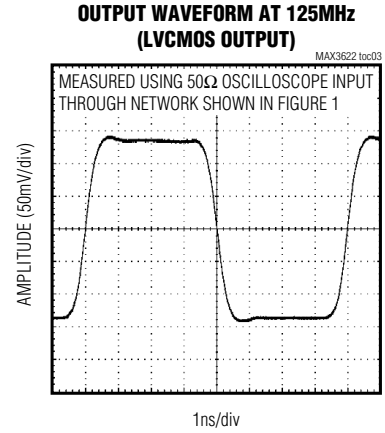
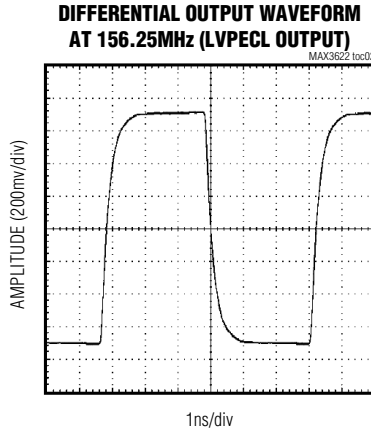
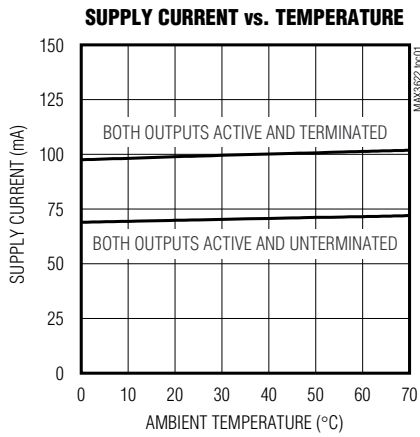


Figure 1. LVC MOS Output Measurement Setup

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Typical Operating Characteristics

(Typical values are at $V_{CC} = +3.3V$, $T_A = +25^\circ C$, crystal frequency = 25MHz.)



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Pin Description

PIN	NAME	FUNCTION
1	QAC_OE	LVC MOS/LVTTL Input. Enables/disables QA_C clock output. Connect pin high to enable QA_C. Connect low to set QA_C to a high-impedance state. Has internal 50kΩ input impedance.
2	GND0_A	Ground for QA_C Output. Connect to supply ground.
3	QA_C	LVC MOS Clock Output
4	VDD0_A	Power Supply for QA_C Clock Output. Connect to +3.3V.
5, 6	RES1, RES2	Reserved. Do not connect.
7	VCCA	Analog Power Supply for the VCO. Connect to +3.3V. For additional power-supply noise filtering, this pin can connect to VCC through 10.5Ω as shown in Figure 2 (requires VCC = +3.3V ±5%).
8	VCC	Core Power Supply. Connect to +3.3V.
9, 15	GND	Supply Ground
10	X_OUT	Crystal Oscillator Output
11	X_IN	Crystal Oscillator Input
12	VCC0_B	Power Supply for QB Clock Output. Connect to +3.3V.
13	\overline{QB}	LVPECL, Inverting Clock Output
14	QB	LVPECL, Noninverting Clock Output
16	QB_OE	LVC MOS/LVTTL Input. Enables/disables QB clock output. Connect pin high to enable LVPECL clock output QB. Connect low to set QB to a logic 0. Has internal 50kΩ input impedance.

Detailed Description

The MAX3622 is a low-jitter clock generator designed to operate at Ethernet frequencies. It consists of an on-chip crystal oscillator, PLL, LVC MOS output buffer, and an LVPECL output buffer. Using a 25MHz crystal as a reference, the internal PLL generates a high-frequency output clock with excellent jitter performance.

Crystal Oscillator

An integrated oscillator provides the low-frequency reference clock for the PLL. This oscillator requires a 25MHz crystal connected between X_IN and X_OUT.

PLL

The PLL takes the signal from the crystal oscillator and synthesizes a low-jitter, high-frequency clock. The PLL contains a phase-frequency detector (PFD), a lowpass filter, and a voltage-controlled oscillator (VCO). The VCO output is connected to the PFD input through a feedback divider. The PFD compares the reference frequency to the divided-down VCO output ($f_{VCO}/25$) and generates a control signal that keeps the VCO locked

to the reference clock. The high-frequency VCO output clock is sent to the output dividers. To minimize noise-induced jitter, the VCO supply (VCCA) is isolated from the core logic and output buffer supplies.

Output Dividers

The output dividers are set to divide-by-five for the LVC MOS output QA_C and divide-by-four for the LVPECL output QB.

LVPECL Driver

The differential PECL buffer (QB) is designed to drive transmission lines terminated with 50Ω to VCC - 2.0V. The output goes to a logic 0 when disabled.

LVC MOS Driver

QA_C, the LVC MOS output, is designed to drive a single-ended high-impedance load. This output goes to a high-impedance state when disabled.

Reset Logic/POR

During power-on, the power-on reset (POR) signal is generated to synchronize all dividers.

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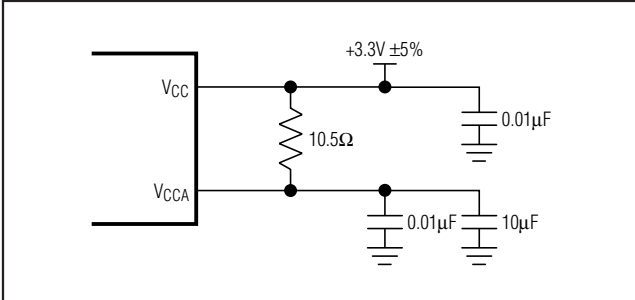


Figure 2. Analog Supply Filtering

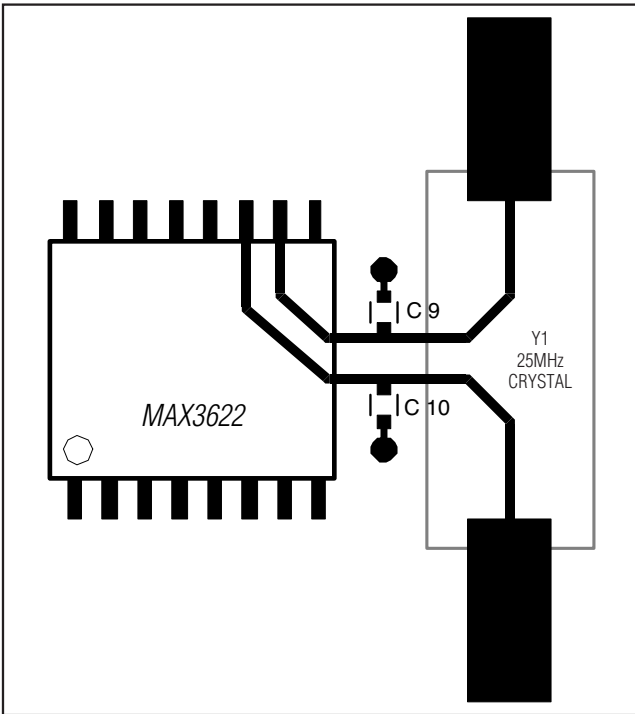


Figure 3. Crystal Layout

Applications Information

Power-Supply Filtering

The MAX3622 is a mixed analog/digital IC. The PLL contains analog circuitry susceptible to random noise. In addition to excellent on-chip power-supply noise rejection, the MAX3622 provides a separate power-supply pin, VCCA, for the VCO circuitry. Figure 2 illustrates the recommended power-supply filter network for VCCA. The purpose of this design technique is to ensure clean input power supply to the VCO circuitry and to improve the overall immunity to power-supply noise. This network requires that the power supply is +3.3V ±5%. Decoupling capacitors should be used on all other supply pins for best performance.

Crystal Selection

The crystal oscillator is designed to drive a fundamental mode, AT-cut crystal resonator. See Table 1 for recommended crystal specifications. See Figure 4 for external capacitor connection.

Crystal Input Layout and Frequency Stability

The crystal, trace, and two external capacitors should be placed on the board as close as possible to the MAX3622's X_IN and X_OUT pins to reduce crosstalk of active signals into the oscillator.

The layout shown in Figure 3 gives approximately 3pF of trace plus footprint capacitance per side of the crystal (Y1). The dielectric material is FR-4 and dielectric thickness of the reference board is 15 mils. Using a 25MHz crystal and the capacitor values of C10 = 27pF and C9 = 33pF, the measured output frequency accuracy is -10ppm at +25°C ambient temperature.

Table 1. Crystal Selection Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Crystal Oscillation Frequency	f _{OSC}		25		MHz
Shunt Capacitance	C _O		2.0	7.0	pF
Load Capacitance	C _L		18		pF
Equivalent Series Resistance (ESR)	R _S			50	Ω
Maximum Crystal Drive Level				300	μW

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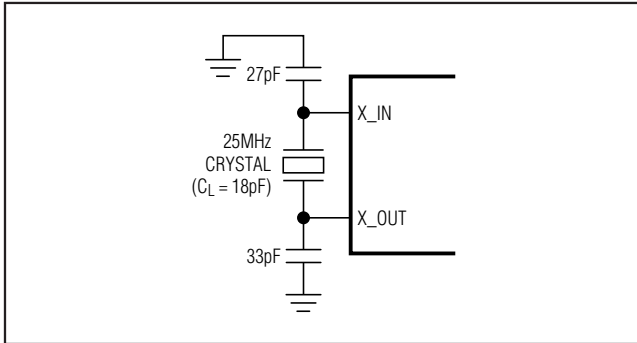


Figure 4. Crystal, Capacitors Connection

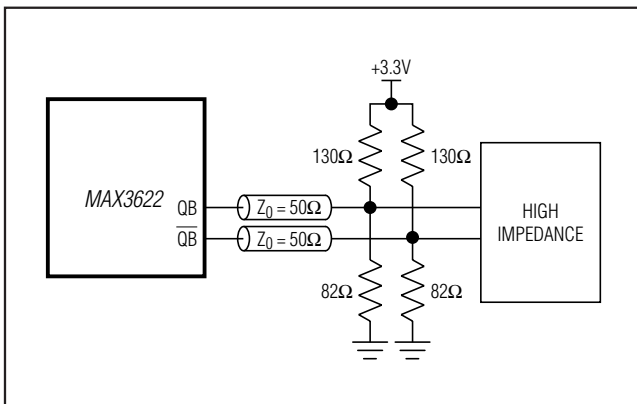


Figure 5. Thevenin Equivalent of Standard PECL Termination

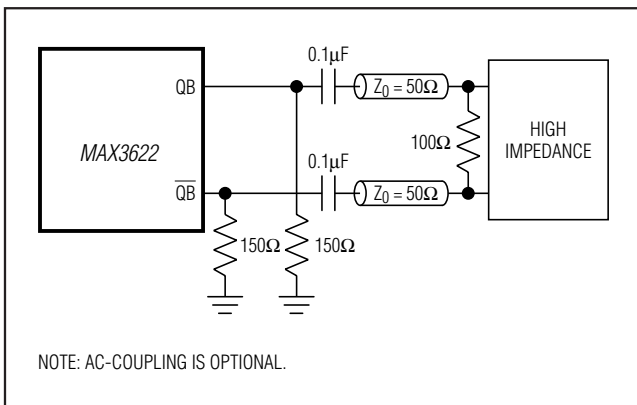


Figure 6. AC-Coupled PECL Termination

Interfacing with LVPECL Outputs

The equivalent LVPECL output circuit is given in Figure 7. This output is designed to drive a pair of 50Ω transmission lines terminated with 50Ω to $V_{TT} = V_{CC} - 2V$. If a separate termination voltage (V_{TT}) is not available, other termination methods can be used such as shown in Figures 5 and 6. Unused outputs should be disabled and may be left open. For more information on LVPECL terminations and how to interface with other logic families, refer to Maxim Application Note HFAN-01.0: *Introduction to LVDS, PECL, and CML*.

Interface Models

Figure 7 and Figure 8 show examples of interface models.

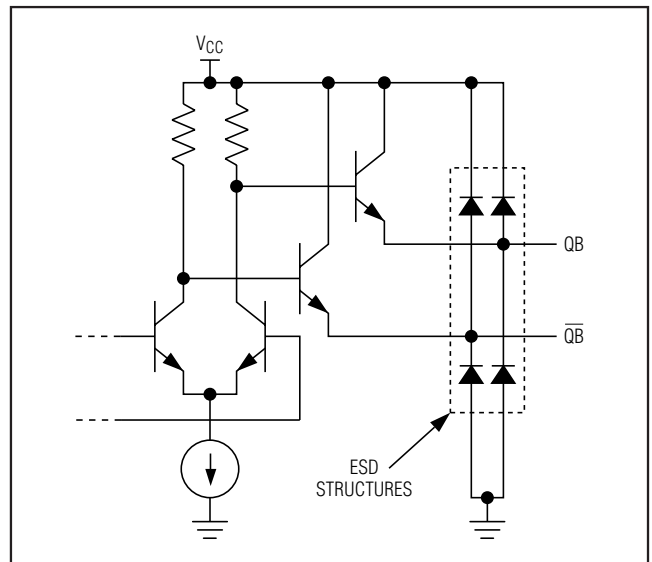


Figure 7. Simplified LVPECL Output Circuit Schematic

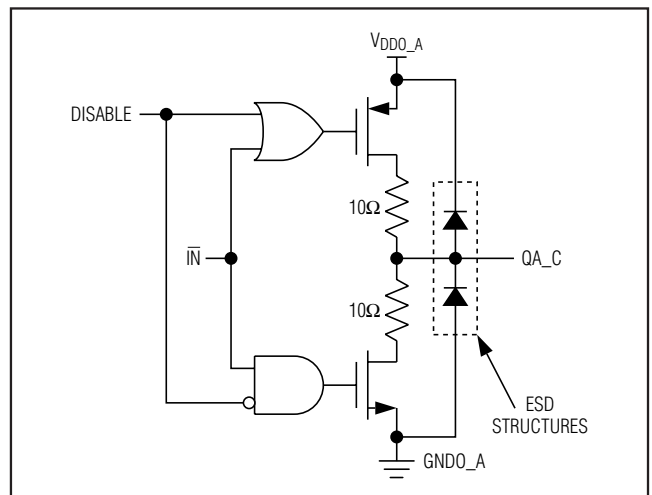


Figure 8. Simplified LVCMOS Output Circuit Schematic

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Layout Considerations

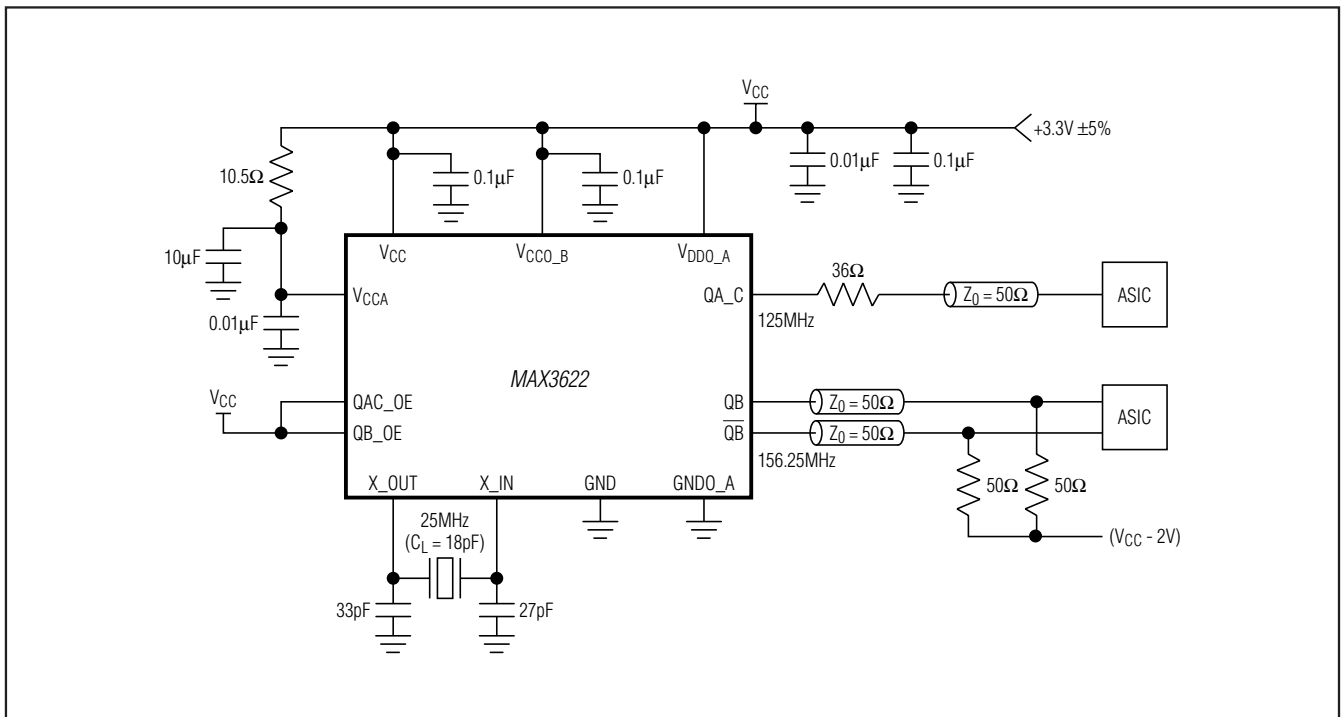
The inputs and outputs are critical paths for the MAX3622, and care should be taken to minimize discontinuities on these transmission lines. Here are some suggestions for maximizing the MAX3622's performance:

- An uninterrupted ground plane should be positioned beneath the clock I/Os.
- Supply and ground pin vias should be placed close to the IC and the input/output interfaces to allow a return current path to the MAX3622 and the receive devices.

- Supply decoupling capacitors should be placed close to the MAX3622 supply pins.
- Maintain 100Ω differential (or 50Ω single-ended) transmission line impedance out of the MAX3622.
- Use good high-frequency layout techniques and a multilayer board with an uninterrupted ground plane to minimize EMI and crosstalk.

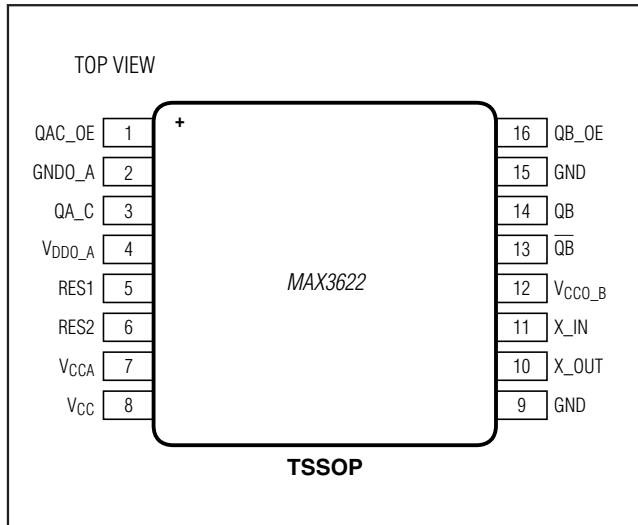
Refer to the MAX3622 Evaluation Kit for more information.

Typical Application Circuit



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Pin Configuration



Chip Information

TRANSISTOR COUNT: 10,490

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to <http://www.microsemi.com>

PACKAGE TYPE	DOCUMENT NO.
16 TSSOP	21-0066



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