HV583

128-Channel Serial to Parallel Converter with Push-Pull Outputs

Features

- 128 High-Voltage Channels
  - Up to 80V Operating Output Voltage
  - 30 mA Peak Output Sink/Source Current
  - Output Diodes to Ground for Efficient Power Recovery
- Four Separate Shift Registers
  - Clockwise and Counter-Clockwise Data Shifting via DIR Pin
- 40 MHz Data Rate

Applications

- Inkjet Printer Driver
- Plasma Display Driver
- 3D Printer Driver

Related Devices

- **HV582**: 96-Channel Serial to Parallel Converter with Push-Pull Outputs

Description

HV583 is a unipolar, 128-channel low-voltage serial to high-voltage parallel converter with push-pull outputs. This device has been designed for applications requiring multiple high-voltage outputs with current sinking and sourcing capabilities, such as plasma displays and inkjet printers.

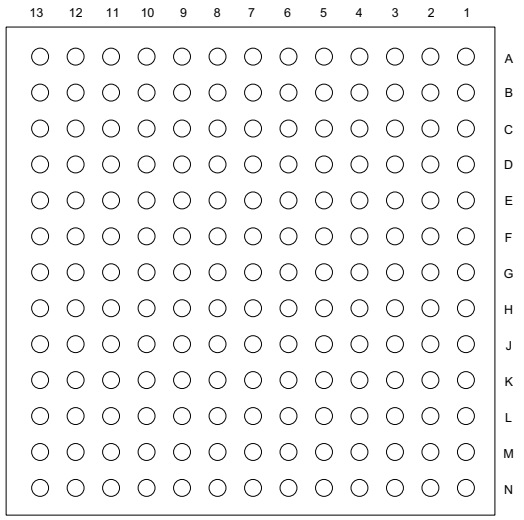
The device consists of four parallel 32-bit shift registers, a 128-bit latch and 128 high-voltage outputs. Data can be input at 40 MHz or up to 25 MHz when cascaded in a multiple device configuration.

HV583 is offered in a 169-ball 10 x 10 x 1.1 mm TFBGA package.

Package Type

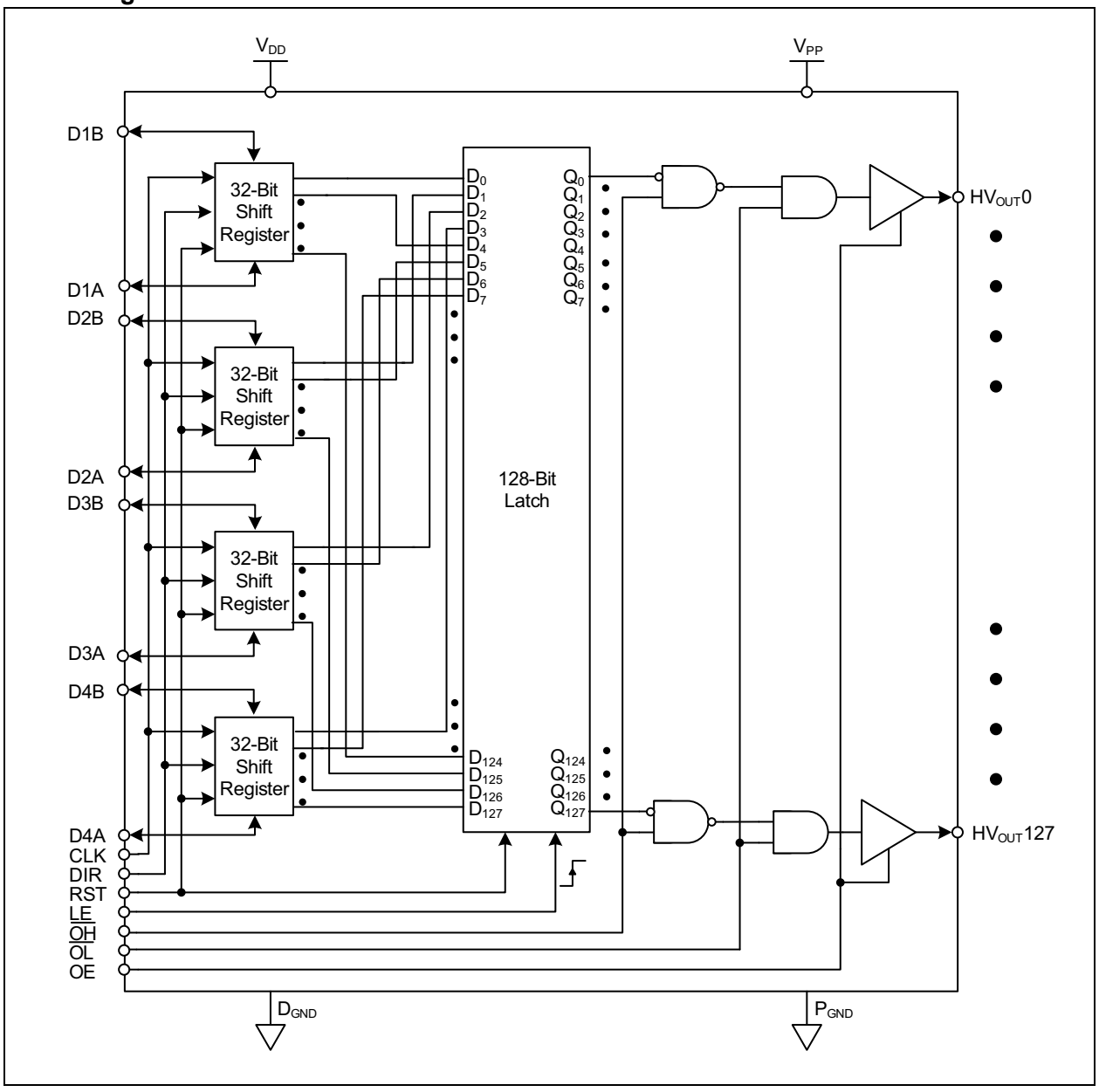
HV583

10x10x1.1 mm TFBGA*
Bottom View



* See Section **Section 2.0 "Package Pin Configurations and Function Description"**.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Rating†

Supply Voltage V_{DD} ..... –0.5V to +6.5V

High-Voltage Supply V_{PP} ..... –0.5V to +90V

Output Sink and Source Current I_{OUT} .....–65 mA to +40 mA

Output Body Diode Current I_{DIODE} .....–65 mA to +65 mA

Logic Input Voltage .....–0.5V to V_{DD} +0.5V

Operating Junction Temperature .....–25°C to +125°C

Storage Temperature .....–40°C to +150°C

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device is ESD sensitive. Use appropriate ESD precautions.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
High-Voltage Supply	V_{PP}	15	-	80	V	
Low-Voltage Supply	V_{DD}	4.5	5.0	5.5	V	
HV_{OUT} Peak Output Current	I_{OUT}	–30	—	30	mA	
V_{PP} Power Supply Slew Rate	SR	-	—	8.0	V/µs	
Clock Frequency	f_{CLK}	-	—	40	MHz	Data Read
		-	—	25	MHz	Cascaded Devices

TABLE 1-1: POWER SEQUENCES

Sequence Type	Steps
Power-Up Sequence	1. Connect ground. 2. Apply V_{DD}. 3. Set all inputs (data, CLK, etc.) to a known state. 4. Apply V_{PP}.
Power-Down Sequence	Repeat the power-up sequence in reverse order.

DC ELECTRICAL CHARACTERISTICS

Electrical specifications: Unless otherwise specified, $T_A = T_J = +25°C$, $V_{DD} = 5.0V$ and $V_{PP} = 80V$.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
V_{PP} Quiescent Supply Current	I_{PPQ}	—	—	10	µA	
V_{DD} Quiescent Supply Current	I_{DDQ}	—	—	10	µA	
High-Level Output Voltage	HV_{OH}	73	76	—	V	I_{OUT} = 15 mA, V_{PP} = 80V
		10	—	—		I_{OUT} = 10 mA, V_{PP} = 20V
Output P-Channel Body Diode	HV_{OHD}	—	—	81.5	V	I_{OUT} = –30 mA, V_{PP} = 80V (**Note 1**)
Low-Level Output Voltage	HV_{OL}	—	3.0	6.0	V	I_{OUT} = –15 mA
Output N-Channel Body Diode	HV_{OLD}	–1.5	—	—	V	I_{OUT} = 30 mA (**Note 1**)

Note 1: Specification is for design guidance only.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical specifications: Unless otherwise specified, $T_A = T_J = +25°C$, $V_{DD} = 5.0V$ and $V_{PP} = 80V$.						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Logic Input High Voltage	V_{IH}	2.3	—	V_{DD}	V	V_{DD} = 4.5V to 5.5V
Logic Input Low Voltage	V_{IL}	0	—	0.7		V_{DD} = 4.5V to 5.5V
Logic Input High Current	I_{IH}	—	—	1.0	µA	V_{IH} = 5.0V, V_{DD} = 5.0V
		10	30	60		V_{IH} = 5.0V, for DIR only
Logic Input Low Current	I_{IL}	–1.0	—	—		V_{IL} = 0V
Logic Output High	V_{OH}	4.5	—	—	V	I_{OUT} = 1.0 mA
Logic Output Low	V_{OL}	—	—	0.5		I_{OUT} = –1.0 mA

Note 1: Specification is for design guidance only.

AC ELECTRICAL CHARACTERISTICS

Electrical specifications: Unless otherwise specified $T_A = T_J = 25°C$, $V_{DD} = 5.0V$ and $V_{PP} = 80V$						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Clock Pulse Width, High and Low(1)	t_{wCLK}	10	—	—	ns	V_{DD} = 4.5V to 5.5V T_J = –25°C to +125°C
LE Pulse Width, High and Low(2)	t_{wLE}	10	—	—		
Setup Time, DnA/B to CLK(1)	t_{su1}	5	—	—		
Setup Time, CLK to LE(1)	t_{su2}	10	—	—		
Setup Time, LE to $\overline{OL}$,$\overline{OH}$(1)	t_{su3}	25	—	—		
Setup Time, RST to CLK(2)	t_{su4}	5	—	—		
Setup Time, RST to LE(2)	t_{su5}	5	—	—		
Hold Time, CLK to DnA/B(1)	t_{h1}	5	—	—		
Hold Time, LE to CLK(1)	t_{h2}	10	—	—		
Hold Time, CLK to RST(2)	t_{h3}	5	—	—		
Hold Time, LE to RST(2)	t_{h4}	5	—	—		
CLK to DnA/B (High-to-Low)	t_{pdHL}	—	—	25		C_L = 15 pF
CLK to DnA/B (Low-to-High)	t_{pdLH}	—	—	25		C_L = 15 pF
LE,$\overline{OL}$,$\overline{OH}$ to HV_{OUT}n (High-to-Low)	t_{pHL}	—	—	150		C_L = 50 pF
LE,$\overline{OL}$,$\overline{OH}$ to HV_{OUT}n (Low-to-High)	t_{pLH}	Typ–40	t_{pHL}+ t_f	Typ+40		C_L = 80 pF
OE to HV_{OUT}n (High-to-Low)	t_{pHZL}	—	—	150		C_L = 50 pF
OE to HV_{OUT}n (Low-to-High)	t_{pLZH}	Typ–40	t_{pHL}+ t_f	Typ+40		C_L = 80 pF
OE to HV_{OUT}n (High-to-Low)	t_{pHZ}	—	—	300		R_L = 10K, C_L = 50 pF
OE to HV_{OUT}n (Low-to-High)	t_{pLZ}	—	—	300		R_L = 10K, C_L = 50 pF
Rise Time HV_{OUT}n	t_r	—	—	120		C_L = 50 pF
Fall Time HV_{OUT}n	t_f	—	—	120		C_L = 50 pF

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Specification is for design guidance only.

TEMPERATURE SPECIFICATIONS

Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Junction Temperature	T_J	–25	—	+125	°C	
Storage Temperature	T_A	–40	—	+150	°C	
Package Thermal Resistance						
Thermal Resistance, 169-Ball TFBGA	θ_{JA}	—	27	—	°C/W	

1.1 Logic Characteristics

TABLE 1-2: SHIFT REGISTER TRUTH TABLE

DIR	CLK	State	Direction
L or Open	↑	Shift	DnB to DnA
L or Open	↓	Hold	DnB to DnA
H	↑	Shift	DnA to DnB
H	↓	Hold	DnA to DnB

Legend:

D = Data
H = Level High
L = Level Low
X = Don't Care
Z = High Impedance
↑ = Low-to-High Transition
↓ = High-to-Low Transition

TABLE 1-3: LATCH TRUTH TABLE

LE	Output State of Latch
L to H	Latch Execution
H to L	Hold

TABLE 1-4: $HV_{OUT}n$ TRUTH TABLE

OE	$\overline{OL}$	$\overline{OH}$	DnA/DnB	$HV_{OUT}n$
L	X	X	X	Z
H	L	X	X	L
H	H	L	X	H
H	H	H	L	L
H	H	H	H	H

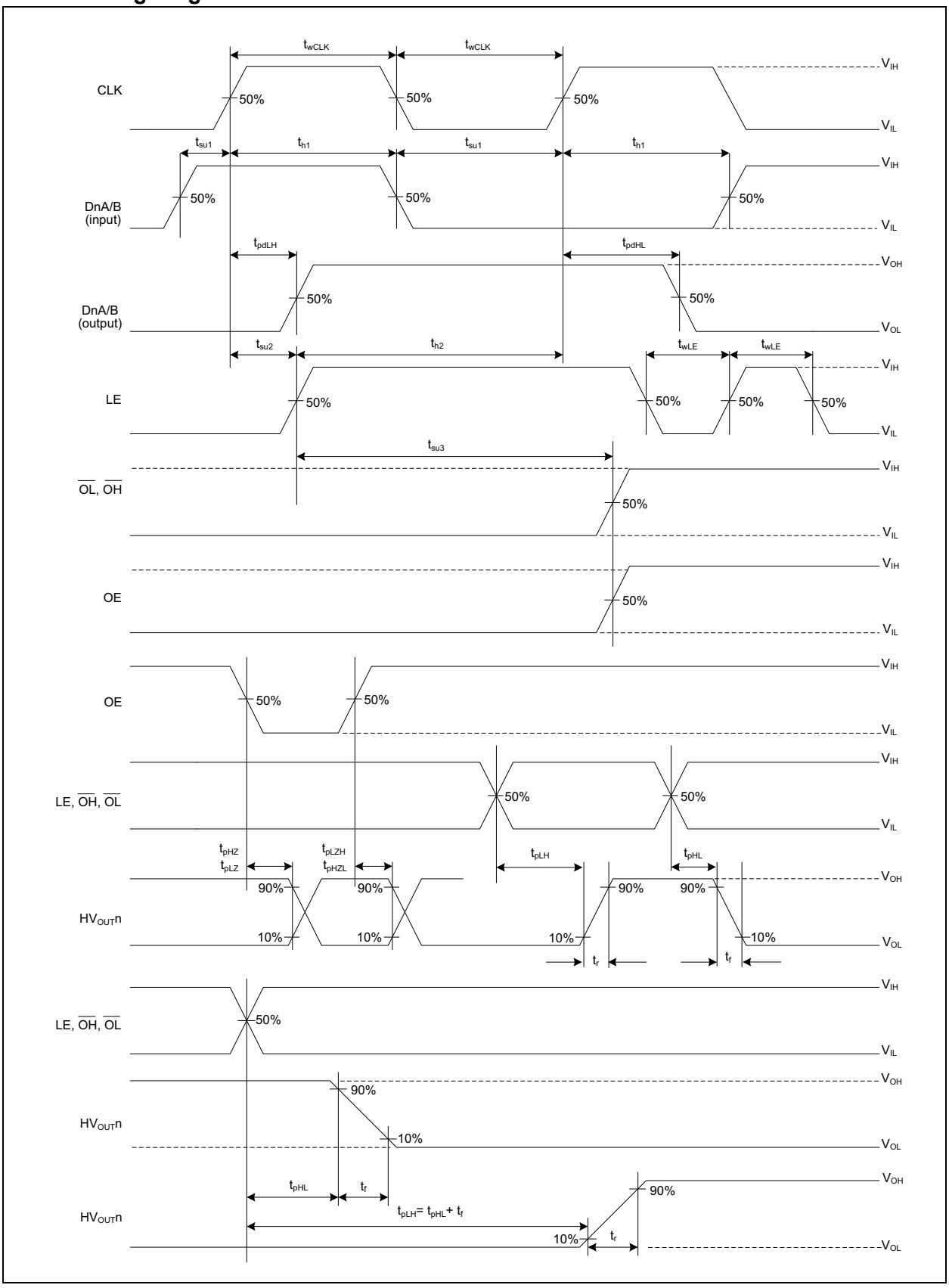
TABLE 1-5: RESET TRUTH TABLE

RST	CLK	LE	Shift Register	Latches
0	↑	X	Shift	X
0	X	↑	X	Latch
1	↑	X	Clear	X
1	X	↑	X	Clear

TABLE 1-6: OUTPUT SHIFT OPERATION

Input	Output	DIR	Shift Operation
D1A = D	D1B	H	D to D124...D0 to D1B
D2A = D	D2B	H	D to D125...D1 to D2B
D3A = D	D3B	H	D to D126...D2 to D3B
D4A = D	D4B	H	D to D127...D3 to D4B
D1B = D	D1A	L or Open	D to D0...D124 to D1A
D2B = D	D2A	L or Open	D to D1...D125 to D2A
D3B = D	D3A	L or Open	D to D2....D126 to D3A
D4B = D	D4A	L or Open	D to D3....D127 to D4A

1.2 Timing Diagram



2.0 PACKAGE PIN CONFIGURATIONS AND FUNCTION DESCRIPTION

This section details the pin designation for the 169-Ball TFBGA package (Figure 2-1). The descriptions of the pins are listed in Table 2-1.

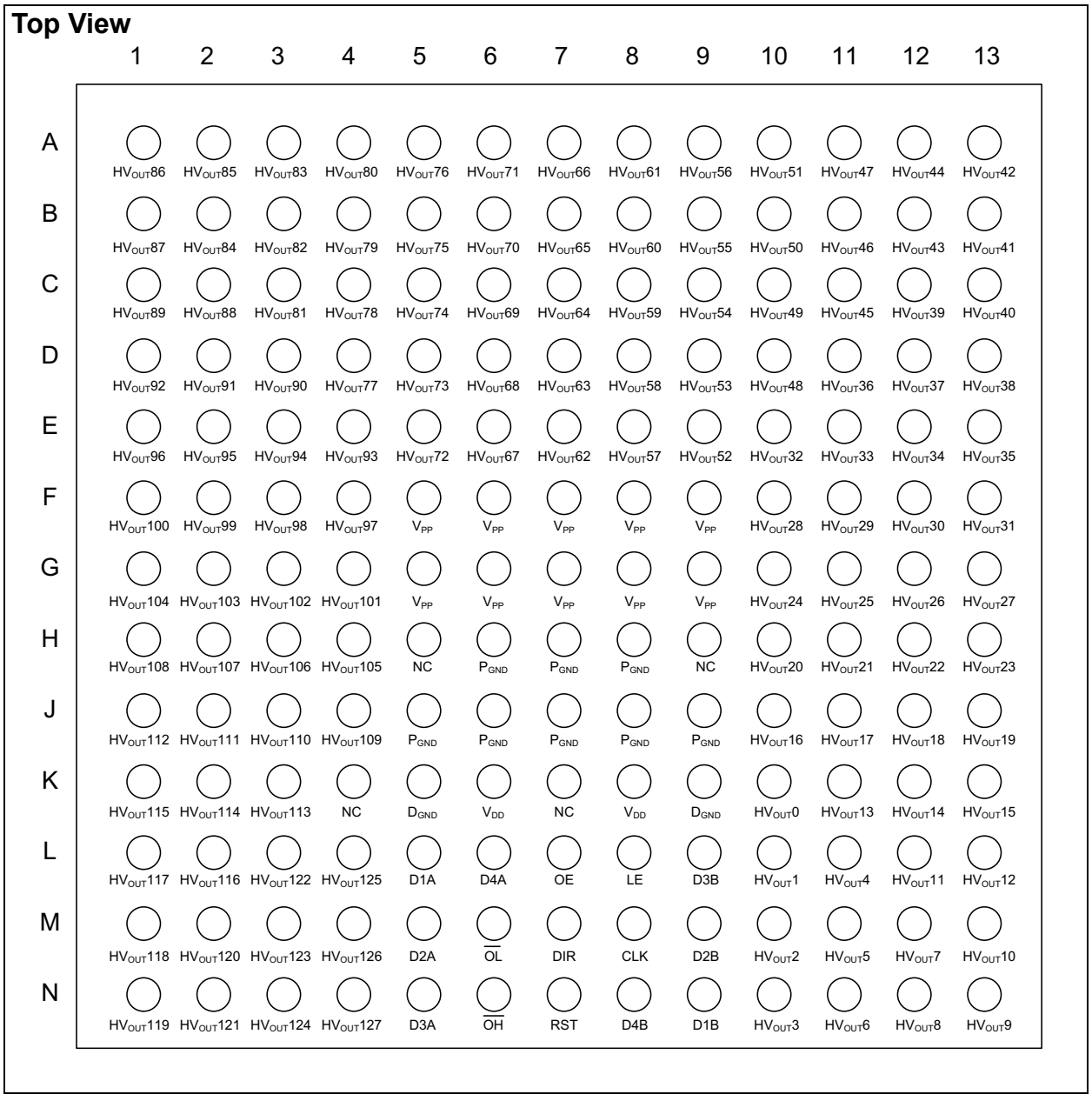


FIGURE 2-1: *169-Ball TFBGA Package.*

TABLE 2-1: PIN ASSIGNMENT

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
A1	$HV_{OUT}86$	D5	$HV_{OUT}73$	H5, H9, K4, K7	NC	M8	CLK
A2	$HV_{OUT}85$	D6	$HV_{OUT}68$	H6, H7, H8, J5, J6, J7, J8, J9	P_{GND}	M9	D2B
A3	$HV_{OUT}83$	D7	$HV_{OUT}63$	H10	$HV_{OUT}20$	M10	$HV_{OUT}2$
A4	$HV_{OUT}80$	D8	$HV_{OUT}58$	H11	$HV_{OUT}21$	M11	$HV_{OUT}5$
A5	$HV_{OUT}76$	D9	$HV_{OUT}53$	H12	$HV_{OUT}22$	M12	$HV_{OUT}7$
A6	$HV_{OUT}71$	D10	$HV_{OUT}48$	H13	$HV_{OUT}23$	M13	$HV_{OUT}10$
A7	$HV_{OUT}66$	D11	$HV_{OUT}36$	J1	$HV_{OUT}112$	N1	$HV_{OUT}119$
A8	$HV_{OUT}61$	D12	$HV_{OUT}37$	J2	$HV_{OUT}111$	N2	$HV_{OUT}121$
A9	$HV_{OUT}56$	D13	$HV_{OUT}38$	J3	$HV_{OUT}110$	N3	$HV_{OUT}124$
A10	$HV_{OUT}51$	E1	$HV_{OUT}96$	J4	$HV_{OUT}109$	N4	$HV_{OUT}127$
A11	$HV_{OUT}47$	E2	$HV_{OUT}95$	J10	$HV_{OUT}16$	N5	D3A
A12	$HV_{OUT}44$	E3	$HV_{OUT}94$	J11	$HV_{OUT}17$	N6	$\overline{OH}$
A13	$HV_{OUT}42$	E4	$HV_{OUT}93$	J12	$HV_{OUT}18$	N7	RST
B1	$HV_{OUT}87$	E5	$HV_{OUT}72$	J13	$HV_{OUT}19$	N8	D4B
B2	$HV_{OUT}84$	E6	$HV_{OUT}67$	K1	$HV_{OUT}115$	N9	D1B
B3	$HV_{OUT}82$	E7	$HV_{OUT}62$	K2	$HV_{OUT}114$	N10	$HV_{OUT}3$
B4	$HV_{OUT}79$	E8	$HV_{OUT}57$	K3	$HV_{OUT}113$	N11	$HV_{OUT}6$
B5	$HV_{OUT}75$	E9	$HV_{OUT}52$	K5, K9	D_{GND}	N12	$HV_{OUT}8$
B6	$HV_{OUT}70$	E10	$HV_{OUT}32$	K6, K8	V_{DD}	N13	$HV_{OUT}9$
B7	$HV_{OUT}65$	E11	$HV_{OUT}33$	K10	$HV_{OUT}0$		
B8	$HV_{OUT}60$	E12	$HV_{OUT}34$	K11	$HV_{OUT}13$		
B9	$HV_{OUT}55$	E13	$HV_{OUT}35$	K12	$HV_{OUT}14$		
B10	$HV_{OUT}50$	F1	$HV_{OUT}100$	K13	$HV_{OUT}15$		
B11	$HV_{OUT}46$	F2	$HV_{OUT}99$	L1	$HV_{OUT}117$		
B12	$HV_{OUT}43$	F3	$HV_{OUT}98$	L2	$HV_{OUT}116$		
B13	$HV_{OUT}41$	F4	$HV_{OUT}97$	L3	$HV_{OUT}122$		
C1	$HV_{OUT}89$	F5, F6, F7, F8, F9, G5, G6, G7, G8, G9	V_{PP}	L4	$HV_{OUT}125$		
C2	$HV_{OUT}88$	F10	$HV_{OUT}28$	L5	D1A		
C3	$HV_{OUT}81$	F11	$HV_{OUT}29$	L6	D4A		
C4	$HV_{OUT}78$	F12	$HV_{OUT}30$	L7	OE		
C5	$HV_{OUT}74$	F13	$HV_{OUT}31$	L8	LE		
C6	$HV_{OUT}69$	G1	$HV_{OUT}104$	L9	D3B		
C7	$HV_{OUT}64$	G2	$HV_{OUT}103$	L10	$HV_{OUTN}1$		
C8	$HV_{OUT}59$	G3	$HV_{OUT}102$	L11	$HV_{OUT}4$		
C9	$HV_{OUT}54$	G4	$HV_{OUT}101$	L12	$HV_{OUT}11$		
C10	$HV_{OUT}49$	G10	$HV_{OUT}24$	L13	$HV_{OUT}12$		
C11	$HV_{OUT}45$	G11	$HV_{OUT}25$	M1	$HV_{OUT}118$		
C12	$HV_{OUT}39$	G12	$HV_{OUT}26$	M2	$HV_{OUT}120$		
C13	$HV_{OUT}40$	G13	$HV_{OUT}27$	M3	$HV_{OUT}123$		
D1	$HV_{OUT}92$	H1	$HV_{OUT}108$	M4	$HV_{OUT}126$		
D2	$HV_{OUT}91$	H2	$HV_{OUT}107$	M5	D2A		
D3	$HV_{OUT}90$	H3	$HV_{OUT}106$	M6	$\overline{OL}$		
D4	$HV_{OUT}77$	H4	$HV_{OUT}105$	M7	DIR		

2.1 High-Voltage Output Pins ($HV_{OUT}0$ to $HV_{OUT}127$)

These are the high-voltage output channels (Push-Pull).

2.2 High-Voltage Power Supply Pins (V_{PP})

High-voltage power supply pins for the output channels ($HV_{OUT}n$).

2.3 No Connection Pins (NC)

NC pins do not have any functionality on the IC. These pins should not be connected.

2.4 High-Voltage Ground Pins (P_{GND})

High-voltage ground pins provide the reference ground level for the high-voltage output channels.

2.5 Digital Logic Ground Pins (D_{GND})

Digital Logic Ground pins provide a reference ground level for the low-voltage section of the IC, shift-registers, latches and decoders.

2.6 Logic Power Supply Pins (V_{DD})

Logic power supply pins for the 32-bit shift registers, 128-bit latch and decoders.

2.7 Data Input/Output Pins (D1A, D2A, D3A, D4A)

Data Input/Output pins are configurable as inputs or outputs for the shift registers depending on the state of the Direction pin (DIR).

When DIR is High, pins D1A to D4A are configured as inputs to the data shift registers. When DIR is Low, these pins are configured as outputs of the data shift registers.

2.8 Output Enable Pin (OE)

The Output Enable pin controls the functionality of the high-voltage output channels.

When OE is High, all $HV_{OUT}n$ channels are enabled and form a push-pull configuration to operate according to input data, $\overline{OL}$ or $\overline{OH}$ configuration states. When OE is Low, all $HV_{OUT}n$ channels are forced to a high-impedance state, regardless of the data stored in the 128-bit latch or the state of the $\overline{OL}$ and $\overline{OH}$ pins.

2.9 Latch Enable Pin (LE)

The Latch Enable pin controls the data transfer from the input shift registers to the 128-bit latch and the $HV_{OUT}n$ channels.

When LE transitions from Low to High (rising edge), data is transferred from the 128-bit data latch to the $HV_{OUT}n$ output channels. When LE is Low, new data can be clocked into the shift registers.

2.10 Data Input/Output Pins (D1B, D2B, D3B, D4B)

Data Input/Output pins are configurable as inputs or outputs for the shift registers, depending on the state of the Direction pin (DIR).

When DIR is Low, pins D1B to D4B are configured as inputs to the data shift registers. When DIR is High, pins are configured as outputs of the data shift registers.

2.11 Output Low Pin ($\overline{OL}$)

The Output Low pin sets all high-voltage output channels ($HV_{OUT}0$ to $HV_{OUT}127$) to a Low-level state (P_{GND}).

When $\overline{OL}$ is set Low and OE is High, all the $HV_{OUT}n$ channels are forced to a Low-level state (P_{GND}), regardless of the data stored in the 128-bit latch.

2.12 Direction Pin (DIR)

The DIR pin controls the direction of the input data flow for the input registers, whether it is clockwise (DnB to DnA) or counter-clockwise (DnA to DnB).

When the DIR pin is set High, data flows from DnA to DnB. When DIR pin is set Low, data flows from DnB to DnA. See Table 1-6 for more information.

2.13 Clock Input Pin (CLK)

This is the Clock Input pin for 32-bit input shift registers.

2.14 Output High Pin ($\overline{OH}$)

The Output High pin sets all high-voltage output channels ($HV_{OUT}0$ to $HV_{OUT}127$) to a High-level state (V_{PP}).

When $\overline{OH}$ is Low while OE and $\overline{OL}$ are High, all the $HV_{OUT}n$ channels are forced to a High-level state (V_{PP}), regardless of the data stored in the 128-bit latch. See Table 1-4 for more information.

2.15 Reset Pin (RST)

The RST pin clears shift registers and the 128-bit latch data content when it is set High during the rising edge of the CLK and LE, respectively. See Table 1-5 for more information.

3.0 FUNCTIONAL DESCRIPTION

The HV583 is a unipolar, 128-channel, low-voltage serial to high-voltage parallel converter. The device consists of four parallel 32-bit shift registers, a 128-bit latch and 128 high-voltage outputs.

The four independent shift registers allow data to be updated into the 128-bit latch at four times the speed of a single register, providing a fast update rate for the 128 output channels. The 128-bit latch holds the data for the high-voltage output channels, whether it is a High-level or Low-level state. The flow of the input data can switch direction from clockwise (DnB to DnA) to counter-clockwise (DnA to DnB) by controlling the DIR pin. A reset pin (RST) is provided to clear the contents of the latches. All channels can be set at the same time to a high-impedance state (high Z), Low-level state, or High-level state through the OE, $\overline{OL}$ and $\overline{OH}$ pins, respectively.

The high-output voltages ($HV_{OUT}n$) can operate from 15V-80V with a maximum current source and sink capability of 30 mA.

3.1 Application Information

HV583 is designed for applications requiring multiple high-voltage outputs with current sinking and sourcing capabilities in the range of ±30 mA. Typical applications where the HV583 is utilized are in plasma displays, Inkjet printer drivers and 3D printer drivers.

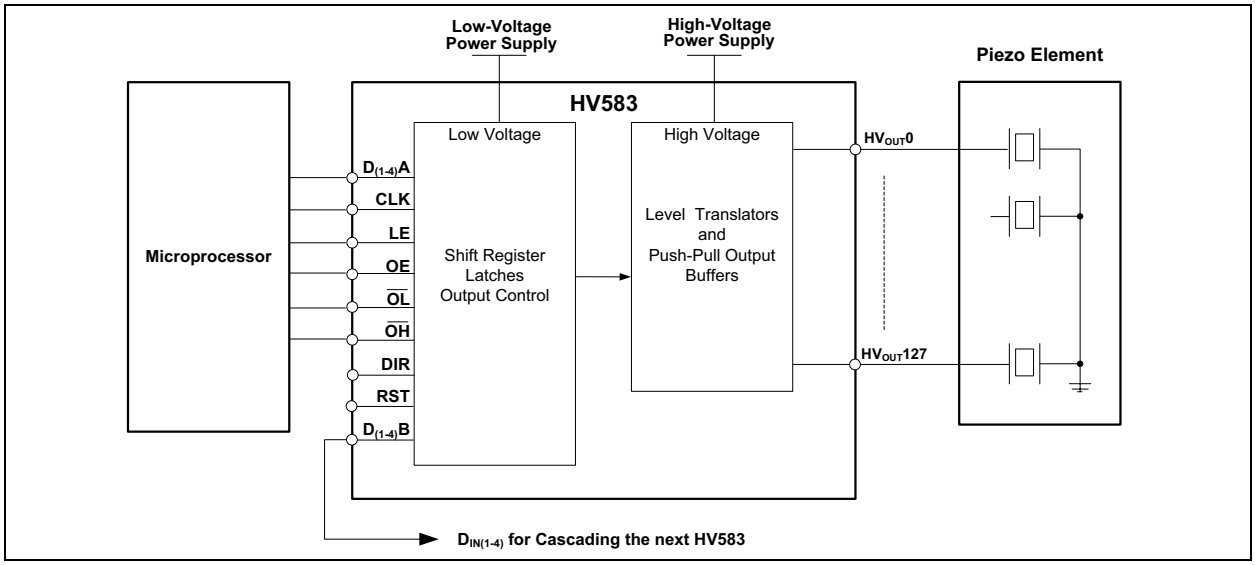
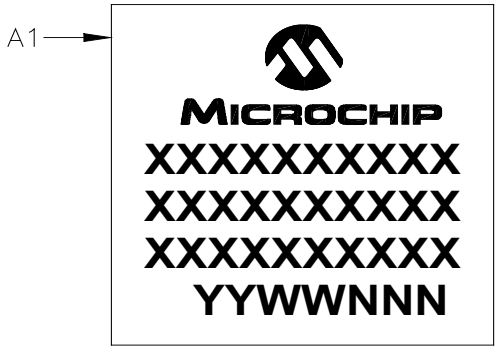


FIGURE 3-1: *Typical Application Block Diagram.*

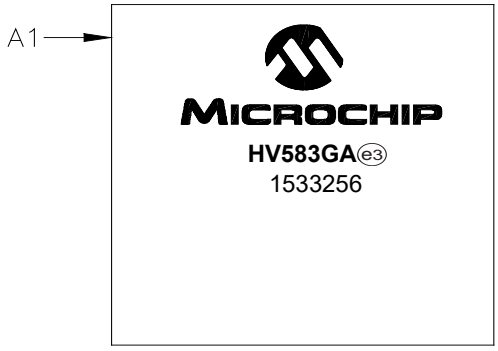
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

169-Ball TFBGA (10 x10 x1.1 mm)



Example

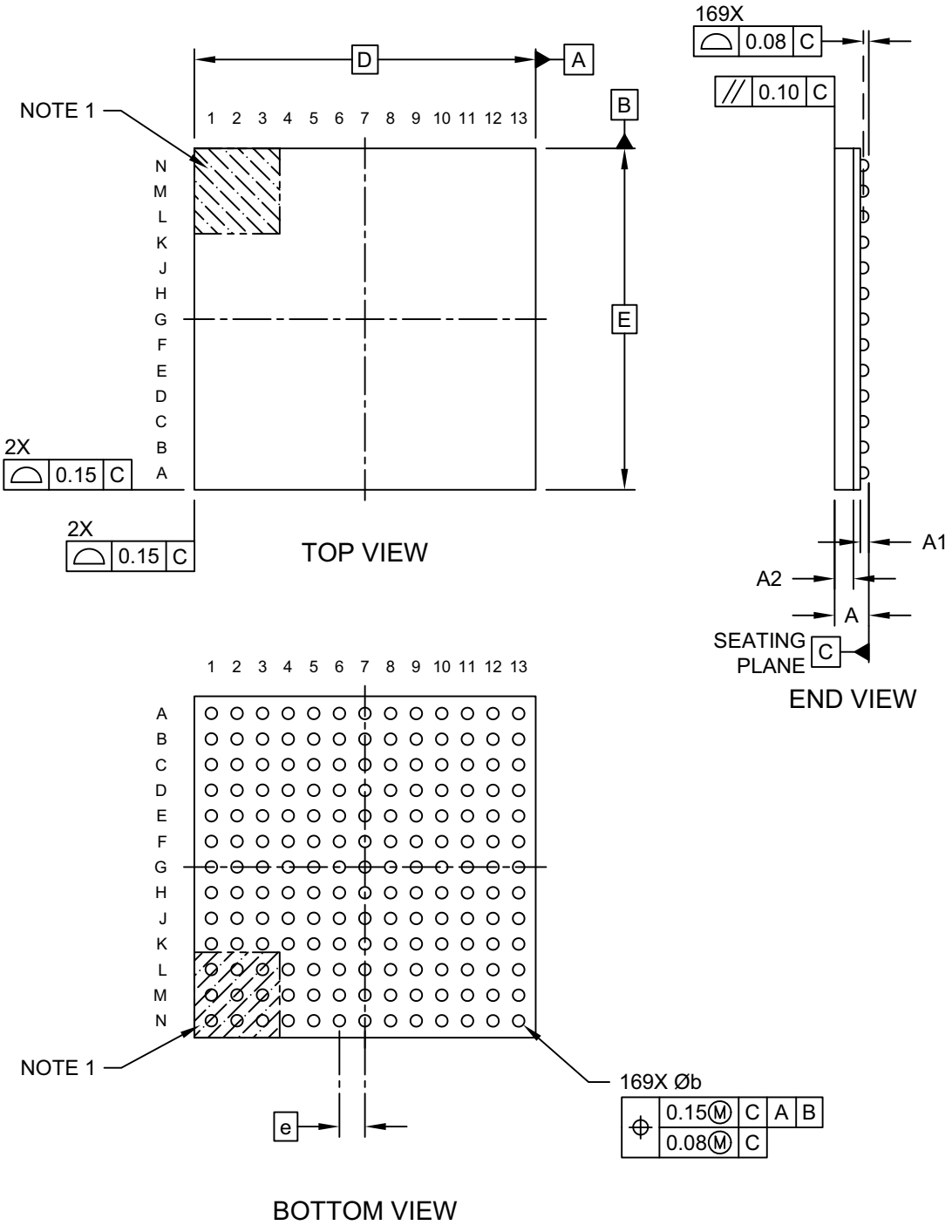


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

169-Ball Thin Fine Pitch Ball Grid Array (7G) - 10x10x1.10 mm Body [TFBGA] Alternate Terminal Assignments (does not comply with JEDEC recommendations)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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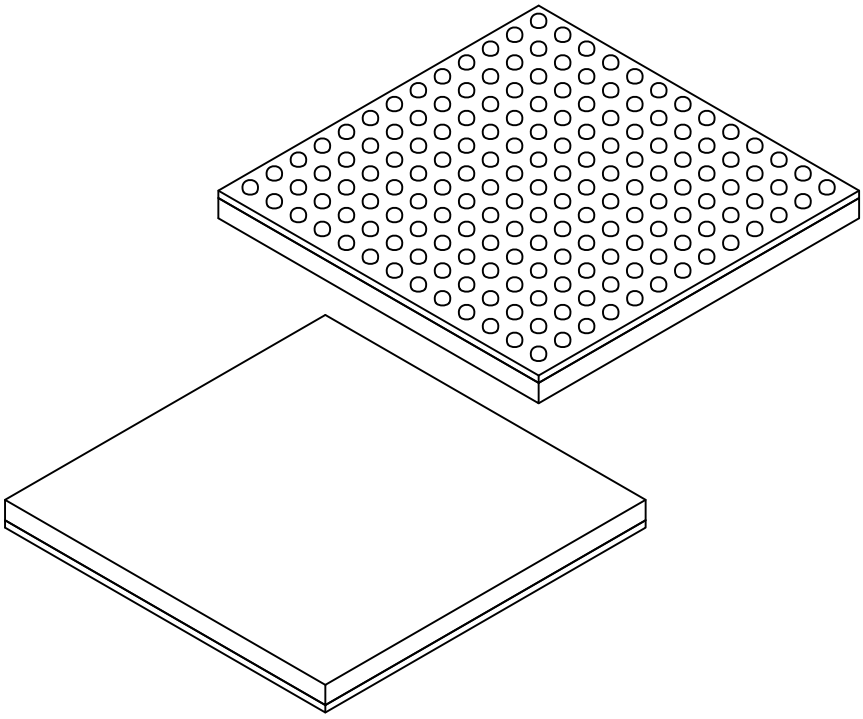
169-Ball Thin Fine Pitch Ball Grid Array (7G) - 10x10x1.10 mm Body [TFBGA] Alternate Terminal Assignments (does not comply with JEDEC recommendations)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		169	
Pitch	e		0.75 BSC	
Overall Height	A	–	–	1.10
Ball Height	A1	0.21	0.32	–
Mold Thickness	A2	0.40	0.45	0.50
Overall Length	D		10.00 BSC	
Overall Width	E		10.00 BSC	
Ball Diameter	b	0.35	0.40	0.45

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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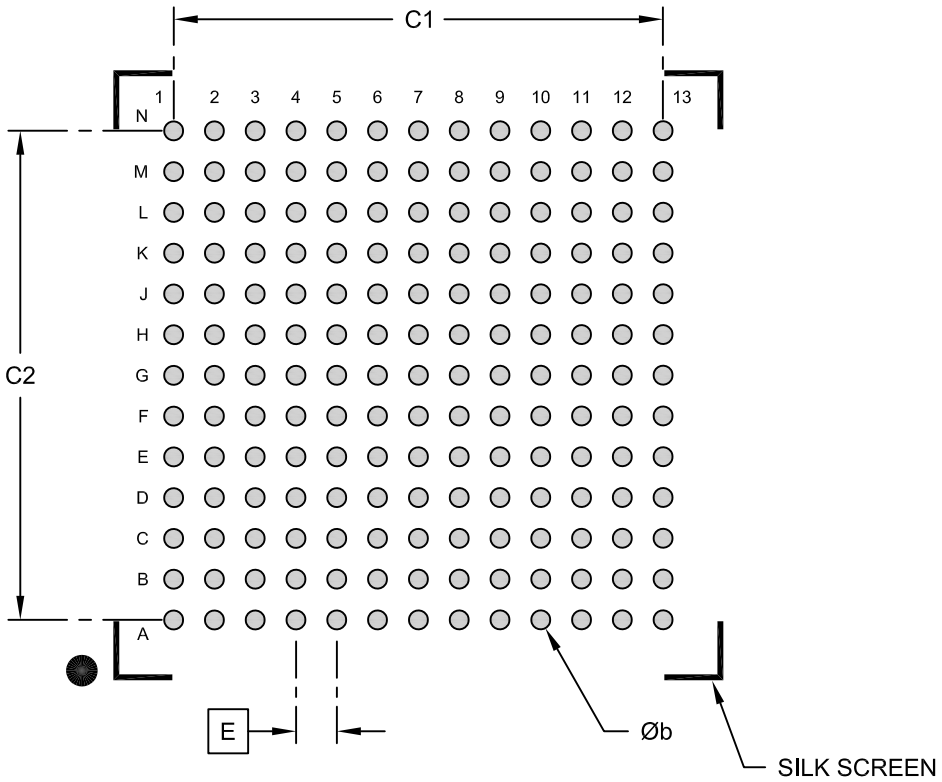
169-Ball Thin Fine Pitch Ball Grid Array (7G) - 10x10x1.10 mm Body [TFBGA] Alternate Terminal Assignments (does not comply with JEDEC recommendations)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.75 BSC	
Contact Pad Spacing	C1		9.00	
Contact Pad Spacing	C2		9.00	
Contact Pad Diameter (X169)	b		0.35	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2377-NJ Rev D

NOTES:

APPENDIX A: REVISION HISTORY

Revision C (September 2022)

- Updated DC Electrical Characteristics table.
- Updated **Section 4.0 "Packaging information"**.

Revision B (February 2017)

- Updated AC Electrical Characteristics table.
- Minor typographical corrections.

Revision A (December 2015)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX-X
Device	Package

Device:	HV583:	Low-Voltage Serial to High-Voltage Parallel Converter with HV Outputs
Package:	GA-G =	Thin Fine Pitch Ball Grid Array - 10 x 10 x 1.1 mm Body, 169-lead (TFBGA)

Examples:

a) HV583GA-G: 169-Ball 10x10 TFBGA package

NOTES:

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