EVB-LAN8814 Evaluation Board User's Guide

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Table of Contents

Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our website (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the Microchip EVB-LAN8814 Evaluation Board. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- The Microchip Website
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document features the EVB-LAN8814 Evaluation Board. The manual layout is as follows:

- **Chapter 1. "Overview"** – This section provides an overview of the evaluation board and a brief description of the board feature list.
- **Chapter 2. "Getting Started"** – This section provides details on how to download and cross-compile the EVB-LAN8814 software and load the custom Switchdev application into the board.
- **Chapter 3. "Hardware Features"** – This section shows the different connection types found on the evaluation board.
- **Chapter 4. "PTP4L Demonstration using the EVB"** - This section covers step-by-step setup instructions using the Calnex Paragon-X software.
- **Appendix A. "Schematics"** - This section shows the schematic drawings of the EVB-LAN8814 Evaluation Board.
- **Appendix B. "PCB Layers"**- This section shows the PCB layers of the EVB-LAN8814 Evaluation Board.
- **Appendix C. "Bill of Materials"** - This section shows the Bill of Materials for the EVB-LAN8814 Evaluation Board.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file.o`*`, where `*`file`*` can be any valid filename`
Square brackets [ ]	Optional arguments	`mcc18 [options] file [options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

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- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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The Development Systems product group categories are:

- **Compilers** – The latest information on Microchip C compilers, assemblers, linkers and other language tools. These include all MPLABCC compilers; all MPLAB assemblers (including MPASM™ assembler); all MPLAB linkers (including MPLINK™ object linker); and all MPLAB librarians (including MPLIB™ object librarian).
- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB® REAL ICE™ and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit™ 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows® Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are non-production development programmers such as PICSTART® Plus and PICkit™ 2 and 3.

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- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the website at:
http://www.microchip.com/support

DOCUMENT REVISION HISTORY

Revisions	Section/Figure/Entry	Correction
DS50003358B (10-27-22)	Figure 1-1 and Figure 1-2	Replaced evaluation board picture with images of the top and bottom sides.
	Chapter 4. "PTP4L Demonstration using the EVB"	Added a new chapter.
	Appendix A. "Schematics"	Added schematic diagrams.
	Appendix B. "PCB Layers"	Added images of the PCB layers.
	Appendix C. "Bill of Materials"	Added a list of Bill of Materials.
	All	Made minor edits and formatting changes.
DS50003358A (06-24-22)	Initial release	

Chapter 1. Overview

1.1 INTRODUCTION

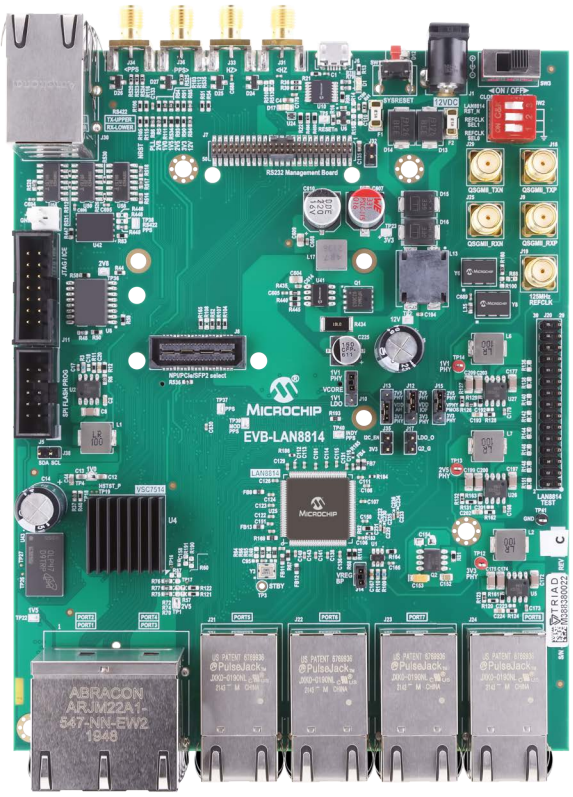
The EVB-LAN8814 Evaluation Board is used to evaluate the LAN8814 physical layer (PHY) device. The LAN8814 is a low-power, quad-port triple-speed (10BASE-T/100BASE-TX/1000BASE-T) Ethernet PHY transceiver. It supports industry-standard Quad Serial Gigabit Media Independent Interface (QSGMII) and Quad Universal Serial Gigabit Media Independent Interface (Q-USGMII), as well as high-accuracy timestamping functions to support IEEE-1588 solutions.

The EVB-LAN8814 allows users to gain understanding of the product, develop working proof-of-concepts using the LAN8814 hardware and software driver, and thus accelerating integration of the LAN8814 into their end-product.

1.1.1 Features

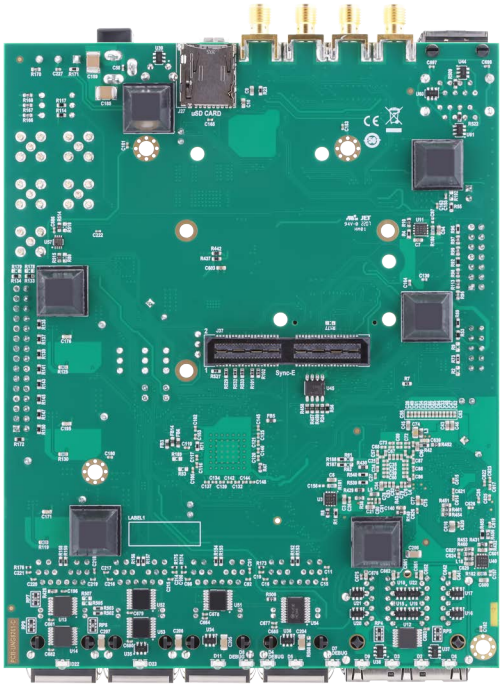
- Quad-port triple-speed (10BASE-T/100BASE-TX/1000BASE-T) Ethernet PHY transceiver ports available through LAN8814
- Four VSC7514XKS integrated triple-speed Ethernet ports for general test traffic flow as well as board image netbooting
- PTP timestamping-in-the-PHY — LAN8814 Linux® driver can support Linux PTP (ptp4l) application
- Voltage-mode Integrated Connector Magnetic (ICM) footprint-compatible with Pulse JXK0 devices (JXK0-0136NL, JXK0-0190NL, etc.)
- Interrupt-capable MDIO management of LAN8814 to the VSC7514XKS host
- On-chip regulation for LAN8814 1V1 power supported
- Clock-source selection options for LAN8814
- Direct-connect RS-232 management interface via USB2 UART interface

FIGURE 1-1: EVB-LAN8814 EVALUATION BOARD (TOP SIDE)



Note: Production board revision label is marked "C1."

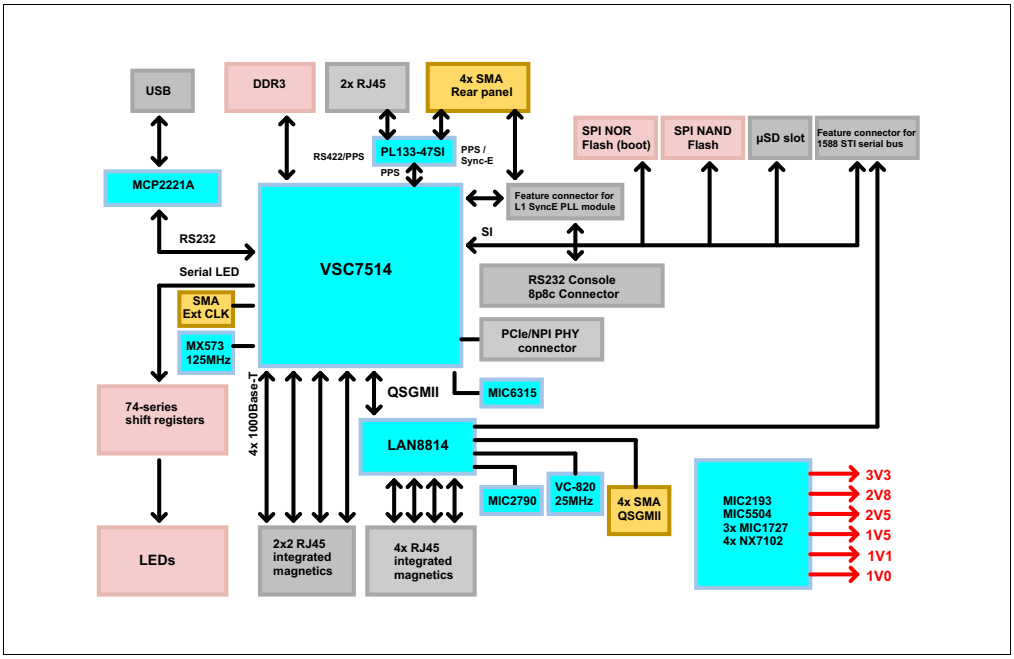
FIGURE 1-2: EVB-LAN8814 EVALUATION BOARD (BOTTOM SIDE)



Note: Sync-E connector (J37) is unsupported.

1.1.2 Block Diagram

FIGURE 1-3: EVB-LAN8814 BLOCK DIAGRAM



1.1.3 References

Concepts and materials available in the following documents may be helpful when reading this document. Visit www.microchip.com for the latest documentation.

- *LAN8814 Data Sheet* (www.microchip.com/LAN8814)
- *LAN8814 Silicon Errata and Data Sheet Clarifications* (www.microchip.com/en-us/product/LAN8814)

1.1.4 Terms and Abbreviations

The following are the terms and abbreviations used in this document:

- ARP – Address Resolution Protocol
- COM – Communications Port
- DHCP – Dynamic Host Configuration Protocol
- DIP – Dual In-line Package
- DSUB – D-Subminiature
- EP – Extended Page
- GPIO – General Purpose Input/Output
- ICM – Integrated Connector Magnetic
- IEEE – Institute of Electrical and Electronics Engineers
- I/O – Input/Output
- IP – Internet Protocol
- LAN – Local Area Network
- LSB – Least Significant Byte/Bit
- MAC – Media Access Controller
- MDIO – Management/Data Input/Output
- MII – Media Independent Interface

- NIC – Network Interface Card
- OUI – Organizationally Unique Identifier
- PC – Personal Computer
- PCB – Printed Circuit Board
- PCS – Physical Coding Sublayer
- PHY – Physical Layer Transceiver
- PDU – Payload Data Unit
- PN – Part Number
- QSGMII – Quad Serial Gigabit Media Independent Interface
- Q-USGMII – Quad Universal Serial Gigabit Media Independent Interface
- SMA – Sub-Miniature version A
- TCXO – Temperature-Compensated Crystal Oscillator
- TFTP – Trivial File Transfer Protocol
- UART – Universal Asynchronous Receiver/Transmitter
- USB – Universal Serial Bus
- VDFN – Very-small Dual Flat, No Leads
- VM – Virtual Machine
- VREG – Voltage regulator
- XO – Crystal oscillator

Chapter 2. Getting Started

2.1 INTRODUCTION

This section describes how to download the EVB-LAN8814 software, cross-compile it, and load the custom Linux® Switchdev application into the evaluation board. The Switchdev software running inside the on-board VSC7514XKS chip configures and controls the LAN8814 PHY via the Microchip LAN8814/8804 Linux driver.

2.1.1 Kit Contents

The EVB-LAN8814 kit includes only the evaluation board itself.

Note: For basic operations, the end-user must provide:
- Type-A to micro USB 2.0 cable
- 12 VDC power supply (≥ 2A current capability, 5.5 mm OD x 2.5 mm ID plug)

2.1.2 Tools for EVB-LAN8814 Setup

2.1.2.1 SOFTWARE COMPILATION

Note: Where any platform-particular commands are specified, note that the following steps were carried out on an Ubuntu®-based host PC environment. Please adapt the instructions to your own PC environment. Otherwise, install and set up a VM with Ubuntu guest to follow the instructions exactly as given below.

1. Download the Linux kernel source code and prepare the development system.
   a) Clone from the github mirror mainline distribution, located at https://github.com/torvalds/linux.

Example command:

```
$ git clone https://github.com/torvalds/linux mainline
```

   b) Roll back to the kernel version containing the latest Ocelot driver compatible with this board. Commit hash begins with *46efe4efb9*.

Example commands:

```
$ cd mainline
$ git checkout 46efe4efb9
```

c) Clone the Microchip UNG cross-compiler toolchain suitable for the Ocelot CPU on the board, from the cloud provided located at http://mscc-ent-open-source.s3-eu-west-1.amazonaws.com/public_root/toolchain/mscc-toolchain-bin-2021.02-094.tar.gz.

Example commands:

```
$ sudo mkdir /opt/mscc
$ cd /opt/mscc
$ sudo wget http://mscc-ent-open-source.s3-eu-west-1.amazonaws.com/public_root/toolchain/mscc-toolchain-bin-2021.02-094.tar.gz
$ sudo gunzip *.gz
$ sudo tar -xvf *.tar
```

2. Download the EVB-LAN8814 reference design software.

   The EVB-LAN8814 reference design software is bundled in a `.zip` archive located at the LAN8814 product page.

3. Unpack the overlay developer archive, *including the latest compatible micrel.c driver*, into your local build folder as in the following (example root folder is named 'mainline').

```
$ cd mainline
$ cp <source folder>/evb-lan8814.tar.gz .
$ gunzip evb-lan8814.tar.gz
$ tar -xvf evb-lan8814.tar
```

4. Update the CROSS_COMPILE env variable inside the compilation script `make-env.sh` to the path location of the cross-compiler downloaded in step 1.
5. Overwrite the default Kconfig to set up the kernel compilation properly, and then compile the kernel:

```
$ cp ocelot_indy_defconfig .config
$ ./make-env.sh
```

Note: Any desired customization to the kernel image should manually be written into `.config` prior to executing `make-env.sh` above.
Example: See **Section 2.1.7.2 "Enabling Logging"**.
Once compilation begins, answer default (press the <Enter> key) for any kernel configuration questions prompted by the Kconfig process.

2.1.2.2 PREPARING HOST PC AND TOOLS FOR DOWNLOADING THE COMPILED EXECUTABLE ONTO THE EVB

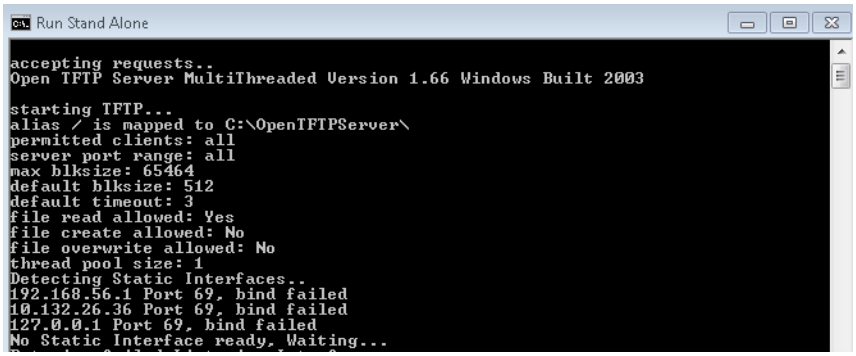
The fastest method for loading software into the EVB-LAN8814 is through the U-Boot bootloader installed on the Flash memory of the EVB-LAN8814. U-Boot has a DHCP client capable of TFTP-loading a kernel image over a local area network.

To load a software image via U-Boot, a TFTP server is required as is a DHCP on the local area network. Since most routers and corporate networks already provide DHCP services for assigning IP addresses, only installation of a TFTP server is covered in this document.

A good, freely-available TFTP server for Windows® PCs is Open TFTP Server, which is used in the following example.

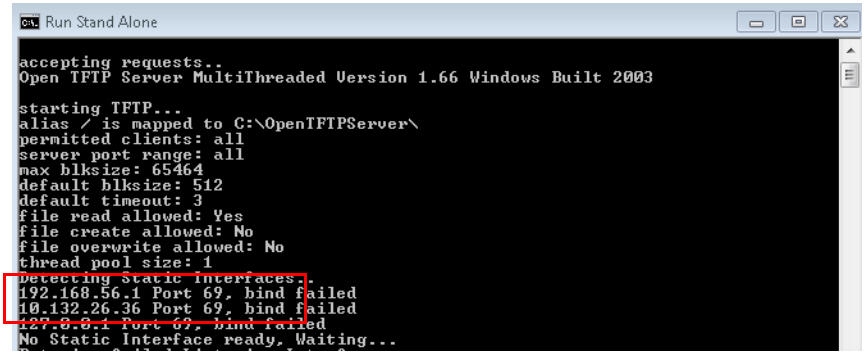
1. Install a TFTP server (`.msi` installer package).
2. Start the TFTP server with default settings ("Run Stand Alone" in Windows® Start menu), and confirm the root directory of the TFTP server. The default is usually `C:\OpenTFTPServer\` as in Figure 2-1.

FIGURE 2-1: STARTING TFTP SERVER



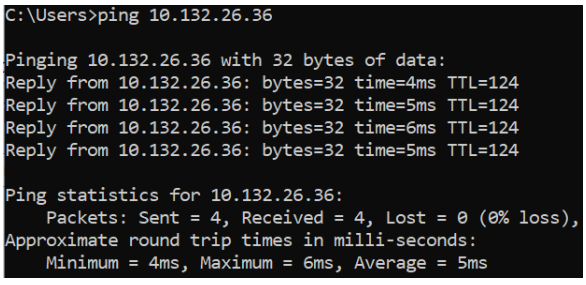
3. Confirm if the TFTP server detects the IP address of the host PC network interface. In this example, the Windows PC running Open TFTP Server uses NIC with IP address 10.132.26.36 in Figure 2-2.

FIGURE 2-2: TFTP SERVER DETECTING HOST IP ADDRESS



4. Confirm if the Open TFTP Server host PC has a NIC port reachable from your development system shown in Figure 2-3.

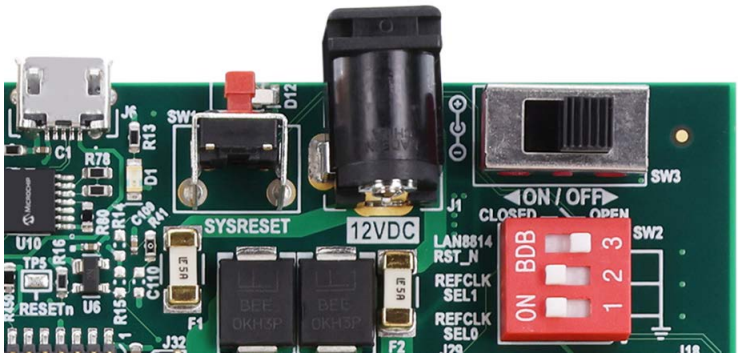
FIGURE 2-3: PING TFTP SERVER FROM NIC



2.1.3 Connecting the Power Supply

The DC input connector is placed to the right on the back, when looking at the board from the side. The switch SW3 is recommended to remain in the OFF position, while connecting (or disconnecting) the DC input connector to 12 VDC. See Figure 2-4 with both switch and barrel jack below.

FIGURE 2-4: EVB-LAN8814 DC INPUT CONNECTION



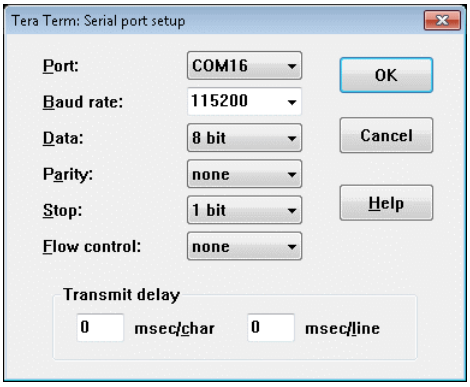
The board uses approximately 500 mA, when not programmed or in Reset state. A programmed board uses a peak of approximately 750 mA during boot-up, when no RJ45 ports are connected and no add-on boards are attached to the main board. If a programmable bench supply is used, an *Imax* setting of 1.25A is recommended.

2.1.4 Connecting the Board to the PC (Via USB2UART)

The J6 connector (shown in Figure 2-4) is recommended for establishing a console connection with the host switch on the board. A commonly available Type-A to micro-USB 2.0 cable should be used to connect J6 to a host PC.

The serial port settings for the PC terminal is shown in Figure 2-5.

FIGURE 2-5: EVB-LAN8814 SERIAL PORT SETUP



Note: For reliable serial communications between the host PC and the board, J6 should be connected to a host PC before powering on the board.

Note: It is recommended to not use any protocol converters (for example, Thunderbolt-USB) between the desktop PC's USB port and the board's J6 connector, as erratic console behavior may result.

2.1.5 Booting the Board

2.1.5.1 CONFIGURING THE U-BOOT LOADER

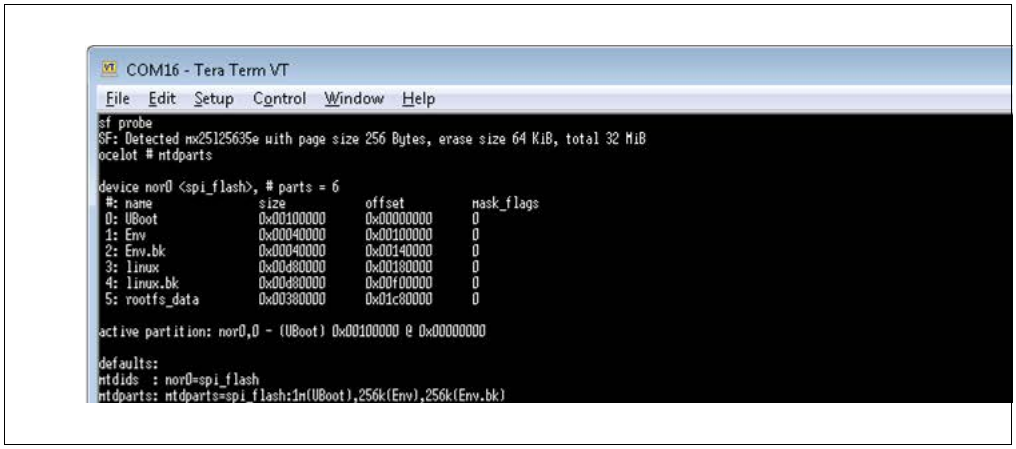
After establishing a serial console via the J6 interface and powering on the EVB-LAN8814, a U-Boot first-stage bootloader executes.

U-Boot auto-boot should be stopped. Press the keyboard space bar before auto-boot counter reaches 0.

Note: Wait for the U-Boot console output by the VSC7514XKS chip:
`ocelot #`

Figure 2-6 shows an example U-Boot command `mtdparts` examining the file system of the NOR Flash memory of EVB-LAN8814.

FIGURE 2-6: U-BOOT COMMAND PROMPT



Note: If for any reason the ocelot # prompt does not appear, the board can be reset by pressing the SYSRESET push-button switch SW1 (refer to Figure 2-4). After releasing the push-button, reset takes 2-3 seconds to complete.

2.1.5.2 STARTING LINUX®

TFTP-loading a kernel image over a local area network is strongly recommended to avoid delays while writing the on-board NOR Flash memory, as well as to avoid inadvertently erasing the U-Boot bootloader that resides on it.

In order to perform TFTP boot, the EVB-LAN8814 first needs to be connected to an appropriate TFTP server over a LAN.

Note: Valid ports for TFTP boot are front-panel ports 1-4 (that is, any Ethernet port on the 2x2 RJ45 ICM).

To TFTP-load a binary image, follow these steps:

1. Run the following commands:

   `setenv serverip <your TFTP server IP – example below is 10.132.26.24>`

   `dhcp ${serverip}:<path/to/your/kernelimage/>`

   `vmlinux.gz.itb` (example in the figure below has path in the hhicks/ folder that is located at absolute path C:\OpenTFTP\hhicks\ on the TFTP server Windows PC)

   `bootm #conf-ocelot_pcb123_elise`

2. The username is `root`.
3. The password is blank (press the <Enter> key).
4. The Linux rootshell is prompted ('#').
5. Typical e-Linux shell commands are available for interacting with the switch's file system and Linux resources.

See Figure 2-7 and Figure 2-8 for examples of kernel output booting.

FIGURE 2-7: KERNEL OUTPUT BOOTING TFTP LOADER

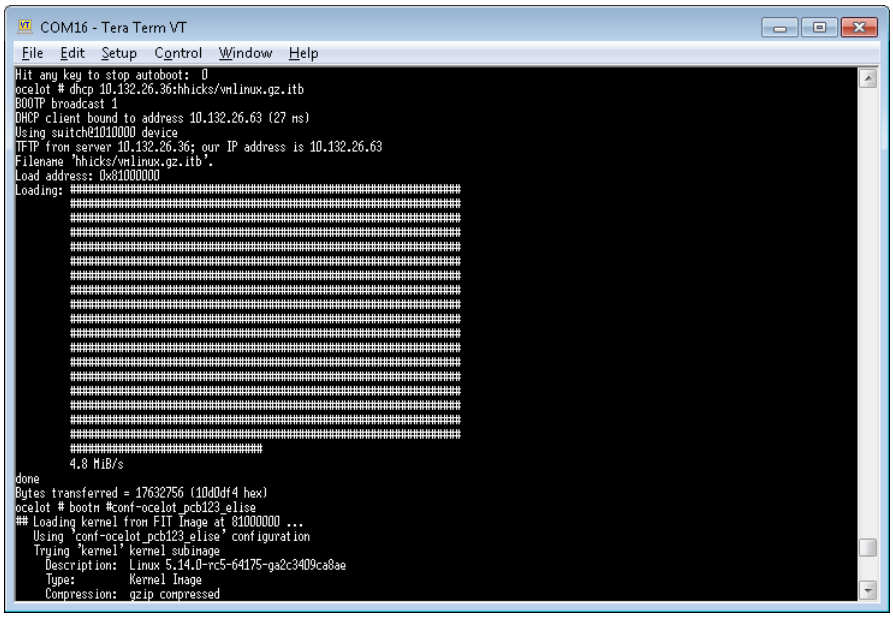
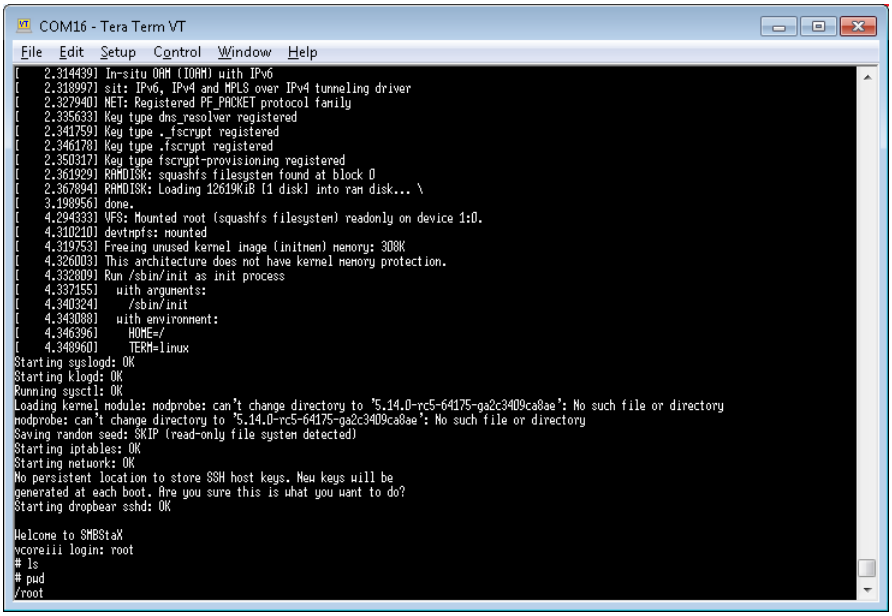


FIGURE 2-8: KERNEL OUTPUT LOGIN PROMPT



2.1.5.3 FAMILIARIZING WITH SWITCHDEV KERNEL

Users familiar with Linux will already be familiar with the shell interface at system login. The Switchdev kernel allows Linux networking tools to be used on the switch and PHY hardware by off-loading network operations to the switch and PHY chips as much as possible.

The ports of the board are represented within the kernel file system at `/sys/class/net/` directory tree. However, general access and configuration of each Ethernet port are done through the existing networking tools, which Linux already provides (examples are ip, ethtool, bridge, and so on).

Note: Use the Linux user-space tools to configure the Ethernet ports by following examples of common configurations below.

2.1.5.4 IMPORTANT NETWORKING TOOLS (IPROUTE2, ETHTOOL, AND PORT MAPPING TO NETWORK DEVICES)

Linux has powerful networking tools available for managing network ports, which can be utilized to test and operate the LAN8814 ports on EVB-LAN8814. These tools include the following:

- *Iproute* includes the set of *ip* commands for configuring traffic routes through the LAN8814 physical interfaces.
- *Ethtool* manages Layer-1 properties of LAN8814, such as speed an auto-negotiation.
- *Phytool* provides access to the MII management register set of LAN8814.
- *Phydev_dbg()* macros provide debug loglevel messaging, output to file, and are available for post-processing in LAN8814 driver development. These macros can be added to LAN8814 driver source code.
- Easy-frame test tool is meant for generating user-defined test frames.

2.1.6 Interface Reconfiguration

2.1.6.1 EXAMPLE USING IPROUTE2 TO CONFIGURE THE PORTS

```
ip link set dev eth4 up
ip link set dev eth5 up
```

After running the commands above, both LAN8814 front-panel port J21 (eth4) and front-panel port J22 (eth5) are logically activated and can exchange traffic with an established media link-partner.

2.1.6.2 EXAMPLE USING ETHTOOL TO CONFIGURE MEDIA PARTICULARS (SPEED, DUPLEX)

To change the speeds of any LAN8814 port, adjust the auto-negotiation advertisements of a particular ethX port using ethtool. The following is an example of changing the speed advertisement for LAN8814 eth4 port:

```
ethtool -s eth4 speed 100 duplex full autoneg on # change to 100Mbps fdx
ethtool -s eth4 speed 10 duplex full autoneg on # change to 10Mbps fdx
```

2.1.6.3 EXAMPLE OF BRIDGING MULTIPLE PORTS TO SWITCH UNFILTERED TRAFFIC PORT-TO-PORT

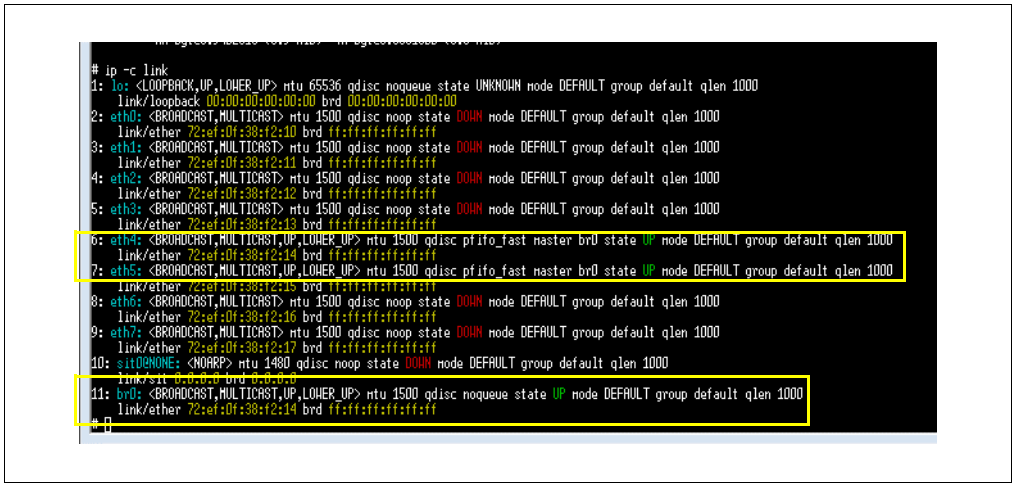
```
ip link add name br0 type bridge
ip link set dev eth4 master br0
ip link set dev eth5 master br0
ip link set dev br0 up
```

After running the commands above, both LAN8814 front-panel port J21 and front-panel port J22 are configured properly to switch Ethernet traffic via the VSC7514XKS host switch.

The link and bridge status can be checked using iproute2 again as shown in Figure 2-9.

```
ip -c link
```

FIGURE 2-9: CHECKING LINK AND BRIDGE STATUS VIA IPROUTE2



2.1.7 Useful Test Features

2.1.7.1 TEST TRAFFIC GENERATOR

A useful tool for sourcing user-defined test traffic on the EVB-LAN8814 is the Linux easy frame (ef) tool. For example, to transmit 100 frames with 1025 payload bytes from the LAN8814 front-panel port J21 (eth4):

```
# ef tx eth4 repeat 100 eth smac ::1 dmac ::2 arp data repeat
1025 0x12
```

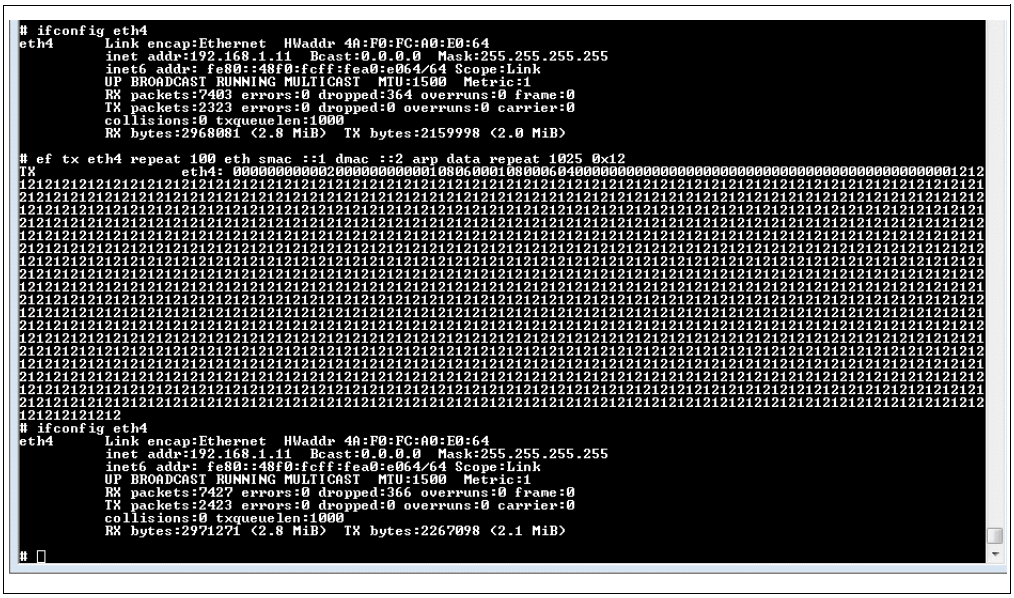
The *ef tx* arguments above are as follows:

- *eth4* is the physical Ethernet port.
- The first *repeat* argument is for a count of 100 frames.
- Ethernet Layer2 arguments *smac* and *dmac* ignore (zero-pad) the first five bytes, and fill the LSB of the Layer 2 address fields with the arguments above.
- Test frame EtherType will be of ARP protocol (0x0806) PDU.
- Frame PDU will be padded with 1025 Bytes of user-defined data 0x12.

Note: The test frame above is intended for incrementing Layer2 frame debug counters (such as those reported by 'ifconfig') but is not a valid ARP frame for use on a production network. In other words, all optional ARP header fields undefined will be ignored (zero-pad), and thus the test traffic will not be valid for ARP protocol operations.

Figure 2-10 shows the Layer-2 counters from the MAC corresponding to eth4, before and after running the ef tool to generate 100 frames with a 1025 Bytes payload:

FIGURE 2-10: USING MAC COUNTERS USING EF TOOL



2.1.7.2 ENABLING LOGGING

The default loglevel passed to the Linux kernel via U-Boot is loglevel = 9. That is the maximum console level debug and will capture any phydev_dbg() macro outputs scattered throughout the LAN8814 driver code for debug messages.

Note: For kernel device debug to work, your kernel must be compiled with CONFIG_DYNAMIC_DEBUG = y in the `.config`.

However, the loglevel can be dynamically reduced at run time (for example, eliminate console clutter for a targeted part of PHY driver execution) via shell:

```
# echo "6" > /proc/sys/kernel/printk
```

2.1.7.3 DIRECT REGISTER INSPECTION OF LAN8814

The phytool can access the MII management register set of LAN8814 over the MDIO bus, as follows:

Note:	The phytool MDIO register access requires that the corresponding network interface is started for LAN8814. eth4, eth5, eth6, and eth7 are the interface names for the four physical ports of the LAN8814 quad-PHY.

Note:	Running 'ifconfig' prior to using phytool can confirm which network interface ports are started (if any) within Linux.

2.1.7.3.1 LAN8814 Register Read Example

The format of phytool arguments is IFACE/ADDR/REG.

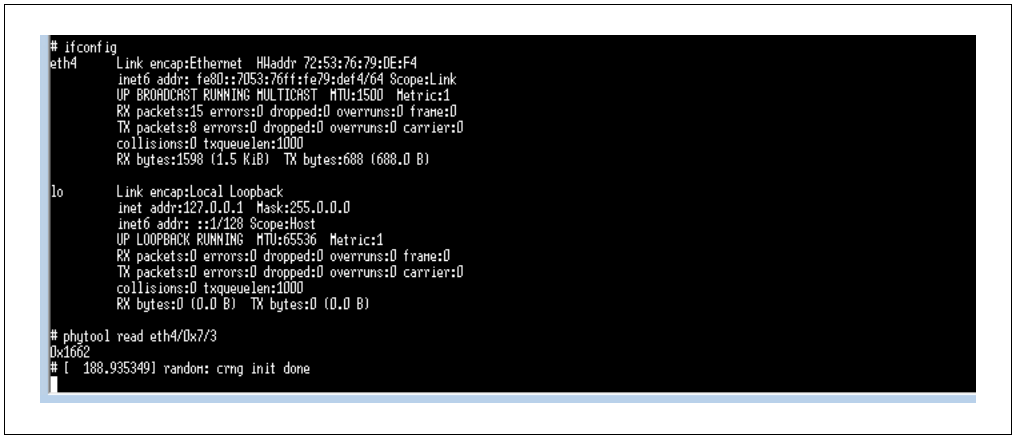
ADDR corresponds to the physical MDIO address. The EVB-LAN8814 by default as-shipped uses PHY base address 0x7.

Note:	IFACE and ADDR always increment in a 1:1 mapping (eth4/0x7, eth5/0x8, eth6/0x9, eth7/0xA) for the four LAN8814 ports.

Figure 2-11 shows an example of inspecting the Model and Revision numbers of the LAN8814 chip via the Device Identifier 2 standard register located at direct register address 3h:

```
# phytool read eth4/0x7/3
```

FIGURE 2-11: INSPECTING DEVICE ID2 REGISTER OF LAN8814



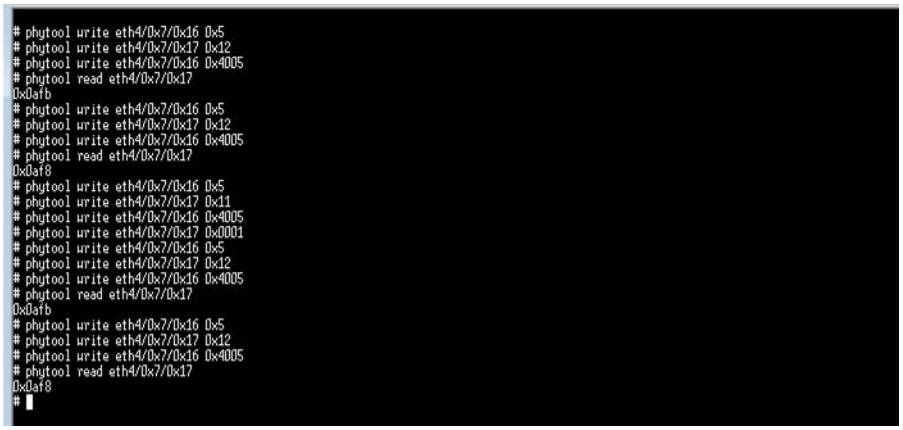
Return value 0x1662 is the OUI and silicon revision information for the LAN8814 revision C chip.

2.1.7.3.2 LAN8814 Register Read-Modify-Write Example

This example shows how to monitor QSGMII PCS status and restart the QSGMII PCS on the host-side interface. It is a useful example for the purpose of replicating hardware operations on the EVB-LAN8814, which might be used in an end-customer design using the LAN8814.

```
1 # phytool write eth4/0x7/0x16 0x5
2 # phytool write eth4/0x7/0x17 0x12
3 # phytool write eth4/0x7/0x16 0x4005
4 # phytool read eth4/0x7/0x17
5 # phytool write eth4/0x7/0x16 0x5
6 # phytool write eth4/0x7/0x17 0x12
7 # phytool write eth4/0x7/0x16 0x4005
8 # phytool read eth4/0x7/0x17
9 # phytool write eth4/0x7/0x16 0x5
10 # phytool write eth4/0x7/0x17 0x11
11 # phytool write eth4/0x7/0x16 0x4005
12 # phytool write eth4/0x7/0x17 0x0001
13 # phytool write eth4/0x7/0x16 0x5
14 # phytool write eth4/0x7/0x17 0x12
15 # phytool write eth4/0x7/0x16 0x4005
16 # phytool read eth4/0x7/0x17
```

FIGURE 2-12: LAN8814 REGISTER READ-MODIFY-WRITE EXAMPLE



As per the “GPHY” register specification for LAN8814, the Extended Page Registers of LAN8814 are accessed through the EP Access Control and EP Address/Data portal registers:

```
1 # phytool write eth4/0x7/0x16 0x5
2 # phytool write eth4/0x7/0x17 0x12
3 # phytool write eth4/0x7/0x16 0x4005
4 # phytool read eth4/0x7/0x17
5 # phytool write eth4/0x7/0x16 0x5
6 # phytool write eth4/0x7/0x17 0x12
```

```
7 # phytool write eth4/0x7/0x16 0x4005
8 # phytool read eth4/0x7/0x17
9 # phytool write eth4/0x7/0x16 0x5
10 # phytool write eth4/0x7/0x17 0x11
11 # phytool write eth4/0x7/0x16 0x4005
12 # phytool write eth4/0x7/0x17 0x0001
13 # phytool write eth4/0x7/0x16 0x5
14 # phytool write eth4/0x7/0x17 0x12
```

- Command 1 sets up the EP "page" 5.
- Command 2 sets the register address to 18.
- Command 3 sets up the data phase of read transaction for EP "page" 5.
- Command 4 reads back the data value indirectly latched from EP5 register 18.
- Commands 5-8 repeat the read of EP5, register 18 again.
- Command 9 sets up the EP "page" 5 for the write portion of transaction.
- Command 10 sets up the register address to 17.
- Command 11 sets up the data phase of write transaction for EP "page" 5.
- Command 12 writes-through the data value 0x1 indirectly, into EP5 register 19.
- Commands 13-16 repeat the read of EP5, register 18 again.

The initial read transaction (commands 1-4) performed an initial check of the QSGMII "PCS1G" configuration and status register, while commands 5-8 flushed that register's Self-Clear bits.

The Soft-Reset bit of the QSGMII PCS1G located at EP5.17 bit 0 was asserted. (It is Self-Clearing hence no need to write the bit again with a 0 value.)

A final recheck of the QSGMII "PCS1G" configuration and status register shows the link and synchronization status bits toggled, as a consequence of resetting the QSGMII PCS1G block. Trailing commands appearing in the terminal window in Figure 2-12 confirmed that those status bits return to a stable state as expected.

Chapter 3. Hardware Features

3.1 STRAPPING SETTINGS FOR LAN8814 PHY

3.1.1 LAN8814 PHY Reference Clock Selection

To configure the LAN8814 PHY clocking option for on-board crystal oscillator, set the SW2 "REFCLK_SEL1" and "REFCLK_SEL0" DIP switches to the ON/closed/left-handed position. See Figure 3-1.

FIGURE 3-1: CONFIGURING LAN8814 PHY CLOCKING OPTIONS

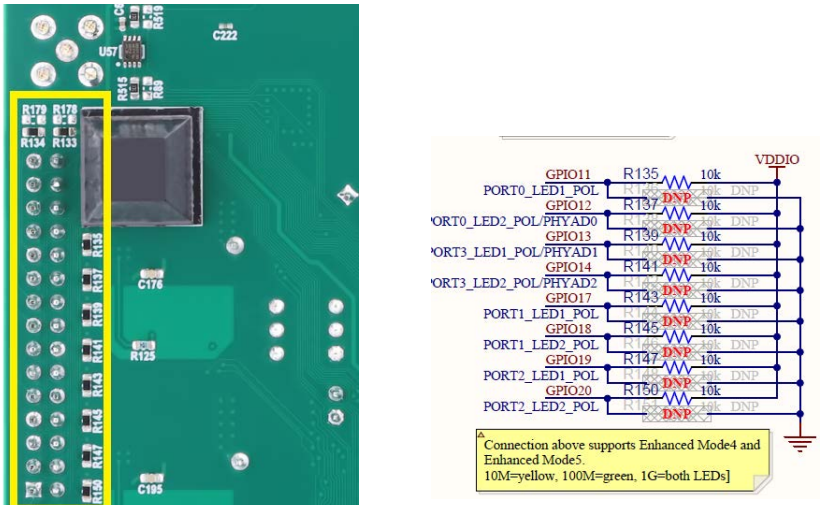
Note: Ensure that the LAN8814 PHY LAN8814_RST_N (top) switch of the SW2 DIP remains OFF/open/right-handed position during functional operation of the PHY.

3.1.2 LAN8814 MDIO Address Selection

The LAN8814 is assigned a unique PHY base address by the PHYAD[4:0] strapping pins for its MDIO interface.

On the EVB-LAN8814, the PHYAD[4:0] pin-strap settings are installed via a resistor "tree," which is located on the underside of the PCB. See Figure 3-2.

FIGURE 3-2: EVB-LAN8814 PHYAD[4:0] STRAPPING PINS



Note: Modifying the PHY base address strapping, corresponding to LAN8814 PHYAD[4:0] strapping pins, requires a corresponding update in the Linux device tree of the bootable Switchdev image for the application to communicate with the LAN8814 PHY. The EVB-LAN8814 is shipped with a PHY base address of 0x7.

3.2 BOARD CONFIGURATION PRECAUTIONS

CAUTION

Pay extra caution in the following board configurations. Otherwise, these may result in board damage or an erroneous behavior.

3.2.1 Bypassing SerDes Regulator while Powering VDDAH with 3V3

The SerDes circuit internal to the LAN8814 chip requires a 2.5V supply. Feeding it 2.5V is done in either of the following:

- Supplying 3.3V to VDDAH and enabling a step-down VREG internal to the LAN8814 chip to generate 2.5V from VDDAH
- Passing a 2.5V VDDAH directly and disabling the internal VREG by pulling LAN8814 VREG_BYPASS pin high (to VDDIO)

Use caution when removing the VREG_BYPASS jumper (J14). *Never leave the VREG_BYPASS jumper uninstalled when the VDDAH on-board jumper located at J13 is positioned for a 3V3 supply.* Doing so will result in overvoltage of the on-chip SerDes circuit.

3.2.2 Changing VDDIO to 3V3 when Interfacing with Other On-Board ICs

LAN8814 powers its digital I/O drivers via the VDDIO on-board jumper, J12. Normally, J12 is positioned for the 2V5 supply as the digital I/O of the LAN8814 interface with the 2.5V I/O on the VSC7514XKS chip.

Pay careful attention when positioning J12 LAN8814 VDDIO to 3V3, because the board has not been tested to guarantee reliable operation of the MDIO bus in this situation. The station manager, VSC7514XKS, digital I/O drive is limited to 2.5V.

3.2.3 Reflashing the On-board Flash Memory

It is important to note when reflashing of the on-board Flash memory is needed and how to do it safely.

3.2.3.1 EXAMINING THE NOR PARTITION TABLE

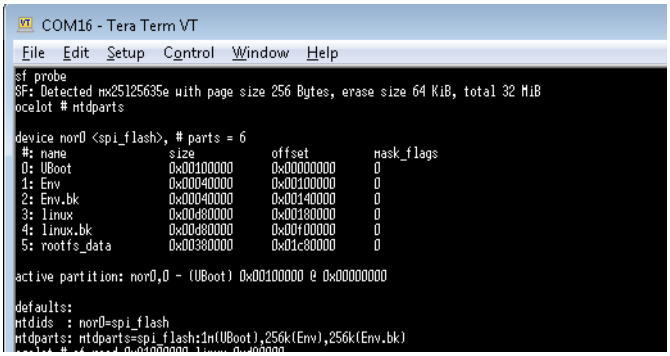
When first booting the board, U-Boot auto-boot should be stopped (press the keyboard space bar before the auto-boot counter reaches 0).

Once the U-Boot console prompt appears:

```
ocelot #
```

Type `mtdparts` to examine the NOR Flash memory file system of the EVB-LAN8814. See Figure 3-3.

FIGURE 3-3: MTDPARTS TO EXAMINE THE NOR FLASH MEMORY FILE SYSTEM



The U-Boot partition (numbered 0) is essential for board boot-up.

The primary application partition is number 3, labeled as ‘linux’. This is the recommended partition to overwrite (if required) to persistently store a newly-compiled image on the board.

Note: Never reflash partition 0 unless you understand the risks involved with overwriting the bootloader of the evaluation board, and have taken appropriate counter measures to avoid such an outcome.

3.2.3.2 REFLASHING THE LINUX® PARTITION

Note: This procedure utilizes the DHCP/TFTP protocol boot of the U-Boot (that is, over a network). Ensure that a LAN connection is available to the EVB-LAN8814 that has both a DHCP service as well as tftpd service.

Note: This reflash procedure is only recommended for prepping the EVB-LAN8814 ahead of usage in environments without a LAN network. In any developer situation with LAN access to the EVB-LAN8814, DCHP/TFTP netbooting is a faster and safer method for booting the board.

To reflash the 'linux' partition, perform the following from the U-Boot console:

```
ocelot # mtdparts
ocelot #
setenv linux_size '0xd80000'
ocelot # setenv serverip <your TFTP server IP www.xxx.yyy.zzz>
ocelot #
dhcp ${loadaddr} ${serverip}: <path/to/your/kernelimage/
vmlinux.gz.itb>
ocelot #
sf update ${loadaddr} linux ${linux_size}
```

Note: The `linux_size` (in yellow text above) should be set to the 'linux' partition size reported by mtdparts. It could change from size 0xd80000 shown above.

3.2.4 Confirming U-Boot Partition Remains Intact

Reset the U-Boot application as follows:

```
ocelot # reset
```

The EVB-LAN8814 should now execute a full self-reset and restart U-Boot.

Note: The NAND Flash memory located at U42 on the EVB-LAN8814 currently lacks software support. All embedded firmware files are stored in the NOR Flash U8.

3.3 RESETTING THE LAN8814 PHY CHIP

Use the LAN8814 (top) switch of the SW2 DIP to hardware-reset *only* the LAN8814 chip.

FIGURE 3-4: USING SW2 DIP SWITCH TO HARDWARE RESET LAN8814

To activate the LAN8814 hardware Reset signal, move the LAN8814_RST_N switch to the ON/closed/left-handed position, and then return it to OFF/open/right-handed position as per silkscreen markings in Figure 3-4.

Note: General reboot of the board and the LAN8814 PHY is accomplished using the SYSRESET push-button switch SW1 located next to the 12V barrel jack of the board. The push-button switch SW1 is recommended for general rebooting as it induces a “cold-start” condition to the software application, which configures the board.

3.4 EXPANSION CONNECTORS

3.4.1 GPIO Bank for LAN8814 PHY Test/Measurement

A 30-pin, 2.54 mm square-pin header is populated at J20, primarily for the purpose of observing LAN8814 outputs (clocks, event indicators, and so on). It also provides access to certain LAN8814 inputs, such as COMA_MODE, in order to create temporary input connections (prototyping).

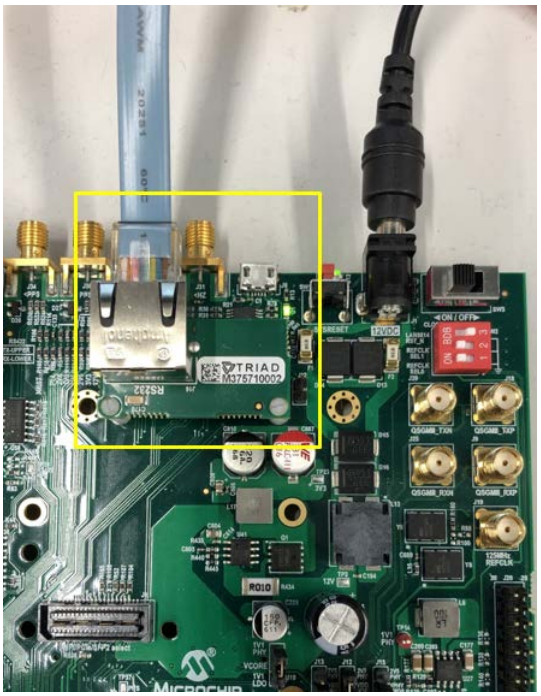
FIGURE 3-5: EVB-LAN8814 HEADER J20 ACCESS TO GPIOS

J20 even-numbered pins are all directly connected to board VSS. See numbering silk-screen markings in Figure 3-5.

3.4.2 UART Management Port for Serial Terminal Server Connections

Certain development environments may preclude the use of the J6 USB2UART connector or require native RS-232 with some hosts. To address those situations, the RS-232 "break-off" daughterboard included may be installed at J7 to provide a native RS-232 serial communications port. Figure 3-6 shows the RS-232 daughterboard installed.

FIGURE 3-6: RS-232 DAUGHTERBOARD INSTALLED



Note:	J7 is intended for use with the RS-232 management board included as part of the EVB-LAN8814 kit. The EVB-LAN8814 should be powered off while installing or removing the RS-232 management board. A Cisco 8p8c-to-DSUB9 COM cable PN 20251 or equivalent connects to the RJ45 connector of the RS-232 management board.

To proceed with this step, mount the RS-232 add-on module to the EVB-LAN8814 at J7, aligning with the snap-on spacers installed in the previous step.

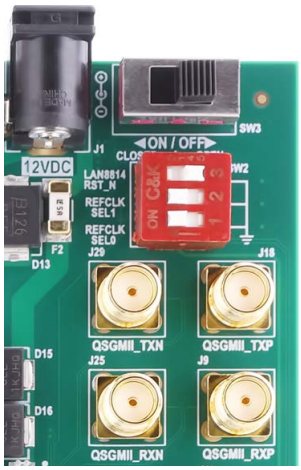
Note:	The RS-232 board will not seat flush onto the snap-on spacer's shoulder. However, it will still be mechanically stable in this configuration.

Note:	Do not attempt to connect both serial ports J7 (RS-232) and J6 (USB2UART) simultaneously. Only one serial port (either J7 or J6) should be used at a time with a host.

3.4.3 QSGMII Breakouts to LAN8814 PHY

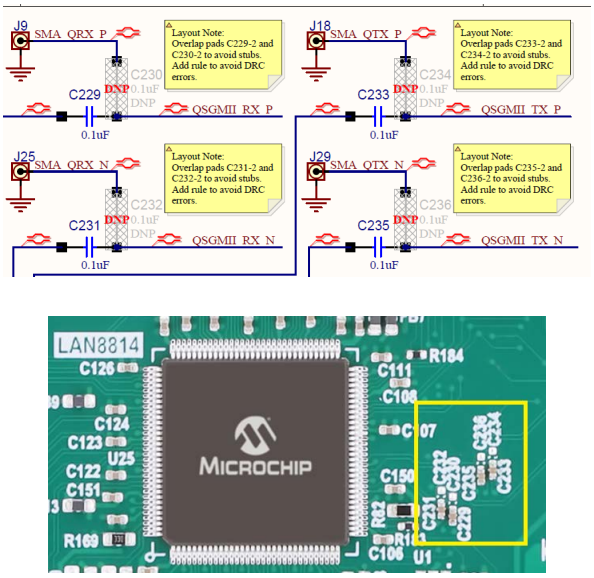
To observe the QSGMII transmitter output of the LAN8814 PHY, or for unswitched (back-back, bypassing the on-board VSC7514XKS) flows of Ethernet traffic through the LAN8814 PHY, SMAs are available at the top right-hand side of the EVB-LAN8814.

FIGURE 3-7: QSGMII SMAS



To connect the SMAs shown in Figure 3-7 with the LAN8814 pins, four 0.1 µF capacitors must be repositioned in the following area as shown in Figure 3-8.

FIGURE 3-8: CONNECTING QSGMII SMAS TO LAN8814 PINS



Note:	Relocate the capacitors as follows: C229 → C230, C231 → C232, C233 → C234, C235 → C236

Note:	QSGMII_RXP/N are differential inputs to LAN8814. QSGMII_TXP/N are differential outputs from LAN8814.

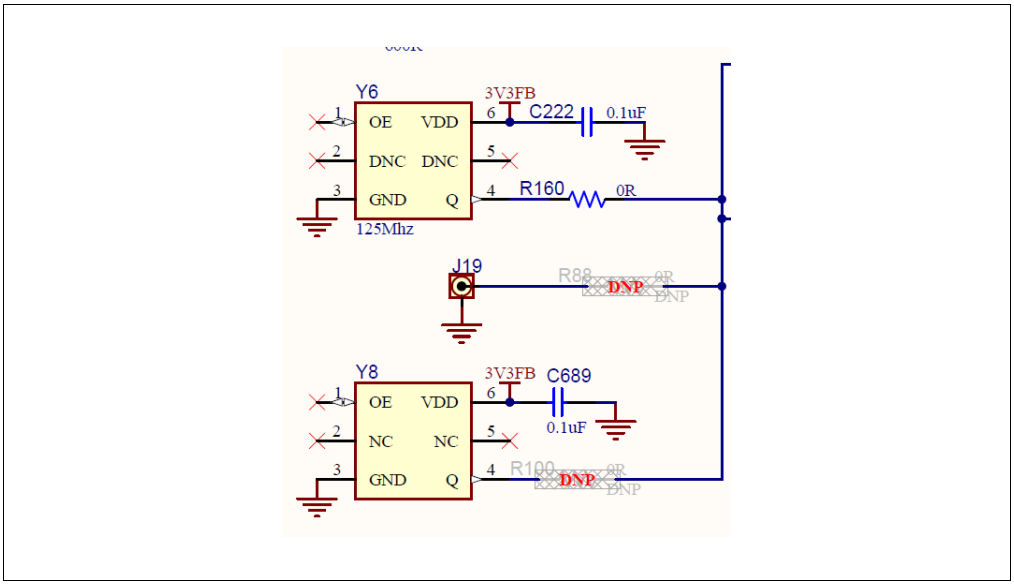
Note: If coaxial cables are connected for back-back Ethernet traffic flows, pay careful attention to match the signal polarity: QSGMII_RXP to QSGMII_TXP, and QSGMII_RXN to QSGMII_TXN. Always use high-quality, braided/double-shielded RF cables rated up to a 5 GHz+ passband, and always ensure that a differential-cable pair (RXP/N or TXP/N) matches in length.

3.4.4 Clock Reference to the EVB

An external 125 MHz system clock reference can be furnished to the EVB-LAN8814 via SMA J19. This may be particularly desirable for higher-stability timing applications such as 1588 operation using the EVB-LAN8814.

To connect J19 to the VSC7514XKS master clock, move 0Ω bridge just to left of J19 from R160/R100 to R88. The electrical connection is shown in Figure 3-9.

FIGURE 3-9: CONNECTING EXTERNAL 125 MHZ CLOCK TO EVB MASTER CLOCK



Note: A TCXO-class on-board 125 MHz oscillator option is also available via Y8. Move 0Ω R160 to R100 to connect with the on-board TCXO.

3.5 LAN8814 FREE-RUNNING CLOCK

The LAN8814 25 MHZ VDFN-4 XO can be changed at Y3 to use a parallel-resonant crystal instead. See the EVB-LAN8814 Schematic for connection details on how to change the circuit for use with a parallel-resonant crystal.

Note: A compatible parallel-resonant crystal for this circuit is part no. VXM7-9013-25M0000.

3.6 BOARD DEBUG TEST POINTS

Useful observation points for debugging EVB-LAN8814 are shown in Table 3-1:

TABLE 3-1: EVB-LAN8814 TEST POINTS

Test Point Reference Designator	Purpose
TP14	Board ground
TP12, TP13, TP14	On-board voltage regulator rails supplying the LAN8814 PHY
TP2, TP23	Main board voltage regulator rails 12V and 3V3
TP5	nSYSRESET system HW Reset signal
TP37, TP38, TP39, TP40	1588 1PPS strobe signal observation points
R86/PLL probe point	Verifying PLL toggle inside VSC7514XKS eCPU

Chapter 4. PTP4L Demonstration using the EVB

4.1 CONNECTION SETUP

4.1.1 EVB Clock Configuration

The EVB-LAN8814 requires a TCXO or higher-stability frequency reference. The on-board TCXO is suitable, or the customer can alternatively connect a bench 125 MHz frequency reference (e.g. a OCXO-disciplined frequency synthesizer) to the J19 SMA. Refer to **Section 3.4.4 "Clock Reference to the EVB"** for rework/connection instructions.

4.1.2 Calnex Paragon-X Connections

1. Connect the EVB J20 pin 1 to 'Upper Aux port' on the front panel of the Paragon-X using the Calnex-supplied cable (black BNC) in Figure 4-1.

FIGURE 4-1: CALNEX-SUPPLIED CABLE

The black BNC coaxial connector can be adapted to the 0.100 stake header J20.1 using a female BNC-Microclip adapter. (Pomona model no. 3788 is a commonly-available part.)

See Figure 3-5 for the picture of the J20 signal header. Pin 1 is easily identified by the white dot in the lower right-hand corner of the header. The TP41 GND test point can be connected to the BNC cable's outer shield (black clip of the BNC-Microclip).

2. Connect the front-panel PORT5 of the EVB to the Paragon-X Ethernet Port 1.

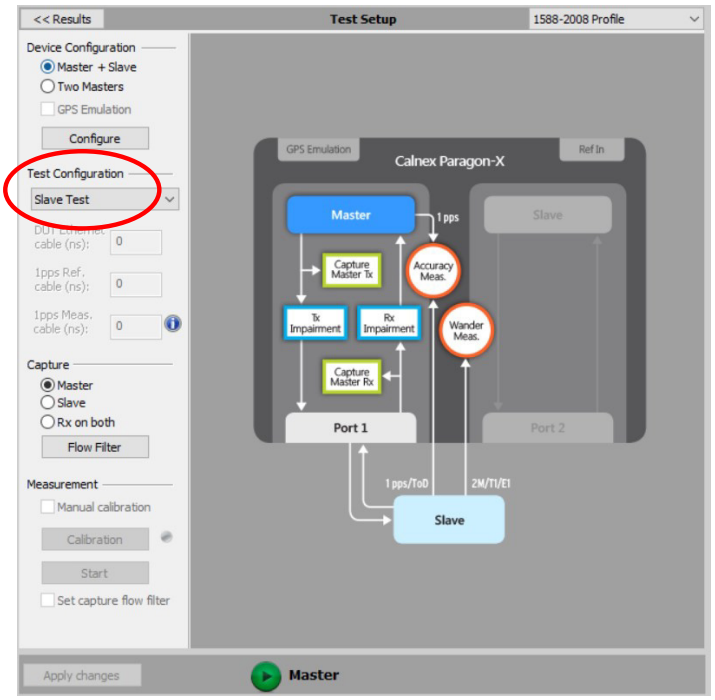
Note: Use a short CAT5e (< 1.5m) to use the same compensation values and measure approximately the path delays as shown in the example in **Section 4.8 "Confirming OffsetfromMaster from PTP4L"**.

4.2 CALNEX PTP MASTER SETUP

Only the settings which are required to change are shown below. In the Paragon-X Control GUI for the Calnex, configure the following:

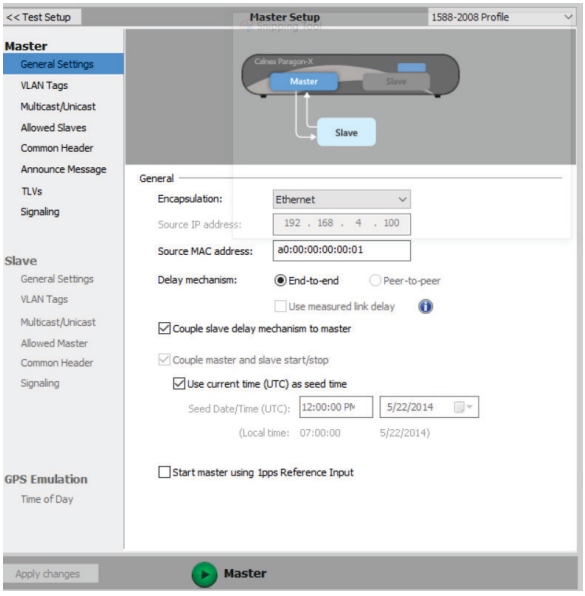
1. In Master/Slave Emulation, select Slave test configuration. See Figure 4-2.

FIGURE 4-2: MASTER/SLAVE EMULATION



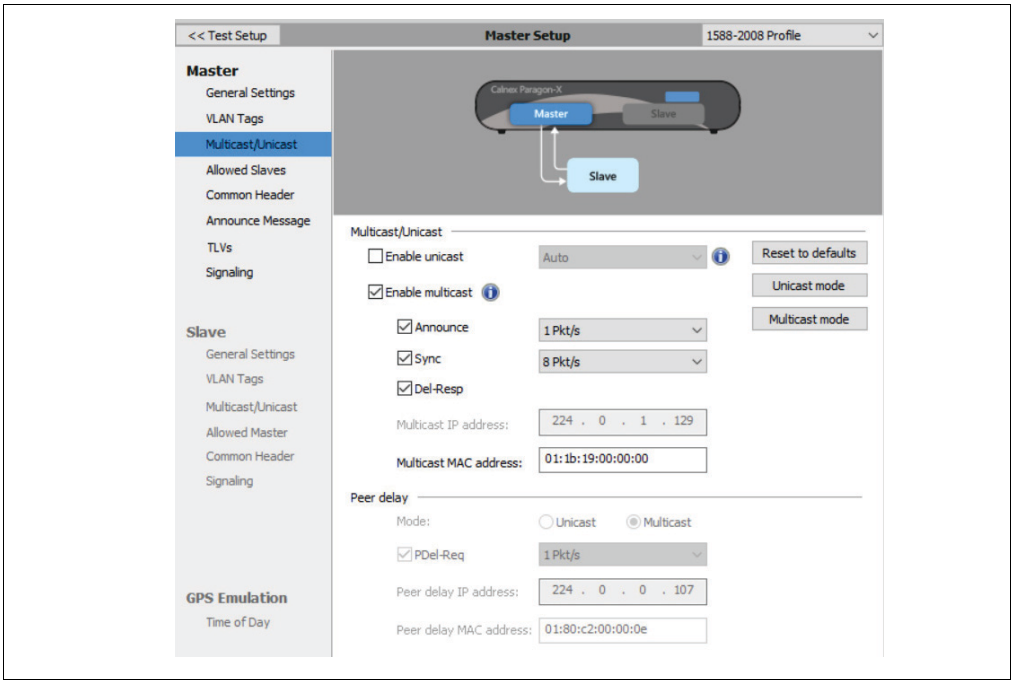
2. Click on Configure (See Figure 4-3.), and select the following Master settings:
   a) Ethernet (Layer-2) PTP Encapsulation
   b) End-to-End Delay Mechanism

FIGURE 4-3: MASTER SETTINGS



3. Click on Multicast/Unicast selections (See Figure 4-4.), and select the following:
   a) Enable multi-cast mode **only**
   b) Enable all messages: Announce, Sync, and Delay-Resp
   c) Set Sync repetition rate as desired (recommended 8 pkts/s)

FIGURE 4-4: MULTICAST/UNICAST SETTINGS

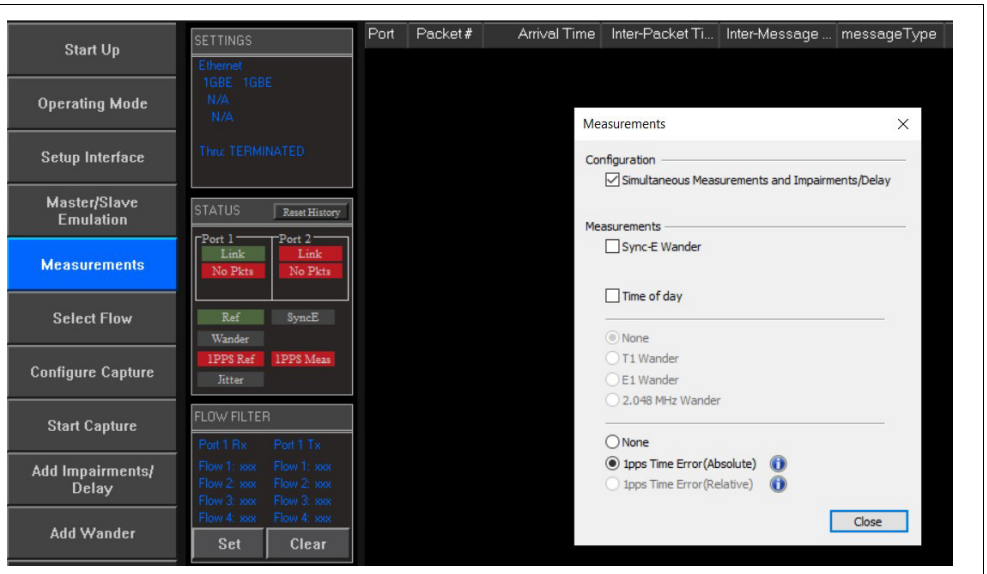


4. Leave PTP Header/Announce settings at default.

4.2.1 Click Measurements

5. Enable 1 pps Time Error (absolute), in the Measurement pop-up window. See Figure 4-5.

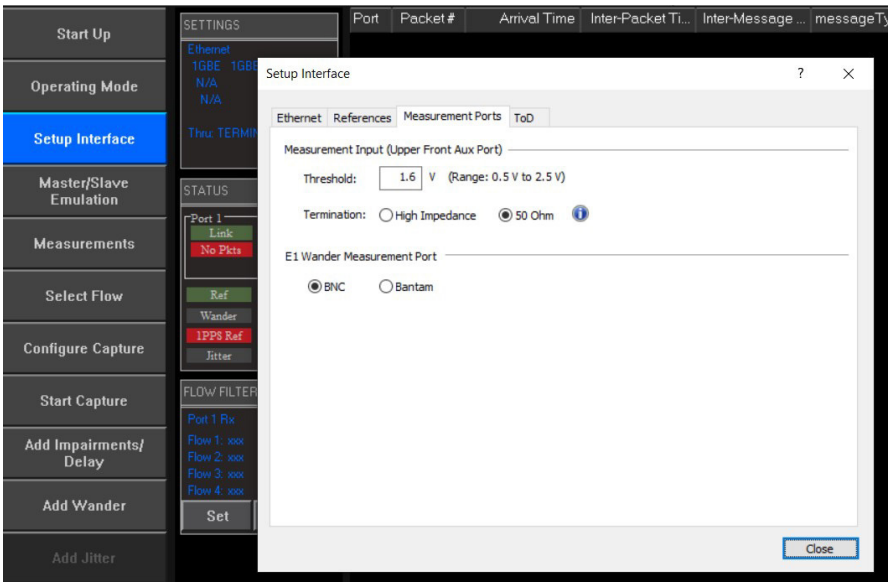
FIGURE 4-5: MEASUREMENT WINDOW



4.2.2 Click Setup Interface

6. Change 1 pps reference input settings, on the Measurement Ports panel - default 1.6V. See Figure 4-6.

FIGURE 4-6: MEASUREMENT PORTS PANEL



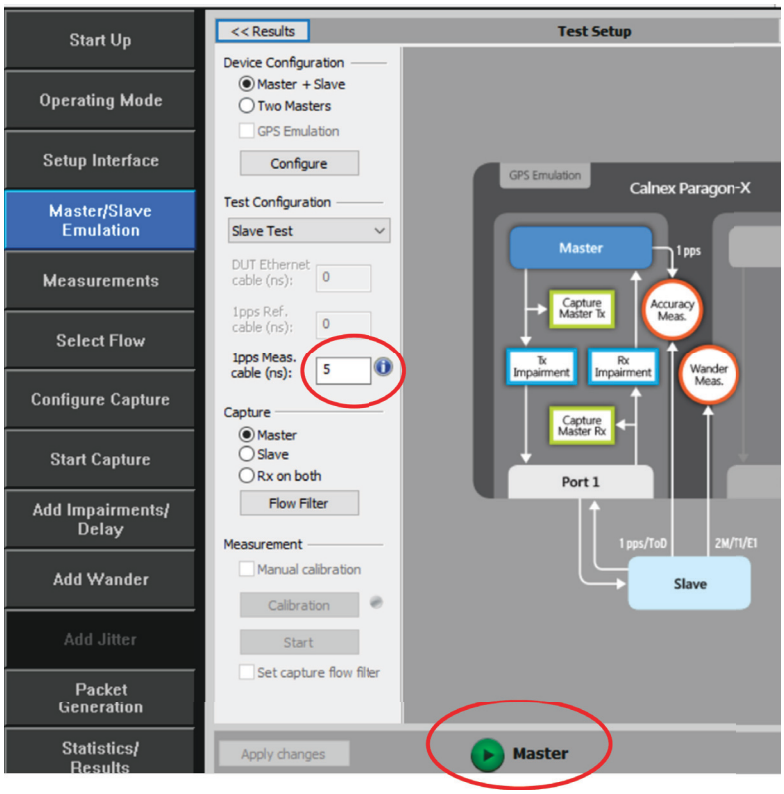
Note: The VDDIOF setting on the EVB should be checked at the on-board jumper, J12, to confirm it is set for the 2V5 supply to remain in-specification for the Paragon-X input port.

4.2.3 Return to the Calnex PTP Master Emulation Setup Panel

7. Start Calnex PTP Master emulation. Click on the green play button as illustrated in Figure 4-7.

Note: Before clicking the play button, enter delay compensation for the 1PPS measurement cable (BNC cable). Paragon-X recommends ~5 nanoseconds/meter of BNC.

FIGURE 4-7: MASTER/SLAVE EMULATION SETUP



4.3 CONFIGURING THE SWITCH PTP OORT AND PTP APPLICATION

1. Write a static configuration file out in order to specify the 1588 clock setup.

Note:	For the EVB switchdev image, this file must be written to /tmp/def_cfg_ptp on this particular file system.

In Example 4-1 def_cfg_ptp file, note the [ethn] designation for the desired PTP OC port, where n = 4 for the LAN8814 base port:

EXAMPLE 4-1: DEF_CFG_PTP FILE

```
# cat /tmp/def_cfg_ptp
[global]
delay_mechanism            E2E
network_transport          L2
time_stamping              hardware
tx_timestamp_timeout       1000
step_threshold             0.000001
twoStepFlag                0
first_step_threshold       0.000001
clock_type                 OC
logAnnounceInterval        0
logSyncInterval            –3
logMinDelayReqInterval     –3
clockClass                 248
clockAccuracy              254
slaveOnly                  0
socket_priority            0
ingressLatency             15
egressLatency              0

delay_filter               moving_median
clock_servo                linreg
delay_filter_length        10

[eth4]
```

2. Refer to **2.1.6 "Interface Reconfiguration"** when using iproute2 to establish 1000BASE-T on eth4 port.

4.4 ENABLING THE 1PPS TIMING OUTPUT FROM THE LAN8814 DEVICE

Use the following command to enable the 1PPS timing output:

```
# echo 1 >
/sys/devices/platform/ahb@
70000000/710700c0.mdio/mdio_bus/7
10700c0.mdio-mii/710700c0.mdio-mii:07/ptp/ptp0/pps_enable
```

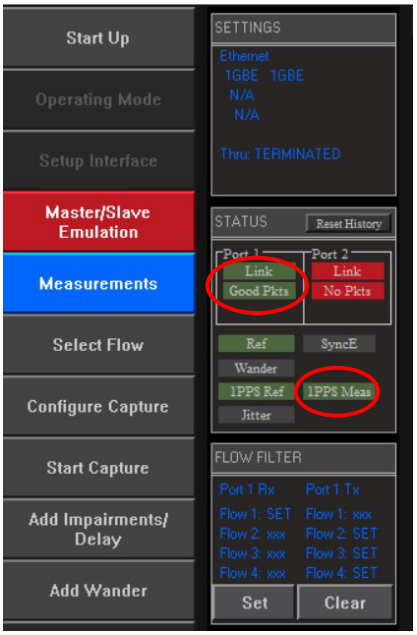
4.5 STARTING PTP4L

1. Run the EVB-LAN8814 as a PTP follower node, as shown below:

```
# ptp4l -msf /tmp/def_cfg_ptp
```

2. Select *Flow>Capture Packets* to perform a dummy capture of PTP packets.
3. Confirm that "Good" PTP packets are received, and the 1PPS output from DUT is valid at the Calnex PTP Master. See Figure 4-8.

FIGURE 4-8: CALNEX PTP MASTER PORT STATUS



Note: Circled statuses indicate valid PTP traffic flow and valid 1PPS input to the Calnex front panels.

4.6 CONFIRMING PTP4L MESSAGE OUTPUTS

Confirm if the message output is similar to the following:

```
ptp4l[709261.521]: rms    1 max    2 freq   -162 +/- 10 delay 6721 +/-   0
```

Note 1: Allow ten (10) minutes for the oscillator to warm completely and for the PTP4L software delay filter to settle.

2: The PTP4L output message format is:
ptp4l[message timestamp in seconds]
rms: time offset in nanoseconds, root-mean-squared
max: maximum (worst-case) time offset, in nanoseconds
freq: frequency offset, in part-per-billion with ± tolerance
delay: path delay, in nanoseconds with ± tolerance

3: The path delay increases with CAT5e cable length and will include the intrinsic path delay of Paragon test equipment. Paragon-X intrinsic delay is approximately 6.7 microseconds. Therefore, a 6.721-microsecond value indicates a typical path delay measurement between the Paragon and the DUT.

4.7 RESTARTING PTP4L AS A BACKGROUND PROCESS

Stop PTP4L (Ctrl-C to break) and restart PTP4L in the background using the command:

```
# ptp4l -sf /tmp/def_cfg_ptp &
```

4.8 CONFIRMING OFFSETFROMMASTER FROM PTP4L

For a synchronized EVB DUT, the output should return something similar to:

```
# pmc -u -b 0 'GET CURRENT_DATA_SET'
```

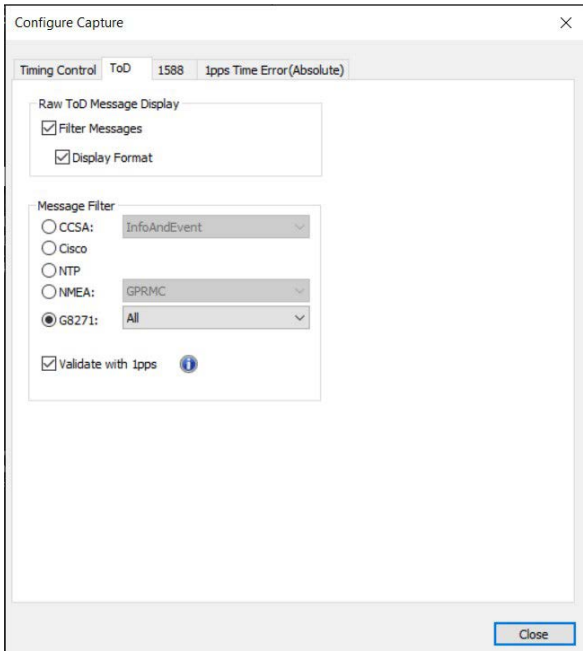
```
sending: GET CURRENT_DATA_SET
06823a.fffe.8caa74-0 seq 0 RESPONSE MANAGEMENT CURRENT_DATA_SET
stepsRemoved     1

offsetFromMaster 0.0

meanPathDelay    6721.0
```

Note: offsetFromMaster is the key performance metric reported by the PTP4L application. It will drift within a peak-peak range of ± 8 nanoseconds.

4.9 PERFORMING 1588 1PPS MEASUREMENTS USING THE PARAGON-X

1. Select *Flow>Capture Packets* to capture PTP packets
2. Use the Flow Wizard to confirm that 1588 PTP flows are indeed appearing within the Wizard, thus indicating that detectable PTP flows exist.
3. Select *Flow>Stop Capture.*
4. Return to the main Paragon-X window, then select Configure Capture, **ToD** tab, and G.8271 (All messages) as well as tick the Validate with 1PPS selection. See Figure 4-9.

FIGURE 4-9: CONFIGURE CAPTURE FOR PARAGON-X

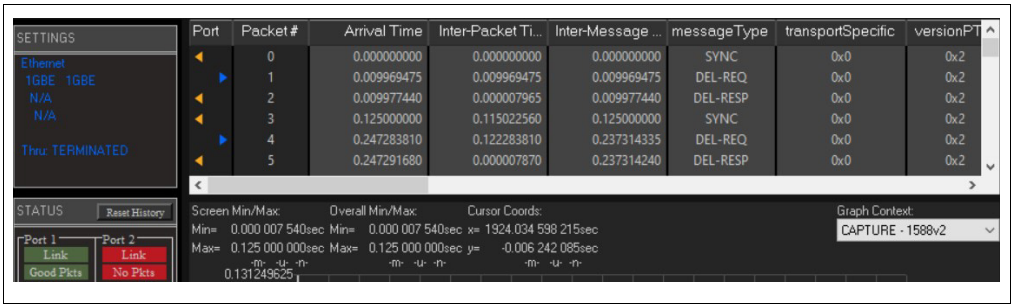


Note: On the Raw ToD Message Display, it is recommend to select both Filter Messages and Display Format to get PTP message data decoded into human-readable format.

5. Close the Capture window and return to the main Paragon-X window.
6. Select Start Capture. Two-way (Sync + Delay_req/Delay_resp) messages

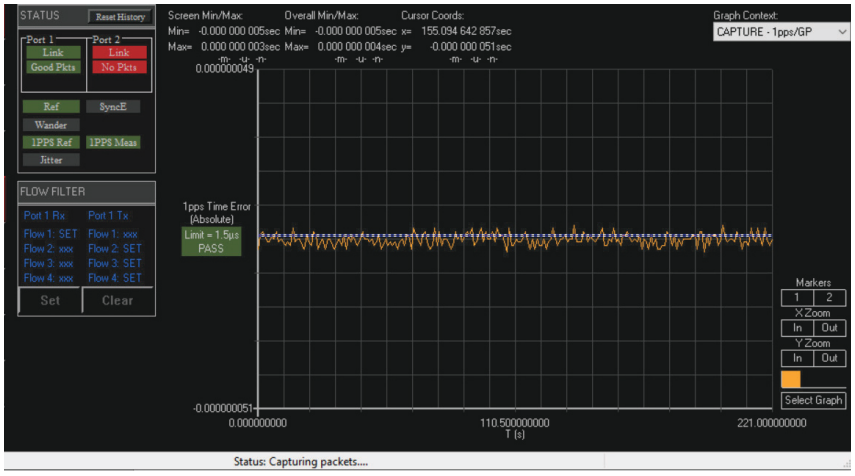
should be scrolling on the Paragon-X Capture window, as shown in the upper-right tile in Figure 4-10.

FIGURE 4-10: PARAGON-X CAPTURE WINDOW MESSAGES



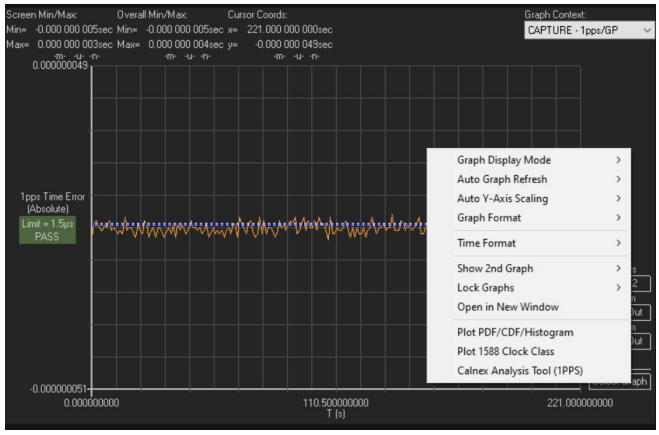
7. Select Graph Context = 1PPS/GP, when the time error graph appears. See Figure 4-11.

FIGURE 4-11: GRAPH CONTEXT



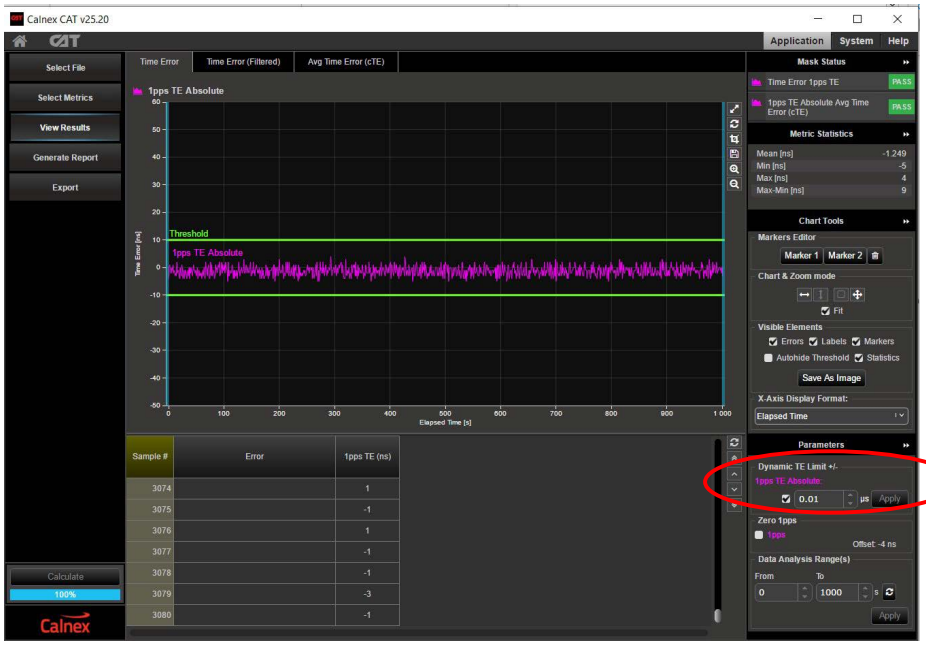
8. Select Graph in the lower right-hand corner of the same screen, and then select Calnex Analysis Tool (1PPS). See Figure 4-12.

FIGURE 4-12: SELECT CALNEX ANALYSIS TOOL (1PPS)



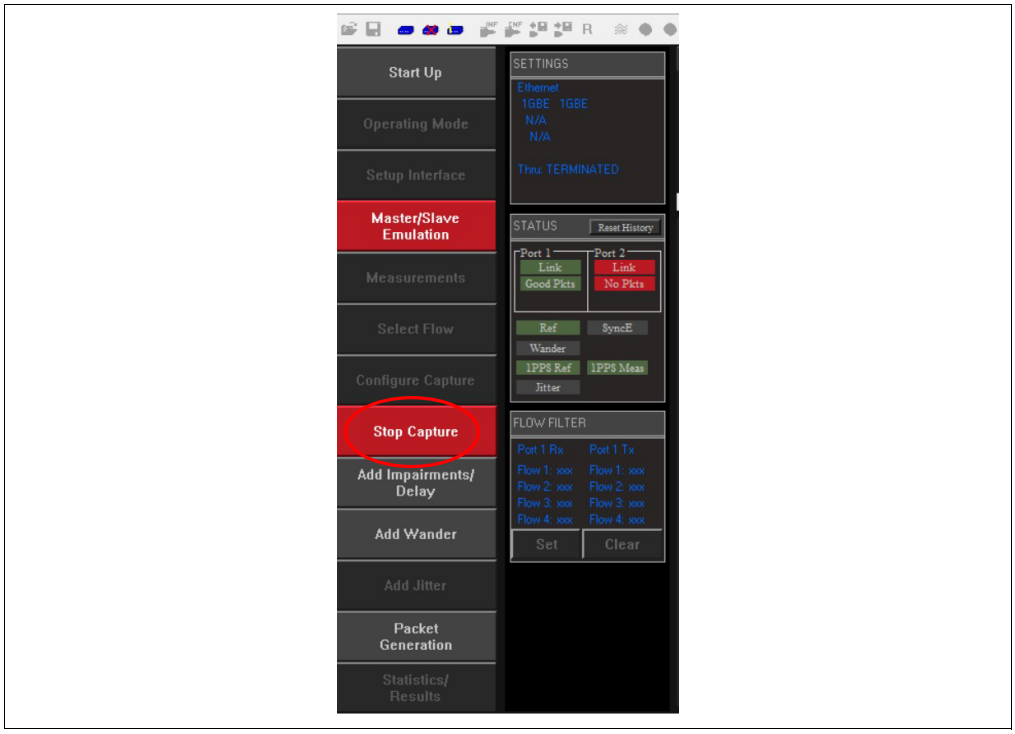
9. Once the CAT app finishes loading, click on **View Results.**
10. The Time Error dynamic plot appears. Set the Dynamic TE Limit +/– to the minimum allowable value (±0.01 microseconds) and click on **Apply**. See Figure 4-13.

FIGURE 4-13: DYNAMIC TE LIMIT



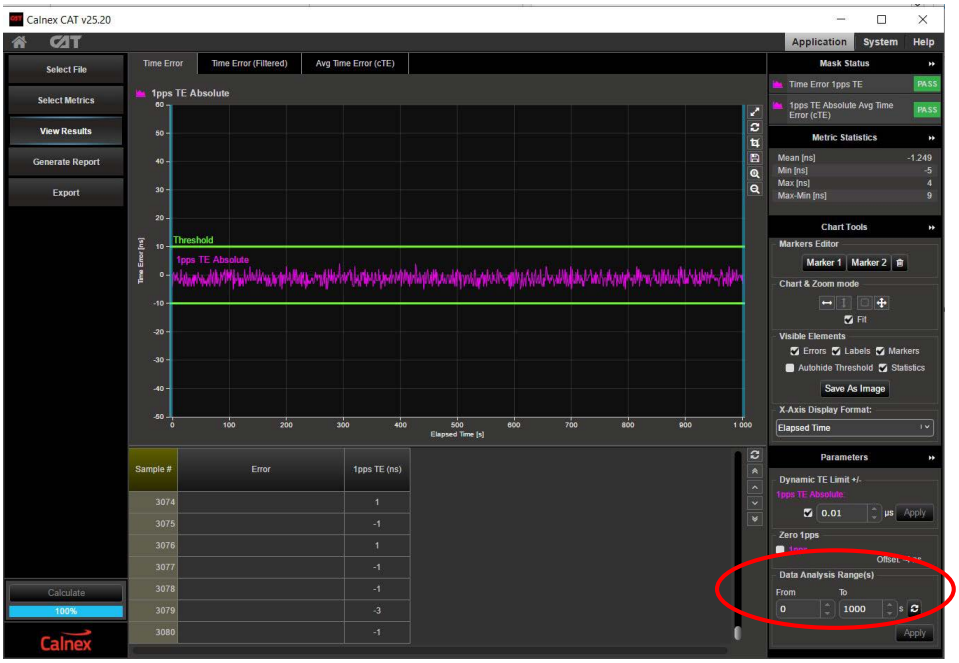
11. Allow sufficient time to capture the number of 1588 packet as well as 1PPS measurements for your desired observation interval. Once the desired interval has elapsed, return to the main Paragon-X window and click on **Stop Capture**. See Figure 4-14.

FIGURE 4-14: STOP CAPTURE



12. Once Capture has stopped, zoom to the desired observation window as shown in the lower right-hand circle in Figure 4-15.

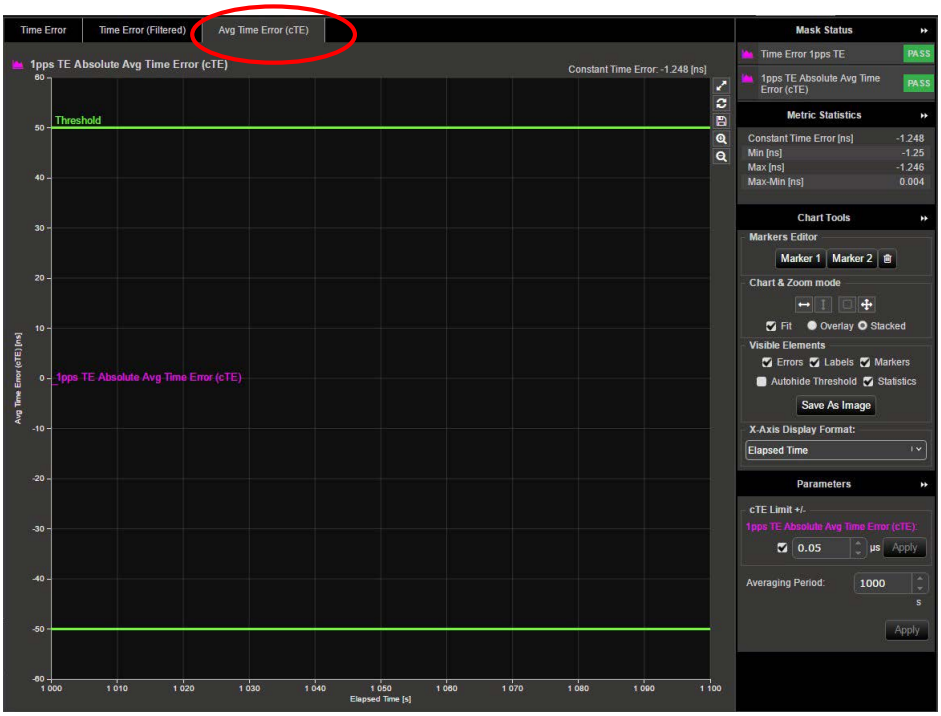
FIGURE 4-15: SETTING AN OBSERVATION WINDOW



Note 1:	A typical observation window for 1588-related performance metrics is 1000 seconds. The graphing toolbar allows zoom-to-range and ensures the x-axis plot of the TE metric matches the interval of calculated statistics.
2:	The 1PPS Metric Statistics minimum/maximum has been verified to within ±8 ns for this EVB over a 1000 second observation window, which can be verified in the Metric Statistics reported in the above window. (The Dynamic TE Limit resolution limitation is ±10 ns)

13. As desired, the average time error tab can be selected to dynamically view cTE calculations. Refer to Figure 4-16. (This chart updates every 60 seconds, by default, and will continue to draw updated cTE calculations in the x-dimension via the purple line)

FIGURE 4-16: AVERAGE TIME ERROR (CTE)



NOTES:

Appendix A. Schematics

A.1 INTRODUCTION

This appendix shows the EVB-LAN8814 schematics.

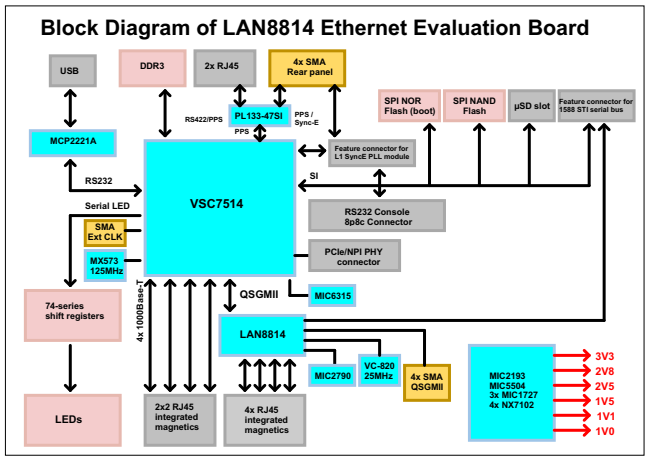
FIGURE A-1: EVB-LAN8814 BLOCK DIAGRAM

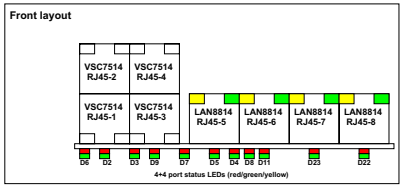
Table of Contents

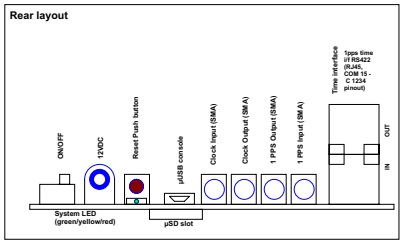
Sheet	Description
1	Table of Contents, Revision History, Block Diagram
2	Power Input, VSC7514 Regulators
3	VSC7514 Memory, GPI
4	LAN8814, Ethernet Ports
5	Clocks, 1588, SyncE
6	LAN8814 GPIOs, Regulators, Breakoffs

Revision History

Revision	Date	Revision Summary	Author
00C	11/11/2021	Import from Rev B	Arnaldo Cruz
01C	1/31/2022	U42 footprint change, silkscreen updates	Arnaldo Cruz
C0	2/04/2022	Release to manufacturing	Arnaldo Cruz
C1	5/17/2022	FB4 replaced with 100R, 22uF capacitor added in paralled with C118	Arnaldo Cruz







Notes

1	All resistors are 1% unless specified otherwise
2	Shunt jumper default selections are marked with an asterisk [*].

Project Owner: Howard Hicks			MICROCHIP
PCB Layout Contact: Arnaldo Cruz			
PartNumber: EV53D52A	Project Title: UNG8261 EVB-LAN8814	Variant: Standard	
Sheet Title: Table of Contents, History, Block Diagram			Designed with Altium
Size: Tabloid	SCH #: EVB-LAN8814 Rev: C1	Date: 5/17/2022	Altium.com
	PCB #: UNG8261 Rev: C0	Sheet 1 of 6	
File: 1 - TOC SchDoc			

FIGURE A-2: EVB-LAN8814 POWER INPUT AND VSC7514 REGULATORS

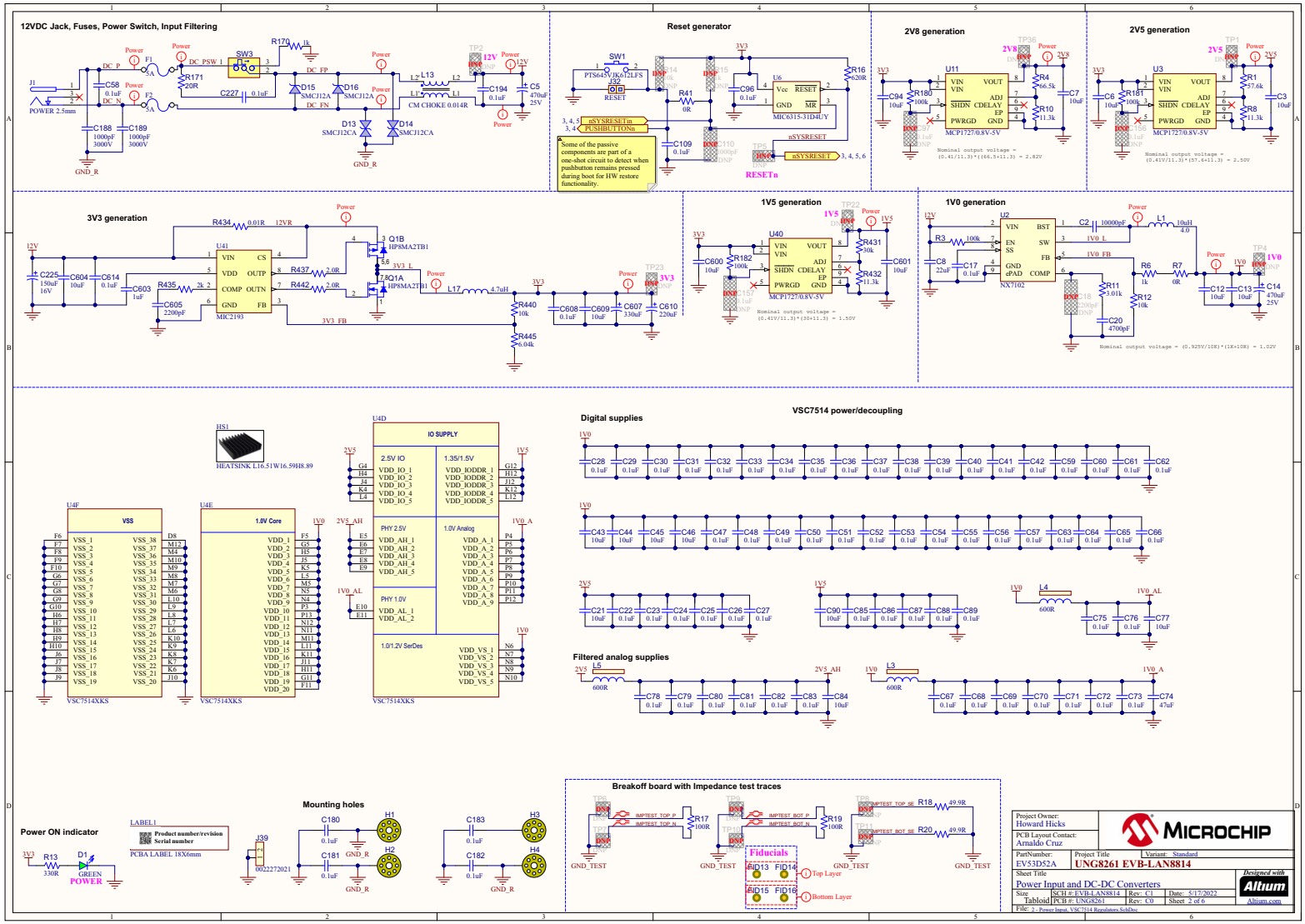


FIGURE A-3: VSC7514 MEMORY AND GPI

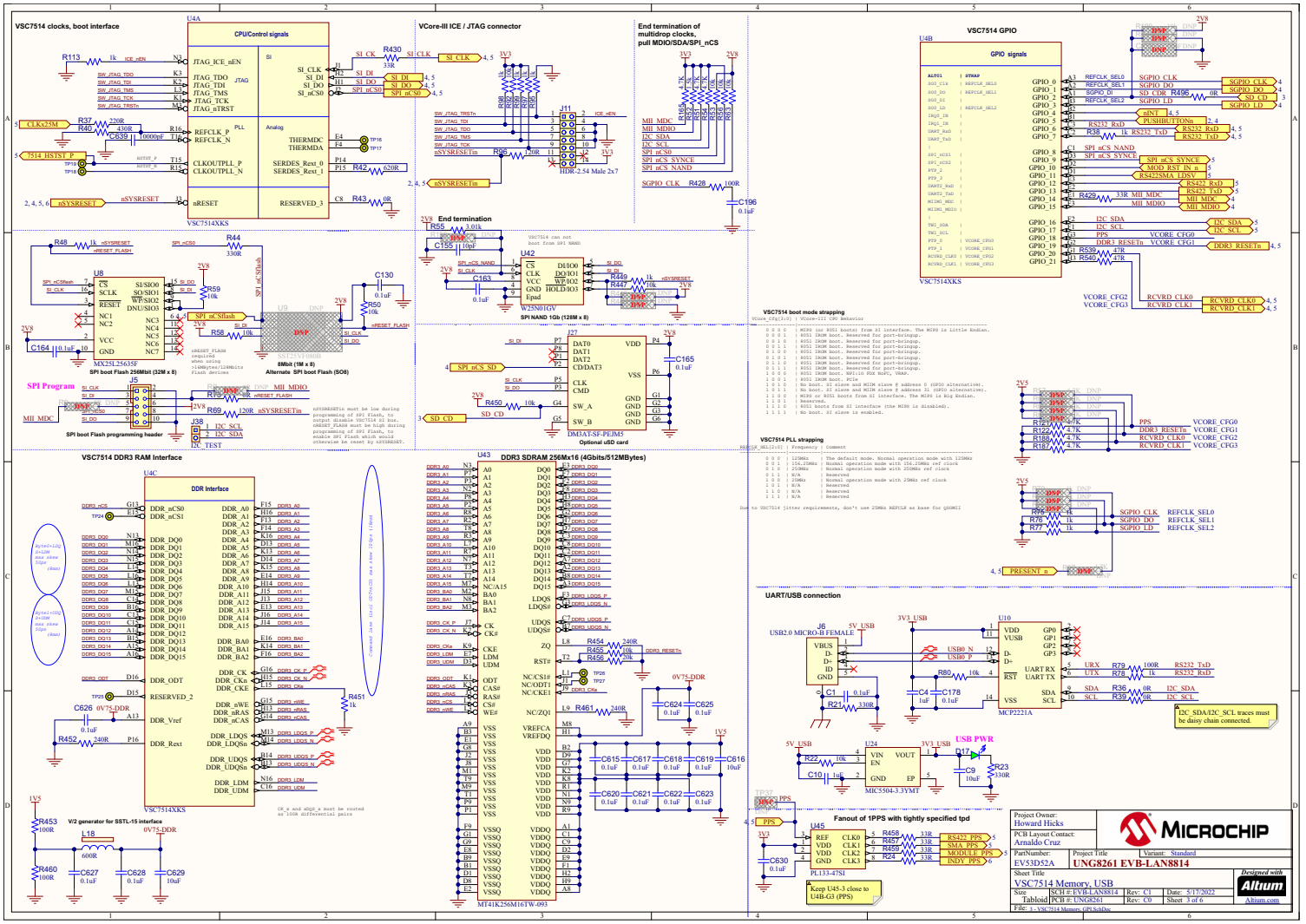


FIGURE A-4: LAN8814N ETHERNET PORTS

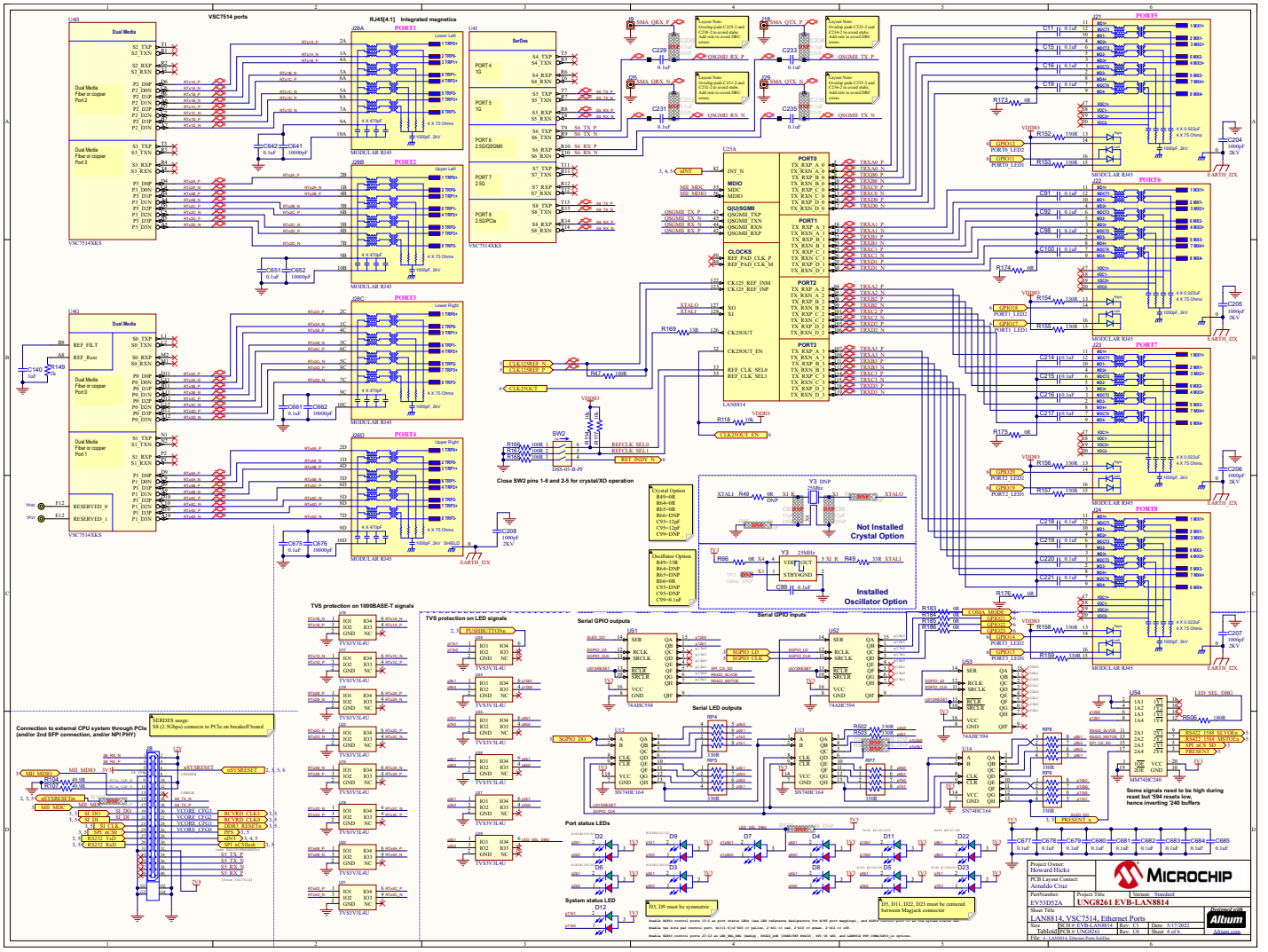


FIGURE A-5: CLOCKS, 1588, AND SYNCE

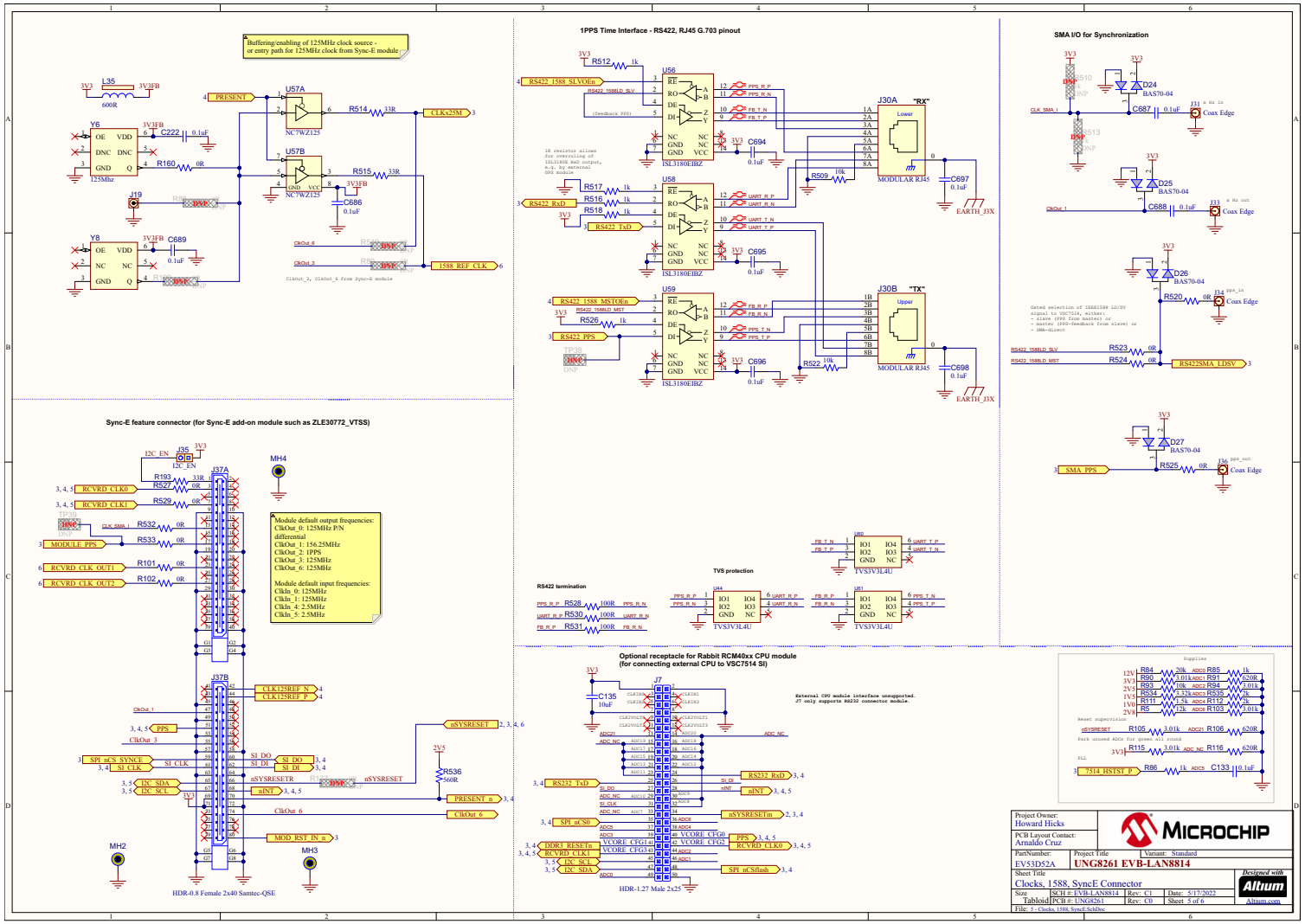
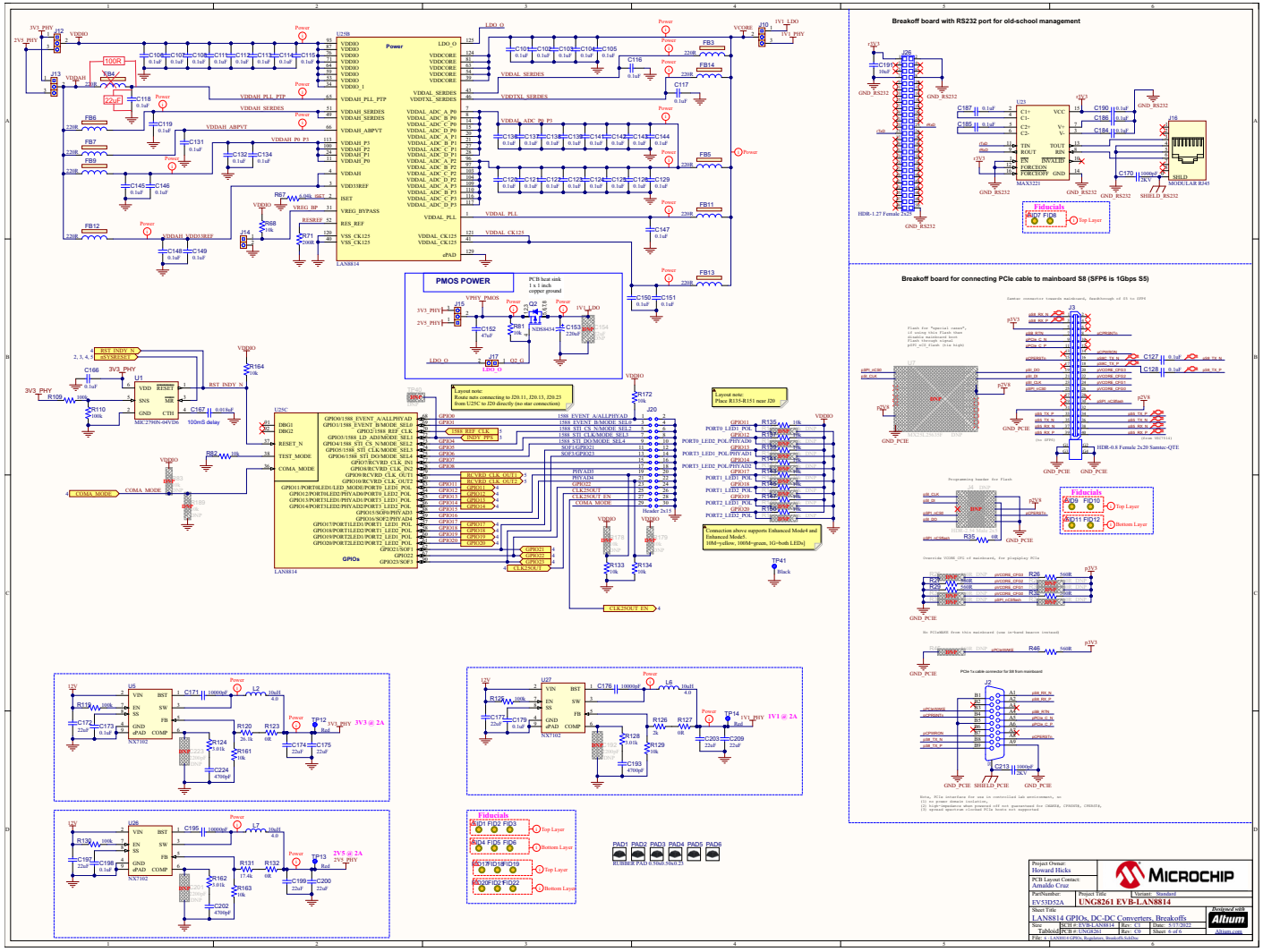


FIGURE A-6: LAN8814 GPIOS, REGULATORS, AND BREAK-OFFS



NOTES:

Appendix B. PCB Layers

B.1 INTRODUCTION

This appendix contains the EVB-LAN8814 PCB Layers.

FIGURE B-1: TOP SILK

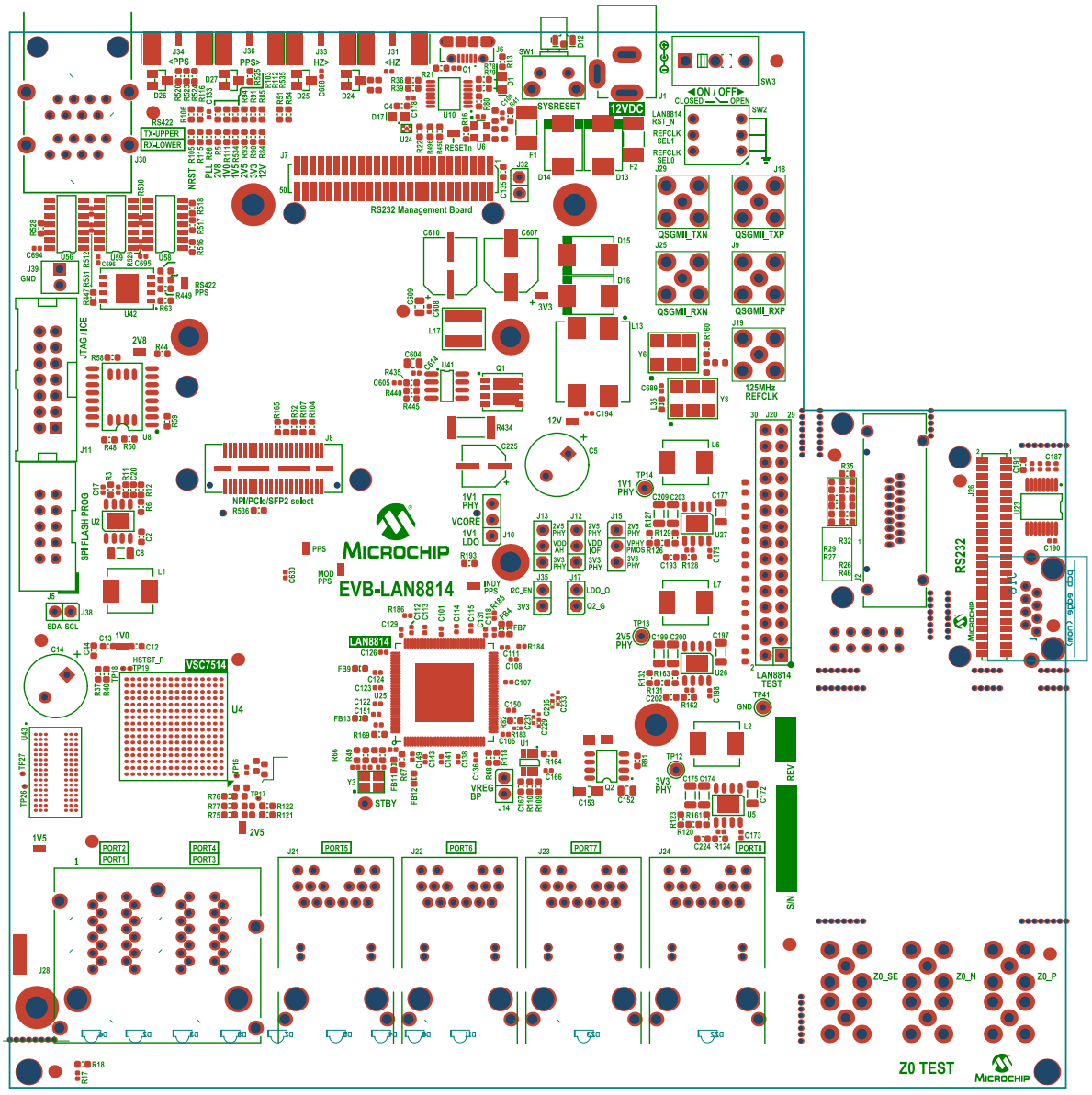


FIGURE B-2: TOP COPPER

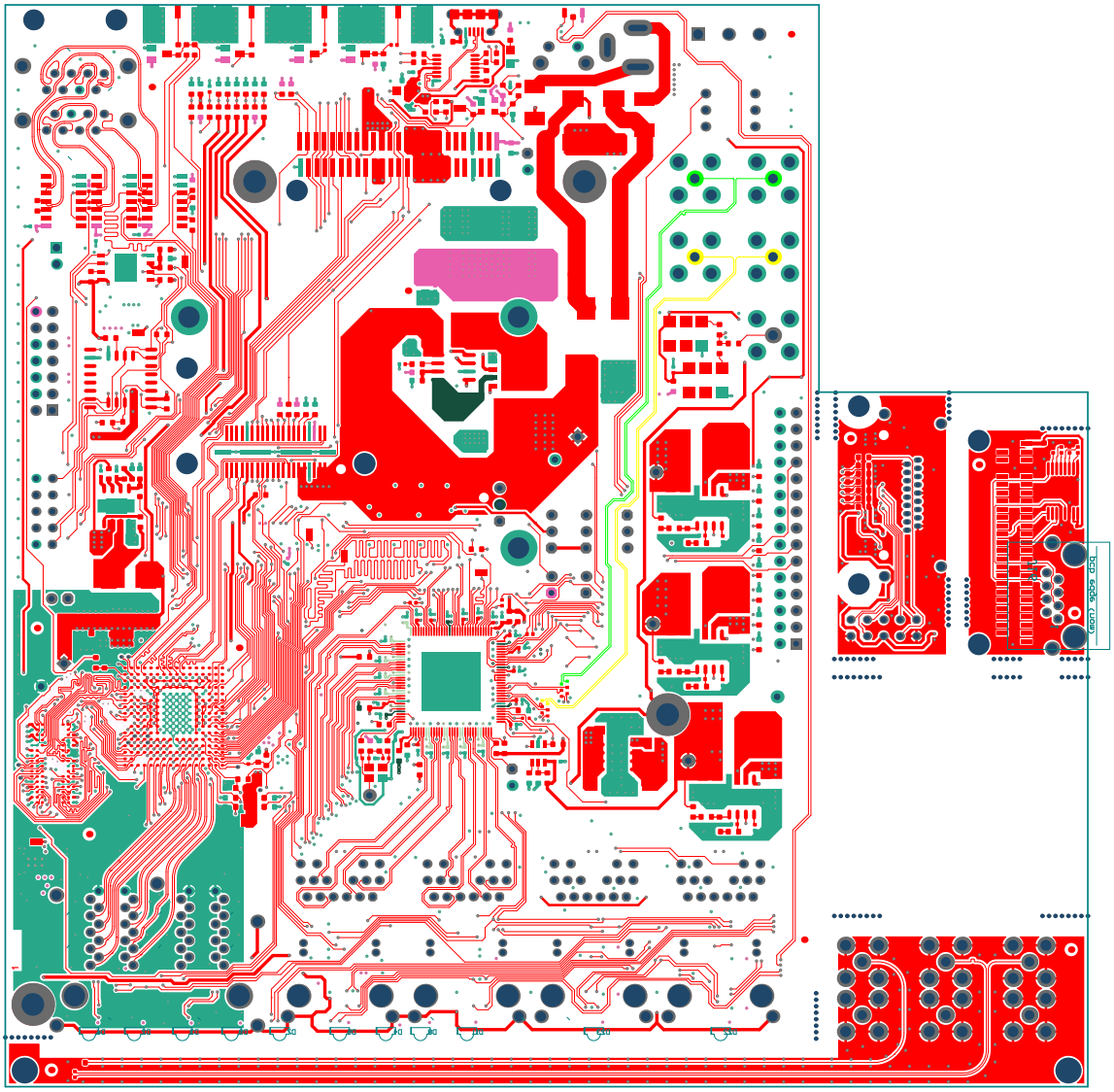


FIGURE B-3: LAYER 2 GND

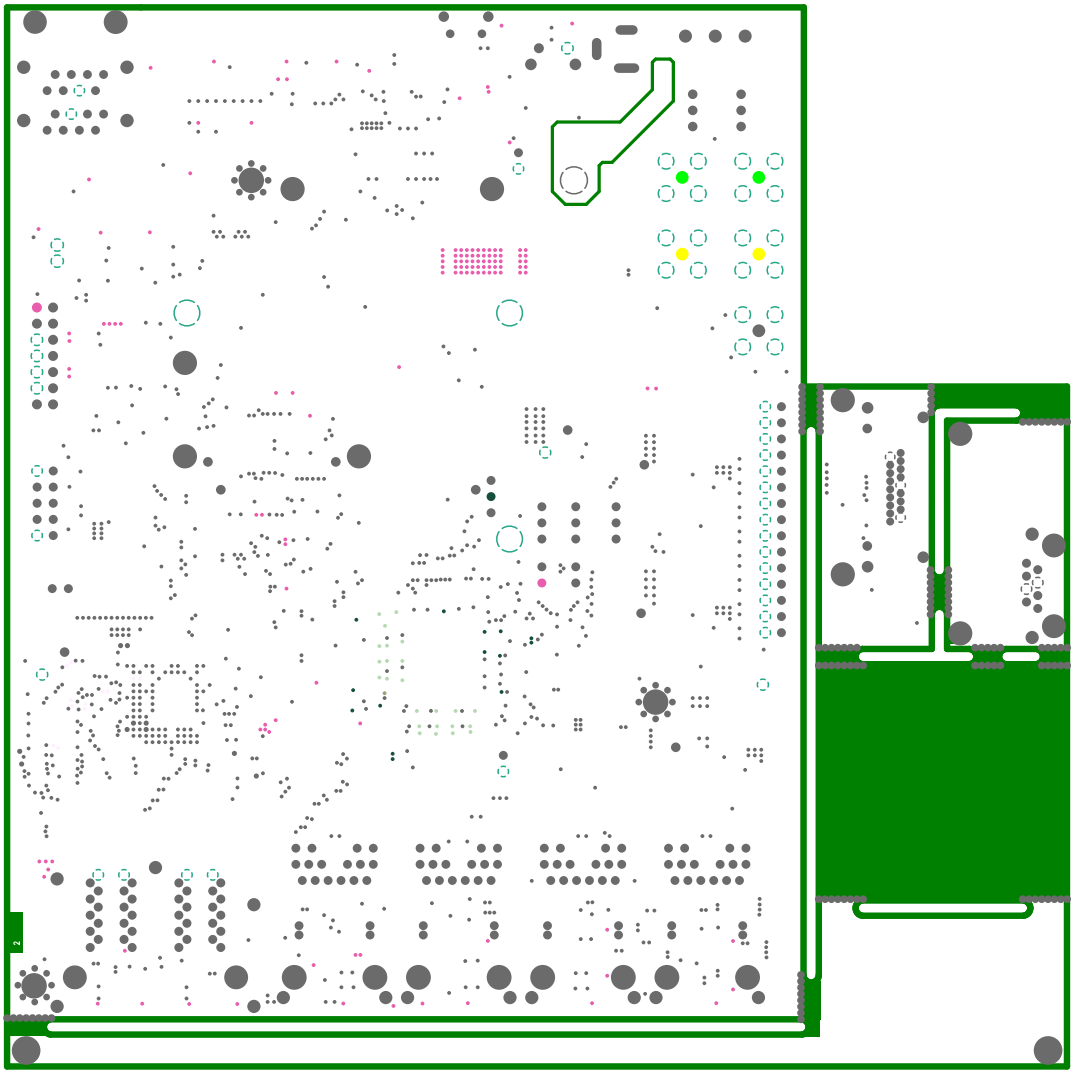


FIGURE B-4: LAYER 3 POWER

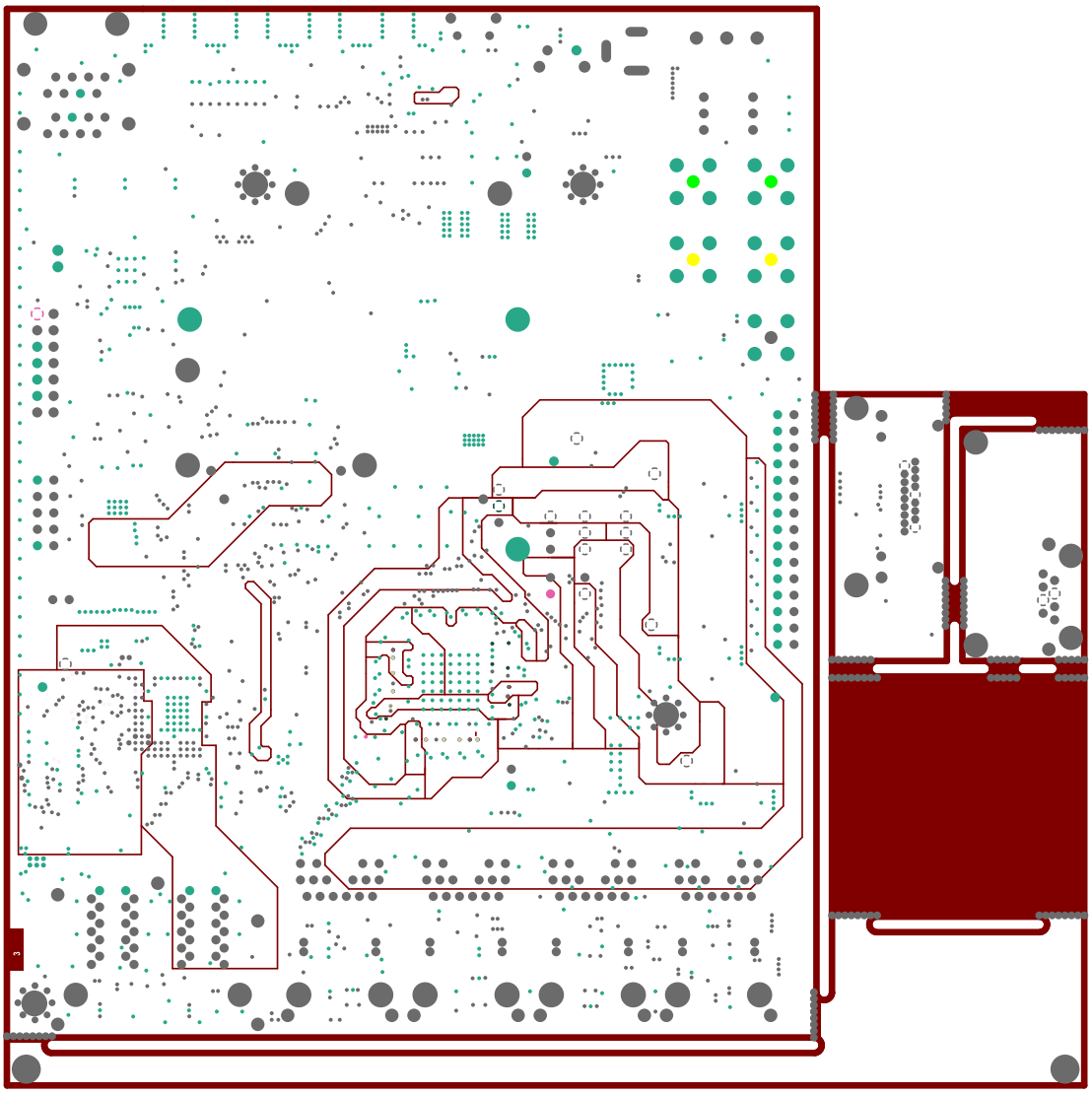


FIGURE B-5: LAYER 4 SIGNAL

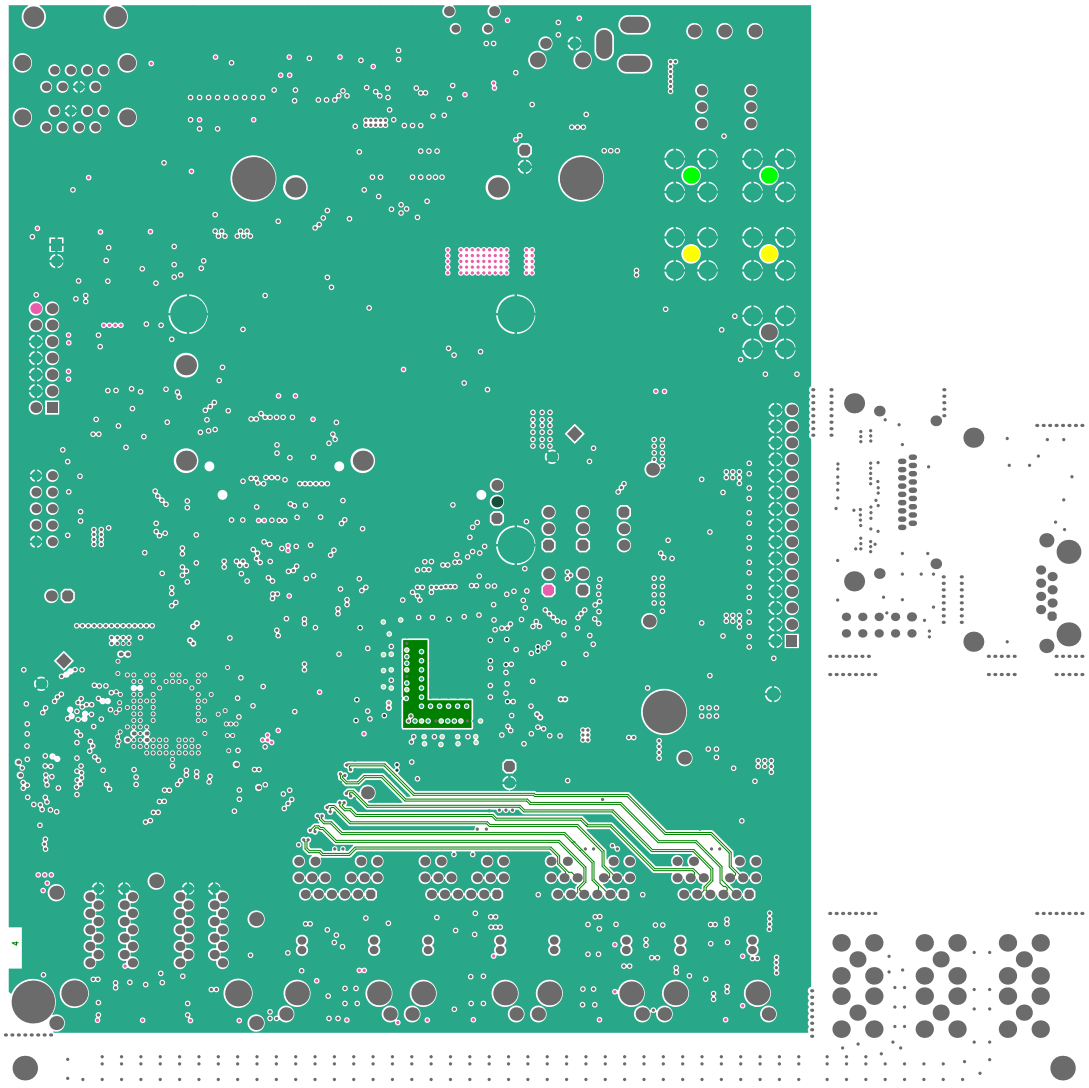


FIGURE B-6: LAYER 5 GND

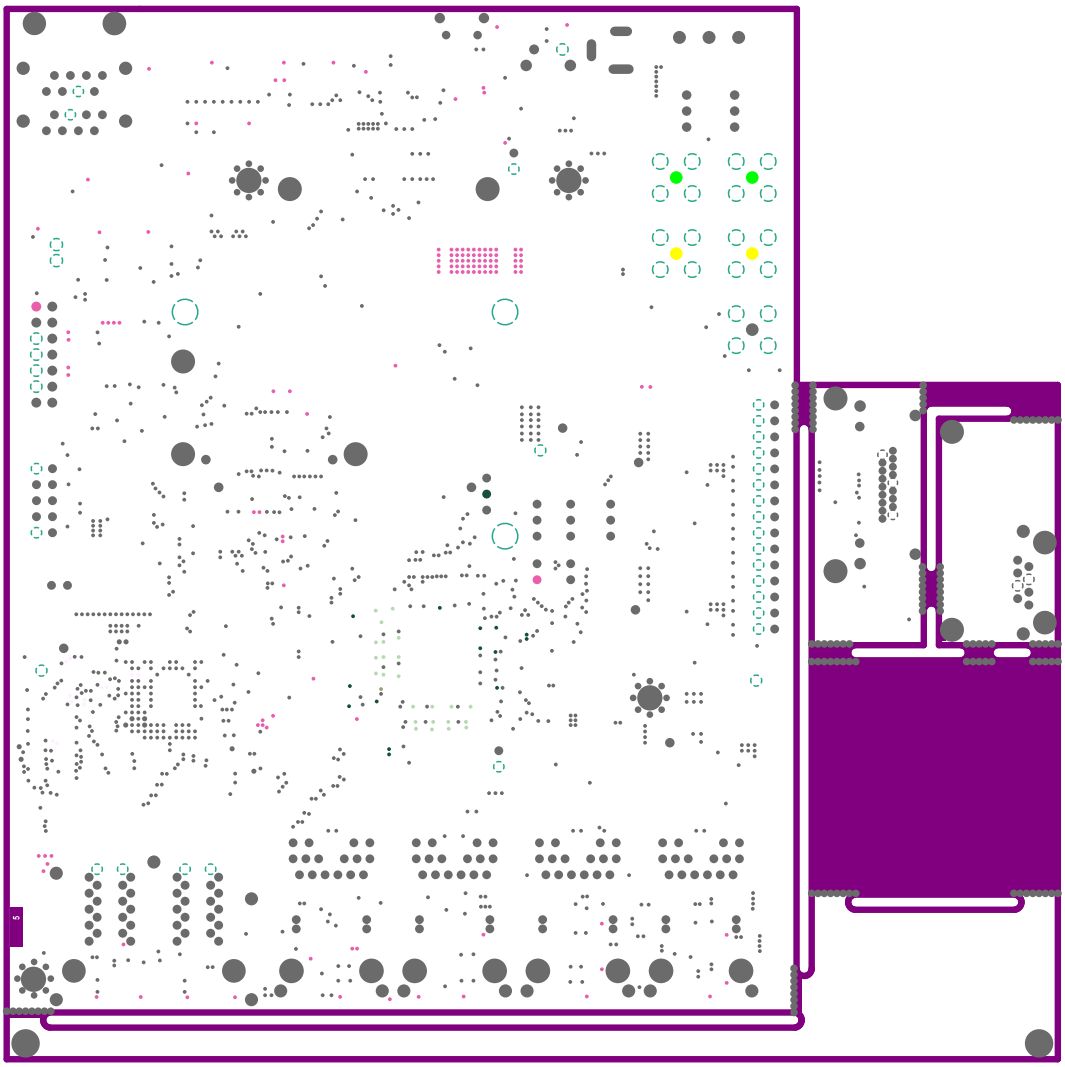


FIGURE B-7: BOTTOM COPPER

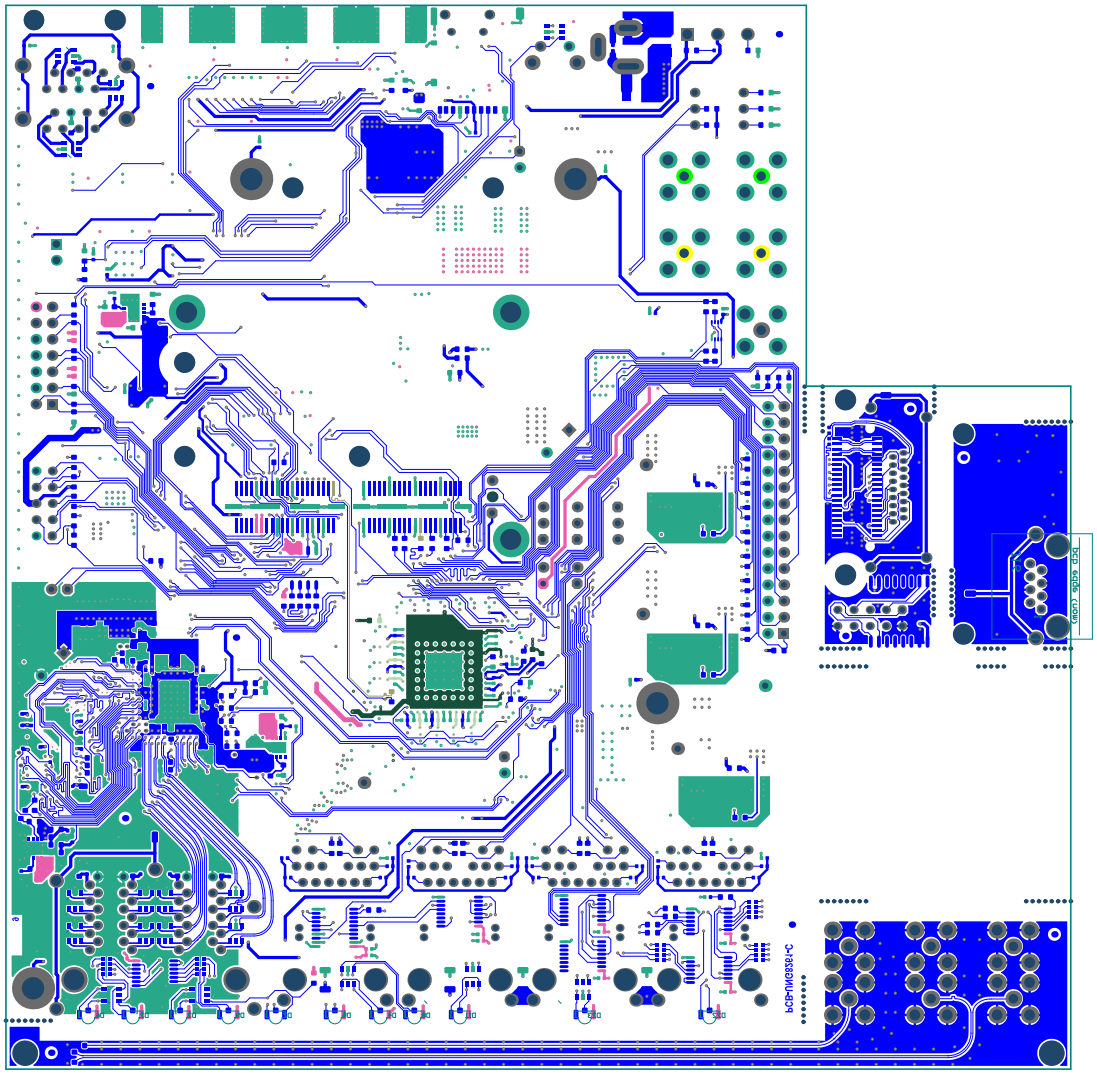


FIGURE B-8: BOTTOM SILK

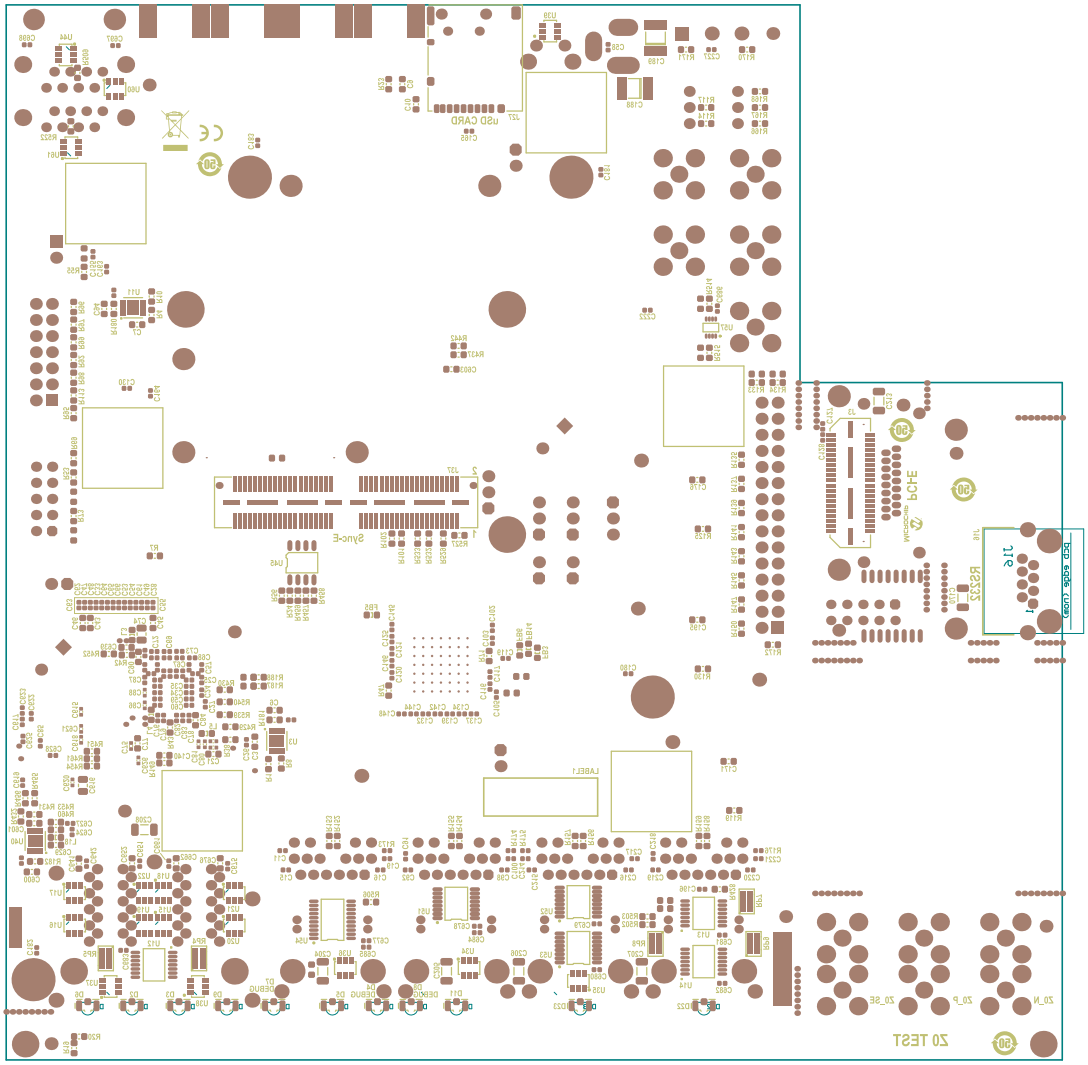
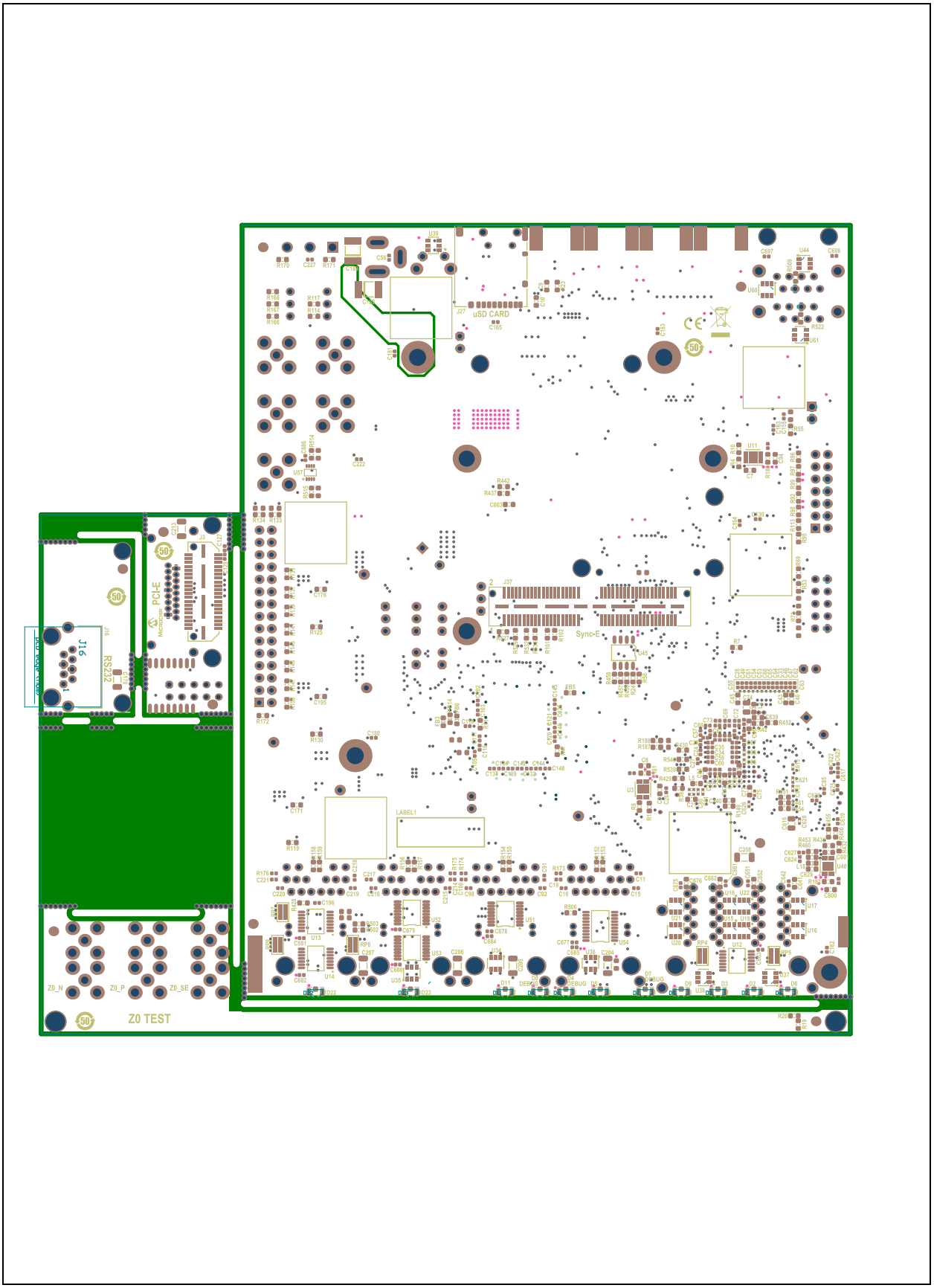


FIGURE B-9: BOTTOM SILK MIRRORED



Appendix C. Bill of Materials

C.1 INTRODUCTION

This appendix contains the EVB-LAN8814 Bill of Materials (BOM).

TABLE C-1: BILL OF MATERIALS

Item	Qty	Reference	Description	Populated	Manufacturer	Manufacturer Part Number
1	192	C1, C11, C15, C16, C17, C19, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C75, C76, C78, C79, C80, C81, C82, C83, C85, C86, C87, C88, C89, C91, C92, C96, C98, C99, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C111, C112, C113, C114, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124, C125, C126, C127, C128, C129, C130, C131, C132, C133, C134, C136, C137, C138, C139, C141, C142, C143, C144, C145, C146, C147, C148, C149, C150, C151, C163, C164, C165, C166, C173, C178, C179, C180, C181, C182, C183, C184, C185, C186, C187, C190, C194, C196, C198, C214, C215, C216, C217, C218, C219, C220, C221, C222, C227, C229, C231, C233, C235, C608, C614, C615, C617, C618, C619, C620, C621, C622, C623, C624, C625, C626, C627, C628, C630, C642, C651, C661, C675, C677, C678, C679, C680, C681, C682, C683, C684, C685, C686, C687, C688, C689, C694, C695, C696, C697, C698	CAP CER 0.1uF 50V 10% X7R SMD 0402	Yes	Taiyo Yuden	UMK105B7104KV-FR
2	9	C2, C171, C176, C195, C639, C641, C652, C662, C676	CAP CER 10000pF 50V 10% X7R SMD 0603	Yes	KEMET	C0603C103K5RACTU
3	20	C3, C6, C7, C9, C12, C13, C21, C43, C44, C45, C46, C77, C84, C90, C94, C135, C191, C600, C601, C629	CAP CER 10uF 10V 10% X5R SMD 0603	Yes	Samsung Electro-Mechanics	CL10A106KP8NNNC
4	1	C118 piggyback	CAP CER 22uF 6.3V 20% X5R SMD 0402	Yes	Kyocera AVX	CM05X5R226M06AH080
5	4	C4, C10, C140, C603	CAP CER 1uF 16V 10% X7R SMD 0603	Yes	Wurth Electronics Inc	885012206052
6	2	C5, C14	CAP ALU 470uF 25V 20% RAD P5D10H16	Yes	Nichicon	UHE1E471MPD6

TABLE C-1: BILL OF MATERIALS (CONTINUED)

Item	Qty	Reference	Description	Populated	Manufacturer	Manufacturer Part Number
7	10	C8, C172, C174, C175, C177, C197, C199, C200, C203, C209	CAP CER 22uF 25V 10% X5R SMD 1206	Yes	Samsung Electro-Mechanics, Murata Electronics North America Murata Electronics North America	CL31A226KAHNNNE, GRM31CR61E226KE15L
8	0	C18, C192, C201, C223	CAP CER 2200pF 10% 50V X7R SMD 0402 QEC-Q200	DNP	Murata Electronics North America	GCM155R71H222KA37D
9	4	C20, C193, C202, C224	CAP CER 4700pF 50V 10% X7R SMD 0603	Yes	KEMET	C0603C472K5RACTU
10	2	C74, C152	CAP CER 47uF 10V 20% X5R SMD 0805	Yes	TDK Corporation	C2012X5R1A476M125AC
11	0	C93, C95	CAP HiQ 12pF 50V 5% NP0 2.56GHz SMD 0402	DNP	Johanson Technology Inc	500R07S120JV4T
12	0	C97, C156, C157, C230, C232, C234, C236	CAP CER 0.1uF 50V 10% X7R SMD 0402	DNP	Taiyo Yuden	UMK105B7104KV-FR
13	0	C110	CAP CER 1000pF 50V 10% X7R SMD 0603	DNP	TDK	C1608X7R1H102K
14	1	C153	CAP TANT 220uF 4V 20% 1.8R SMD A	Yes	Vishay Sprague	TMCMA0G227MTRF
15	0	C154	CAP TANT 22uF 10V 10% 3Ohm SMD A	DNP	AVX	TAJA226K010R
16	1	C155	CAP CER 10pF 50V 5% NP0 SMD 0402	Yes	AVX Corporation	04025A100JAT2A
17	0	C158	CAP CER 10pF 50V 5% NP0 SMD 0402	DNP	AVX Corporation	04025A100JAT2A
18	1	C167	CAP CER 0.018uF 50V 10% X7R SMD 0603	Yes	KEMET	C0603C183K5RACTU
19	7	C170, C204, C205, C206, C207, C208, C213	CAP CER 1000pF 2KV 10% X7R SMD 1206	Yes	Johanson Dielectrics Inc	202R18W102KV4E
20	2	C188, C189	CAP CER 1000pF 3000V 10% X7R SMD 1812 AEC-Q200	Yes	KEMET	C1812C102KHRACAUTO
21	1	C225	CAP ALU 150uF 16V 20% SMD D8	Yes	Panasonic Electronic Components	EEE-FPC151XAP
22	3	C604, C609, C616	CAP CER 10uF 16V 10% X7R SMD 0805	Yes	Samsung Electro-Mechanics	CL21B106KOQNNNE
23	1	C605	CAP CER 2200pF 10% 50V X7R SMD 0402 QEC-Q200	Yes	Murata Electronics North America	GCM155R71H222KA37D
24	1	C607	CAP ALU 330uF 16V 20% 0.01R SMD L8.3W8.3H11D8	Yes	Würth Elektronik	875075355004
25	1	C610	CAP ALU 220uF 16V 20% SMD E	Yes	Panasonic	EEE-1CA221UP
26	2	D1, D17	DIO LED GREEN 2V 30mA 35mcd Clear SMD 0805	Yes	Lite-On	LTST-C170KGKT
27	12	D2, D3, D4, D5, D6, D7, D8, D9, D11, D12, D22, D23	DIO LED BI GREEN, RED 2V 80mA SMD R/A	Yes	Lite-On Inc.	LTST-S326KGJRKT
28	2	D13, D14	DIO TVS SMCJ12CA 12V 1500W SMD SMC	Yes	Littelfuse Inc.	SMCJ12CA
29	2	D15, D16	DIO TVS SMCJ12A 12V 1500W SMD SMC	Yes	Bourns Inc.	SMCJ12A
30	4	D24, D25, D26, D27	DIO SCTKY ARRAY BAS70-04-7-F 1V 15mA SOT-23-3	Yes	Diodes Incorporated	BAS70-04-7-F
31	2	F1, F2	RES FUSE BRD MNT 5A 125V Fast SMD L6.1W2.69	Yes	Littelfuse Inc.	0451005.MRL

TABLE C-1: BILL OF MATERIALS (CONTINUED)

Item	Qty	Reference	Description	Populated	Manufacturer	Manufacturer Part Number
32	9	FB3, FB5, FB6, FB7, FB9, FB11, FB12, FB13, FB14	FERRITE 220R @ 100MHz 2A SMD 0603	Yes	Murata Electronics North America	BLM18EG221SN1D
33	1	FB4	RES TKF 100R 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF1000V
34	1	HS1	MECH HW HEATSHINK SMD L16.51W16.59H8.89	MECH	Wakefield-Vette	LTN20069
35	1	J1	CON POWER 2.5mm 5.5mm SWITCH Slotted TH R/A	Yes	CUI Inc	PJ-002BH
36	1	J2	CON DSHAPED 076641 18 FEMALE TH VERT	Yes	Molex	0766410001
37	1	J3	CON HDR-0.8 Male 2x20 GOLD Q-Strip-QTE SMD VERT	Yes	Samtec Inc.	QTE-020-01-F-D-A
38	0	J4	CON HDR 2.54mm Male 2x5 Gold SHROUD 5.84 TH	DNP	On Shore Technology Inc.	302-S101
39	1	J5	CON HDR 2.54mm Male 2x5 Gold SHROUD 5.84 TH	Yes	On Shore Technology Inc.	302-S101
40	1	J6	CON USB2.0 MICRO-B FEMALE TH/SMD R/A	Yes	FCI	10118194-0001LF
41	1	J7	CON HDR-1.27 Male 2x25 Gold .12MH SMD VERT	Yes	Samtec Inc.	FTSH-125-01-L-DV-K-P-TR
42	1	J8	CON HDR-0.8 Female 2x20 GOLD Q-Strip-QSE SMD VERT	Yes	Samtec Inc.	QSE-020-01-L-D-A
43	5	J9, J18, J19, J25, J29	CON RF Coaxial SMA Female 2P TH VERT	Yes	Adam Tech	RF2-04A-T-00-50-G
44	4	J10, J12, J13, J15	CON HDR-2.54 Male 1x3 Gold 5.84MH TH VERT	Yes	FCI	68000-103HLF
45	1	J11	CON HDR-2.54 Male 2x7 Gold Shroud 6.35MH TH VERT	Yes	Samtec	TST-107-01-L-D
46	5	J14, J17, J32, J35, J38	CON HDR-2.54 Male 1x2 Gold 5.84MH TH VERT	Yes	FCI	77311-118-02LF
47	1	J16	CON MODULAR JACK RJ45 CAT5 TH R/A	Yes	Amphenol ICC (Commercial Products)	RJHSE-5380
48	1	J20	30 Positions Header, Unshrouded, Breakaway Connector 0.100" (2.54mm) Through Hole Gold	Yes	Wurth Electronics Inc.	61303021121
49	4	J21, J22, J23, J24	CON MODULAR JACK RJ45 10/100/1000 POE/MAGNETICS 2xLEDs SHIELD TH	Yes	Pulse Electronics Network	JXK0-0190NL
50	1	J26	CON HDR-1.27 Female 2x25 Gold SMD VERT	Yes	Samtec Inc.	FLE-125-01-G-DV-K
51	1	J27	CON FLASH microSD 8+2P Push-Push SMD	Yes	Hirose Electric Co Ltd	DM3AT-SF-PEJM5
52	1	J28	CON MODULAR JACK RJ45 10/100/1000 MAGNETICS 0xLEDs SHIELD SMD R/A	Yes	Abracon LLC	ARJM22A1-547-NN-EW2
53	1	J30	CON MODULAR JACK RJ45 CAT5 TH R/A	Yes	Amphenol ICC (Commercial Products)	RJSAE538002
54	4	J31, J33, J34, J36	CON RF Coaxial SMA Female 2P SMD Edge MNT	Yes	Cinch Connectivity Solutions Johnson	142-0701-851
55	1	J37	CON HDR-0.8 Female 2x40 GOLD Q-Strip-QSE SMD VERT	Yes	Samtec Inc.	QSE-040-01-F-D-A
56	1	J39	CON HDR-2.54 Male 1x2 Friction Lock MLX 0022272021 TH	Yes	Molex	0022272021
57	4	L1, L2, L6, L7	INDUCTOR 10uH 4A 20% SMD L6.65W6.65H3	Yes	Abracon LLC	ASPI-0630LR-100M-T15
58	5	L3, L4, L5, L18, L35	FERRITE 600R@100MHz 1A SMD 0603	Yes	TDK Corporation	MPZ1608S601ATA00
59	1	L13	CM CHOKE 1K 100MHz 0.014R SMD L12W11H6	Yes	TDK Corporation	ACM1211-102-2PL-TL01

TABLE C-1: BILL OF MATERIALS (CONTINUED)

Item	Qty	Reference	Description	Populated	Manufacturer	Manufacturer Part Number
60	1	L17	IND 4.7uH 8.5A 20% 0.0184R SMD SRP6050CA AEC-Q200	Yes	Bourns Inc.	SRP6050CA-4R7M
61	1	LABEL1	LABEL PCBA 18x6mm BarCode-AssyID-Rev-Serno	MECH	Sunrise Paper (M) Sdn Bhd	037268-5
62	6	PAD1, PAD2, PAD3, PAD4, PAD5, PAD6	MECH HW RUBBER PAD SQ Taper 0.50x0.50x0.23 Black	Yes	3M	SJ-5518
63	1	Q1	TRANS FET DUAL N+P HP8MA2T +-30V +-18A +-15A 0.0096R 0.0179R 7W HSOP-8	Yes	Rohm Semiconductor	HP8MA2TB1
64	1	Q2	TRANS FET P-CH NDS8434 20V 6.5A 2.5W SOIC-8	Yes	ON Semiconductor	NDS8434
65	1	R1	RES TKF 57.6k 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF5762V
66	0	R2, R9, R88, R89, R100, R108, R177, R519	RES TKF 0R 1/10W AEC-Q200 SMD 0603	DNP	Panasonic Electronic Components	ERJ-3GEY0R00V
67	9	R3, R109, R110, R119, R125, R130, R180, R181, R182	RES TKF 100k 1% 1/10W AEC-Q200 SMD 0603	Yes	Panasonic Electronic Components	ERJ-3EKF1003V
68	1	R4	RES TKF 66.5k 1% 1/10W SMD 0603	Yes	Panasonic Electronic Components	ERJ-3EKF6652V
69	1	R5	RES TKF 12k 1% 1/10W SMD 0603	Yes	Yageo	RC0603FR-0712KL
70	20	R6, R38, R48, R75, R76, R77, R78, R85, R86, R95, R97, R98, R99, R113, R170, R449, R451, R516, R517, R518	RES TKF 1k 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF1001V
71	23	R7, R35, R36, R39, R41, R43, R66, R73, R101, R102, R123, R127, R132, R160, R496, R520, R523, R524, R525, R527, R529, R532, R533	RES TKF 0R 1/10W AEC-Q200 SMD 0603	Yes	Panasonic Electronic Components	ERJ-3GEY0R00V
72	3	R8, R10, R432	RES TKF 11.3K 1% 1/10W SMD 0603	Yes	Stackpole Electronics Inc	RMCF0603FT11K3
73	10	R11, R55, R90, R94, R103, R105, R115, R124, R128, R162	RES TKF 3.01k 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF3011V
74	38	R12, R22, R50, R53, R56, R58, R59, R63, R68, R80, R81, R82, R92, R93, R114, R117, R118, R129, R133, R134, R135, R137, R139, R141, R143, R145, R147, R150, R161, R163, R164, R172, R440, R447, R450, R455, R509, R522	RES TKF 10k 1% 1/10W SMD 0603	Yes	Vishay	CRCW060310K0FKEA
75	14	R13, R21, R23, R44, R152, R153, R154, R155, R156, R157, R158, R159, R502, R503	RES TKF 330R 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF3300V
76	0	R14, R83, R136, R138, R140, R142, R144, R146, R148, R151, R178, R179, R189, R190, R191, R192, R446	RES TKF 10k 1% 1/10W SMD 0603	DNP	Vishay	CRCW060310K0FKEA

TABLE C-1: BILL OF MATERIALS (CONTINUED)

Item	Qty	Reference	Description	Populated	Manufacturer	Manufacturer Part Number
77	0	R15, R70, R72, R74, R448, R510, R513	RES TKF 1k 1% 1/10W SMD 0603	DNP	Panasonic	ERJ-3EKF1001V
78	5	R16, R42, R91, R106, R116	RES TKF 620R 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF6200V
79	3	R17, R530, R531	RES TKF 100R 1% 1/10W SMD 0402	Yes	Panasonic Electronic Components	ERJ-2RKF1000X
80	4	R18, R20, R104, R107	RES TKF 49.9R 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF49R9V
81	10	R19, R47, R79, R166, R167, R168, R428, R453, R460, R528	RES TKF 100R 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF1000V
82	11	R24, R49, R169, R193, R429, R430, R457, R458, R459, R514, R515	RES TKF 33R 1% 1/10W SMD 0603	Yes	ROHM	MCR03EZPFX33R0
83	0	R25, R28, R30, R31, R33, R34, R45	RES TKF 560R 1% 1/10W SMD 0603	DNP	Yageo	RC0603FR-07560RL
84	6	R26, R27, R29, R32, R46, R536	RES TKF 560R 1% 1/10W SMD 0603	Yes	Yageo	RC0603FR-07560RL
85	1	R37	RES TKF 220R 1% 1/10W SMD 0603	Yes	Yageo	RC0603FR-07220RL
86	1	R40	RES TKF 430R 1% 1/10W SMD AEC-Q200 0603	Yes	Panasonic	ERJ-3EKF4300V
87	7	R51, R54, R121, R122, R165, R187, R188	RES TKF 4.7K 1% 1/10W SMD 0603	Yes	Panasonic Electronic Components	ERJ-3EKF4701V
88	2	R52, R111	RES TKF 1.5k 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF1501V
89	0	R57, R60, R61, R62, R87	RES TKF 4.7K 1% 1/10W SMD 0603	DNP	Panasonic Electronic Components	ERJ-3EKF4701V
90	0	R64, R65	RES TKF 0R 1/10W SMD 0603	DNP	Panasonic	ERJ-3GSY0R00V
91	2	R67, R445	RES TKF 6.04k 1% 1/10W SMD 0603 AEC-Q200	Yes	Vishay / Dale	CRCW06036K04FKEA
92	2	R69, R96	RES TKF 120R 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF1200V
93	1	R71	RES TKF 200R 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF2000V
94	2	R84, R456	RES TKF 20k 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF2002V
95	5	R112, R126, R149, R435, R535	RES TKF 2k 1% 1/10W SMD 0603	Yes	Stackpole Electronics Inc	RMCF0603FT2K00
96	1	R120	RES TKF 26.1k 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF2612V
97	1	R131	RES TKF 17.4k 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF1742V
98	1	R171	RES TKF 20R 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF20R0V
99	8	R173, R174, R175, R176, R183, R184, R185, R186	RES TKF 0R 1/10W SMD 0402	Yes	Panasonic Electronic Components	ERJ-2GE0R00X
100	1	R431	RES TKF 30k 1% 1/10W SMD 0603	Yes	Stackpole Electronics Inc	RMCF0603FT30K0
101	1	R434	RES TKF 0.01R 1% 2W SMD 2512	Yes	TT Electronics	LRF2512-R01FW
102	2	R437, R442	RES TKF 2.0R 1% 1/10W SMD 0603	Yes	Vishay Dale	CRCW06032R00FKEA
103	3	R452, R454, R461	RES TKF 240R 1% 1/10W SMD 0603	Yes	Yageo	RC0603FR-07240RL
104	0	R505, R507, R508	RES TKF 330R 1% 1/10W SMD 0603	DNP	Panasonic	ERJ-3EKF3300V

TABLE C-1: BILL OF MATERIALS (CONTINUED)

Item	Qty	Reference	Description	Populated	Manufacturer	Manufacturer Part Number
105	1	R506	RES TKF 180R 1% 1/10W SMD 0603	Yes	Yageo	RC0603FR-07180RL
106	2	R512, R526	RES TKF 1k 1% 1/10W SMD 0402	Yes	Panasonic	ERJ-2RKF1001X
107	1	R534	RES TKF 3.32k 1% 1/10W SMD 0603	Yes	ROHM	MCR03EZPFX3321
108	2	R539, R540	RES TKF 47R 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF47R0V
109	5	RP4, RP5, RP7, RP8, RP9	RES NET TKF 330R 5% 1/16W SMD 1206x4	Yes	Panasonic Electronic Components	EXB-38V331JV
110	1	SW1	SWITCH TACT SPST 12V 50mA Sq Plunger for Cap PTS645VJK612LFS RA TH	Yes	C&K	PTS645VJK612LFS
111	1	SW2	SWITCH DIP 3 SPST 24VDC 25MA DSS-03-B-PF TH	Yes	C&K	BDB03
112	1	SW3	SWITCH SLIDE SPDT 120V 6A 1101M2S3CQE2 TH	Yes	C&K Components	1101M2S3CQE2
113	0	TP1, TP2, TP4, TP5, TP22, TP23, TP36, TP37, TP38, TP39, TP40	CON TP TAB Silver Mini 1.6x0.8 SMD	DNP	Harwin Inc.	S2761-46R
114	0	TP3	MISC, TEST POINT PC MINI, 0.040" D YELLOW	DNP	Keystone	5004
115	0	TP6, TP7, TP8, TP9, TP10, TP11	CON RF Coaxial SMA Female 2P TH VERT	DNP	Adam Tech	RF2-04A-T-00-50-G
116	3	TP12, TP13, TP14	MISC, TEST POINT MULTI PURPOSE MINI RED	Yes	Keystone	5000
117	1	TP41	MISC, TEST POINT MULTI PURPOSE MINI BLACK	Yes	Keystone	5001
118	1	U1	MCHP ANALOG SUPERVISOR 0.4V to 5.5V MIC2790N-04VD6 SOT-23-3	Yes	Microchip Technology	MIC2790N-04VD6
119	4	U2, U5, U26, U27	MCHP ANALOG SWITCHER Buck 0.925V to 16.2V NX7102IDETR SOIC-8-EP	Yes	Microchip Technology	NX7102IDETR
120	3	U3, U11, U40	MCHP ANALOG LDO 0.8V-5V MCP1727T-ADJE/MF DFN-8	Yes	Microchip	MCP1727T-ADJE/MF
121	1	U4	MCHP INTERFACE ETHERNET VSC7514XKS BGA-256	Yes	Microchip Technology	VSC7514XKS
122	1	U6	MCHP ANALOG SUPERVISOR 2.63V MIC6315-26D2UY-TR SOT-143	Yes	Microchip Technology	MIC6315-31D4UY-TR
123	0	U7	IC MEMORY MX25L25635F FLASH 256M SOP-16	DNP	Macronix	MX25L25635FMI-10G
124	1	U8	IC MEMORY MX25L25635F FLASH 256M SOP-16	Yes	Macronix	MX25L25635FMI-10G
125	0	U9	MCHP MEMORY SERIAL FLASH 8M 80MHz SST25VF080B-50-4I-S2AF SOIC-8	DNP	Microchip Technology	SST25VF080B-50-4I-S2AF
126	1	U10	MCHP INTERFACE USB I2C UART MCP2221A-I/ST TSSOP-14	Yes	Microchip Technology	MCP2221A-I/ST
127	3	U12, U13, U14	IC LOGIC 8-Bit Parallel-Out SHIFT REGISTER TSSOP-14	Yes	Texas Instruments	SN74HC164PWR
128	17	U15, U16, U17, U18, U19, U20, U21, U22, U34, U35, U36, U37, U38, U39, U44, U60, U61	DIO TVS TVS3V3L4U 3.3V SMD SC74-6	Yes	Infineon Technologies	TVS3V3L4UE6327HTSA1
129	1	U23	IC TRANSCEIVER MAX3221 RS-232 Driver SSOP-16	Yes	Maxim Integrated	MAX3221ECAE+T

TABLE C-1: BILL OF MATERIALS (CONTINUED)

Item	Qty	Reference	Description	Populated	Manufacturer	Manufacturer Part Number
130	1	U24	MCHP ANALOG LDO 3.3V 300mA MIC5504-3.3YMT DFN-4	Yes	Microchip Technology	MIC5504-3.3YMT
131	1	U25	MCHP INTERFACE ETHERNET LAN8814 QUAD 10BASE-T/100BASETX/1000BASE-T PHY TQFP-128	Yes	Microchip	LAN8814/ZMX
132	1	U41	MCHP ANALOG SWITCHER BUCK 1.8V-12V MIC2193 SOIC-8	Yes	Microchip Technology	MIC2193YM
133	1	U42	IC MEMORY W25N01GV FLASH 1G SPI WSON-8	Yes	Winbond Electronics	W25N01GVZEIG TR
134	1	U43	IC MEMORY MT41K256M16TW SDRAM DDR3L TFBGA-96	Yes	Micron Technology Inc.	MT41K256M16TW-093:P
135	1	U45	MCHP CLOCK GENERATION BUFFER1:4 0, 150Mhz SOP-8	Yes	Microchip Technology	PL133-47SI
136	3	U51, U52, U53	IC LOGIC SN74AHC594PWR Shift Register TSSOP-16	Yes	Texas Instruments	SN74AHC594PWR
137	1	U54	IC BUFFER MM74HC240 INV TRI-STATE TSSOP-20	Yes	ON Semiconductor	MM74HC240MTCX
138	3	U56, U58, U59	IC TRANSCEIVER RS-422/485 ISL3180EIBZ SOIC-14	Yes	Renesas Electronics America Inc	ISL3180EIBZ
139	1	U57	IC BUFFER NC7WZ125K8X DUAL NON-INV VFSOP-8	Yes	ON Semiconductor	NC7WZ125K8X
140	1	Y3	MCHP CLOCK OSCILLATOR SINGLE 25MHZ VDFN-4	Yes	Microchip Technology	VC-820-EAE-KAAN-25M000000
141	1	Y6	MCHP CLOCK OSCILLATOR SINGLE 125Mhz MX573EBC125M000 LGA-6	Yes	Microchip Technology	MX573EBC125M000-TR
142	1	Y8	MCHP CLOCK OSCILLATOR TCXO 125Mhz MXT573ABC125M000 LGA-6	Yes	Microchip	MXT573ABC125M000

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