MCP2035

Analog Front-End Device for BodyCom Applications

Device Features:

- Single Analog Input Pin for Signal Detection
- High Input Detection Sensitivity (3 mV_{PP}, typical)
- High Modulation Depth Sensitivity (as low as 8%)
- Three Output Type Selections:
  - Demodulated Data
  - Carrier Clock
  - Received Signal Strength Indicator (RSSI)
- Input Carrier Frequency: 125 kHz, typical
- Input Data Rate: 10 Kbps, maximum
- 8 Internal Configuration Registers
- Bidirectional Transponder Communication via the same input pin (LF talk-back)
- Programmable Antenna Tuning Capacitance (up to 63 pF, 1 pF/step)
- Programmable Output Enable Filter
- Low Standby Current: 2 µA, typical
- Low Operating Current: 10 µA, typical
- Serial Peripheral Interface (SPI) with external devices
- Industrial and Extended Temperature Range: -40°C to +85°C (Industrial)

Typical Applications:

- BodyCom Applications
- Security Industry Applications
- Automotive Industry Applications

Description:

The MCP2035 is a single-channel, stand-alone Analog Front-End (AFE) device for low-frequency (LF) signal detection and low-power short range transponder applications, such as BodyCom communications.

The device can detect an input signal with amplitude as low as ~1 mV_{PP}, and can demodulate an amplitude-modulated input signal with as low as 8% modulation depth. The device can also transmit data (LF talk-back) by clamping and unclamping the input LC antenna voltage.

The device can output demodulated data, carrier clock or RSSI current, depending on the output-type selection configuration register bit settings. The demodulated data and carrier clock outputs are available on the LFDATA pin, while the RSSI output is available on the RSSI pin. The RSSI current output is linearly proportional to the input signal strength.

The device has programmable internal tuning capacitors for the input channel. The user can program the input tuning capacitors up to 63 pF, 1 pF per step. The internal tuning capacitors can be used effectively for fine-tuning of the external LC resonant circuit.

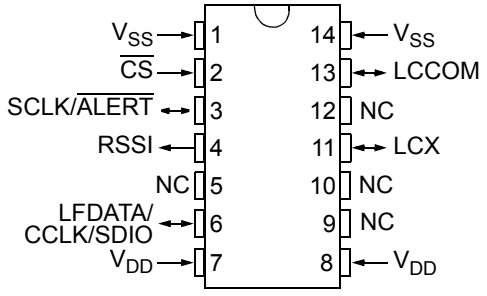
The device has eight volatile internal configuration registers for dynamic configurations of the device operation on-the-fly. All registers are readable and programmable using the serial SPI commands, except the read-only STATUS register.

The device is optimized for very low current consumption and has various battery-saving low-power modes (Sleep, Standby, Active).

This device is available in a 14-pin TSSOP package.

Package Type:

MCP2035
TSSOP



NOTES:

1.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +6.5V
Voltage on all other pins with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Maximum current out of V_{SS} pin ..... 300 mA
Maximum current into V_{DD} pin ..... 250 mA
Maximum LC Input Voltage (LCX) loaded, with device ..... 10.0 V_{PP}
Maximum LC Input Voltage (LCX) unloaded, without device ..... 700.0 V_{PP}
Maximum Input Current (rms) into device (LCX Input Channel) ..... 10 mA
Human Body ESD rating ..... 2000 (minimum) V
Machine Model ESD rating ..... 200 (minimum) V

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Standard Operating Conditions (unless otherwise stated), Operating temperature: -40°C ≤ T_A ≤ +85°C, LCX Input Signal: Sinusoidal 300 mV_{PP}, Carrier Frequency = 125 kHz, LCCOM connected to V_{SS}, **Bits <3:1>** of Configuration Register 0: LCXEN = 0, LCZEN = LCYEN = 1.

Parameters	Sym.	Min.	Typ.(2)	Max.	Units	Conditions
Supply Voltage	V_{DD}	2.0	3.0	3.6	V	
V_{DD} Start Voltage to ensure internal Power-on Reset signal	V_{POR}	—	—	1.8	V	
Modulation Transistor-on Resistance	R_M	—	50	100	Ω	V_{DD} = 3.0V
Active Current (detecting signal) 1 LC Input Channel (LCX) is Receiving Signal	I_{ACT}	—	10	—	µA	$\overline{CS}$ = V_{DD} Input = Continuous Wave (CW) Amplitude = 300 mV_{PP} LCX input channel is enabled.
Standby Current (wait to detect signal)	I_{STDBY}	—	2	5	µA	$\overline{CS}$ = V_{DD}; $\overline{ALERT}$ = V_{DD} LCX input channel is enabled.
Sleep Current	I_{SLEEP}	—	0.2	1	µA	$\overline{CS}$ = V_{DD}; $\overline{ALERT}$ = V_{DD}
Analog Input Leakage Current on LCX and LCCOM pins	I_{AIL}	—	—	±1	µA	V_{DD} = 3.6V, V_{SS} ≤ V_{IN} ≤ 1V with respect to ground. Internal tuning capacitors are switched off, tested in Sleep mode
Digital Input Low Voltage	V_{IL}	V_{SS}	—	0.3 V_{DD}	V	SCLK, SDI, $\overline{CS}$
Digital Input High Voltage	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	SCLK, SDI, $\overline{CS}$

Note 1: These parameters are characterized but not tested.
2: Data in "Typ." column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
3: Negative current is defined as current sourced by the pin.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Standard Operating Conditions (unless otherwise stated), Operating temperature: -40°C ≤ T_A ≤ +85°C, LCX Input Signal: Sinusoidal 300 mV_{PP}, Carrier Frequency = 125 kHz, LCCOM connected to V_{SS}, **Bits <3:1>** of Configuration Register 0: LCXEN = 0, LCZEN = LCYEN = 1.

Parameters	Sym.	Min.	Typ.(2)	Max.	Units	Conditions
Digital Input Leakage Current SDI, SCLK, $\overline{CS}$ **(Note 3)**	I_{IL}	—	—	±1	µA	V_{DD} = 3.6V $V_{SS} \le V_{PIN} \le V_{DD}$ $V_{PIN} \le V_{DD}$
Digital Output Low Voltage $\overline{ALERT}$, LFDATA/SDIO	V_{OL}	—	—	V_{SS} + 0.4	V	Analog Front-End section I_{OL} = 1.0 mA, V_{DD} = 2.0V
Digital Output High Voltage $\overline{ALERT}$, LFDATA/SDIO	V_{OH}	V_{DD} - 0.5	—	—	V	I_{OH} = -400 µA, V_{DD} = 2.0V
Digital Input Pull-Up Resistor $\overline{CS}$, SCLK	R_{PU}	50	200	350	kΩ	V_{DD} = 3.6V

Note 1: These parameters are characterized but not tested.

2: Data in "Typ." column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

3: Negative current is defined as current sourced by the pin.

AC CHARACTERISTICS

Electrical Specifications: Standard Operating Conditions (unless otherwise stated), Supply Voltage: 2.0V ≤ V_{DD} ≤ 3.6V, Operating temperature: -40°C ≤ T_A ≤ +85°C, LCCOM connected to V_{SS}, LCX Input Signal: Sinusoidal 300 mV_{PP}, Carrier Frequency = 125 kHz, **Bits <3:1>** of Configuration Register 0: LCXEN = `0`, LCZEN = LCYEN = `1`.

Parameters	Sym.	Min.	Typ(2)	Max.	Units	Conditions
Input Sensitivity	V_{SENSE}	1	3.0	6	mV_{PP}	V_{DD} = 3.0V Output enable filter disabled AGCSIG = `0`; MODMIN = `00` (33% modulation depth setting) Input = Continuous Wave (CW) Output = Logic level transition from low-to-high at sensitivity level for CW input.
Coil de-Q'ing Voltage - RF Limiter (R_{FLM}) must be active	V_{DE_Q}	3	—	5	V	V_{DD} = 3.0V, Force I_{IN} = 5 μA (worst case)
RF Limiter Turn-on Resistance at LCX pin	R_{FLM}	—	300	700	Ω	V_{DD} = 2.0V, V_{IN} = 8 V_{DC}
Sensitivity Reduction	S_{ADJ}	—	0	—	dB	V_{DD} = 3.0V No sensitivity reduction selected Maximum reduction selected Monotonic increment in attenuation value from setting = `0000` to `1111` by design
		—	-30	—	dB	
Minimum Modulation Depth						
60% setting	V_{IN_MOD}	—	60	84	%	V_{DD} = 3.0V See **Section 5.20 "Minimum Modulation Depth Requirement for Input Signal"**. See Modulation Depth Definition in Figure 5-5.
33% setting		—	33	49	%	
14% setting		—	14	26	%	
8%			8		%	
Carrier frequency	$F_{CARRIER}$	—	125	—	kHz	
Input modulation frequency	F_{MOD}	—	—	10	kHz	Input data rate with NRZ data format. V_{DD} = 3.0V Minimum modulation depth setting = 33% Input conditions: Amplitude = 300 mV_{PP} Modulation depth = 100%

Note 1: Parameter is characterized but not tested.

2: Data in "Typ." column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

3: Required output enable filter high time must account for input path analog delays (= T_{OEH} - T_{DR} + T_{DF}).

4: Required output enable filter low time must account for input path analog delays (= T_{OEL} + T_{DR} - T_{DF}).

AC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Standard Operating Conditions (unless otherwise stated), Supply Voltage: 2.0V ≤ V_{DD} ≤ 3.6V, Operating temperature: -40°C ≤ T_A ≤ +85°C, LCCOM connected to V_{SS}, LCX Input Signal: Sinusoidal 300 mV_{PP}, Carrier Frequency = 125 kHz, **Bits <3:1>** of Configuration Register 0: LCXEN = 0, LCZEN = LCYEN = 1.

Parameters	Sym.	Min.	Typ[2]	Max.	Units	Conditions
LCX Tuning Capacitor	C_{TUNX}	—	0	—	pF	V_{DD} = 3.0V, Config. Reg. 1, bits <6:1> Setting = 000000
		44	59	82	pF	63 pF ±30% Config. Reg. 1, bits <6:1> Setting = 111111 63 steps, approx. 1 pF/step Monotonic increment in capacitor value from setting = 000000 to 111111 by design
Q of Internal Input Tuning Capacitors	Q_C	50[1]	—	—		
Demodulator Charge Time (delay time of demodulated output to rise)	T_{DR}	—	50	—	µs	V_{DD} = 3.0V Minimum modulation depth setting = 33% Input conditions: Amplitude = 300 mV_{PP} Modulation depth = 100%
Demodulator Discharge Time (delay time of demodulated output to fall)	T_{DF}	—	50	—	µs	V_{DD} = 3.0V MOD depth setting = 33% Input conditions: Amplitude = 300 mV_{PP} Modulation depth = 100%
Rise time of LFDATA	TR_{LFDATA}	—	0.5	—	µs	V_{DD} = 3.0V. Time is measured from 10% to 90% of amplitude
Fall time of LFDATA	TF_{LFDATA}	—	0.5	—	µs	V_{DD} = 3.0V Time is measured from 10% to 90% of amplitude
Automatic Gain Control (AGC) stabilization time (T_{AGC} + T_{PAGC})	T_{STAB}	4	—	—	ms	
AGC initialization time	T_{AGC}	—	3.5	—	ms	
High time after AGC initialization time	T_{PAGC}	—	62.5	—	µs	

Note 1: Parameter is characterized but not tested.

2: Data in "Typ." column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

3: Required output enable filter high time must account for input path analog delays (= T_{OEH} - T_{DR} + T_{DF}).

4: Required output enable filter low time must account for input path analog delays (= T_{OEL} + T_{DR} - T_{DF}).

AC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Standard Operating Conditions (unless otherwise stated), Supply Voltage: 2.0V ≤ V_{DD} ≤ 3.6V, Operating temperature: -40°C ≤ T_A ≤ +85°C, LCCOM connected to V_{SS}, LCX Input Signal: Sinusoidal 300 mV_{PP}, Carrier Frequency = 125 kHz, **Bits <3:1>** of Configuration Register 0: LCXEN = 0, LCZEN = LCYEN = 1.

Parameters	Sym.	Min.	Typ(2)	Max.	Units	Conditions
Gap time after AGC stabilization time	T_{GAP}	200	—	—	µs	
Time element of pulse	T_E	100	—	—	µs	Minimum pulse width
Time from exiting Sleep or POR to being ready to receive signal	T_{RDY}	—	—	50(1)	ms	
Minimum time AGC level must be held after receiving AGC Preserve command	T_{PRES}	5(1)	—	—	ms	AGC level must not change more than 10% during T_{PRES}
Internal RC oscillator frequency	F_{OSC}	27	32	35.5	kHz	Internal clock trimmed at 32 kHz during test
Inactivity Timer time-out	T_{INACT}	13.5	16	17.75	ms	512 cycles of RC oscillator @ F_{OSC}
Alarm Timer time-out	T_{ALARM}	27	32	35.5	ms	1024 cycles of RC oscillator @ F_{OSC}
Input Resistance (LCX)	R_{IN}	—	800(1)	—	kΩ	LCCOM grounded, V_{DD} = 3V, $F_{CARRIER}$ = 125 kHz
Input Parasitic Capacitance (LCX)	C_{IN}	—	24(1)	—	pF	LCCOM grounded, V_{DD} = 3V, $F_{CARRIER}$ = 125 kHz
Minimum output enable filter high time **OEH (Bits Config0<8:7>)**						
01 = 1 ms	T_{OEH}	32 (~1 ms)	—	—	clock count	RC oscillator = F_{OSC} (see F_{OSC} specification for variations). Viewed from the pin input: **(Note 3)**
10 = 2 ms		64 (~2 ms)	—	—		
11 = 4 ms		128 (~4 ms)	—	—		
00 = Filter Disabled		—	—	—		
Minimum output enable filter low time **OEL (Bits Config0<6:5>)**						
00 = 1 ms	T_{OEL}	32 (~1 ms)	—	—	clock count	RC oscillator = F_{OSC} Viewed from the pin input: **(Note 4)**
01 = 1 ms		32 (~1 ms)	—	—		
10 = 2 ms		64 (~2 ms)	—	—		
11 = 4 ms		128 (~4 ms)	—	—		

Note 1: Parameter is characterized but not tested.

2: Data in "Typ." column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

3: Required output enable filter high time must account for input path analog delays (= T_{OEH} - T_{DR} + T_{DF}).

4: Required output enable filter low time must account for input path analog delays (= T_{OEL} + T_{DR} - T_{DF}).

AC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Standard Operating Conditions (unless otherwise stated), Supply Voltage: 2.0V ≤ V_{DD} ≤ 3.6V, Operating temperature: -40°C ≤ T_A ≤ +85°C, LCCOM connected to V_{SS}, LCX Input Signal: Sinusoidal 300 mV_{PP}, Carrier Frequency = 125 kHz, **Bits <3:1>** of Configuration Register 0: LCXEN = 0, LCZEN = LCYEN = 1.

Parameters	Sym.	Min.	Typ[2]	Max.	Units	Conditions
Maximum output enable filter period **OEH OEL T_{OEH} T_{OEL}**						
01 00 = 1 ms 1 ms (Filter 1)	T_{OET}	—	—	96 (~3 ms)	clock count	RC oscillator = F_{OSC}
01 01 = 1 ms 1 ms (Filter 1)		—	—	96 (~3 ms)		
01 10 = 1 ms 2 ms (Filter 2)		—	—	128 (~4 ms)		
01 11 = 1 ms 4 ms (Filter 3		—	—	192 (~6 ms)		
10 00 = 2 ms 1 ms (Filter 4)		—	—	128 (~4 ms)		
10 01 = 2 ms 1 ms (Filter 4)		—	—	128 (~4 ms)		
10 10 = 2 ms 2 ms (Filter 5)		—	—	160 (~5 ms)		
10 11 = 2 ms 4 ms (Filter 6)		—	—	250 (~8 ms)		
11 00 = 4 ms 1 ms (Filter 7)		—	—	192 (~6 ms)		
11 01 = 4 ms 1 ms (Filter 7)		—	—	192 (~6 ms)		
11 10 = 4 ms 2 ms (Filter 8)		—	—	256 (~8 ms)		
11 11 = 4 ms 4 ms (Filter 9)		—	—	320 (~10 ms)		
00 XX = Filter Disabled		—	—	—		LFDATA output appears as long as input signal level is greater than V_{SENSE}.
RSSI current output	I_{RSSI}	—	0.65	2	µA	V_{IN} = 37 mV_{PP}
		6	12	20.3	µA	V_{IN} = 370 mV_{PP}
		—	100	—	µA	V_{DD} = 3.0V, V_{IN} = 0 to 4 V_{PP} Linearly increases with input signal amplitude. Tested at V_{IN} = 37 mV_{PP}, 100 mV_{PP}, and 370 mV_{PP} at +25ºC.
RSSI current linearity	ILR_{RSSI}	-15	—	15	%	Tested at room temperature only (see Equation 5-1 and Figure 5-7 for test method).

Note 1: Parameter is characterized but not tested.

2: Data in "Typ." column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

3: Required output enable filter high time must account for input path analog delays (= T_{OEH} - T_{DR} + T_{DF}).

4: Required output enable filter low time must account for input path analog delays (= T_{OEL} + T_{DR} - T_{DF}).

SPI TIMING

Electrical Specifications: Standard Operating Conditions (unless otherwise stated),
Supply Voltage: 2.0V ≤ V_{DD} ≤ 3.6V, Operating temperature: -40°C ≤ T_A ≤ +85°C,
LCX Input Signal: Sinusoidal 300 mV_{PP}, Carrier Frequency: 125 kHz, LCCOM connected to V_{SS}

Parameters	Sym	Min	Typ(1)	Max	Units	Conditions
SCLK Frequency	F_{SCLK}	—	—	3	MHz	
$\overline{CS}$ fall to first SCLK edge setup time	T_{CSSC}	100	—	—	ns	
SDI setup time	T_{SU}	30	—	—	ns	
SDI hold time	T_{HD}	50	—	—	ns	
SCLK high time	T_{HI}	150	—	—	ns	
SCLK low time	T_{LO}	150	—	—	ns	
SDO setup time	T_{DO}	—	—	150	ns	
SCLK last edge to $\overline{CS}$ rise setup time	T_{SCCS}	100	—	—	ns	
$\overline{CS}$ high time	T_{CSH}	500	—	—	ns	
$\overline{CS}$ rise to SCLK edge setup time	T_{CS1}	50	—	—	ns	
SCLK edge to $\overline{CS}$ fall setup time	T_{CS0}	50	—	—	ns	SCLK edge when $\overline{CS}$ is high
Rise time of SPI data (SPI Read command)	TR_{SPI}	—	10	—	ns	V_{DD} = 3.0V; time is measured from 10% to 90% of amplitude
Fall time of SPI data (SPI Read command)	TF_{SPI}	—	10	—	ns	V_{DD} = 3.0V; time is measured from 90% to 10% of amplitude

Note 1: Data in “Typ.” column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = 2.0V to 3.6V, V_{SS} = GND.

Parameters	Symbol	Min	Typical	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = 3V, Carrier Frequency = 125 kHz, LCCOM = connected to V_{SS}, T_A = +25°C.

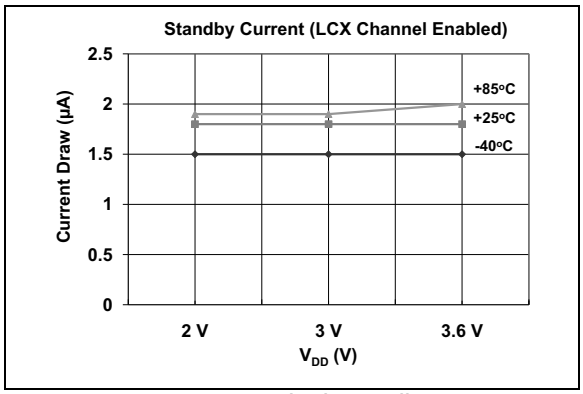


FIGURE 2-1: *Typical Standby Current.*

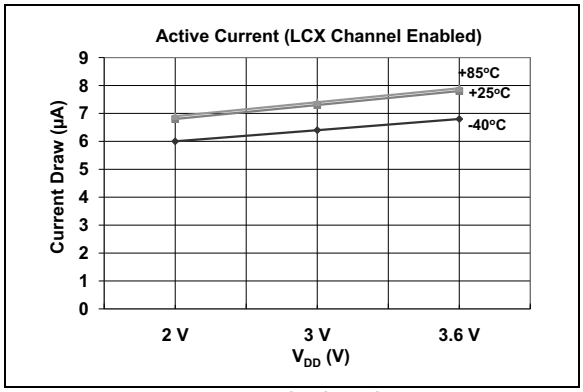


FIGURE 2-2: *Typical Active Current.*

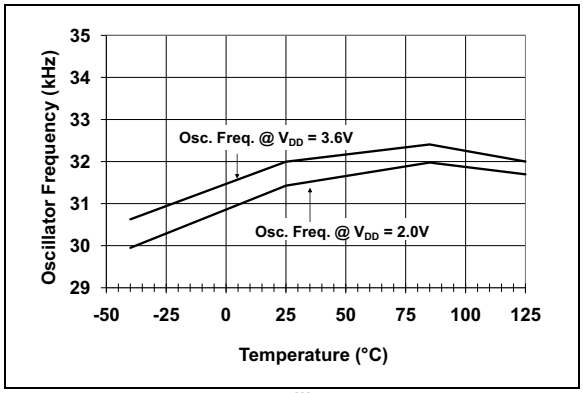


FIGURE 2-3: *Oscillator Frequency vs. Temperature, V_{DD} = 3.6V and 2.0V.*

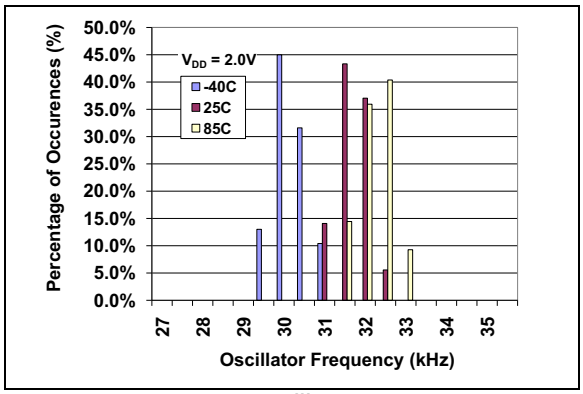


FIGURE 2-4: *Oscillator Frequency Histograms vs. Temperature, V_{DD} = 2V.*

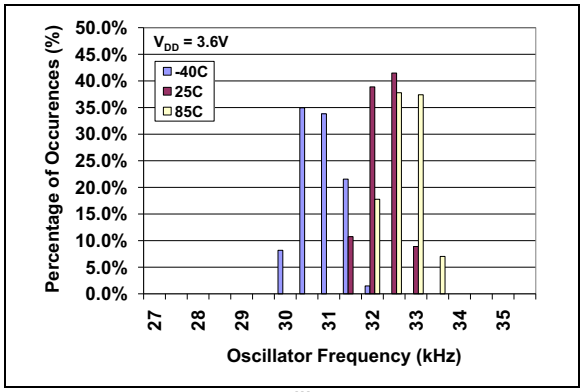


FIGURE 2-5: *Oscillator Frequency Histograms vs. Temperature at V_{DD} = 3V.*

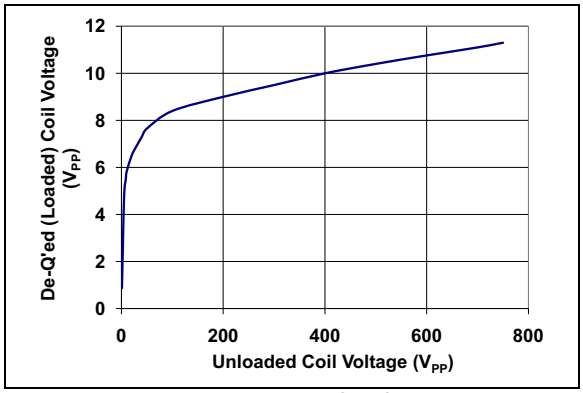


FIGURE 2-6: *De-Q'ed Voltage vs. Unloaded Coil Voltage.*

Note: Unless otherwise indicated, V_{DD} = 3V, Carrier Frequency = 125 kHz, LCCOM = connected to V_{SS}.

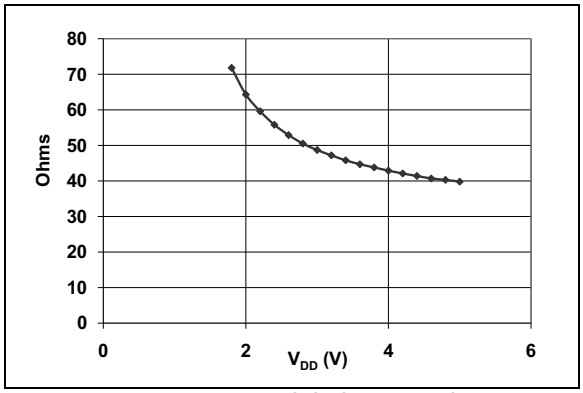


FIGURE 2-7: *Modulation Transistor-on Resistance (+25°C).*

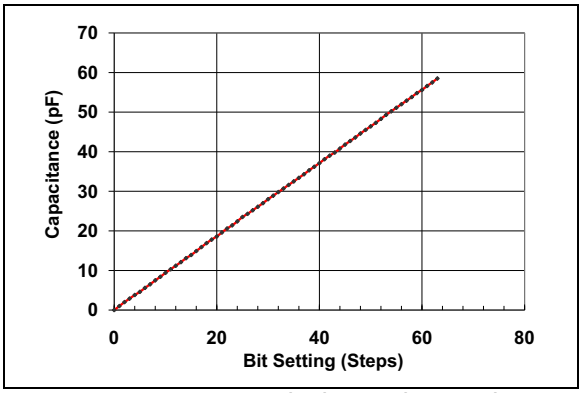


FIGURE 2-10: *Typical Tuned Capacitance Value vs. Configuration Register Bit Setting (V_{DD} = 3V, Temperature = +25°C).*

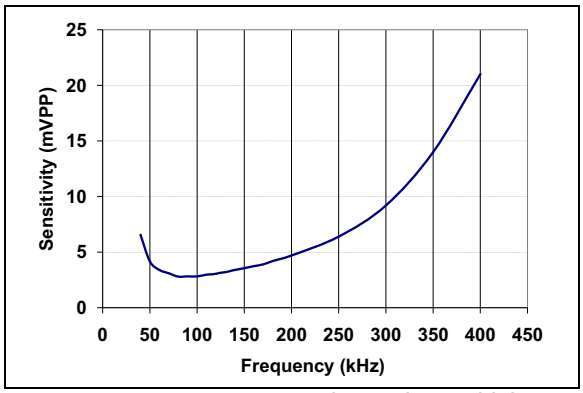


FIGURE 2-8: *Input Channel Sensitivity vs. Bandwidth.*

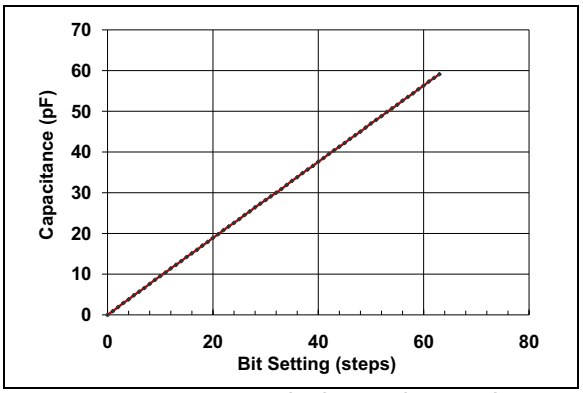


FIGURE 2-11: *Typical Tuned Capacitance Value vs. Configuration Register Bit Setting (V_{DD} = 3V, Temperature = -40°C).*

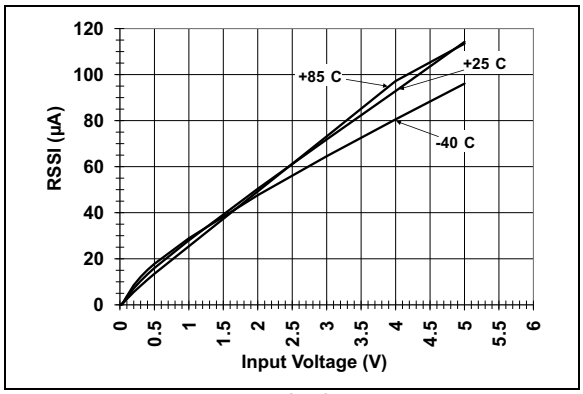


FIGURE 2-9: *Typical RSSI Output Current vs. Input Signal Strength.*

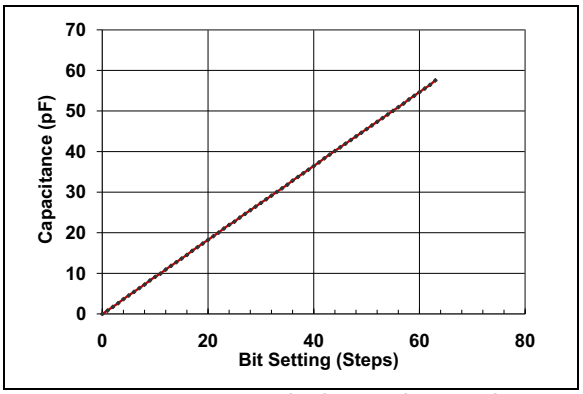
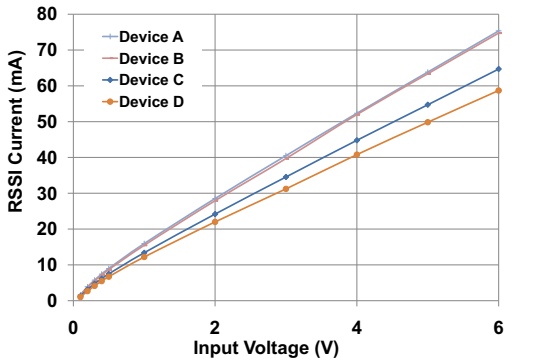


FIGURE 2-12: *Typical Tuned Capacitance Value vs. Configuration Register Bit Setting (V_{DD} = 3V, Temperature = +85°C).*

Note: Unless otherwise indicated, V_{DD} = 3V, Carrier Frequency = 125 kHz, LCCOM = connected to V_{SS}.



Note: Equal amplitude is applied to each device.

FIGURE 2-13: *Examples of RSSI Output Current Variations Between Device to Device at Room Temperature.*

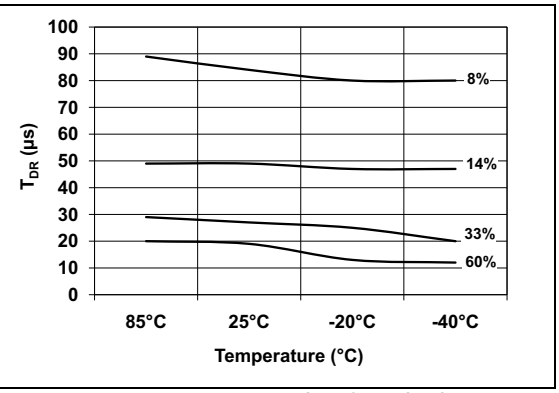


FIGURE 2-14: *Example of Typical T_{DR} Changes over Temperature.*
Input Signal Condition: Amplitude = 300 mV_{PP}, Modulation Depth = 100 %.

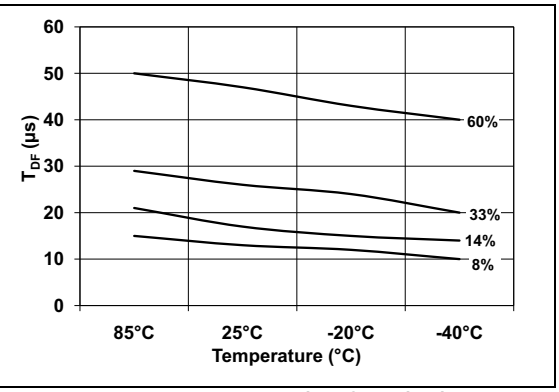


FIGURE 2-15: *Example of Typical T_{DF} Changes over Temperature.*
Input Signal Condition: Amplitude = 300 mV_{PP}, Modulation Depth = 100 %.

2.1 Performance Plots

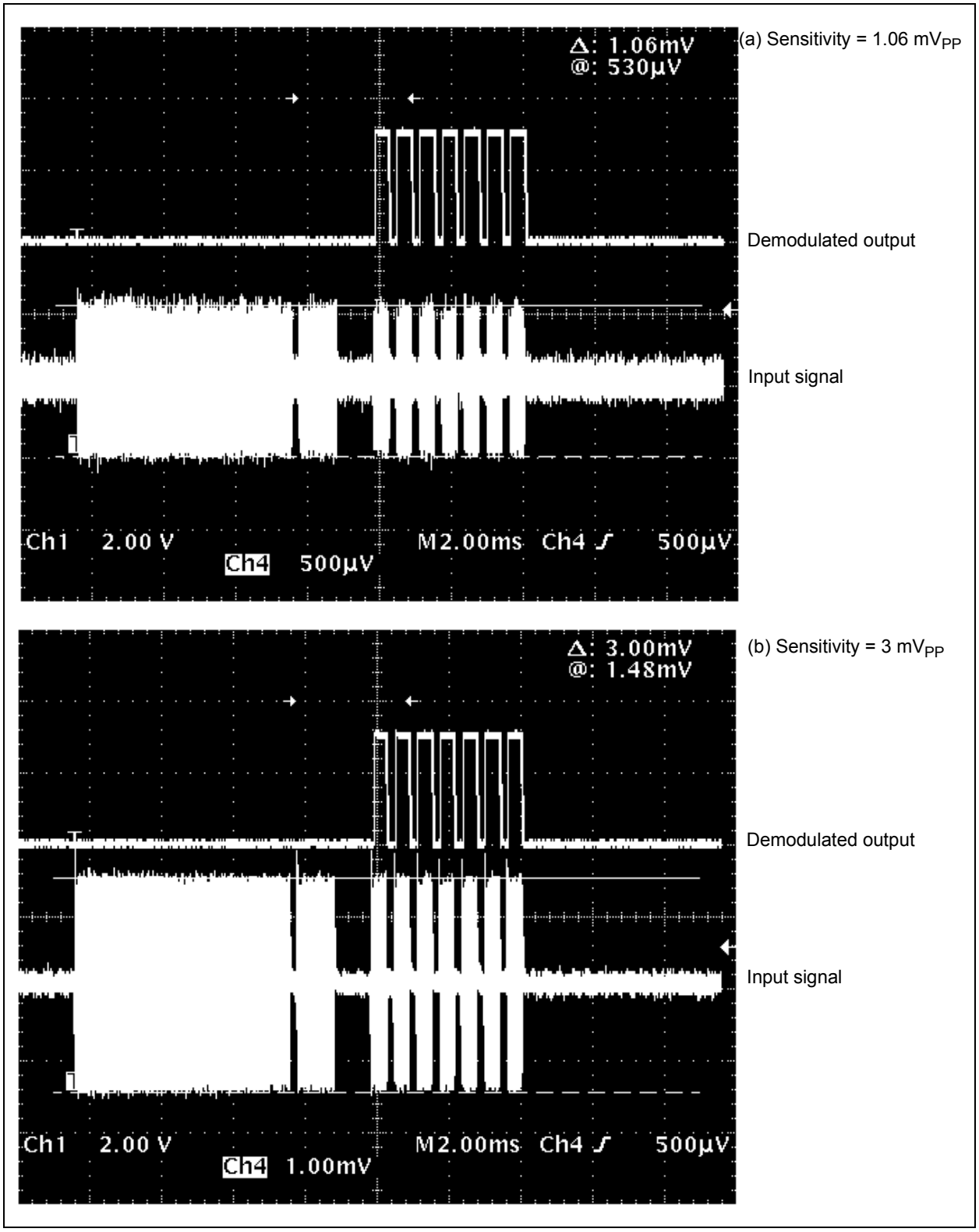
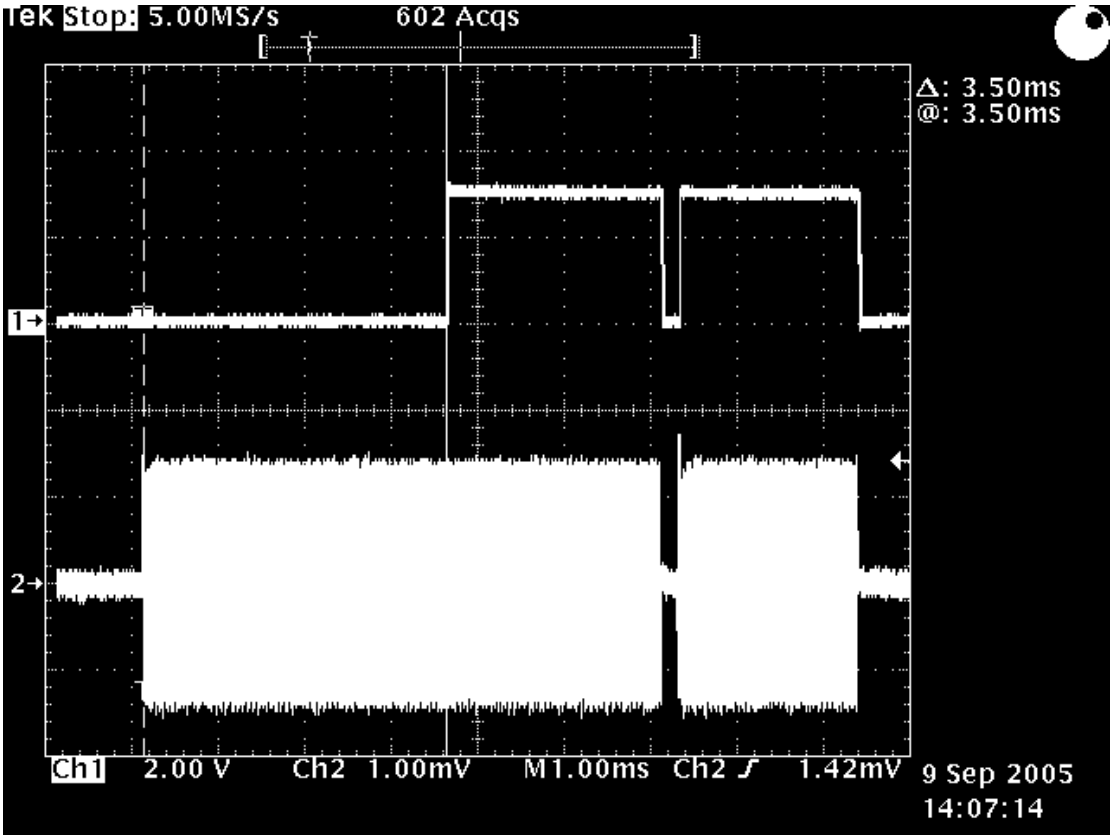
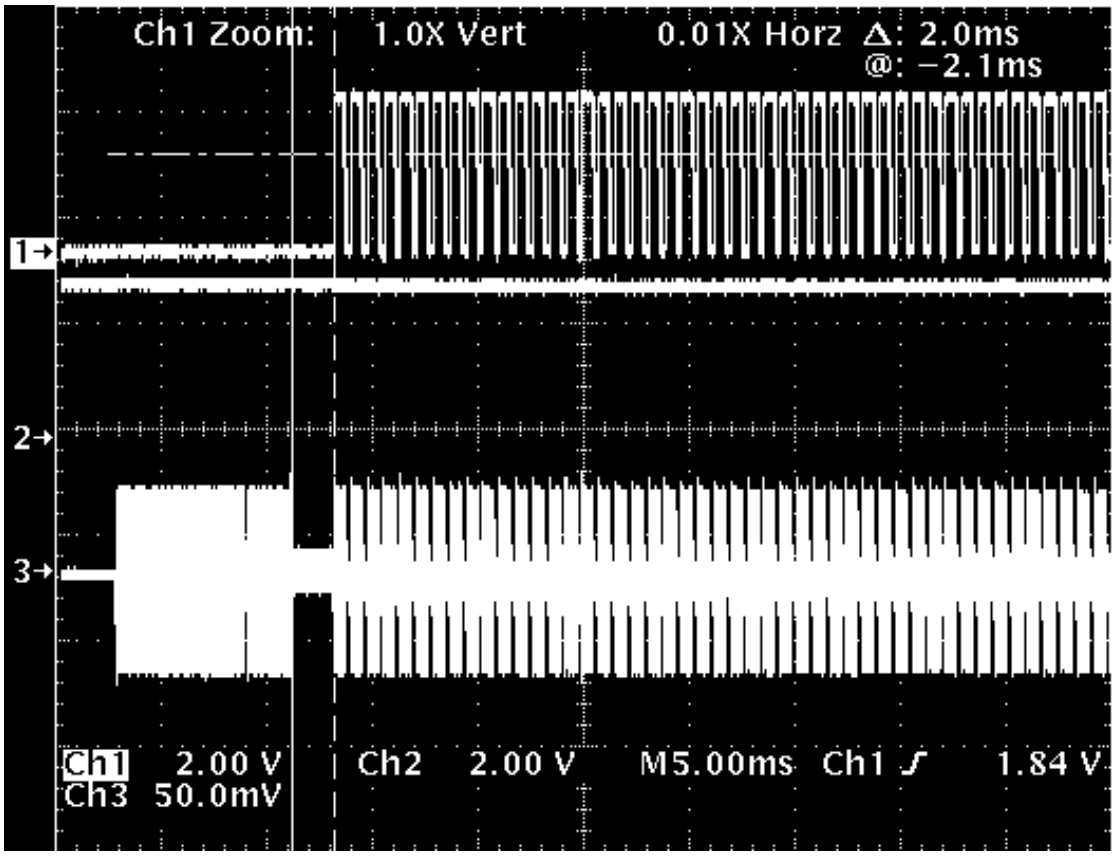


FIGURE 2-16: *Input Sensitivity Example.*



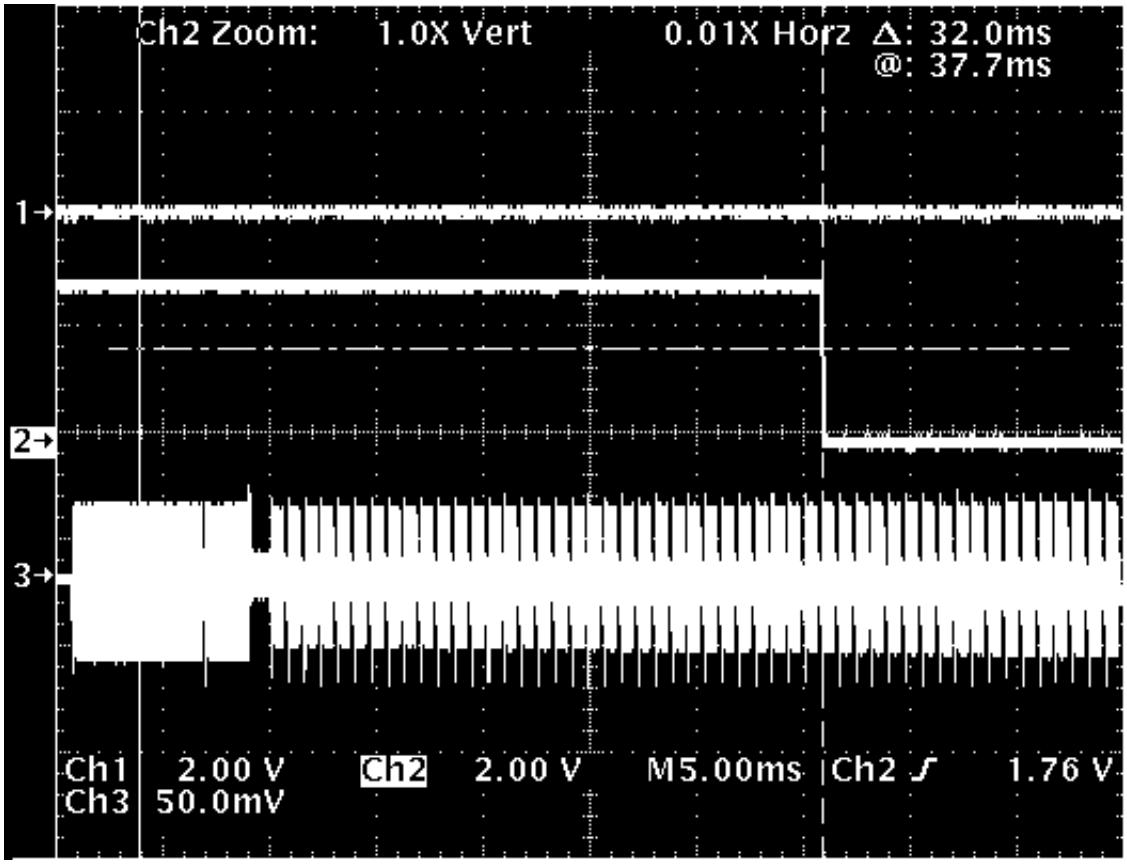
Note: Ch2 is the input and Ch1 is the output (demodulated data appears after AGC Initialization time (T_{AGC})). Output Enable Filter is disabled.

FIGURE 2-17: *Typical AGC Initialization Time at Room Temperature (V_{DD} = 3V).*



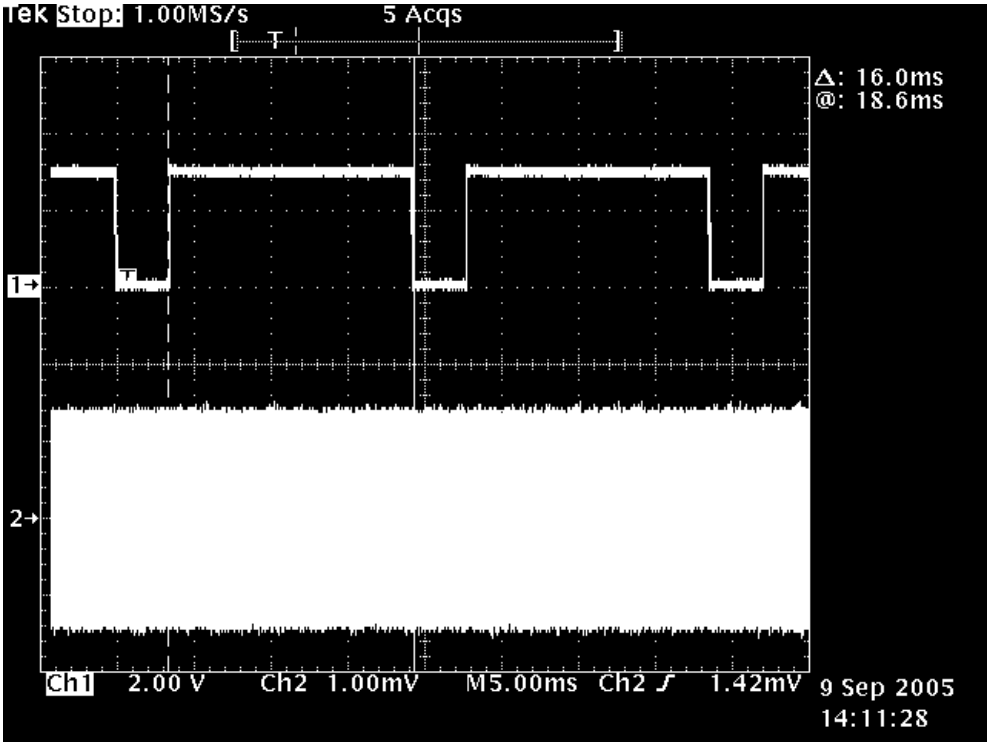
Note: Ch3 is the input with correct Output Enable Filter timing.
Ch1 is the demodulated LFDATA output.
Ch2 is the $\overline{\text{ALERT}}$ pin output. It shows that the $\overline{\text{ALERT}}$ output pin maintains logic high if the input signal meets the programmed filter timing requirement.

FIGURE 2-18: *$\overline{\text{ALERT}}$ Output Example: With No Parity Error and no 32 ms Alarm Timer Time-out.*



Note: The 32 ms Alarm Timer is enabled only if the Output Enable Filter is enabled.
Ch3 is the input signal with incorrect Output Enable Filter timing.
Ch1 is the demodulated LFDATA output. No output since the input filter is not matched.
Ch2 is the $\overline{\text{ALERT}}$ output.
The output shows that the logic level changes after 32 ms from the AGC initialization time (T_{AGC}) if the input signal does not meet the programmed filter timing requirement.

FIGURE 2-19: *$\overline{\text{ALERT}}$ Output Example: With 32 ms Alarm Timer Timed Out.*



(a) Output (Ch1): Device repeats Soft Reset after 16 ms, Inactivity Timer has timed out

(b) Input (Ch2): Input has no modulation

Note: Ch2 is the input without modulation (i.e., noise).
Ch1 is the output at the LFDATA pin due to the 16 ms Soft Inactivity Timer time out. Note the 3.5 ms AGC initialization time after the Soft Reset.
The cases shown above apply when the Output Filter is disabled.

FIGURE 2-20: *Examples of Soft Inactivity Timer Time Out: This output is available only if the Output Enable Filter is disabled.*

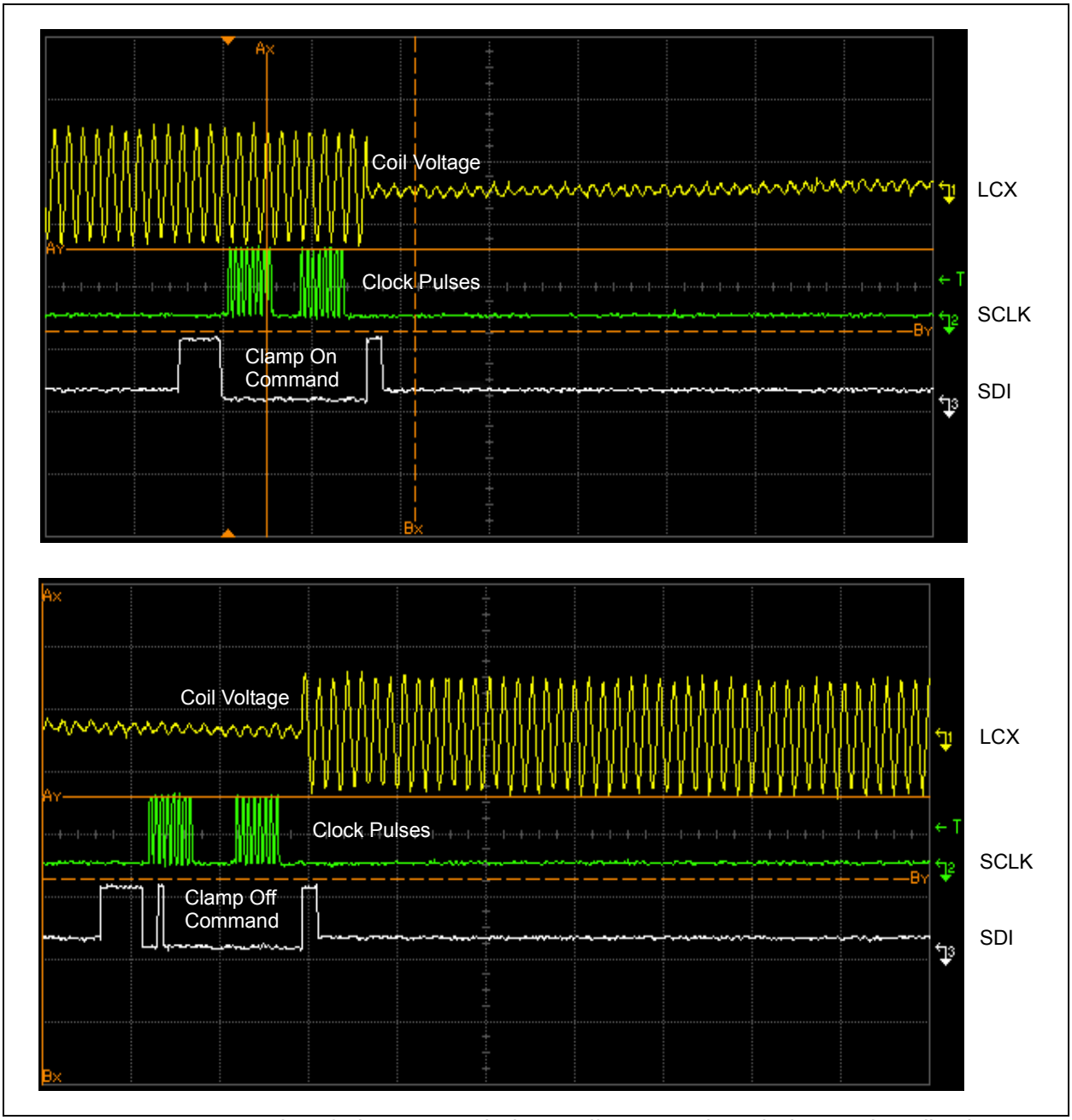


FIGURE 2-21: *Examples of Clamp-On and Clamp-Off Commands and Changes in Coil Voltage.*

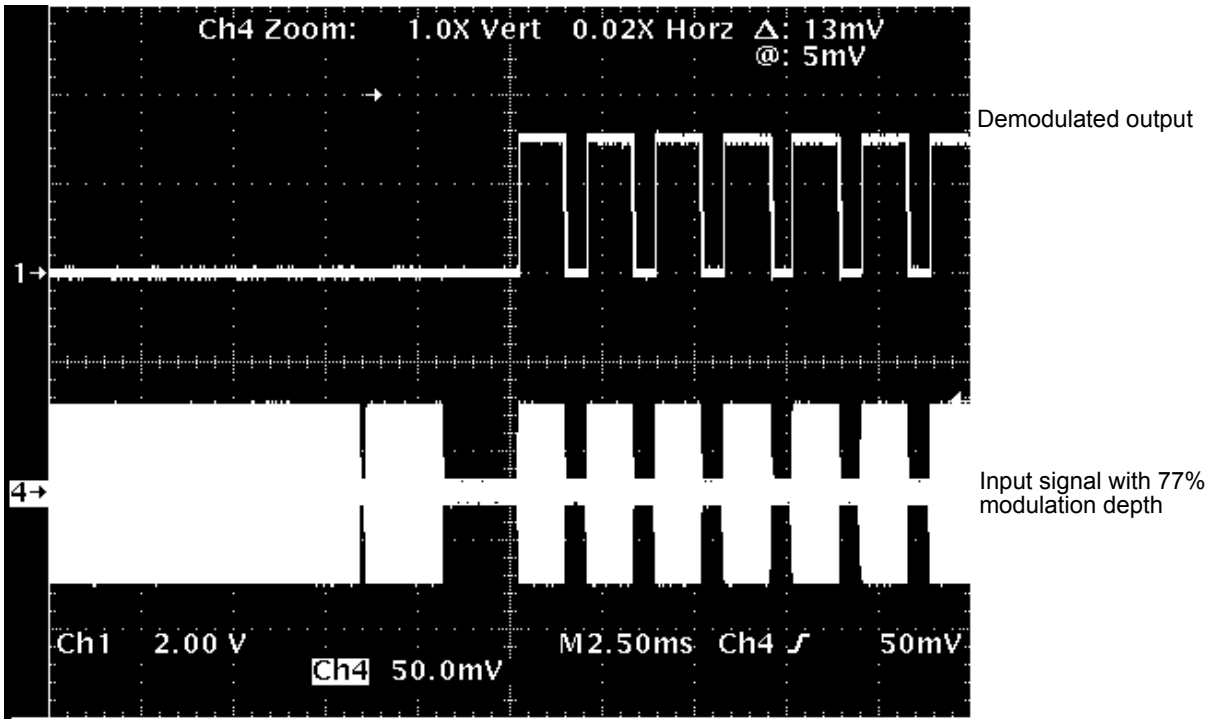
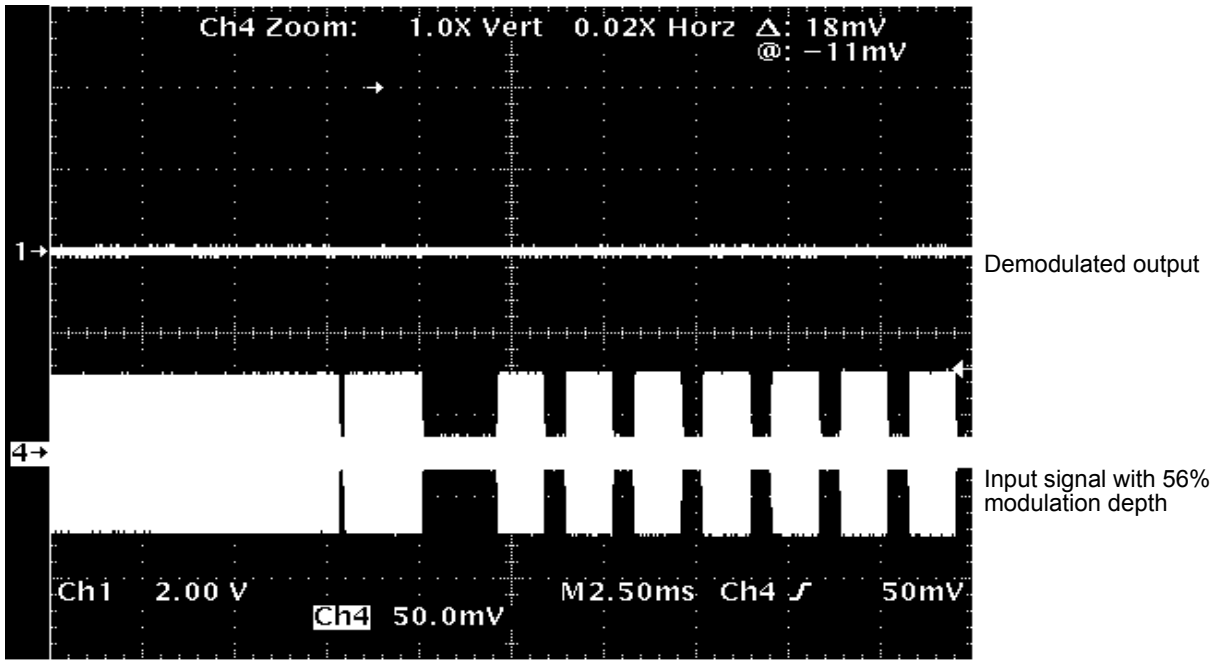


FIGURE 2-22: *Example of Minimum Modulation Depth Setting: Modulation Depth of Input Signal = 77%, Minimum Modulation Depth (MODMIN) Setting = 60%.*



Note: There is no demodulated output since the modulation depth of the input signal is lower than the minimum modulation depth setting. The device will have demodulated output if the Minimum Modulation Depth option is set to 8%, 14%, or 33%.

FIGURE 2-23: *Example of Minimum Modulation Depth Setting: Modulation Depth of Input Signal = 56%, Minimum Modulation Depth (MODMIN) Setting = 60%.*

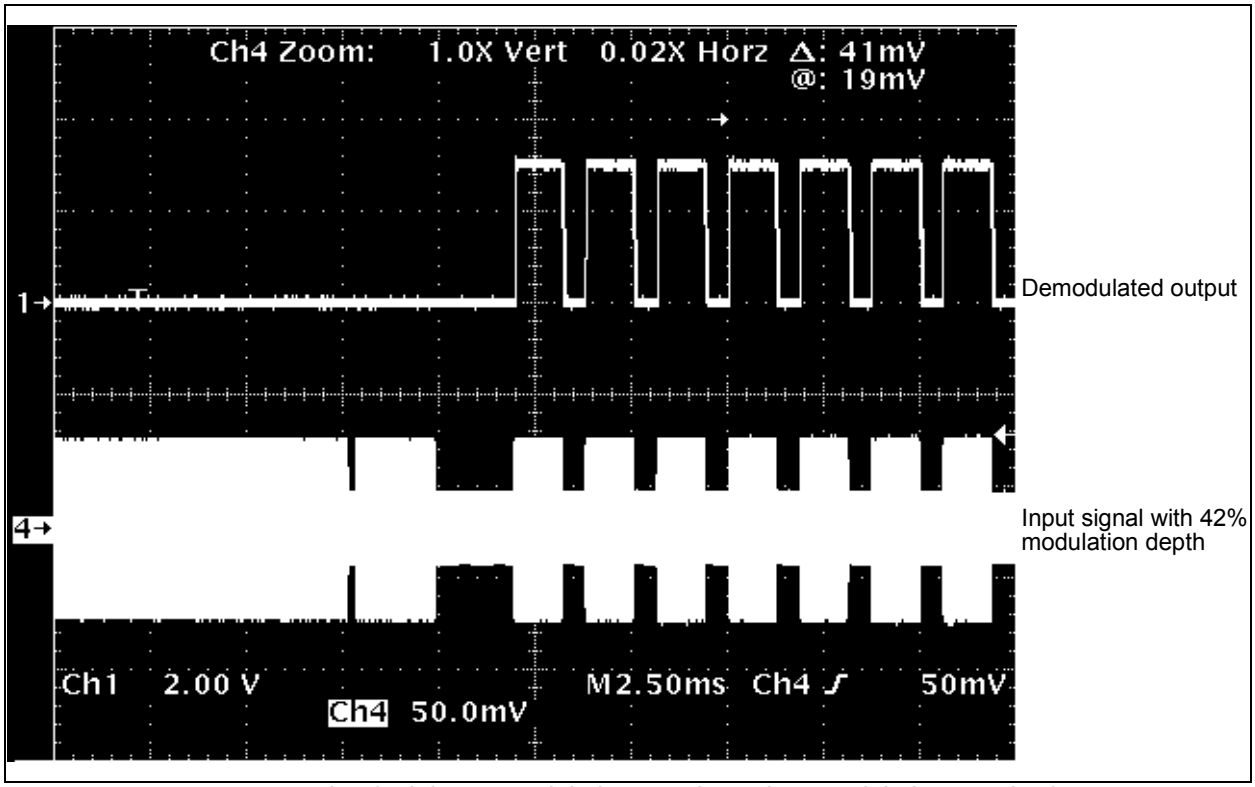


FIGURE 2-24: *Example of Minimum Modulation Depth Setting: Modulation Depth of Input Signal = 42%, Minimum Modulation Depth (MODMIN) Setting = 33%.*

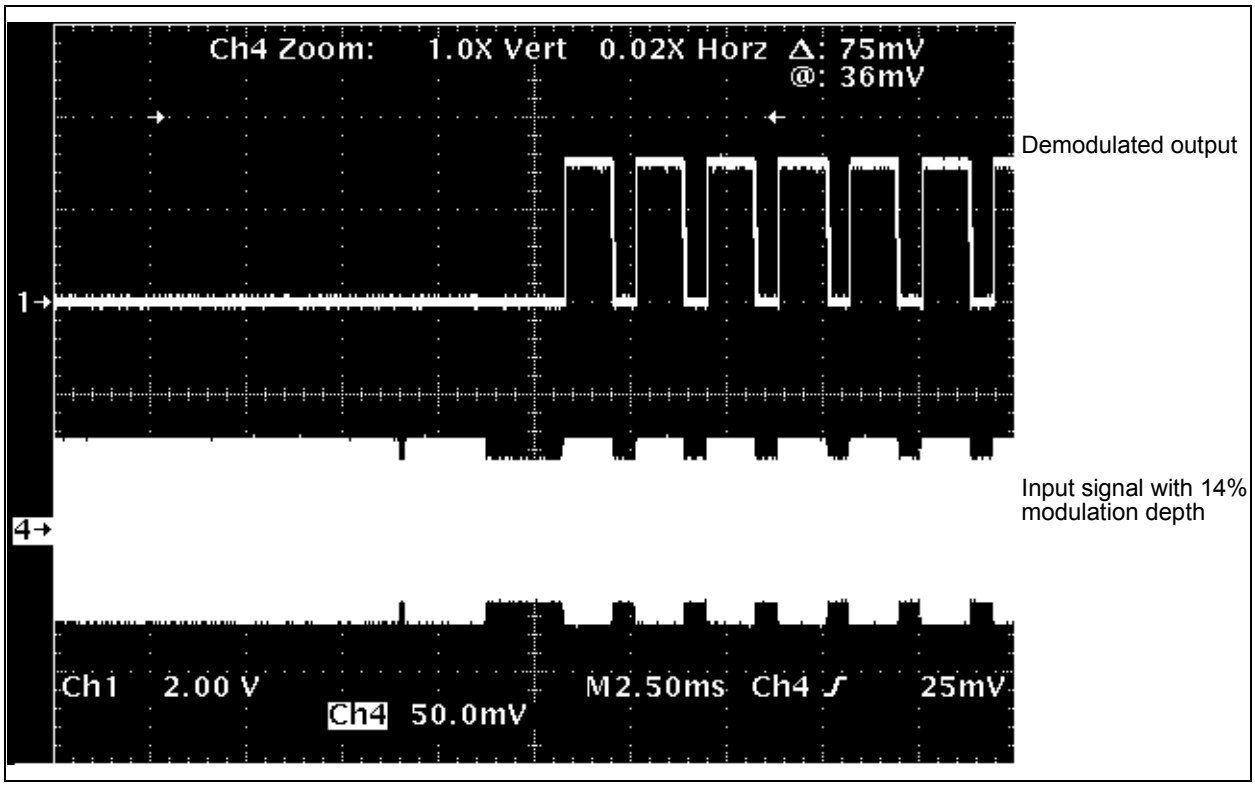
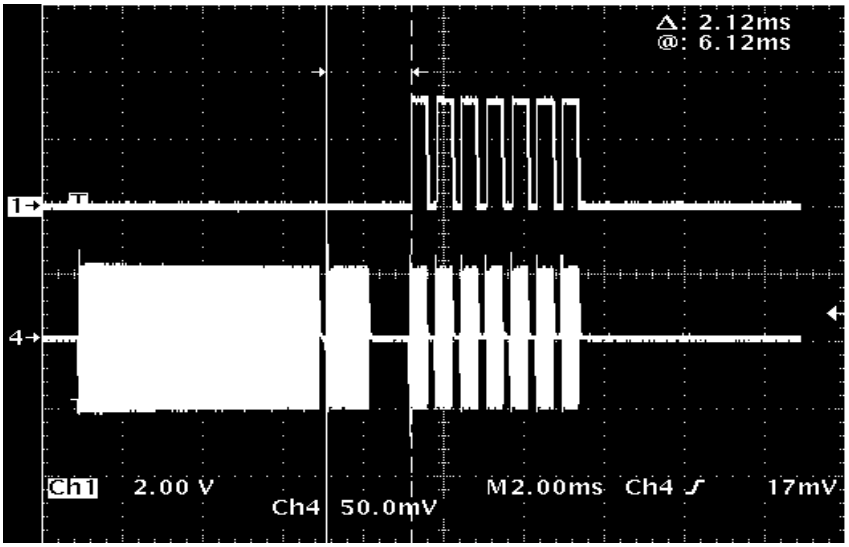
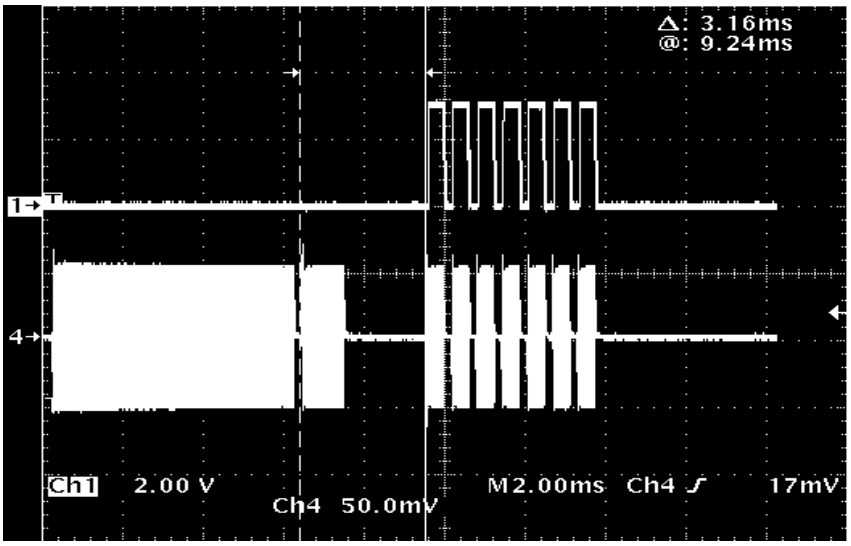


FIGURE 2-25: *Example of Minimum Modulation Depth Setting: Modulation Depth of Input Signal = 14%, Minimum Modulation Depth (MODMIN) Setting = 14%.*



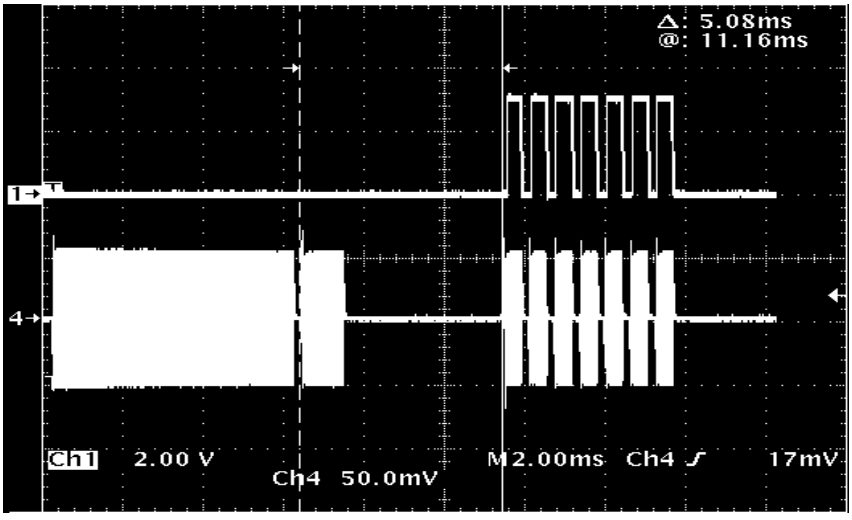
Filter 1

Output Enable Filter Timing of Input Signal	Configuration Bit Settings	
	OEH	OEL
T_{OEH} = 1 ms T_{OEL} = 1 ms T_{OET} = 3 ms	01 or 01	00 01



Filter 2

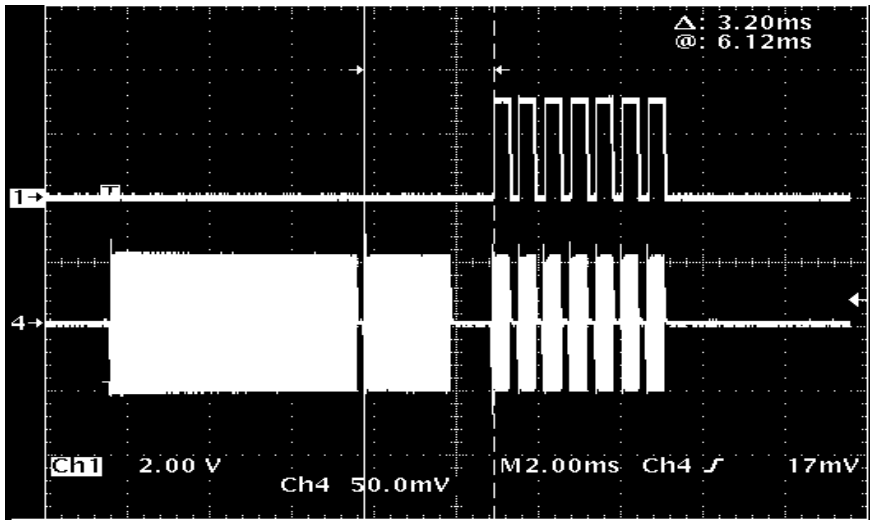
Output Enable Filter Timing of Input Signal	Configuration Bit Settings	
	OEH	OEL
T_{OEH} = 1 ms T_{OEL} = 2 ms T_{OET} = 4 ms	01	10



Filter 3

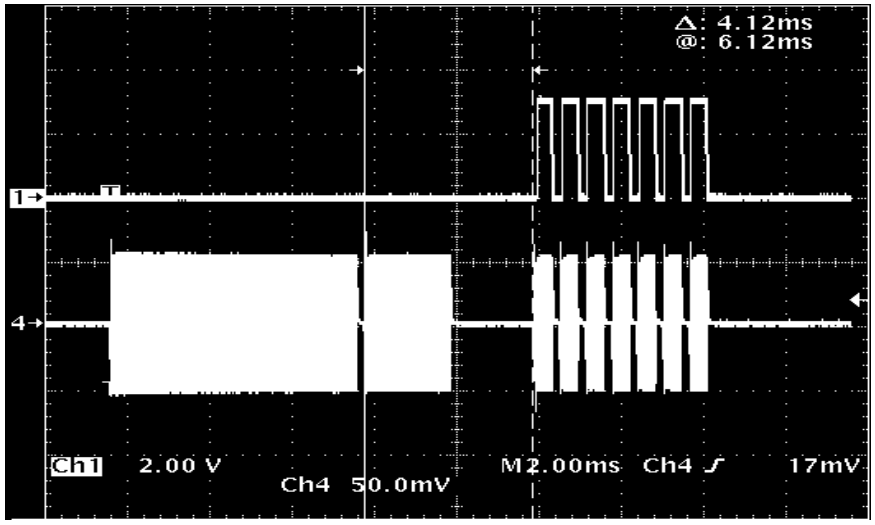
Output Enable Filter Timing of Input Signal	Configuration Bit Settings	
	OEH	OEL
T_{OEH} = 1 ms T_{OEL} = 4 ms T_{OET} = 6 ms	01	11

FIGURE 2-26: *Examples of Output Enable Filters 1 through 3 (Wake-up Filters) and Demodulated Outputs.*



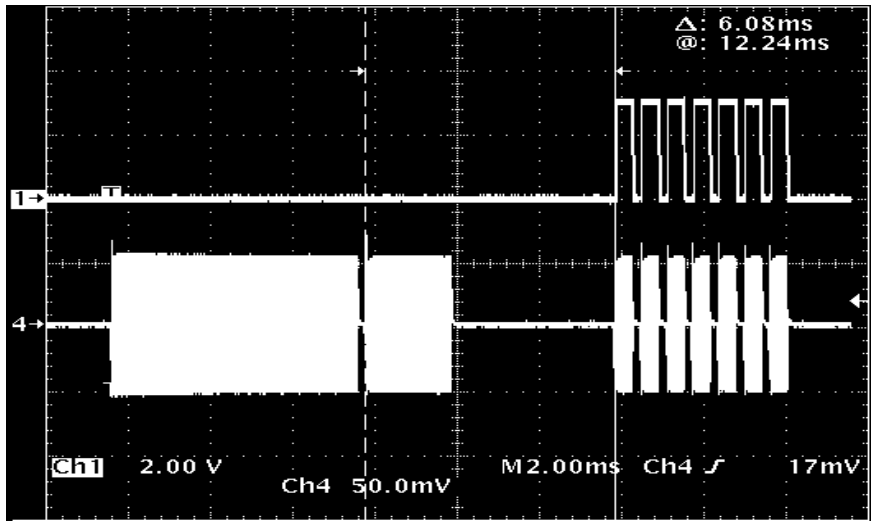
Filter 4

Output Enable Filter Timing of Input Signal	Configuration Bit Settings	
	OEH	OEL
T_{OEH} = 2 ms T_{OEL} = 1 ms T_{OET} = 4 ms	10 or 10	00 01



Filter 5

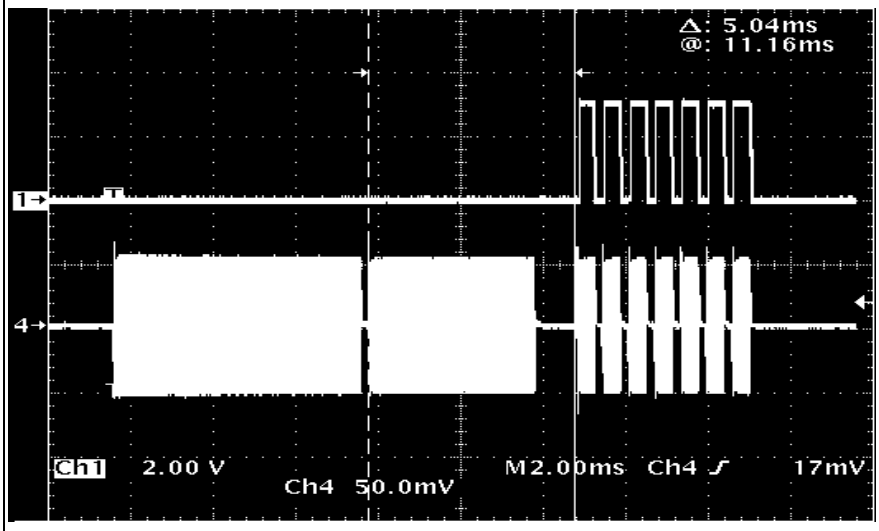
Output Enable Filter Timing of Input Signal	Configuration Bit Settings	
	OEH	OEL
T_{OEH} = 2 ms T_{OEL} = 2 ms T_{OET} = 5 ms	10	10



Filter 6

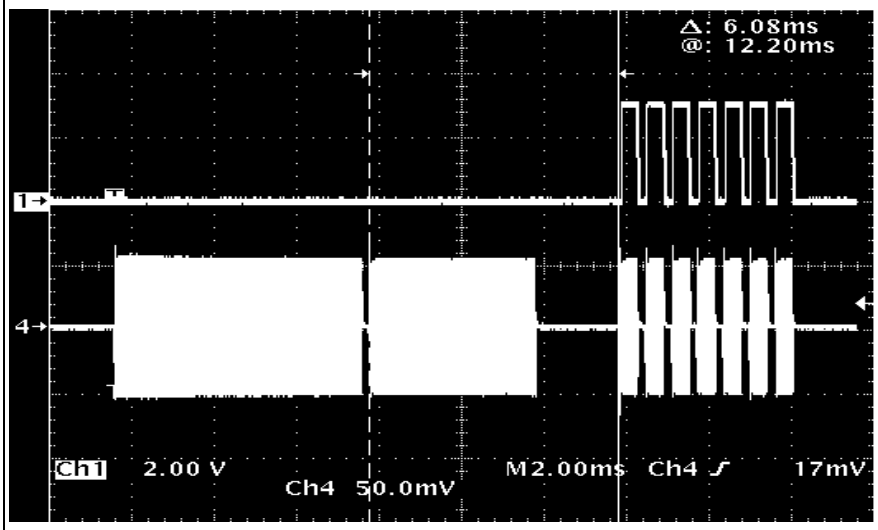
Output Enable Filter Timing of Input Signal	Configuration Bit Settings	
	OEH	OEL
T_{OEH} = 2 ms T_{OEL} = 4 ms T_{OET} = 8 ms	10	11

FIGURE 2-27: *Examples of Output Enable Filters 4 through 6 (Wake-up Filters) and Demodulated Outputs.*



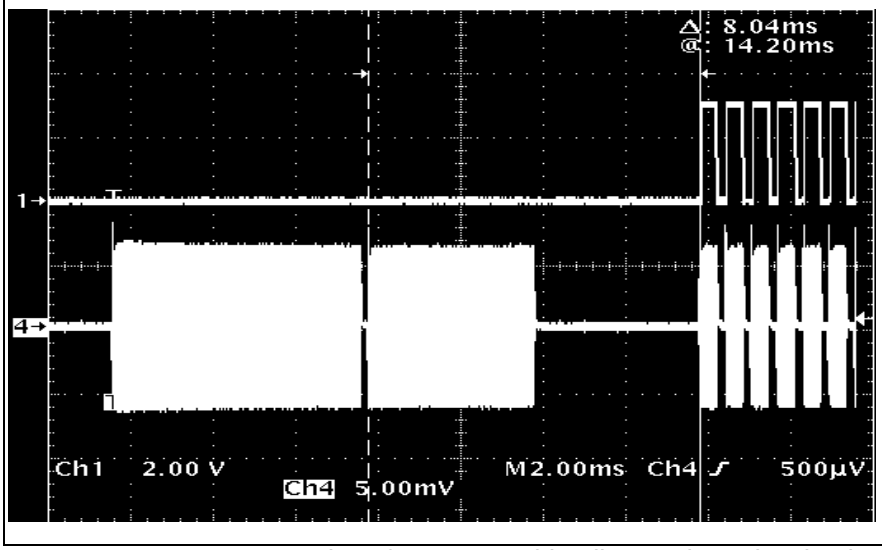
Filter 7

Output Enable Filter Timing of Input Signal	Configuration Bit Settings	
	OEH	OEL
T_{OEH} = 4 ms T_{OEL} = 1 ms T_{OET} = 6 ms	11 or 11	00 01



Filter 8

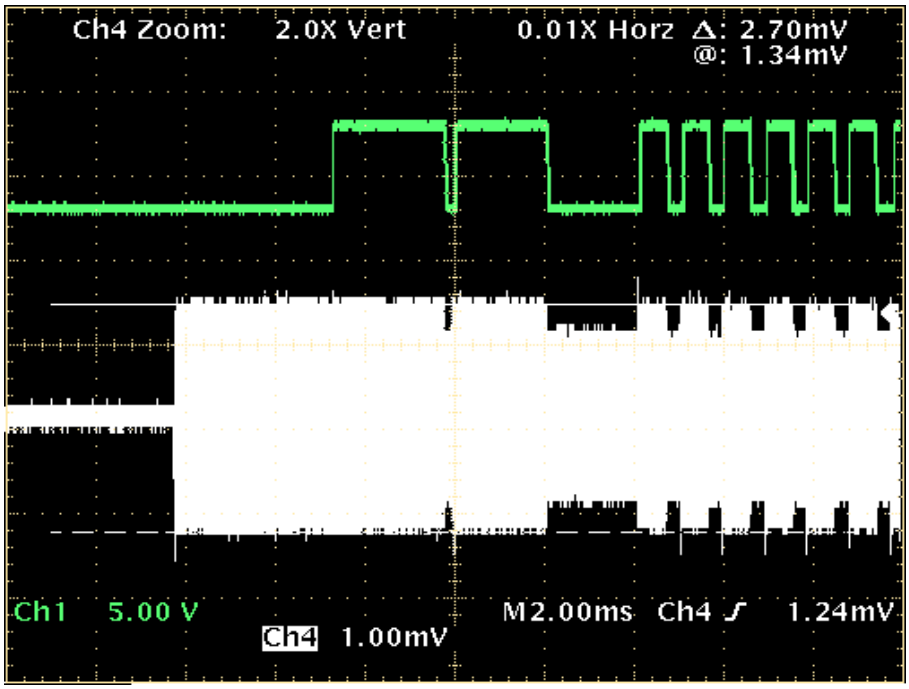
Output Enable Filter Timing of Input Signal	Configuration Bit Settings	
	OEH	OEL
T_{OEH} = 4 ms T_{OEL} = 2 ms T_{OET} = 8 ms	11	10



Filter 9

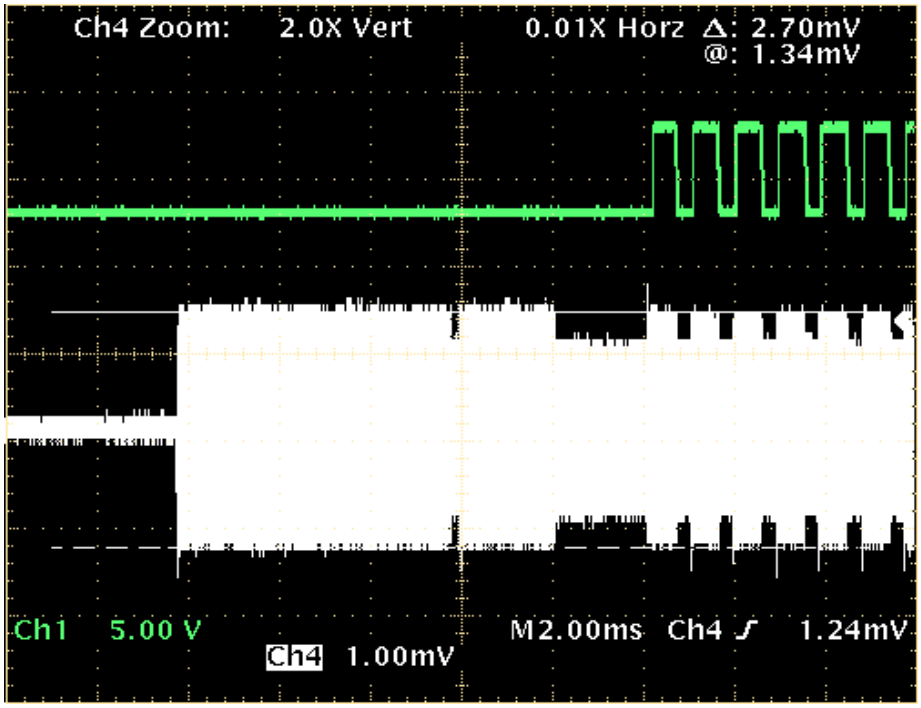
Output Enable Filter Timing of Input Signal	Configuration Bit Settings	
	OEH	OEL
T_{OEH} = 4 ms T_{OEL} = 4 ms T_{OET} = 10 ms	11	11

FIGURE 2-28: *Examples of Output Enable Filters 7 through 9 (Wake-up Filters) and Demodulated Outputs.*



Note: Demodulated output is available immediately after AGC initialization.

FIGURE 2-29: *Input Signal and Demodulated Output When the Output Enable Filter is Disabled.*



Note: Demodulated output is available only if the incoming signal meets the enable filter timing criteria that is defined in the Configuration Register 0 (Register 5-1). If the criteria is met, the output is available after the low timing (T_{OEL}) of the Enable Filter.

FIGURE 2-30: *Input Signal and Demodulator Output When Output Enable Filter is Enabled and Input Meets Filter Timing Requirements.*

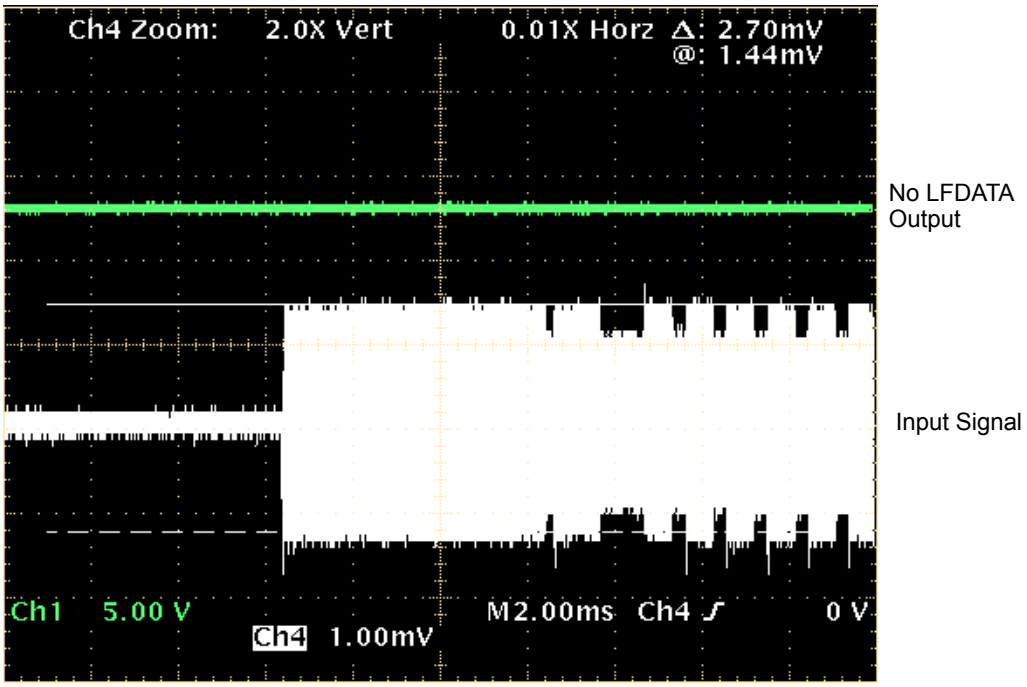
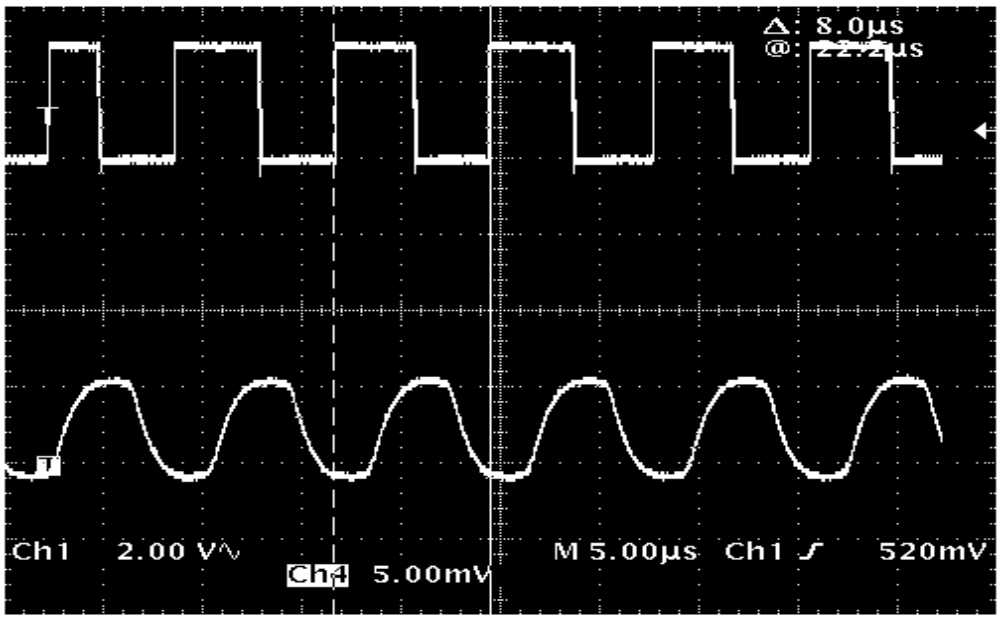
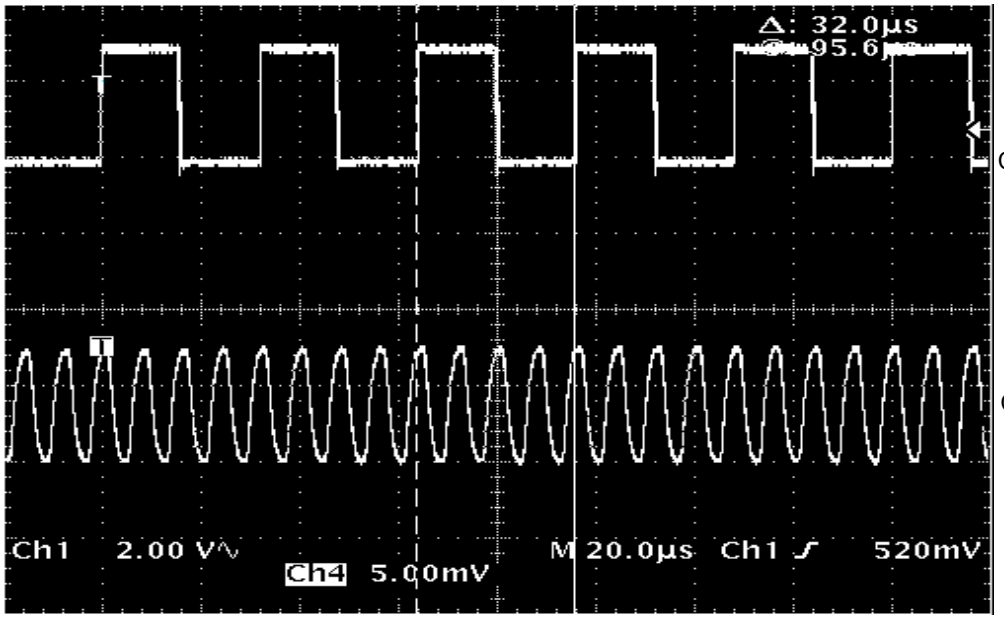


FIGURE 2-31: *No Demodulator Output When Output Enable Filter is Enabled But Input Does Not Meet Filter Timing Requirements.*



(a) Carrier Clock Output with Carrier/1 Option



(b) Carrier Clock Output with Carrier/4 Option

FIGURE 2-32: *Carrier Clock Output Examples.*

NOTES:

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLES

MCP2035 TSSOP	Symbol	I/O/P	Function
1	V_{SS}	P	Ground Pin
2	$\overline{CS}$	I	Chip Select Digital Input Pin
3	SCLK/$\overline{ALERT}$	I/O	Clock input for the modified 3-wire SPI interface. $\overline{ALERT}$ output: This pin goes low if there is a parity error in the Configuration register or the 32 ms Alarm Timer is timed out.
4	RSSI	O	Received Signal Strength Indicator (RSSI) current output
5	NC	N/A	No Connect
6	LFDATA/CCLK/SDIO	I/O	Demodulated data output Carrier clock output Serial input or output data for the modified 3-wire SPI interface
7	V_{DD}	P	Positive Supply Voltage Pin
8	V_{DD}	P	Positive Supply Voltage Pin
9	NC	N/A	No Connect **(Note 1)**
10	NC	N/A	No Connect **(Note 1)**
11	LCX	I	Input pin for external LC antenna
12	NC	N/A	No Connect
13	LCCOM	I	Common reference input for the external LC antenna
14	V_{SS}	P	Ground Pin

Type Identification: I = Input; O = Output; P = Power

Note 1: This pin is bonded out to ground internally.

3.1 Supply Voltage (V_{DD}, V_{SS})

The V_{DD} pin is the power supply pin for the analog and digital circuitry within the MCP2035. This pin requires an appropriate bypass capacitor of 0.1 µF. The voltage on this pin should be maintained in the 2.0V-3.6V range for specified operation.

The V_{SS} pin is the ground pin and the current return path for both analog and digital circuitry of the MCP2035. If an analog ground plane is available, it is recommended that this device be tied to the analog ground plane of the PCB.

3.2 Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin needs to stay high when the device is receiving input signals. Leaving the $\overline{CS}$ pin low will place the device in the SPI Programming mode.

The $\overline{CS}$ pin is an open collector output. This pin has an internal pull-up resistor to ensure that no spurious SPI communication occurs between power-up and pin configuration of the MCU.

3.3 SPI Clock Input (SCLK/$\overline{ALERT}$)

This pin becomes the SPI clock input (SCLK) when $\overline{CS}$ is low, and becomes the $\overline{ALERT}$ output when $\overline{CS}$ is high.

The $\overline{ALERT}$ pin is an open collector output. This pin has an internal pull-up resistor to ensure that no spurious SPI communication occurs between power-up and pin configuration of the MCU.

3.4 Received Signal Strength Indicator (RSSI)

This pin becomes the Received Signal Strength Indicator (RSSI) output current sink when the RSSI output option is selected.

3.5 Demodulated Data Output (LFDATA) Carrier Clock Output (CCLK) SPI Data I/O (SDIO)

When the $\overline{CS}$ pin is high, this pin is an output pin for demodulated data or carrier clock, depending on output-type selection. When carrier clock output (CCLK) is selected, the LFDATA output is a square pulse of the input carrier clock and is available as soon as the AGC stabilization time (T_{STAB}) is completed.

When the $\overline{CS}$ pin is low, this pin becomes the SPI data input and output (SDIO).

3.6 LCX Input

This is the input pin of the LCX channel. An external LC resonance antenna circuit can be connected between the LCX and LCCOM pins.

3.7 LC Common Reference (LCCOM)

This pin is the common reference input pin for the external LC resonant circuit.

4.0 APPLICATION INFORMATION

Microchip's MCP2030 and MCP2035 are stand-alone analog-front devices for low frequency (LF) signal detection and low-power/short range transponder applications. The MCP2035 is a single-channel device, while the MCP2030 is a three-channel device for more advanced applications.

The device's high input sensitivity (1 mV_{PP}) and ability to detect very weakly modulated input signals (as low as 8%), makes the device suitable for various intelligent short range transponder applications, such as Microchip's BodyCom applications.

4.1 MCP2035 BodyCom Application Example

Figure 4-1 shows an example of a BodyCom system that is utilizing the human body as a signal transmission medium. The system has two units: (a) Base Station Unit and (b) Mobile Unit. An example of the BodyCom communication sequence is as follows:

- When the human interfaces with the Base Station, it is initialized by an event of either touch or proximity, and the Base Station transmits a modulated 128 kHz command signal.
- This signal is then capacitively coupled to the human body, propagates and is detected by the Mobile Unit's high sensitivity MCP2035 front-end device.
- The Mobile Unit processes the Base Station's command information, and responds back using a high frequency (HF, 8 MHz) carrier.
- This respond signal is then received by the HF receiver in the Base Station, and demodulated and fed to another MCP2035 in the Base Station unit for digital waveforms. This return signal is then processed by the MCU in the Base Station.

Figure 4-2 shows an example of the Mobile Unit schematics. This BodyCom solution can be used in various applications such as secure access control and passive keyless entry for automobiles.

Note:	See Microchip's Application Note AN1391 for more details of the BodyCom applications solutions.

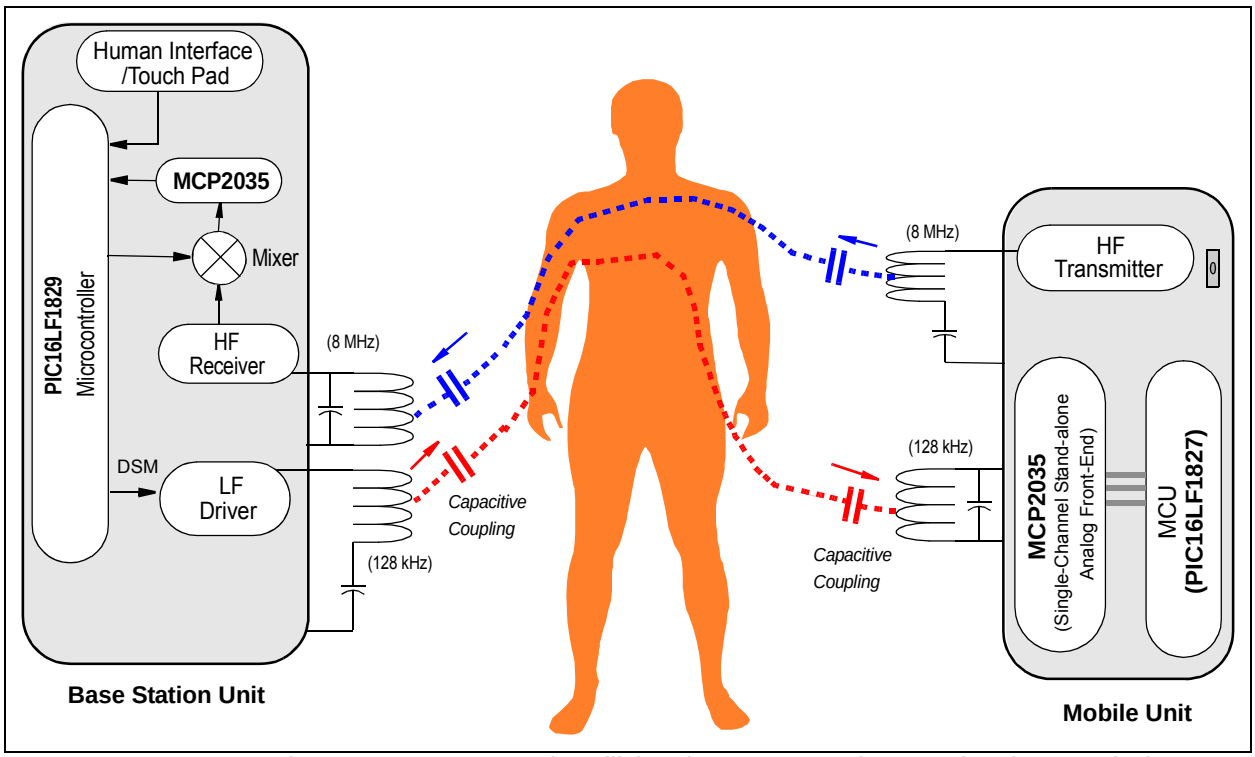


FIGURE 4-1: *BodyCom System Example Utilizing the Human Body as a Signal Transmission Medium.*

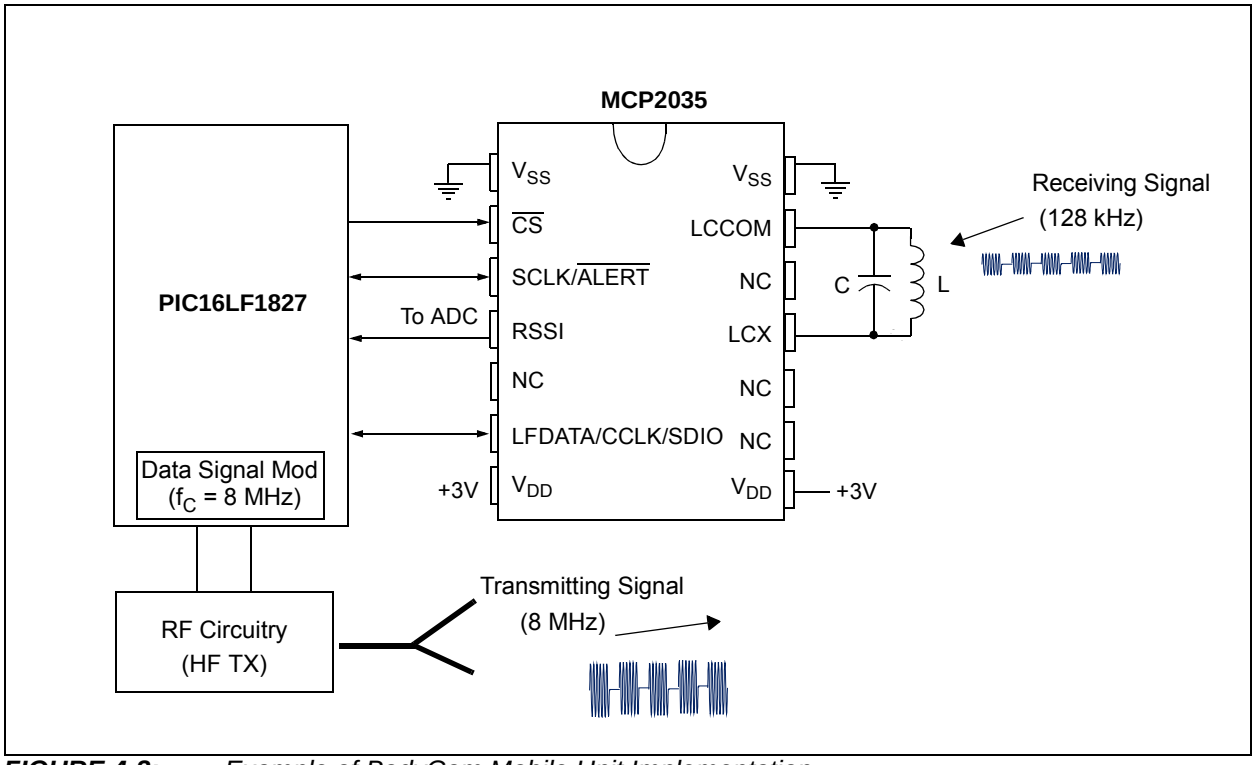


FIGURE 4-2: *Example of BodyCom Mobile Unit Implementation.*

5.0 FUNCTIONAL DESCRIPTION AND THEORY OF DEVICE OPERATION

The MCP2035 contains an analog input channel for signal detection and LF talk-back. This section provides the functional description of the device.

The input channel has internal tuning capacitors, sensitivity control circuits, an input signal strength limiter and an LF talk-back modulation transistor. An AGC loop is used for input channel gains. The output of the input channel is fed into a demodulator. The digital output is passed to the LFDATA pin. Figure 5-1 shows the block diagram of the device and Figure 5-2 shows the input signal path.

There are a total of eight Configuration registers. Six of them are used for device operation options, one for column parity bits and one for status indication of device operation. Each register has nine bits including one row parity bit. These registers are readable and writable by SPI commands, except for the STATUS register, which is read-only.

The device's features are dynamically controllable by programming the Configuration registers.

5.1 RF Limiter

The RF Limiter limits LC pin input voltage by de-Q'ing the external LC resonant antenna circuit. The limiter begins de-Q'ing the external LC antenna when the input voltage exceeds V_{DE_Q}, progressively de-Q'ing harder to reduce the antenna input voltage.

5.2 Modulation Circuit for LF Talk-Back

The LF talk-back is achieved by turning on and off the modulation transistor. The modulation circuit consists of a modulation transistor (FET), internal tuning capacitors and external LC antenna components. The modulation transistor and the internal tuning capacitors are connected between the LCX input pin and LCCOM pin. Each LC input has its own modulation transistor.

When the modulation transistor turns on, its low Turn-on Resistance (R_M) clamps the induced LC antenna voltage. The coil voltage is minimized when the modulation transistor turns on, and maximized when the modulation transistor turns off. The modulation transistor's low turn-on resistance (R_M) results in a high modulation depth.

The modulation data comes from the external micro-controller section via the digital SPI as "Clamp On", "Clamp Off" commands. A basic block diagram of the modulation circuit is shown in Figure 5-1 and Figure 5-2.

The modulation FET is also shorted momentarily after Soft Reset and Inactivity Timer time-out.

Note: The LF-Talk back is only used when it needs to communicate back to the Base Station using the same Base Station's low frequency (128 kHz) carrier frequency. A typically LF-Talk back range is up to a few inches. For the BodyCom applications, it uses HF (~8 MHz) for the return signal.

5.3 Tuning Capacitor

The input tuning capacitor values are programmed by the Configuration registers up to 63 pF, 1 pF per step.

Note: The user can control the tuning capacitor by programming the Configuration registers. See Register 5-2 for details.

5.4 Variable Attenuator

The variable attenuator is used to attenuate, via AGC control, the input signal voltage to avoid saturating the amplifiers and demodulators.

Note: The variable attenuator function is accomplished by the device itself. The user cannot control its function.

5.5 Sensitivity Control

The sensitivity of the input channel can be reduced by the Configuration register sensitivity setting. This is used to desensitize the channel from optimum.

Note: The user can desensitize the channel sensitivity by programming the Configuration registers. See Register 5-5 for details.

5.6 AGC Control

The AGC controls the variable attenuator to limit the internal signal voltage to avoid saturation of internal amplifiers and demodulators (Refer to **Section 5.4 "Variable Attenuator"**).

Note: The AGC control function is accomplished by the device itself. The user cannot control its function.

5.7 Fixed Gain Amplifiers 1 and 2

FGA1 and FGA2 provide a maximum two-stage gain of 40 dB.

Note: The user cannot control the gain of these two amplifiers.

5.8 Carrier Clock Detector

The Carrier Clock Detector senses the input carrier cycles. The output of the detector switches digitally at the signal carrier frequency. Carrier clock output is available when the output is selected by the DATOUT bit in Configuration Register 1 (Register 5-2).

5.9 Demodulator

The Demodulator consists of a full-wave rectifier, low-pass filter, peak detector and Data Slicer that detects the envelope of the input signal.

5.10 Data Slicer

The Data Slicer consists of a reference generator and comparator. The Data Slicer compares the input with the reference voltage. The reference voltage comes from the minimum modulation depth requirement setting and input peak voltage.

5.11 Output Enable Filter

The Output Enable Filter enables the LFDATA output once the incoming signal meets the wake-up sequence requirements (see **Section 5.14 "Configurable Output Enable Filter"**).

5.12 Received Signal Strength Indicator (RSSI)

The RSSI provides a current which is proportional to the input signal amplitude (see **Section 5.29.3 "Received Signal Strength Indicator (RSSI) Output"**).

5.13 Analog Front-End Timers

The device has an internal 32 kHz RC oscillator. The oscillator is used in several timers:

- Inactivity Timer
- Alarm Timer
- Pulse Width Timer
- Period Timer
- AGC Settling Timer

5.13.1 RC OSCILLATOR

The RC oscillator generates a 32 kHz internal clock.

5.13.2 INACTIVITY TIMER

The Inactivity Timer is used to automatically return the device to Standby mode, if there is no input signal. The time-out period is approximately 16 ms (T_{INACT}), based on the 32 kHz internal clock.

The purpose of the Inactivity Timer is to minimize current draw by automatically returning to the lower current Standby mode, if there is no input signal for approximately 16 ms.

The timer is reset when:

- An amplitude change in the LF input signal, either high-to-low or low-to-high
- $\overline{CS}$ pin is low (any SPI command)
- Timer-related Soft Reset

The timer starts after AGC initialization time (T_{AGC}).

The timer causes a Soft Reset when:

- A previously received input signal does not change either high-to-low or low-to-high for T_{INACT}

The Soft Reset returns the device to Standby mode where most of the analog circuits, such as the AGC, demodulator and RC oscillator, are powered down. This returns the device to the lower Standby Current mode.

5.13.3 ALARM TIMER

The Alarm Timer is used to notify the external MCU that the device is receiving an input signal that does not pass the output enable filter requirement. The time-out period is approximately 32 ms (T_{ALARM}) in the presence of continuing noise.

The Alarm Timer time-out occurs if there is an input signal for longer than 32 ms that does not meet the output enable filter requirements. The Alarm Timer time-out causes:

a) The $\overline{ALERT}$ pin to go low.
b) The ALARM bit to set in the Status STATUS Register 7 (Register 5-8).

The external MCU is informed of the Alarm Timer time-out by monitoring the $\overline{ALERT}$ pin. If the Alarm Timer time-out occurs, the external MCU can take appropriate actions, such as lowering channel sensitivity or disabling the input channel. If the noise source is ignored, the device can return to a lower standby current draw state.

The timer is reset when the:

- $\overline{CS}$ pin is low (any SPI command).
- Output enable filter is disabled.
- LFDATA pin is enabled (signal passed output enable filter).

The timer starts after the AGC initialization time.

The timer causes a low output on the $\overline{ALERT}$ pin when:

- Output enable filter is enabled and modulated input signal is present for T_{ALARM}, but does not pass the output enable filter requirement.

Note:	The Alarm Timer is disabled if the output enable filter is disabled.

5.13.4 PULSE WIDTH TIMER

The Pulse Width Timer is used to verify that the received output enable sequence meets both the minimum T_{OEH} and minimum T_{OEL} requirements.

5.13.5 PERIOD TIMER

The Period Timer is used to verify that the received output enable sequence meets the maximum T_{OET} requirement.

5.13.6 AGC INITIALIZATION TIMER (T_{AGC})

This timer is used to keep the output enable filter in Reset while the AGC settles on the input signal. The time-out period is approximately 3.5 ms. At the end of this time (T_{AGC}), the input should remain high (T_{PAGC}), otherwise the counting is aborted and a Soft Reset is issued. See Figure 5-4 for details.

Note 1: The device needs a continuous and uninterrupted high input signal during AGC initialization time (T_{AGC}). Any absence of signal during this time may reset the timer and a new input signal is needed for AGC settling time, or may result in an improper AGC gain setting, which will produce invalid output.

2: The rest of the device section wakes up if the input channel receives a signal with the AGC settling time correctly. STATUS Register 7 bit <2> (Register 5-8) indicates the status if the input channel wakes up.

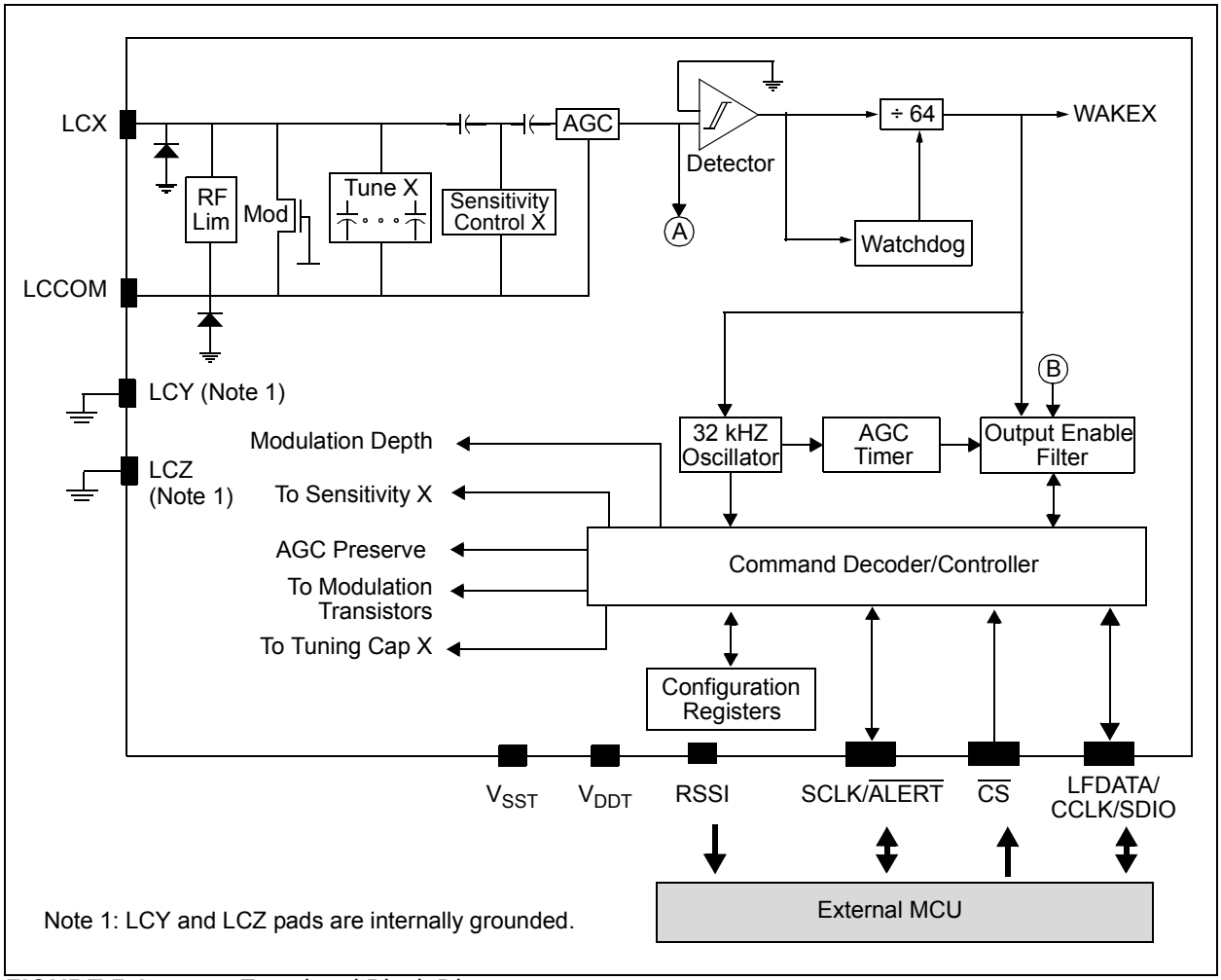


FIGURE 5-1: *Functional Block Diagram.*

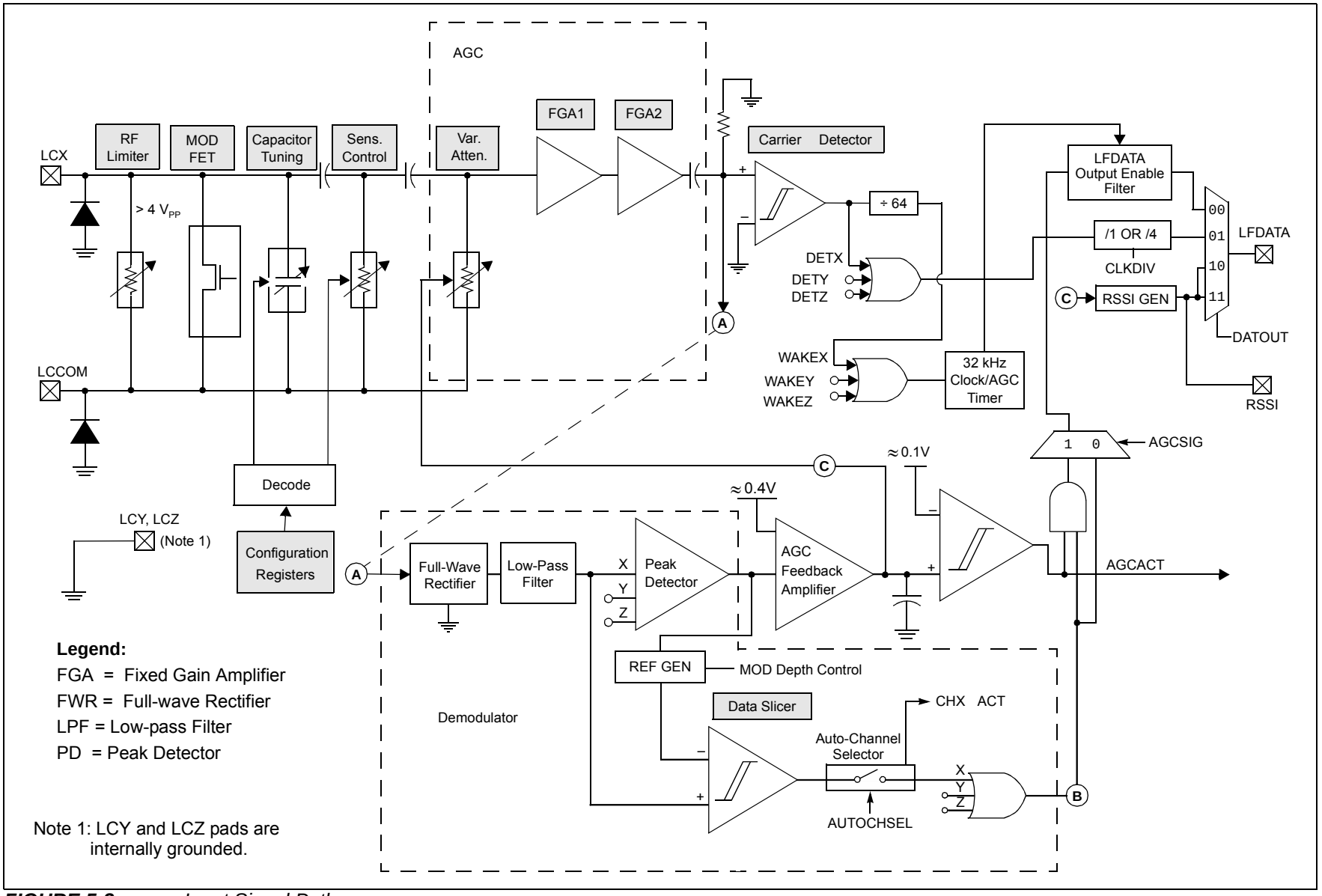


FIGURE 5-2: *Input Signal Path.*

5.14 Configurable Output Enable Filter

The purpose of this filter is to enable the LFDATA output and wake the external microcontroller only after receiving a specific sequence of pulses on the LC input pin. Therefore, it prevents waking up the external microcontroller due to noise or unwanted input signals. The circuit compares the timing of the demodulated header waveform with a pre-defined value, and enables the demodulated LFDATA output when a match occurs.

The output enable filter consists of a high (T_{OEH}) and low duration (T_{OEL}) of a pulse immediately after the AGC settling gap time. The selection of high and low times further implies a max period time. The output enable high and low times are determined by SPI programming. Figure 5-3 and Figure 5-4 show the output enable filter waveforms.

There should be no missing cycles during T_{OEH}. Missing cycles may result in failing the output enable condition.

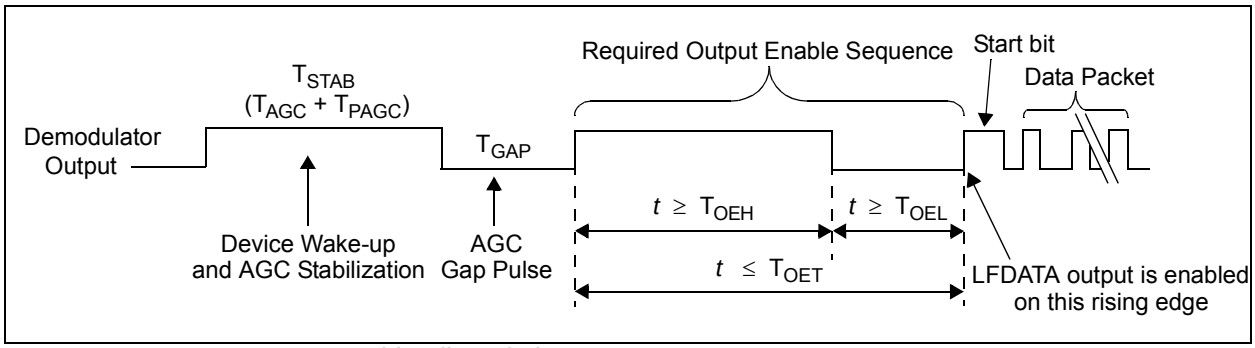


FIGURE 5-3: *Output Enable Filter Timing.*

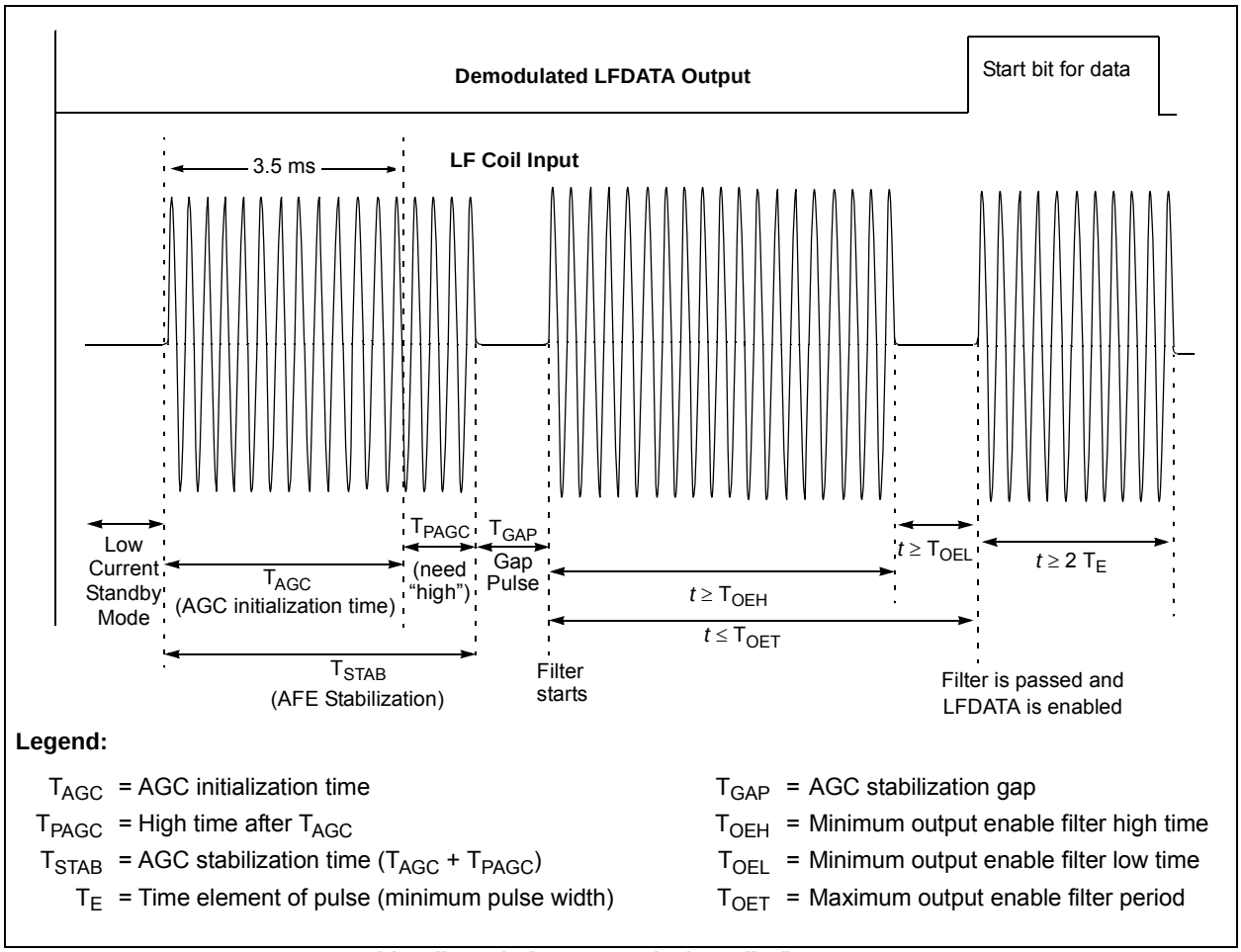


FIGURE 5-4: *Output Enable Filter Timing Example (Detailed).*

TABLE 5-1: OUTPUT ENABLE FILTER TIMING

OEH <1:0>	OEL <1:0>	T_{OEH} (ms)	T_{OEL} (ms)	T_{OET} (ms)
01	00	1	1	3
01	01	1	1	3
01	10	1	2	4
01	11	1	4	6
10	00	2	1	4
10	01	2	1	4
10	10	2	2	5
10	11	2	4	8
11	00	4	1	6
11	01	4	1	6
11	10	4	2	8
11	11	4	4	10
00	xx	Filter Disabled		

Note 1: The timing values of T_{OEH} and T_{OEL} are minimum and T_{OET} is maximum at room temperature and V_{DD} = 3.0V, 32 kHz oscillator.

T_{OEH} is measured from the rising edge of the demodulator output to the first falling edge. The pulse width must fall within $T_{OEH} \le t \le T_{OET}$.

T_{OEL} is measured from the falling edge of the demodulator output to the rising edge of the next pulse. The pulse width must fall within $T_{OEL} \le t \le T_{OET}$.

T_{OET} is measured from rising edge to the next rising edge (i.e., the sum of T_{OEH} and T_{OEL}). The sum of T_{OEH} and T_{OEL} must be $t \le T_{OET}$. If the Configuration Register 0 (Register 5-1), OEH<8:7> is set to '00', then the filter is disabled. See Figure 2-30 for this case.

The filter will reset, requiring a complete new successive high and low period to enable LFDATA, under the following conditions.

- The received high is not greater than the configured minimum T_{OEH} value.
- During T_{OEH}, a loss of signal for longer than 56 µs causes a filter Reset.
- The received low is not greater than the configured minimum T_{OEL} value.
- The received sequence exceeds the maximum T_{OET} value:
  - $T_{OEH} + T_{OEL} > T_{OET}$
  - or $T_{OEH} > T_{OET}$
  - or $T_{OEL} > T_{OET}$
- A Soft Reset SPI command is received.

If the filter resets due to a long high-time ($T_{OEH} > T_{OET}$), the high-pulse timer will not begin timing again until after a gap of T_E and another low-to-high transition occurs on the demodulator output.

Disabling the output enable filter disables the T_{OEH} and T_{OEL} requirement and the device passes all detected data. See Figures 2-30, 2-31 and 2-32 for examples.

When viewed from an application perspective, from the pin input, the actual output enable filter timing must factor in the analog delays in the input path (such as demodulator charge and discharge times).

- $T_{OEH} - T_{DR} + T_{DF}$
- $T_{OEL} + T_{DR} - T_{DF}$

The output enable filter starts immediately after T_{GAP}, the gap after AGC stabilization period.

5.15 Input Sensitivity Control

The device has typical input sensitivity of 3 mV_{PP}. This means any input signal with amplitude greater than 3 mV_{PP} can be detected. The internal AGC loop regulates the detecting signal amplitude when the input level is greater than approximately 20 mV_{PP}. This signal amplitude is called "AGC-active level". The AGC loop regulates the input voltage so that the input signal amplitude range will be kept within the linear range of the detection circuits without saturation. The AGC Active Status bit (AGCACT<5>) in STATUS Register 7 (Register 5-8) is set if the AGC loop regulates the input voltage.

Table 5-2 shows the input sensitivity comparison when the AGCSIG option is used. When AGCSIG option bit is set, the demodulated output is available only when the AGC loop is active (see Table 5-1). The channel input sensitivity can be reduced by setting the appropriate Configuration registers. Configuration Register 3 (Register 5-4), Configuration Register 4 (Register 5-5) and Configuration Register 5 (Register 5-6) have the option to reduce each channel gain from 0 dB to approximately -30 dB.

TABLE 5-2: INPUT SENSITIVITY VS. MODULATED SIGNAL STRENGTH SETTING (AGCSIG <7>)

AGCSIG<7> (Config. Register 5)	Description	Input Sensitivity (Typical)
0	Option Disabled – Detect any input signal level (demodulated data and carrier clock)	3.0 mV_{PP}
1	Option Enabled – No output until AGC Status = 1 (i.e., $V_{PEAK} \approx 20$ mV_{PP}) (demodulated data and carrier clock) • Provides the best signal to noise ratio	20 mV_{PP}

5.16 Enable or Disable of Input Channel

The Input channel can be enabled or disabled by programming the LCXEN bit in Configuration Register 0 (Register 5-1). When the input channel is enabled, it detects the input signal and provides output. When the channel is disabled, the device shuts down the input channel and provides no output, while saving current draws. The exact circuits disabled when an input is disabled are amplifiers, detector, full-wave rectifier, data slicer, and modulation FET. However, the RF input limiter remains active to protect the silicon from excessive antenna input voltages.

5.17 AGC Amplifier

The circuit automatically amplifies input signal voltage levels to an acceptable level for the data slicer. Fast attacking and slow releasing by nature, the AGC tracks the carrier signal level and not the modulated data bits.

The AGC requires an AGC initialization time (T_{AGC}). The AGC will attempt to regulate the input channel's peak signal voltage into the data slicer to a desired regulated AGC voltage – reducing the input path's gain as the signal level attempts to increase above regulated AGC voltage, and allowing full amplification on signal levels below the regulated AGC voltage.

The AGC has two modes of operation:

- During the AGC initialization time (T_{AGC}), the AGC time constant is fast, allowing a reasonably short acquisition time of the continuous input signal.
- After T_{AGC}, the AGC switches to a slower time constant for data slicing.

Also, the AGC is frozen when the input signal envelope is low. The AGC tracks only high envelope levels.

5.18 AGC Preserve

The AGC preserve feature is used to preserve the AGC value during the AGC initialization time (T_{AGC}) and apply the value to the data slicing circuit for the following data streams instead of using a new tracking value. This feature is useful to demodulate the input signal correctly when the input has random amplitude variations at a given time period. This feature is enabled when the device receives an AGC Preserve On command and disabled if it receives an AGC Preserve Off command. Once the AGC Preserve On command is received, the device acquires a new AGC value during each AGC initialization time and preserves the value until a Soft Reset or an AGC Preserve Off command is issued. Therefore, it does not need to issue another AGC Preserve On command. An AGC Preserve Off command is needed to disable the AGC preserve feature (see **Section 5.30.2.5 "AGC Preserve On Command"** and **Section 5.30.2.6 "AGC Preserve Off Command"** for AGC Preserve commands).

5.19 Soft Reset

The Soft Reset is issued in the following events:

a) After Power-on Reset (POR)
b) After Inactivity Timer time-out
c) If an "Abort" occurs
d) After receiving SPI Soft Reset command

The "Abort" occurs if there is no positive signal detected at the end of the AGC initialization period (T_{AGC}). The Soft Reset initializes internal circuits and brings the device into a low current Standby mode operation. The internal circuits that are initialized by the Soft Reset include:

- Output Enable Filter
- AGC circuits
- Demodulator
- 32 kHz Internal Oscillator

The Soft Reset has no effect on the Configuration register setup, except for some of the AFE STATUS Register 7 bits. (Register 5-8).

The circuit initialization takes one internal clock cycle (1/32 kHz = 31.25 µs). During the initialization, the modulation transistors between each input and LCCOM pins are turned-on to discharge any internal/external parasitic charges. The modulation transistors are turned-off immediately after the initialization time.

The Soft Reset is executed in Active mode only. It is not valid in Standby mode.

5.20 Minimum Modulation Depth Requirement for Input Signal

The device demodulates the modulated input signal if the modulation depth of the input signal is greater than the minimum requirement that is programmed in Configuration Register 5 (Register 5-6). Figure 5-5 shows the definition of the modulation depth and examples. MODMIN<6:5> of the Configuration Register 5 offer four options. They are 60%, 33%, 14% and 6%. The default setting is 33%.

The purpose of this feature is to enhance the demodulation integrity of the input signal. The 6% setting is the best choice for the input signal with weak modulation depth, which is typically observed near the high-voltage Base Station antenna and also at far-distance from the Base Station antenna. It gives the best demodulation sensitivity, but is very susceptible to noise spikes that can result in a bit detection error. The 60% setting can reduce the bit errors caused by noise, but gives the least demodulation sensitivity. See Table 5-3 for minimum modulation depth requirement settings.

TABLE 5-3: SETTING FOR MINIMUM MODULATION DEPTH REQUIREMENT

MODMIN Bits (Config. Register 5)		Modulation Depth
Bit 6	Bit 5	
0	0	33% (default)
0	1	60%
1	0	14%
1	1	8%

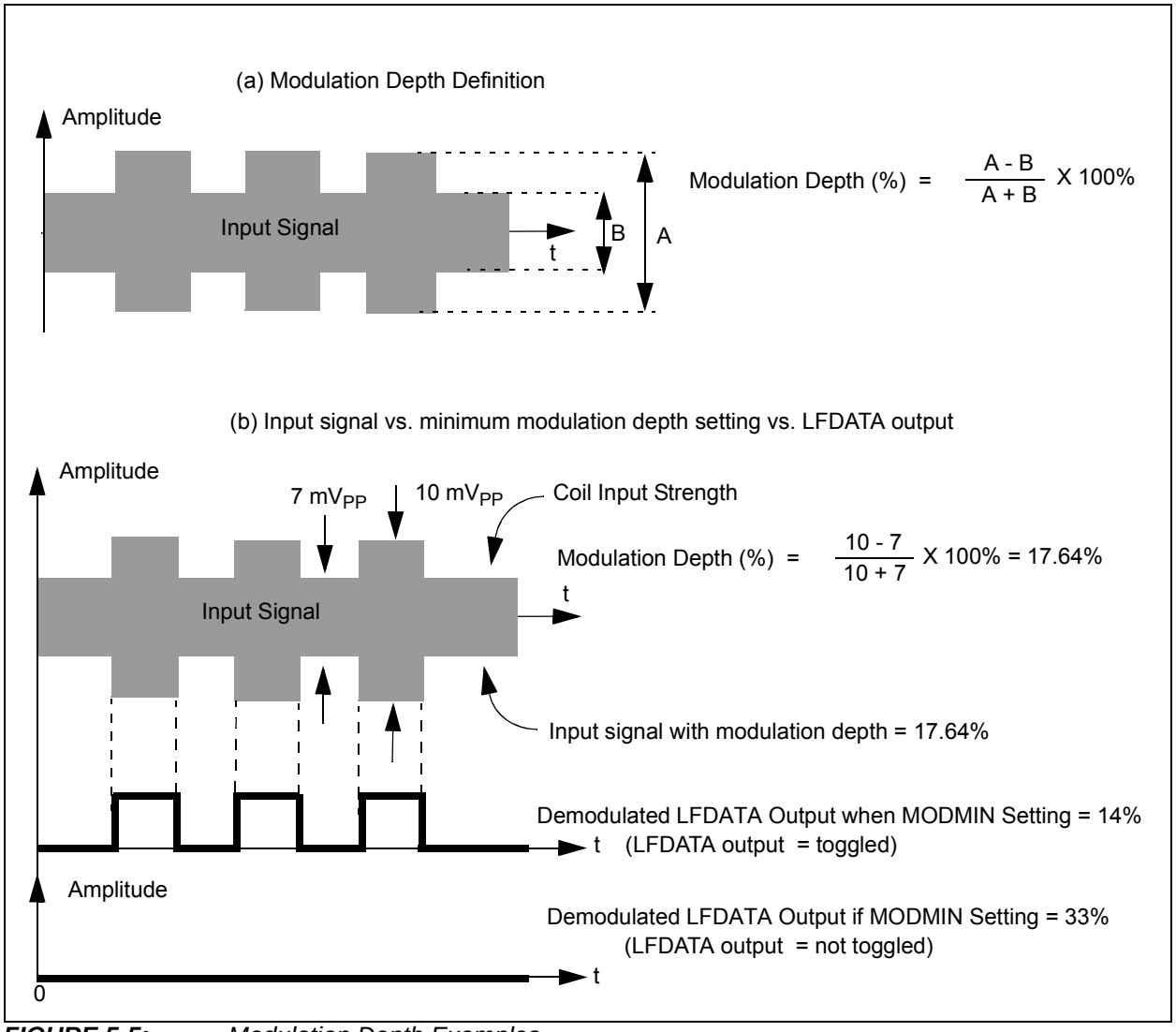


FIGURE 5-5: *Modulation Depth Examples.*

5.21 Low-Current Sleep Mode

The device can stay at an ultra low-current mode (Sleep mode) when it receives a Sleep command via the Serial Peripheral Interface (SPI). All circuits including the RF Limiter, except the minimum circuitry required to retain register memory and SPI capability, will be powered down to minimize the current draw. Power-on Reset or any SPI command, other than the Sleep command, is required to wake the device from Sleep.

5.22 Low-Current Standby Mode

The device is in Standby mode when no input signal is present on the input pin, but is powered and ready to receive any incoming signals.

5.23 Low-Current Active Mode

The device is in Low-Current Active mode when an input signal is present on any input pin and internal circuitry is switching with the received data.

5.24 Error Detection of Configuration Register Data

The Configuration registers are volatile memory. Therefore, the contents of the registers can be corrupted or cleared by any electrical incidence, such as battery disconnect. To ensure data integrity, the device has an error detection mechanism using row and column parity bits of the Configuration register memory map. The bit 0 of each register is a row parity bit which is calculated over the eight Configuration bits (from bit 1 to bit 8). The Column Parity Register (Configuration Register 6) holds column parity bits; each bit is calculated over the respective columns (Configuration registers 0 to 5) of the Configuration bits. The STATUS register is not included for the column parity bit calculation. Parity is to be odd. The parity bit, set or cleared, makes an odd number of set bits. The user needs to calculate the row and column parity bits using the contents of the registers and program them. During operation, the device continuously calculates the row and column parity bits of the configuration memory map. If a parity error occurs, the device lowers the SCLK/$\overline{\text{ALERT}}$ pin (interrupting the microcontroller section) indicating the configuration memory has been corrupted or unloaded and needs to be reprogrammed.

At an initial condition after a Power-on Reset, the values of the registers are all clear (default condition). Therefore, the device will issue the parity bit error by lowering the SCLK/$\overline{\text{ALERT}}$ pin. If the user reprograms the registers with the correct parity bits, the SCLK/$\overline{\text{ALERT}}$ pin will be toggled to logic high level immediately.

The parity bit errors do not change or affect any functional operation.

Table 5-4 shows an example of the register values and corresponding parity bits.

TABLE 5-4: CONFIGURATION REGISTER PARITY BIT EXAMPLE

Register Name	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (Row Parity)
Configuration Register 0	1	0	1	0	1	0	0	0	0
Configuration Register 1	0	0	0	0	0	0	0	0	1
Configuration Register 2	0	0	0	0	0	0	0	0	1
Configuration Register 3	0	0	0	0	0	0	0	0	1
Configuration Register 4	0	0	0	0	0	0	0	0	1
Configuration Register 5	1	0	0	0	0	0	0	0	0
Configuration Register 6 (Column Parity Register)	1	1	0	1	0	1	1	1	1

5.25 Factory Calibration

The device is calibrated during probe test to reduce the device-to-device variation in standby current, internal timing and sensitivity, as well as channel-to-channel sensitivity variation.

5.26 De-Q'ing of Antenna Circuit

When the transponder is close to the Base Station, the transponder coil may develop coil voltage higher than V_{DE_Q}. This condition is called "near field". The device detects the strong near field signal through the AGC control, and de-Q'ing the antenna circuit to reduce the input signal amplitude.

5.27 Demodulator

The demodulator recovers the modulation data from the received signal, containing carrier plus data, by appropriate envelope detection. The demodulator has a fast rise (charge) time (T_{DR}) and a fall time (T_{DF}) appropriate to an envelope of input signal (see **Section 1.0 "Electrical Specifications"** for T_{DR} and T_{DF} specifications). The demodulator contains the full-wave rectifier, low-pass filter, peak detector and data slicer.

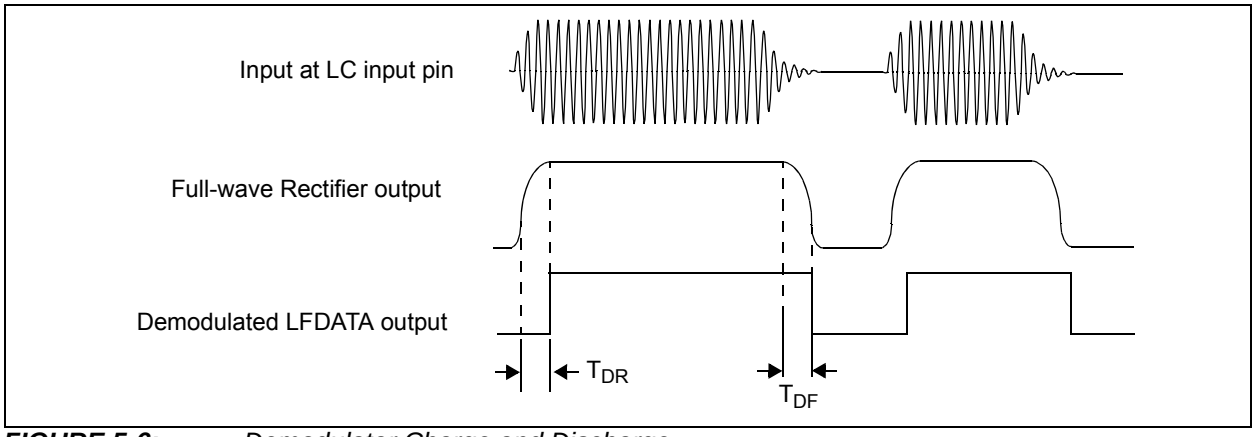


FIGURE 5-6: *Demodulator Charge and Discharge.*

5.28 Power-On Reset

This circuit remains in a Reset state until a sufficient supply voltage is applied. The Reset releases when the supply is sufficient for correct device operation, nominally V_{POR}.

The Configuration registers are all cleared on a Power-on Reset. As the Configuration registers are protected by odd row and column parity, the $\overline{\text{ALERT}}$ pin will be pulled down – indicating to the external micro-controller section that the configuration memory is cleared and requires new programming.

5.29 LFDATA Output Selection

The device output is available only when the input channel is enabled (LCXEN = Enabled in Configuration Register 0).

The LFDATA output can be configured to pass the Demodulator output, Received Signal Strength Indicator (RSSI) output, or Carrier Clock (CCLK). See Configuration Register 1 (Register 5-2) for more details.

5.29.1 DEMODULATOR OUTPUT

The demodulator output is the default configuration of the output selection. This is the output of an envelope detection circuit. See Figure 5-6 for the demodulator output.

When the demodulated output is selected, the output is available in two different conditions depending on how the options of Configuration Register 0 (Register 5-1) are set: Output Enable Filter is disabled or enabled. See **Section 2.0 "Typical Performance Curves"** for various demodulated data output.

Related Configuration register bits:

- Configuration Register 1 (Register 5-2), DATOUT <8:7>:

bit 8	bit 7	
0	0	0: Demodulator Output
0	1	1: Carrier Clock Output
1	0	0: RSSI Output
0	1	1: RSSI Output

- Configuration Register 0 (Register 5-1): all bits

5.29.2 CARRIER CLOCK OUTPUT

When the carrier clock output is selected, the LFDATA output is a square pulse of the input carrier clock and available as soon as the AGC stabilization time (T_{AGC}) is completed. There are two Configuration register options for the carrier clock output: (a) clock divide-by one or (b) clock divide-by four, depending on bit DATOUT<7> of Configuration Register 2 (Register 5-3). The carrier clock output is available immediately after the AGC settling time. The Output Enable Filter, AGCSIG, and MODMIN options are applicable for the carrier clock output in the same way as the demodulated output. See Figure 2-32 for carrier clock output examples.

Related Configuration register bits:

- Configuration Register 1 (Register 5-2), DATOUT <8:7>:

bit 8	bit 7	
0	0	Demodulator Output
0	1	Carrier Clock Output
1	0	RSSI Output
1	1	RSSI Output

- Configuration Register 2 (Register 5-3), CLKDIV<7>:

  0: Carrier Clock/1
  1: Carrier Clock/4

- Configuration Register 0 (Register 5-1): all bits are affected
- Configuration Register 5 (Register 5-6)

5.29.3 RECEIVED SIGNAL STRENGTH INDICATOR (RSSI) OUTPUT

An analog current output is available at the RSSI pin when the Received Signal Strength Indicator (RSSI) output is selected by the Configuration register. The analog current is linearly proportional to the input signal strength.

All timers in the circuit, such as the Inactivity Timer, Alarm Timer, and AGC initialization time, are disabled during the RSSI mode. Therefore, the RSSI output is not affected by the AGC stabilization time, and available immediately when the RSSI option is selected. The device enters Active mode immediately when the RSSI output is selected.

When the device receives an SPI command during the RSSI output, the RSSI mode is temporarily disabled until the SPI communication is completed. It returns to the RSSI mode again after the SPI communication is completed. The RSSI mode is held until another output type is selected ($\overline{CS}$ low turns off the RSSI signal).

The RSSI output current is linearly proportional to the input signal strength. There are variations between device to device. See Figure 2-13 for examples. The linearity (ILR_{RSSI}) of the RSSI output current is tested by sampling the outputs for three input points: 37 mV_{PP}, 100 mV_{PP}, and 370 mV_{PP}. The RSSI output current for 100 mV_{PP} of input signal is compared with the expected output current obtained from the line that is connecting the two endpoints (37 mV_{PP} and 370 mV_{PP}). Equation 5-1 and Figure 5-7 show the details for the RSSI linearity specification.

EQUATION 5-1: RSSI LINEARITY SPECIFICATION

$$ILR_{RSSI}(\%) = \frac{\text{Deviation at 100 } mV_{PP} \text{ of Input Signal}}{I_{RSSI} \text{ for 370 } mV_{PP} \text{ of Input Signal}} \times 100\%$$

Where:

- Deviation at 100 mV_{PP} of Input Signal = [I_{RSSI} measured - I_{RSSI} expected] at 100 mV_{PP} of input signal.
- I_{RSSI} expected = RSSI current obtained from the line that is connecting two endpoints (RSSI output currents for 37 mV_{PP} and 370 mV_{PP} of input).

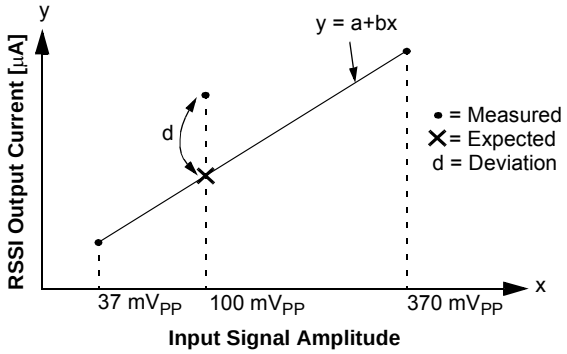


FIGURE 5-7: *RSSI Linearity Test Example.*

Related Configuration register bits:

- Configuration Register 1 (Register 5-2), DATOUT<8:7>:

bit 8	bit 7	
0	0	0: Demodulated Output
0	1	1: Carrier Clock Output
1	0	0: RSSI Output
1	1	1: RSSI Output

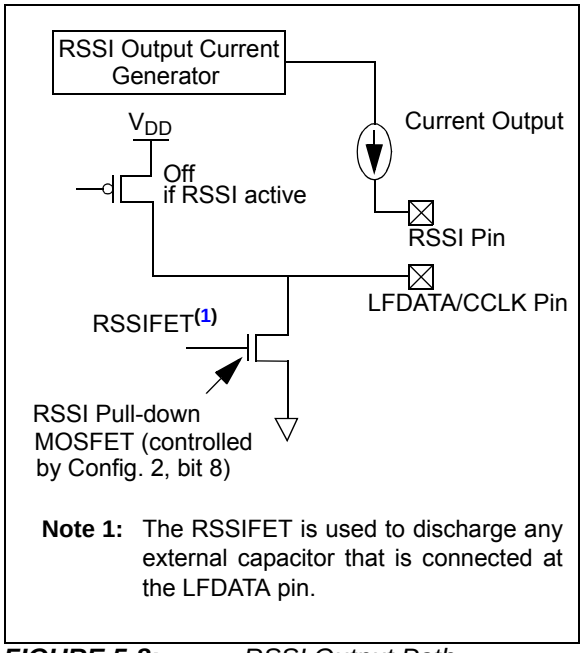
- Configuration Register 2 (Register 5-3), RSSIFET<8>:

  0: Pull-Down MOSFET off

  1: Pull-Down MOSFET on.

Note:	The pull-down MOSFET option is valid only when the RSSI output is selected. The MOSFET is not controllable by users when demodulated or carrier clock output option is selected.

- Configuration Register 0 (Register 5-1): all bits are affected.



Note 1: The RSSIFET is used to discharge any external capacitor that is connected at the LFDATA pin.

FIGURE 5-8: *RSSI Output Path.*

5.29.3.1 ANALOG-TO-DIGITAL DATA CONVERSION OF RSSI SIGNAL

The RSSI output is an analog current. It needs an external Analog-to-Digital (ADC) data conversion device for digitized output. The ADC data conversion can be accomplished by using a stand-alone external ADC device, an external MCU that has internal ADC features, or an external MCU that has no ADC features but instead uses firmware. The RSSIFET is used to discharge any external charge on the LFDATA pin in the RSSI Output mode. The MOSFET can be turned on or off with bit RSSIFET<8> of Configuration Register 2 (Register 5-3). When it is turned on, the internal MOSFET provides a discharge path for the external capacitor that is connected at the LFDATA pin. This MOSFET option is valid only if RSSI output is selected and not controllable by users for demodulated or carrier clock output options.

See separate application notes for various external ADC implementation methods for this device.

See Figure 5-8 for RSSI output path.

5.30 Configuration Registers

5.30.1 SPI COMMUNICATION

The SPI communication is used to read from or write to the Configuration registers and to send command-only messages. Three pins are used for SPI communication: $\overline{CS}$, SCLK/$\overline{ALERT}$, and LFDATA/RSSI/CCLK/SDIO. Figure 5-9, Figure 5-10 and Figure 5-11 show examples of the SPI communication sequences.

When these pins are connected to the external MCU I/O pins, the following are needed:

$\overline{CS}$

- Pin is permanently an input with an internal pull-up.

SCLK/$\overline{ALERT}$

- Pin is an open collector output when $\overline{CS}$ is high. An internal pull-up resistor exists to ensure no spurious SPI communication between powering and the MCU configuring its pins. This pin becomes the SPI clock input when $\overline{CS}$ is low.

LFDATA/CCLK/SDIO

- Pin is a digital output (LFDATA) so long as $\overline{CS}$ is high. During SPI communication, the pin is the SPI data input (SDI) unless performing a register Read, where it will be the SPI data output (SDO).

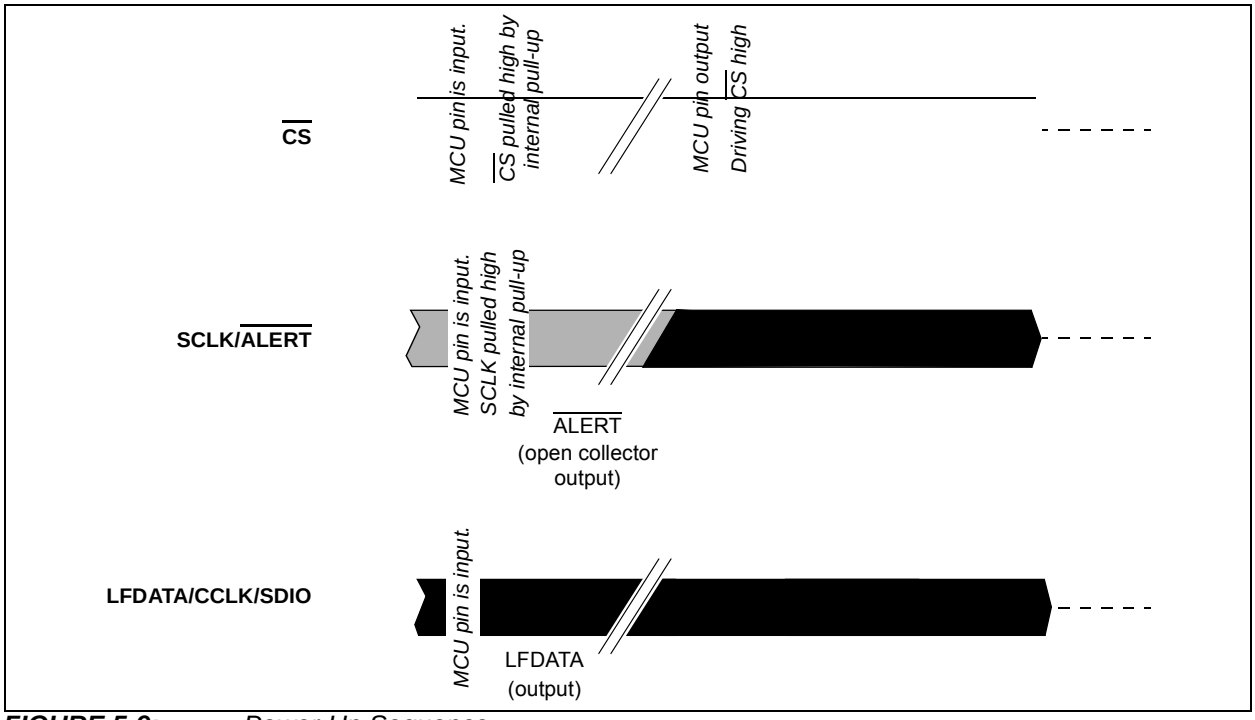
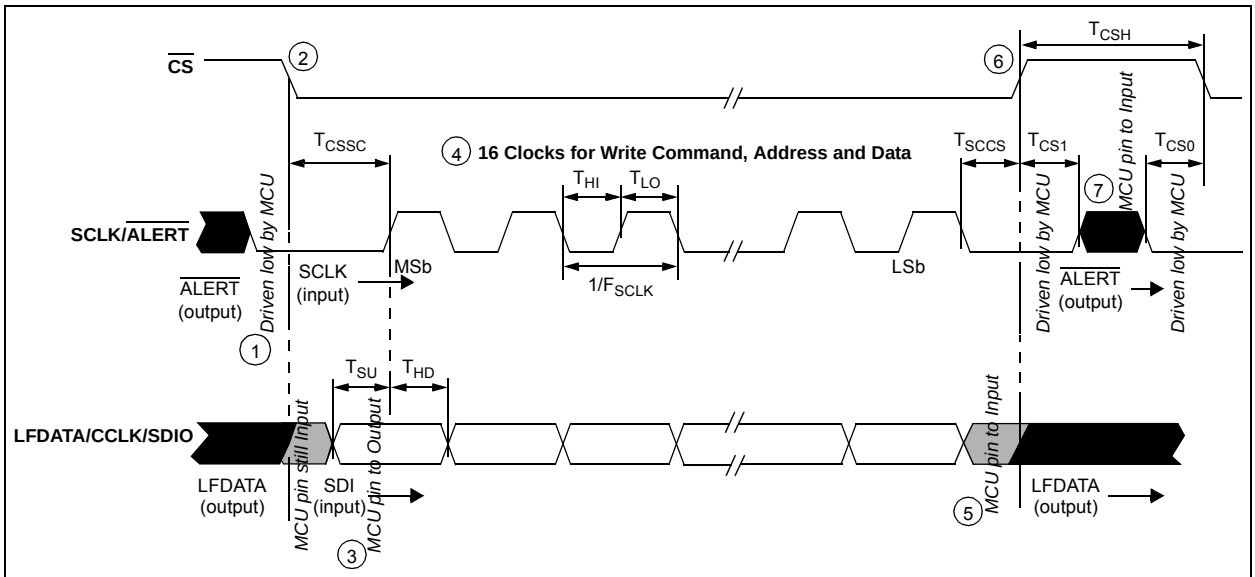


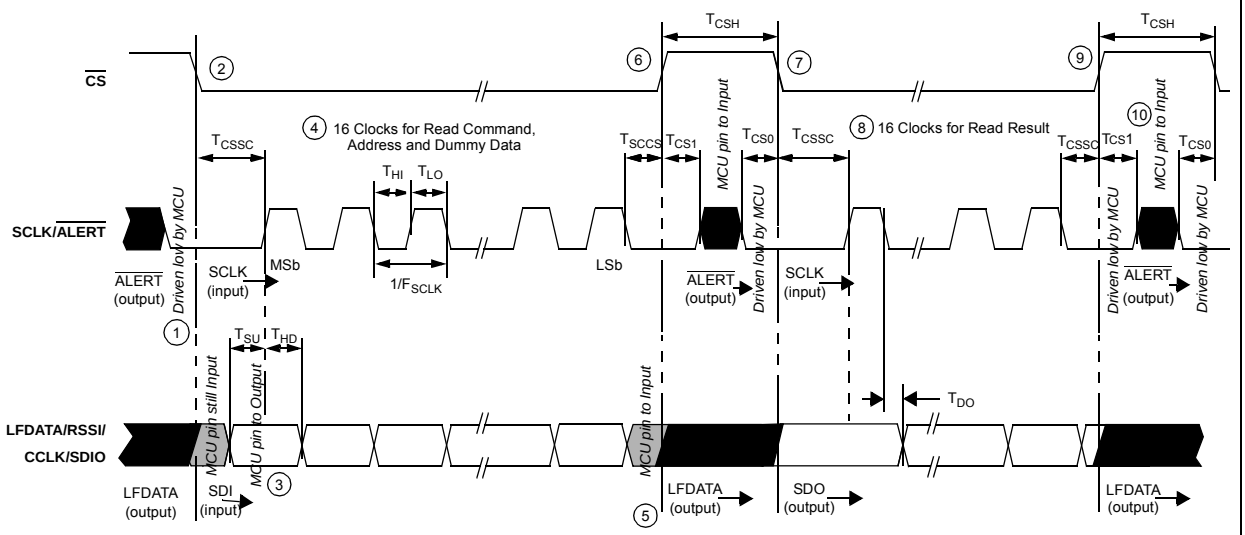
FIGURE 5-9: *Power-Up Sequence.*



MCU SPI Write Details:

1. Drive the open collector $\overline{\text{ALERT}}$ output low
   - To ensure no false clocks occur when $\overline{\text{CS}}$ drops
2. Drop $\overline{\text{CS}}$
   - SCLK/$\overline{\text{ALERT}}$ becomes SCLK input
   - LFDATA/CCLK/SDIO becomes SDI input
3. Change LFDATA/CCLK/SDIO connected pin to output
   - Driving SPI data
4. Clock in 16-bit SPI Write sequence – command, address, data and parity bit
   - Command, address, data and parity bit
5. Change LFDATA/CCLK/SDIO connected pin to input
6. Raise $\overline{\text{CS}}$ to complete the SPI Write
7. Change SCLK/$\overline{\text{ALERT}}$ back to input

FIGURE 5-10: *SPI Write Sequence.*



MCU SPI Read Details:

1. Drive the open collector $\overline{\text{ALERT}}$ output low
   - To ensure no false clocks occur when $\overline{\text{CS}}$ drops
2. Drop $\overline{\text{CS}}$
   - SCLK/$\overline{\text{ALERT}}$ becomes SCLK input
   - LFDATA/CCLK/SDIO becomes SDI input
3. Change LFDATA/CCLK/SDIO connected pin to output
   - Driving SPI data
4. Clock in 16-bit SPI Read sequence
   - Command, address and dummy data
5. Change LFDATA/CCLK/SDIO connected pin to input
6. Raise $\overline{\text{CS}}$ to complete the SPI Read entry of command and address
7. Drop $\overline{\text{CS}}$
   - AFE SCLK/$\overline{\text{ALERT}}$ becomes SCLK input
   - LFDATA/CCLK/SDIO becomes SDO output
8. Clock out 16-bit SPI Read result
   - First seven bits clocked-out are dummy bits
   - Next eight bits are the Configuration register data
   - The last bit is the Configuration register row parity bit
9. Raise $\overline{\text{CS}}$ to complete the SPI Read
10. Change SCLK/$\overline{\text{ALERT}}$ back to input

Note: The T_{CSH} is considered as one clock. Therefore, the Configuration register data appears at 6th clock after T_{CSH}.

FIGURE 5-11: *SPI Read Sequence.*

5.30.2 COMMAND DECODER/ CONTROLLER

The circuit executes eight SPI commands from the external MCU. The command structure is:

Command (3 bits) + Configuration Address (4 bits) + Data Byte and Row Parity Bit with the Most Significant bit first. Table 5-5 shows the available SPI commands.

The device operates in SPI mode 0,0. In mode 0,0 the clock idles in the low state (Figure 5-12). SDI data is loaded into the device on the rising edge of SCLK and SDO data is clocked out on the falling edge of SCLK. There must be multiples of 16 clocks (SCLK) while $\overline{CS}$ is low or commands will abort.

TABLE 5-5: SPI COMMANDS

Command	Address	Data	Row Parity	Description
Command only – Address and Data are "Don't Care", but need to be clocked in regardless.				
000	XXXX	XXXX XXXX	X	Clamp on – enable modulation circuit
001	XXXX	XXXX XXXX	X	Clamp off – disable modulation circuit
010	XXXX	XXXX XXXX	X	Enter Sleep mode (any other command wakes the AFE)
011	XXXX	XXXX XXXX	X	AGC Preserve On – to temporarily preserve the current AGC level
100	XXXX	XXXX XXXX	X	AGC Preserve Off – AGC again tracks strongest input signal
101	XXXX	XXXX XXXX	X	Soft Reset – resets various circuit blocks
Read Command – Data will be read from the specified register address.				
110	0000	Config Byte 0	P	General – options that may change during normal operation
	0001	Config Byte 1	P	Input channel (LCX) antenna tuning and LFDATA output format
	0010	Config Byte 2	P	RSSIFET Condition and CLKDIV settings
	0011	Config Byte 3	P	Not used
	0100	Config Byte 4	P	Input channel (LCX) sensitivity reduction
	0101	Config Byte 5	P	Modulation depth and AGC loop
	0110	Column Parity	P	Column parity byte for Config Byte 0 -> Config Byte 5
	0111	Status	X	The device's internal operation status and parity error indication bits
Write Command – Data will be written to the specified register address.				
111	0000	Config Byte 0	P	Output enable filter, channel enable/disable, etc.
	0001	Config Byte 1	P	Input channel (LCX) antenna tuning and LFDATA output type
	0010	Config Byte 2	P	RSSIFET, CLKDIV
	0011	Config Byte 3	P	Write all bits to "0s"
	0100	Config Byte 4	P	Input channel (LCX) sensitivity reduction
	0101	Config Byte 5	P	AGCSIG, MODMIN
	0110	Column Parity	P	Column parity byte (odd parity) for Configuration Bytes 0 to 5
	0111	Not Used	X	Register is readable, but not writable

Note: 'P' denotes the row parity bit (odd parity) for the respective data byte.

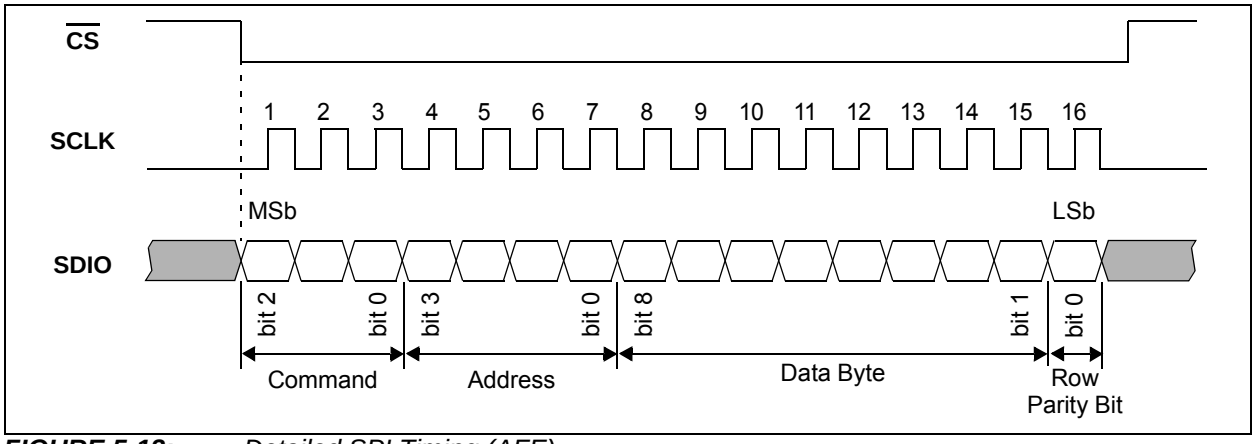


FIGURE 5-12: *Detailed SPI Timing (AFE).*

5.30.2.1 Clamp On Command

This command results in activating (turning on) the modulation transistor of the input channel.

5.30.2.2 Clamp Off Command

This command results in deactivating (turning off) the modulation transistor of input channel.

5.30.2.3 Sleep Command

This command places the device in Sleep mode – minimizing current draw by disabling all but the essential circuitry. Any other command wakes the device from Sleep (e.g., Clamp Off command).

5.30.2.4 Soft Reset Command

The device issues a Soft Reset when it receives an external Soft Reset command. The external Soft Reset command is typically used to end a SPI communication sequence or to initialize the device for the next signal detection sequence, etc. See **Section 5.19 "Soft Reset"** for more details on Soft Reset.

If a Soft Reset command is sent during a "Clamp-on" condition, the device still keeps the "Clamp-on" condition after the Soft Reset execution. The Soft Reset is executed in Active mode only, not in Standby mode. The SPI Soft Reset command is ignored if the device is not in Active mode.

5.30.2.5 AGC Preserve On Command

This command results in preserving the AGC level during each AGC initialization time and applies the value to the data slicing circuit for the following data stream. The preserved AGC value is reset by a Soft Reset, and a new AGC value is acquired and preserved when it starts a new AGC initialization time. This feature is disabled by an AGC Preserve Off command (see **Section 5.18 "AGC Preserve"**).

5.30.2.6 AGC Preserve Off Command

This command disables the AGC preserve feature and returns to the normal AGC tracking mode, fast tracking during AGC settling time and slow tracking after that (see **Section 5.18 "AGC Preserve"**).

5.30.3 READ/WRITE COMMANDS FOR CONFIGURATION REGISTERS

The device includes eight Configuration registers, including a Column Parity register and STATUS register. All registers are readable and writable via SPI commands, except the STATUS register, which is read-only. Bit 0 of each register is a row parity bit (except for STATUS Register 7) that makes the register contents an odd number ("1") including the parity bit itself.

Note:	If the odd parity bits for the row and column are incorrectly programmed, the Parity Error Indicator (PEI) bit in the Status Register 7 is set ("1") and the ALERT output pin will pull low, which causes extra current draws.

5.30.3.1 STATUS Register

The status register indicates the operation condition of the MCP2035 device after various SPI commands and Power-on Reset. See Table 5-7 for more details.

TABLE 5-6: CONFIGURATION REGISTERS SUMMARY

Register Name	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration Register 0	OEH		OEL		ALRTIND	1 **(Note 1)**	1 **(Note 1)**	LCXEN	R0PAR
Configuration Register 1	DATOUT		Input Channel (LCX) Tuning Capacitor						R1PAR
Configuration Register 2	RSSIFET	CLKDIV	Write to all 0's **(Note 1)**						R2PAR
Configuration Register 3	Unimplemented		Write to all 0's **(Note 1)**						R3PAR
Configuration Register 4	Input Channel (LCX) Sensitivity Control				Write to all 0's **(Note 1)**				R4PAR
Configuration Register 5	0 **(Note 1)**	AGCSIG	MODMIN	MODMIN	Write to all 0's **(Note 1)**				R5PAR
Column Parity Bit Register 6	Column Parity Bits								R6PAR
STATUS Register 7	Active Channel Indicators			AGCACT	Wake-up Channel Indicators			ALARM	PEI

Note 1: The values in the colored area are strongly recommended for the best result.

2: The user must compute the odd row parity bit (bit 0 of each row) and odd column parity bits in the Column Parity Bit Register 6, and program them the same as other configuration registers.

3: STATUS Register is read only register.

REGISTER 5-1: CONFIGURATION REGISTER 0 (ADDRESS: 0000)

R/W-0
OEH1
bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OEH0	OEL1	OEL0	ALRTIND	1	1	LCXEN	R0PAR
bit7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 8-7 **OEH<1:0>**: Output Enable Filter High Time (T_{OEH}) bit
`00` = Output Enable Filter disabled (no wake-up sequence required, passes all signals to LFDATA)
`01` = 1 ms
`10` = 2 ms
`11` = 4 ms

bit 6-5 **OEL<1:0>**: Output Enable Filter Low Time (T_{OEL}) bit
`00` = 1 ms
`01` = 1 ms
`10` = 2 ms
`11` = 4 ms

bit 4 **ALRTIND**: $\overline{\text{ALERT}}$ bit, output triggered by:
`1` = Parity error and/or expired Alarm Timer (receiving noise, see **Section 5.13.3 "Alarm Timer"**)
`0` = Parity error

bit 3-2 **Write these two bits to all "1". (Note 1)**

bit 1 **LCXEN:** Input Channel (LCX) Enable bit
`1` = Disabled
`0` = Enabled

bit 0 **R0PAR**: Register 0 Parity bit – set or cleared (`1` or `0`) so the 9-bit register contains odd parity – an odd number of set bits. An incorrect parity bit may draw unnecessary extra current.

Note 1: Writing these bits to "1" ensures disabling of internally grounded unused channels (LCY and LCZ), which guarantees minimizing any current draw through the unused internal channels.

REGISTER 5-2: CONFIGURATION REGISTER 1 (ADDRESS: 0001)

R/W-0
DATOUT1
bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATOUT0	LCXTUN5	LCXTUN4	LCXTUN3	LCXTUN2	LCXTUN1	LCXTUN0	R1PAR
bit7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 8-7 **DATOUT<1:0>:** LFDATA Output type bit
00 = Demodulated output
01 = Carrier clock output
10 = RSSI output
11 = RSSI output

bit 6-1 **LCXTUN<5:0>:** LCX Tuning Capacitance bit
000000 = +0 pF (Default)
•
•
111111 = +63 pF

bit 0 **R1PAR**: Register 1 Parity Bit – set or cleared (1 or 0) so the 9-bit register contains odd parity – an odd number of set bits. An incorrect parity bit may draw unnecessary extra current.

REGISTER 5-3: CONFIGURATION REGISTER 2 (ADDRESS: 0010)

R/W-0
RSSIFET
bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLKDIV	0	0	0	0	0	0	R2PAR
bit7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 8 **RSSIFET**: Pull-down MOSFET on LFDATA pad bit (controllable by user in the RSSI mode only)
1 = Pull-down RSSI MOSFET on
0 = Pull-down RSSI MOSFET off

bit 7 **CLKDIV:** Carrier Clock Divide-by bit
1 = Carrier clock/4
0 = Carrier clock/1

bit 6-1 **Recommended to all 0's. (Note 1)**

bit 0 **R2PAR**: Register 2 Parity bit – set or cleared (1 or 0) so the 9-bit register contains odd parity – an odd number of set bits. An incorrect parity bit may draw unnecessary extra current.

Note 1: These bits are associated to the internally grounded LCY tuning capacitors, and have no effect in the MCP2035.

REGISTER 5-4: CONFIGURATION REGISTER 3 (ADDRESS: 0011)

U-0
bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	0	0	0	0	0	0	R3PAR
bit7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 8-7 **Unimplemented**: Read as '0'

bit 6-1 **Recommended to all 0's. (Note 1)**

bit 0 **R3PAR**: Register 3 Parity Bit – set or cleared (1 or 0) so the 9-bit register contains odd parity – an odd number of set bits. An incorrect parity bit may draw unnecessary extra current.

Note 1: These bits are associated to the internally grounded LCZ tuning capacitors, and have no effect in the MCP2035.

REGISTER 5-5: CONFIGURATION REGISTER 4 (ADDRESS: 0100)

R/W-0
LCXSEN3
bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LCXSEN2	LCXSEN1	LCXSEN0	0	0	0	0	R4PAR
bit7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 8-5 **LCXSEN<3:0>**: Typical Input Channel (LCX) Sensitivity Reduction bit. **(Note 1)**

`0000` = -0 dB (Default)
`0001` = -2 dB
`0010` = -4 dB
`0011` = -6 dB
`0100` = -8 dB
`0101` = -10 dB
`0110` = -12 dB
`0111` = -14 dB
`1000` = -16 dB
`1001` = -18 dB
`1010` = -20 dB
`1011` = -22 dB
`1100` = -24 dB
`1101` = -26 dB
`1110` = -28 dB
`1111` = -30 dB

bit 4-1 **Recommended to all `0`'s. (Note 2)**

bit 0 **R4PAR**: Register 4 Parity bit – set or cleared (`1` or `0`) so the 9-bit register contains odd parity – an odd number of set bits. An incorrect parity bit may draw unnecessary extra current.

Note 1: Assured monotonic increment (or decrement) by design.

2: These bits are associated to the internally grounded LCY sensitivity control, and have no effect in the MCP2035.

REGISTER 5-6: CONFIGURATION REGISTER 5 (ADDRESS: 0101)

R/W-0
0
bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AGCSIG	MODMIN1	MODMIN0	0	0	0	0	R5PAR
bit7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 8 **Recommended to write** '0': This bit has no effect in the MCP2035.

bit 7 **AGCSIG**: Demodulator Output Enable bit, after the AGC loop is active
1 = Enabled – No output until AGC is regulating at around 20 mV_{PP} at input pin. The AGC Active Status bit is set when the AGC begins regulating.
0 = Disabled – The device passes signal of any level it is capable of detecting

bit 6-5 **MODMIN<1:0>**: Minimum Modulation Depth bit
00 = 33%
01 = 60%
10 = 14%
11 = 8%

bit 4-1 **Recommended to all 0's. (Note 1)**

bit 0 **R5PAR**: Register 5 Parity bit – set or cleared (1 or 0) so the 9-bit register contains odd parity – an odd number of set bits. An incorrect parity bit may draw unnecessary extra current.

Note 1: These bits are associated to the internally grounded LCZ sensitivity control.

REGISTER 5-7: COLUMN PARITY REGISTER 6 (ADDRESS: 0110)

R/W-0
COLPAR7
bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
COLPAR6	COLPAR5	COLPAR4	COLPAR3	COLPAR2	COLPAR1	COLPAR0	R6PAR
bit7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 8 **COLPAR7**: Set or Cleared (1 or 0) so that this 8th parity bit (COLPAR7) + the sum of the Config. register row parity bits contain an odd number of set ("1") bits.

bit 7 **COLPAR6**: Set or Cleared (1 or 0) such that this 7th parity bit (COLPAR6) + the sum of the 7th bits in Config. registers 0 through 5 contain an odd number of set ("1") bits.

bit 6 **COLPAR5**: Set or Cleared (1 or 0) such that this 6th parity bit (COLPAR5) + the sum of the 6th bits in Config. registers 0 through 5 contain an odd number of set ("1") bits.

bit 5 **COLPAR4**: Set or Cleared (1 or 0) such that this 5th parity bit (COLPAR4) + the sum of the 5th bits in Config. registers 0 through 5 contain an odd number of set ("1") bits.

bit 4 **COLPAR3**: Set or Cleared (1 or 0) such that this 4th parity bit (COLPAR3) + the sum of the 4th bits in Config. registers 0 through 5 contain an odd number of set ("1") bits.

bit 3 **COLPAR2**: Set or Cleared (1 or 0) such that this 3rd parity bit (COLPAR2) + the sum of the 3rd bits in Config. registers 0 through 5 contain an odd number of set ("1") bits.

bit 2 **COLPAR1**: Set or Cleared (1 or 0) such that this 2nd parity bit (COLPAR1) + the sum of the 2nd bits in Config. registers 0 through 5 contain an odd number of set ("1") bits.

bit 1 **COLPAR0**: Set or Cleared (1 or 0) such that this 1st parity bit (COLPAR0) + the sum of the 1st bits in Config. registers 0 through 5 contain an odd number of set ("1") bits.

bit 0 **R6PAR**: Register 6 Parity bit – Set or Cleared (1 or 0) so the 9-bit register contains odd ("1") parity – an odd number of set ("1") bits

Note 1: The parity bits are calculated from the configuration registers from 0 to 6 and programmed by the user. An incorrect parity bit can cause unnecessary extra current draws although the device may function correctly.

REGISTER 5-8: STATUS REGISTER 7 (ADDRESS: 0111)

R-0
CHZACT
bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CHYACT	CHXACT	AGCACT	WAKEZ	WAKEY	WAKEX	ALARM	PEI
bit7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 8 **CHZACT:** This bit has no meaning in the MCP2035. Therefore, ignore this bit. This bit can be cleared via Soft Reset.

bit 7 **CHYACT:** This bit has no meaning in the MCP2035. Therefore, ignore this bit. This bit can be cleared via Soft Reset

bit 6 **CHXACT**: Input Channel (LCX) Active bit (cleared via Soft Reset). **(Note 1)**
1 = Input Channel (LCX) is passing data after T_{AGC}
0 = Input Channel (LCX) is not passing data after T_{AGC}

bit 5 **AGCACT**: AGC Active Status bit (real time, cleared via Soft Reset)
1 = AGC is active (Input signal is strong). AGC is active when input signal level is approximately > 20 mV_{PP} range.
0 = AGC is inactive (Input signal is weak)

bit 4-3 This bit has no meaning, and can be cleared via Soft Reset.

bit 2 **WAKEX**: Wake-up Channel X Indicator Status bit (cleared via Soft Reset)
1 = Input Channel (LCX) caused a device wake-up (passed ÷64 clock counter)
0 = Input Channel (LCX) did not cause a device wake-up

bit 1 **ALARM**: Indicates whether an Alarm Timer time-out has occurred (cleared via read "STATUS Register command")
1 = The Alarm Timer time-out has occurred. It may cause the $\overline{\text{ALERT}}$ output to go low depending on the state of bit 4 of the Configuration register 0
0 = The Alarm Timer is not timed out

bit 0 **PEI**: Parity Error Indicator bit – indicates whether a Configuration register parity error has occurred (real time)
1 = A parity error has occurred and caused the $\overline{\text{ALERT}}$ output to go low
0 = A parity error has not occurred

Note 1: Bit is high whenever channel is passing data. Bit is low in Standby mode.

TABLE 5-7: STATUS REGISTER BIT CONDITION (AFTER POWER-ON RESET AND VARIOUS SPI COMMANDS)

Condition	Bit 8 (Note 2)	Bit 7 (Note 2)	Bit 6	Bit 5	Bit 4 (Note 2)	Bit 3 (Note 2)	Bit 2	Bit 1	Bit 0
	CHZACT	CHYACT	Input (CHX) ACT	AGCACT	WAKEZ	WAKEY	WAKEX	ALARM	PEI
POR	0	0	0	0	0	0	0	0	1
Read Command (STATUS Register only)	u	u	u	u	u	u	u	0	u
Sleep Command	u	u	u	u	u	u	u	u	u
Soft Reset Executed (Note 1)	0	0	0	0	0	0	0	u	u

Legend: u = unchanged

Note 1: See **Section 5.19 "Soft Reset"** and **Section 5.30.2.4 "Soft Reset Command"** for the condition of Soft Reset execution.

2: These bits have no meaning and are ignored in the MCP2035.

TABLE 5-8: EXAMPLE OF SELECTING CONFIGURATION REGISTER BIT VALUES AND PARITY BITS

Register Name	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (Calculated Row Parity Bit)	Condition
Config. Reg. 0	1	0	1	0	1	1	1	0	**0**	OEH = OEL = 2 ms, ALRTIND = 1, Input Channel (LCX) = Enabled
Config Reg. 1	0	0	0	0	0	0	0	1	**0**	Output Data Type = Demodulated Output, Input Tuning Capacitor Value = 1 pF
Config Reg. 2	0	0	0	0	0	0	0	0	**1**	RSSI Pull-Down MOSFET = Off, CLKDIV = 0
Config Reg. 3	0	0	0	0	0	0	0	0	**1**	Recommended
Config Reg. 4	0	0	0	0	0	0	0	0	**1**	Input Channel Sensitivity Reduction = None
Config Reg. 5	0	1	0	0	0	0	0	0	**0**	AGCSIG = 1, Min Modulation Depth = 33%
Calculated Column Parity Register 6	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	Calculated Column Odd Parity Bits

Note 1: The values in the colored area are strongly recommended for the best result.

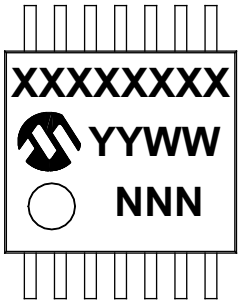
2: See the calculated row and column parity bits. These bits must be programmed by the user. See **Note** in **Section 5.30.3 "Read/Write Commands for Configuration Registers"** for the parity bits.

NOTES:

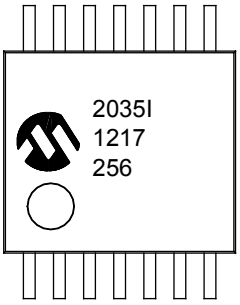
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

14-Lead TSSOP



Example

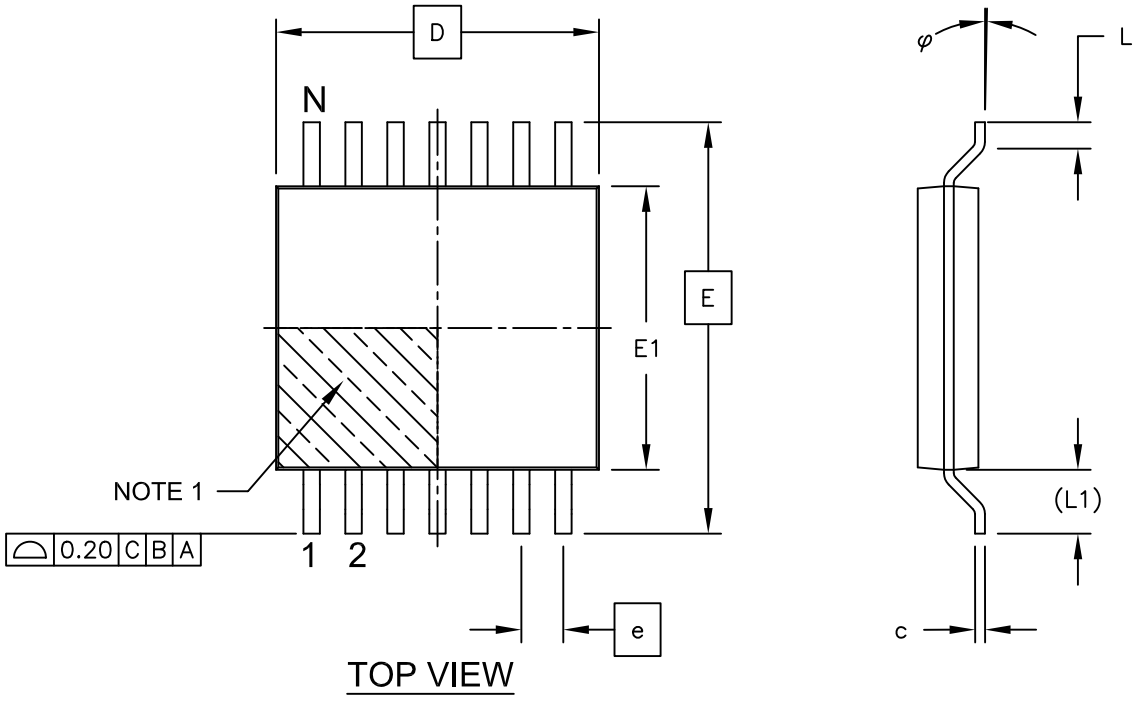


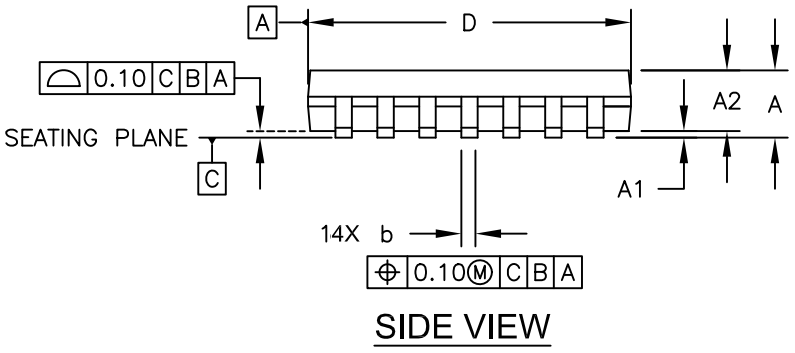
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
		This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

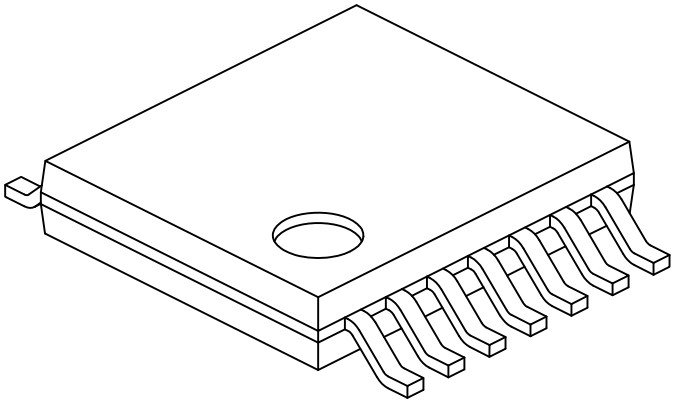




Microchip Technology Drawing C04-087C Sheet 1 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)		1.00 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

Notes:

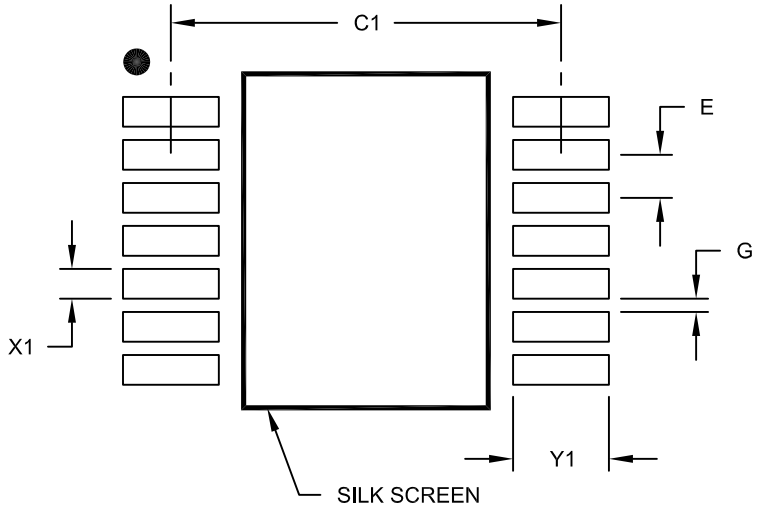
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X14)	X1			0.45
Contact Pad Length (X14)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

APPENDIX A: REVISION HISTORY

Revision A (May 2012)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP2035:		Single-Channel Stand-Alone Analog Front-end (AFE)
Temperature Range:	I	=	-40°C to +85°C (Industrial)
Package:	ST	=	Plastic Shrink Small outline (4.4 mm) - (TSSOP)

Examples:

a) MCP2035-I/ST: Industrial Temperature, 14LD TSSOP Package

b) MCP2035T-I/ST: Tape and Reel, Industrial Temperature, 14LD TSSOP Package

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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ISBN: 978-1-62076-2-684

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