# 13.56 MHz, Class-D Half Bridge, RF Generator with DRF1400

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## INTRODUCTION

The DRF1400 is a MOSFET Half Bridge (HB) Hybrid Device which has been optimized for efficiency and reduced system cost; it is targeted at the HF ISM market arena. The DRF1400 contains two gate drivers and two power MOSFETs, and can generate kilowatt level RF Power Output, at frequencies approaching 40 MHz. Higher power levels can be achieved by combing multiple modules.

This application note describes the DRF1400 Class-D HB design and measurements at 13.56 MHz, 1.7KW RF and > 87% efficiency. The DRF1400 CLASS-D HB reference design is available from Microsemi as a kit. This hardware allows designers to readily verify the design principals and circuit operation at 1.7KW. The Reference Design also teaches the critical design concepts of High Power RF Half Bridge topologies.

## DESIGN CONSIDERATIONS

To design the high-efficiency high-power Half Bridge RF generator the following issues must be addressed.

**Key requirements:**

- Pulse control signals must be exactly 180° out of phase.
- Control signal transformer must have minimum stray capacitance and leakage inductance.
- The bypass capacitors in the output section must large enough to bypass all AC signal to GND.
- A floating GND DC supply for High Side driver is required.
- Optimization of the output matching circuit.
- High-quality RF components
- Ferrite suppressors: on all DC lines, especially High Side driver.
- RF shielding is critical.
- The power levels provided by the DRF1400 require water cooling for most application.

The table below is the major specification of this RF Power Generator.

| Freq | Output Power | Voltage | Current | Efficiency |
|---|---|---|---|---|
| 13.56Mhz | 1.7KW | 300V | 6.45A | 87% |

**Table 1.** Key Specification

## THEORY OF OPERATION

A Simplified Class-D HB is illustrated in Figure 1. This circuit includes 3 sections: a High Side drive, Transformer (T1) and Q1; the Low Side drive, Transformer (T2) and Q2; and the Output Matching Section.

Class-D HB theoretically can provide near 100% efficiency, however conduction and switching losses in the MOSFET and magnetic losses reduce the efficiencies to a range of 85% to 95%.

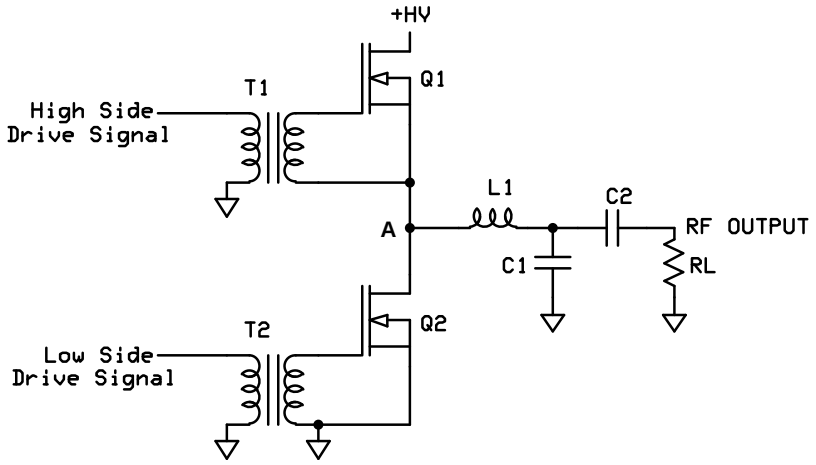



**Figure 1.** Simplified Half Bridge Circuit

Referring to Figure 1, the input transformers T1 and T2 provide gate drive power to MOSFETs, Q1 and Q2. These two MOSFETs are driven 180° out of phase. When Q1 is On, Q2 is Off; then Q1 is Off and Q2 is On. This alternating cycle between Q1 and Q2 produces a square wave at node (A). The square wave transition starts at zero volts and quickly rises to the (+HV), dwells at +HV for one half cycle and then quickly returns to zero volts.

The output matching circuit consists of a series Inductor L1, Shunt Capacitor C1 and Series Capacitor C2. This network provides a sinusoidal RF signal into the 50Ω load. The output matching circuit (L1, C1 and C2) is optimized to provide a sine wave at the Resistive Load (RL) and match the drain on resistance of Q1 and Q2 to the 50Ω load. This match should reflect a real resistance of ≈X10 Rds(on) to the two drains of Q1 and Q2. A drain load lower than X10 or higher than X10 will lower the overall efficiency.

In the Half Bridge topology of Figure 1, the most critical aspect is the control and stability of the high side switch, Q1. Recall that at Node A, there will be a high voltage square wave which will have fast leading edges. These abrupt transitions can induce enough image current through the stray capacitance of the T1 windings to cause Q1 to conduct too soon or too late. This can cause cross conduction of Q1 and Q2. The parasitic coupling can also result in loss of control completely, resulting in the inevitable destruction of Q1 and Q2.

To reduce this effect we must reduce the stray capacitance in the high Side Transformer T1 to the minimum and also install a Common Mode Choke on the primary side of the transformer. See Figure 2.

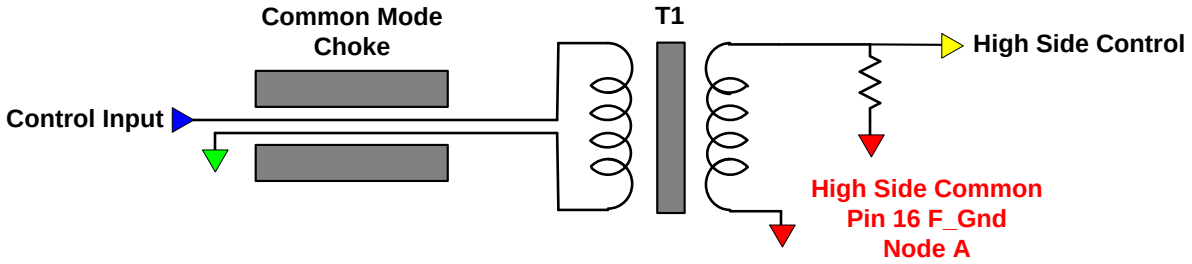



**Figure 2.** Half Bridge High Side Drive

Figure 2 is a schematic representation of T1 and illustrates two critical details for the High Side Transformer (T1 of the Half Bridge, Figure 1). Node A, Pin 16 and the High Side Common are all a reference or equipotential plane. This plane is at a high voltage RF potential with respect to power or signal ground. Low winding to winding capacitance is critical. The addition of the Common Mode Choke (CMC) further reduces the effect of the capacitive coupling winding to winding of T1. All measurements made on the High Side Common must be differential measurements.

## CIRCUIT DESCRIPTION

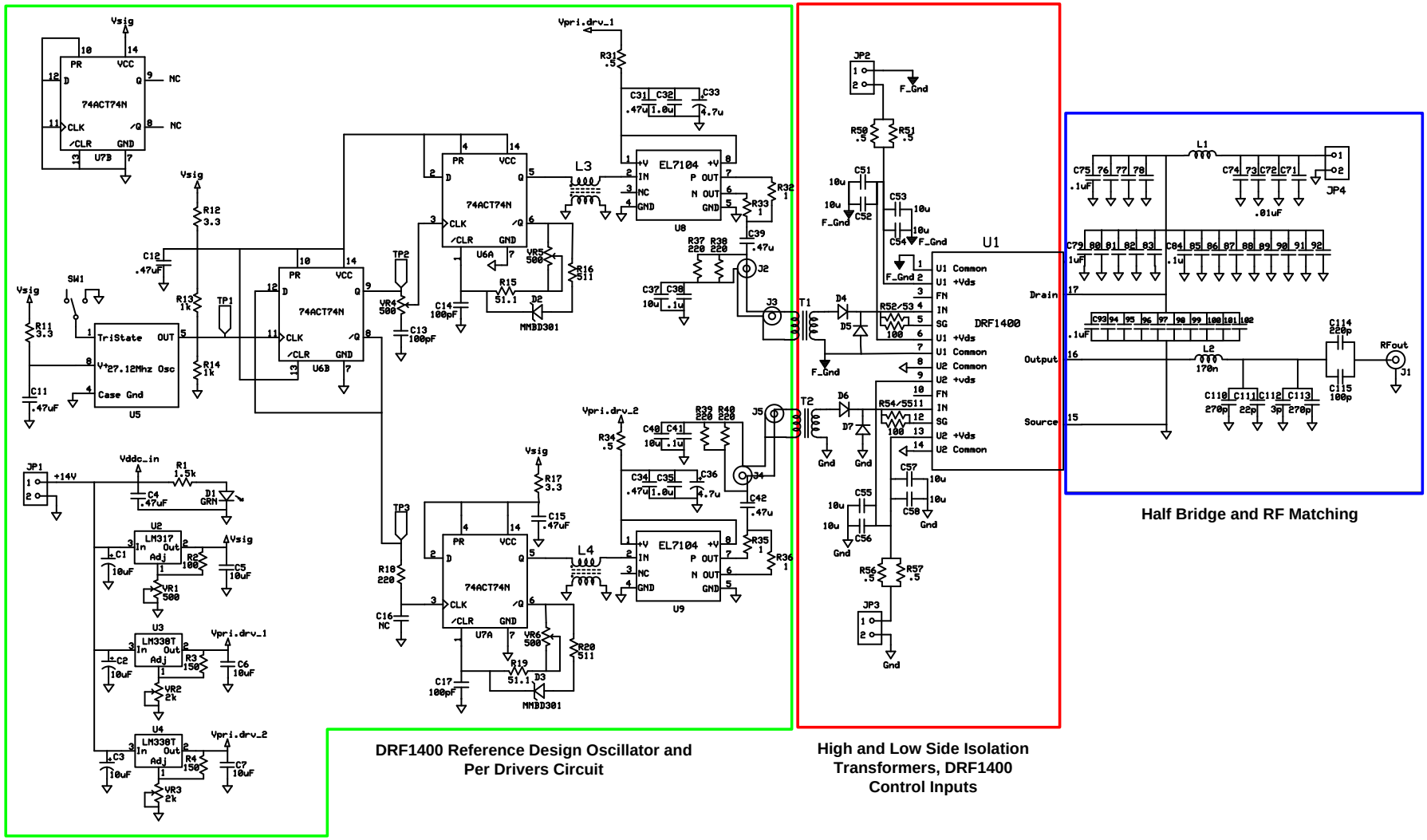



**Figure 3.** Reference Design Circuit Diagram

Figure 3 illustrates the Reference Design Circuit Diagram. In the illustration there are three sections: the Oscillator and Pre Drivers in the green block, the High and Low Side Isolation and Control inputs in the red block, and finally the RF Matching in the blue block. In the following text we will discuss each of the three sections in detail.

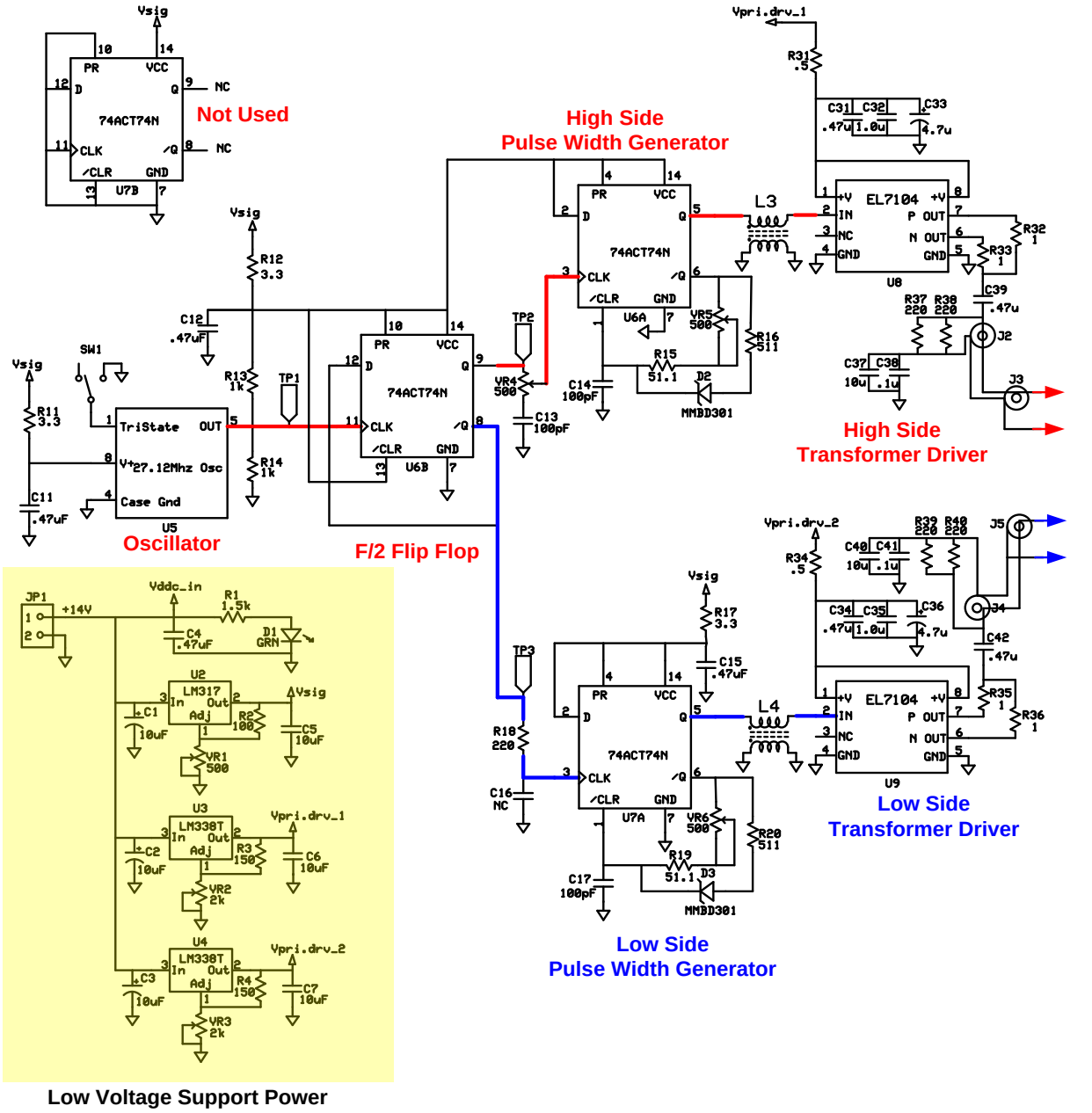



**Figure 4.** DRF1400 Reference Design, Oscillator – Pre-Drivers Circuit

Figure 4 illustrates the logic level and Pre-Drivers of the DRF1400 Reference Design (the green section of the full schematic of Figure 3). U5 is a Temperature Compensated Crystal Oscillator, TCXO. This IC generates a 27.12 MHz, 50% Duty Cycle signal that is applied to U6B pin 11. The Flip-Flop U6B is configured as a divide-by-two circuit. This provides a 13.56 MHz square wave at Pin 9 and Pin 8. These two signals are exactly 180° out of phase. The precision of this relationship is critical for the proper operation of the Half-Bridge topology. U6B pin 9 applies one phase to the High Side Pulse Width Generator and a similar path for Low Side Pulse Width Generator. U6B pin 9 is an RC network, VR4 and C13. This network is used to ensure that the High Side and Low Side drives are 180° out of phase. Given that these two circuit paths perform exactly the same, we will only follow the circuit path for the High Side Pre-Driver. U6A of the High Side Pulse Width Generator is a Flip-Flop circuit configured to produce a pulse with time duration less than the ½ cycle time of the 13.56 MHz clock signal. For the DRF1400 Half Bridge at 13.56 MHz, this is a pulse width of ≈20 ns. This pulse is then applied to U8, the High Side Transformer Driver (red path), and U9, the Low Side Transformer Driver (blue path).

**Pulse Generation**

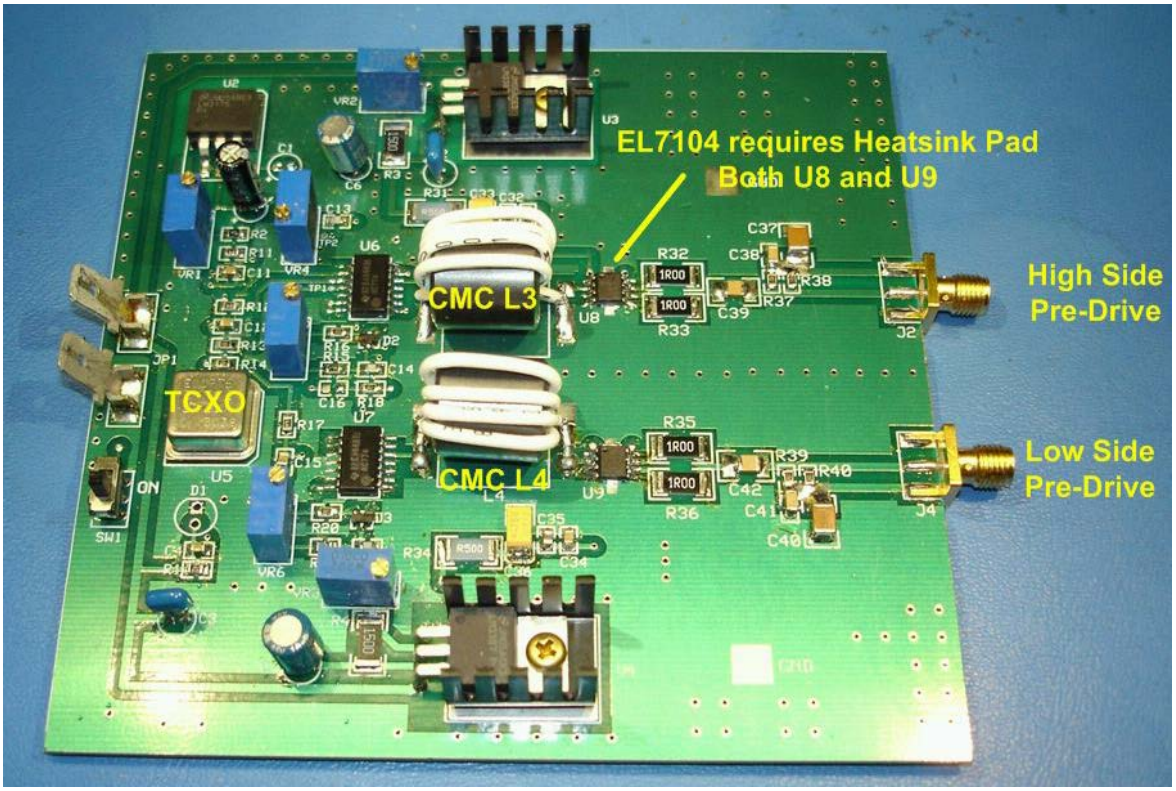



**Figure 5.** Pulse and Pre-driver circuit

Referring to Figure 4, the pulse generation circuit consists of a 27.12 MHz signal from the TCXO, U5. This is divided down to 13.56 MHz and split into two 180° out of phase signals and applied to one-shot circuit of IC, U6A and U7A. By using VR4, the phase can be adjusted to a 180° out of phase setting. The pulse widths are set to 20 ns using potentiometer, VR5 and VR6 respectively. Common Mode Choke (CMC), L3 and L4 are necessary to eliminate EMI and RFI. These two CMCs are made of 43 core material and 50Ω coaxial cable. The two signals are then applied to the Isolation Transformer T1 and T2 from the EL7104s, U8 and U9 transformer drivers. The circuit voltage is 4V~4.5VDC supplied from DC regulation circuit using a regulator, U2. It is highly recommended using EMI shielding box covering the entire PCB, low level control circuits to avoid any interference from the output section.

**Pre-Driver**

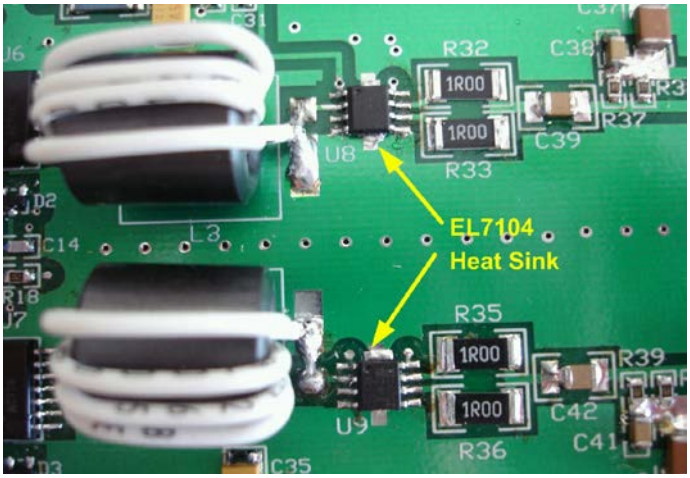



**Figure 6.** Pre-Driver

Two pulse signals are then applied to Power MOSFET Drivers (U8 and U9). The EL7104s are used as transformer drivers, and provide compensation for losses in the Isolation Transformer. This provides improved rise and fall time of the control pulses. The P and N outputs of the pre-driver are combined via R33 and R32 at C39, and via R35 and R36 at C42. U8 and U9 require heat sinking, see Figure 6. The operating voltage for U8 and U9 is set at 10V~11DC. This voltage is supplied from adjustable regulator, U3 and U4. The waveform captured at the output of the pre-driver is shown in Figure 7. There are two RF snubbers on the outputs of U8 and U9: resistors R37, R38 and capacitors C37, C38 for high side; and R39, R40 and C40, C41 for low side, respectively. Both of the EL7104s, U8 and U9 require improved heat sinking. This is accomplished with a small rectangular heat spreader of indium (see Figure 6) placed under the IC body.

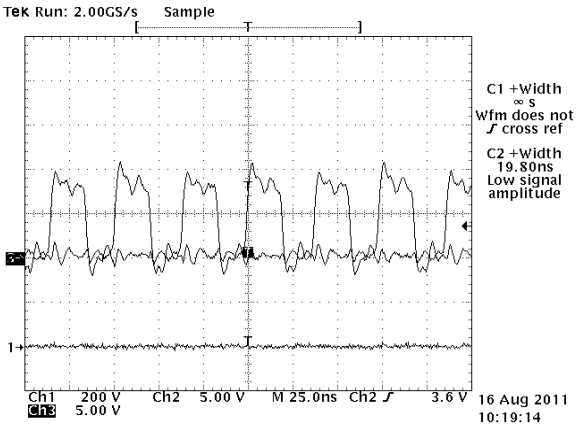



**Figure 7.** Waveform at the Pre-driver

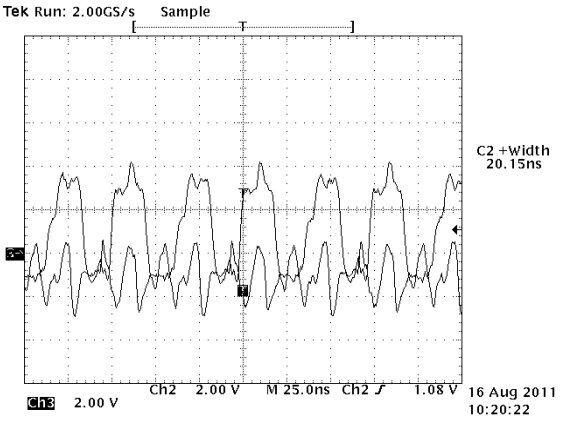



**Figure 8.** Waveform at Input Transformer

Figure 8 illustrates the Pre-driver output at the J3 and J5 launch point. The signals travel thru ≈ 12 inches of 50Ω coaxial cable wound on a ferrite core and then applied to the primary of T1 and T2 in Figures 5 and 6. Figures 7 and 8 illustrate the waveform distortion due to the transformer and the DRF1400 input characteristics.

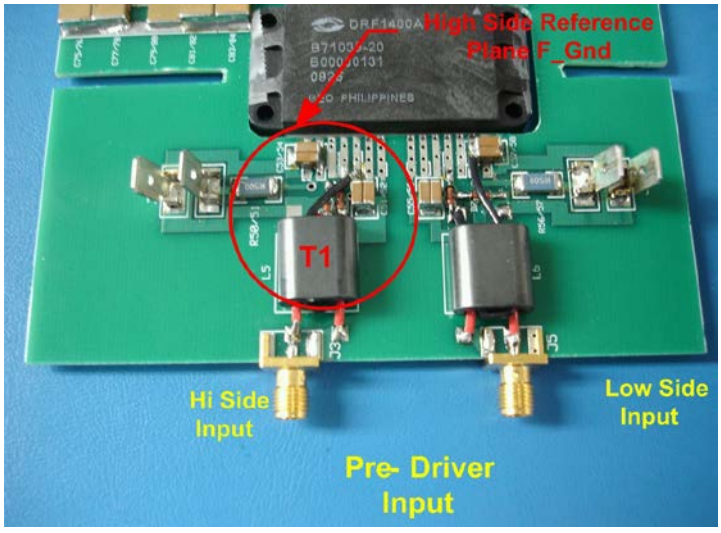



**Figure 9.** Input Transformer

The input transformers are illustrated in Figure 9. This is a very critical and electrically sensitive component. The input transformers are constructed with very short wires using ferrite core material 61 or 43. The wire is 22 AWG or smaller and the size of the ferrite core is approximately 0.52 inch by 0.52 inch multi-aperture cores shape. The Turn Ratio of the primary and secondary is 1:1 for less coupling loss. It is essential that the construction of the transformers minimizes the Stray Capacitance and the leakage inductance. The peak positive voltage at the output is about 4V and the pulse width is ≈ 20 ns. This is a very critical component; therefore special care must be taken in the design and construction to ensure low leakage inductance and low stray capacitance.

Illustrated in Figure 9 above are the two Isolation transformers, the High Side and the Low Side. The High Side is circled in red. Recall from the preceding text that the **High Side Reference Plane (F_Gnd) is not at Ground DC or AC**.

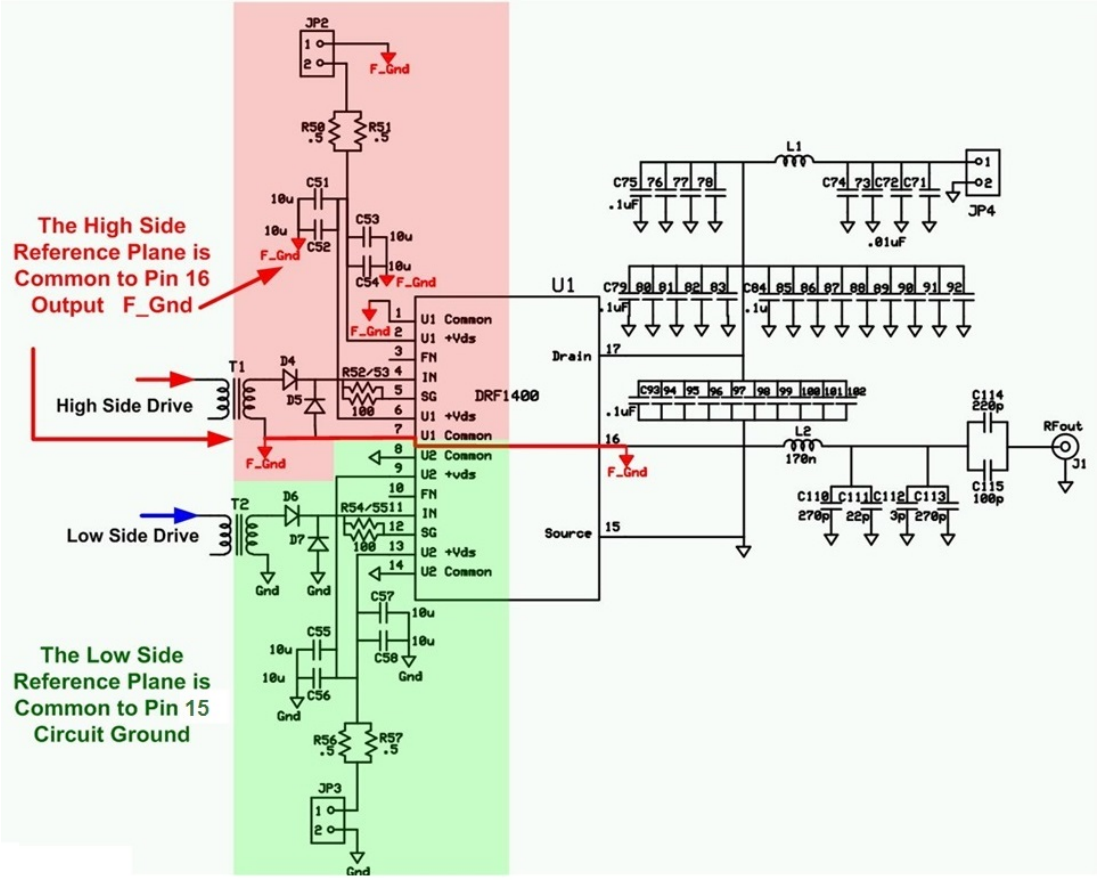



**Figure 10.** High and Low Side Isolation Transformers, DRF1400 Control Inputs

The following discussion is directed at the red shaded section of Figure 10. In this section the single most important and most critical circuit detail is that F_Gnd is not a common ground, it is floating at the output of the Half Bridge Pin 7 and 16 of the DRF1400. Also note that DRF1400 pins 1, 2, 3, 4, 5 and 6 are all referenced to pin 7 and 16. In addition, all circuit components in the red shaded area are also at this potential and must be isolated from the circuit ground.

The input Pre-Driver for the High Side and the Low Side are illustrated in Figure 10, left center. T1 and T2 couple the Pre-Driver signals for the High Side and the Low Side to the input of the DRF1400 while isolating the F_Gnd from the system ground. With a high drive voltage signal at T1, the High Side switch pins 16 and 17 are in a saturated switch condition. At the same time, the Low Side drive is at a 0V state and the Low Side switch is in an off condition, pins 16 and 15. This alternating pattern of drive signals generates a square wave high power signal at pin 16.

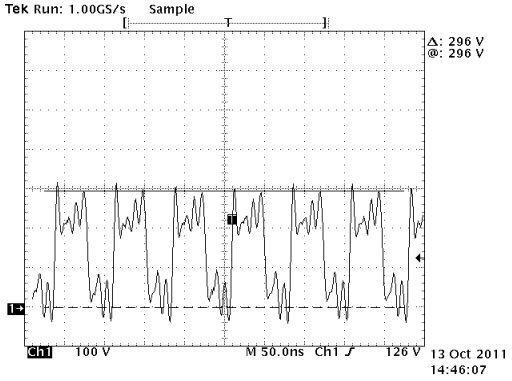



**Figure 11.** Waveform when HV = 250V

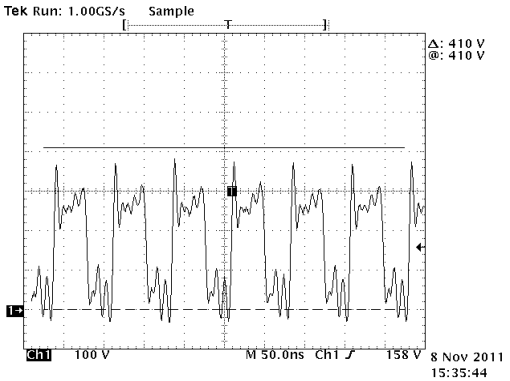
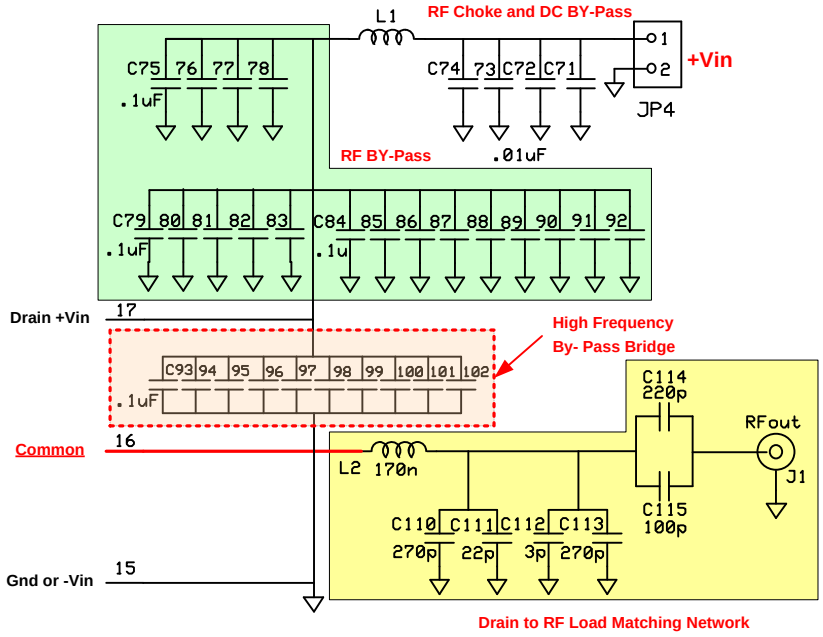



**Figure 12.** Waveform when HV PS = 300V

Figure 11 and Figure 12 illustrate the pin 16 to 15 square wave input to the matching circuit.

## RF Output Matching

Figure 13 illustrates the RF Output and Matching circuit of the DRF1400 Reference Design. This circuit has two requirements with respect to the circuit operation. The first of these is to reflect the optimum drain impedance of 3Ω into the MOSFET drains and provide a match to the 50Ω load. The circuit must also be resonant at 13.56 MHz. This circuit is illustrated in the yellow block of Figure 13.




The Matching circuit consists of a series inductor, L2 and shunt/series capacitors, C110 thru C115. There is a bridge PCB assembly, Figure 15 with 9-10 capacitors (0.1uF/630V) in parallel C93 to C102, located between the Drain, Pin17 and Source, pin 15 of DRF1400. This bridge provides a very low inductance high capacitance bypass component. The bridge minimizes overshoots on the Drain waveform. It is mounted vertically on the pads of Drain and Source of the PCB. All RF circuit components must support voltages over 500V and power levels of several KWs.

**Figure 13.** RF Bypassing and RF Matching

The Bridge is a critical circuit element for overall system performance and in minimizing the peak ring voltage at the common pin 16. The physical nature of this component is also critical and illustrated in Figure 15. The green block of Figure 13 illustrates the more conventional RF by-passing network, RF Choke and DC bypass components.

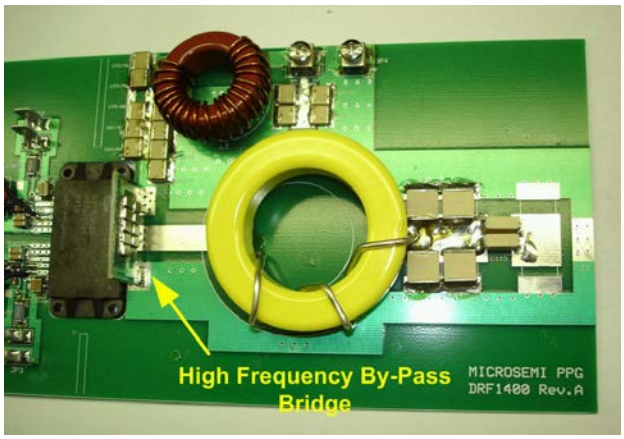



**Figure 14.** Output Matching Circuit

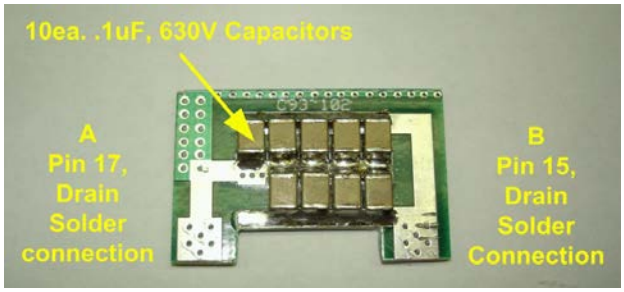



**Figure 15.** High Frequency Bypass Bridge

Figure 14 illustrates the location of the bypass bridge. This specific location is necessary. Without this bypass, the high frequency components in the Drain (pin 16 common) waveform would limit performance and affect the circuit stability.

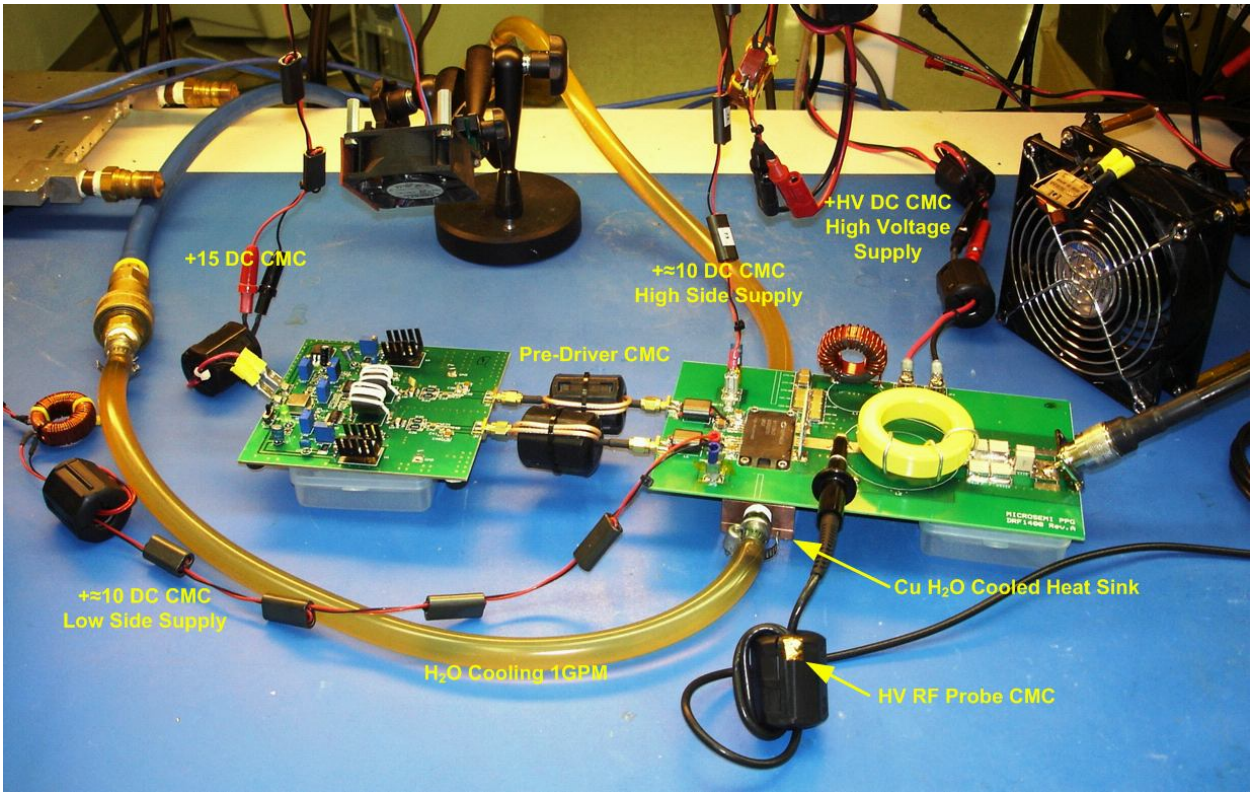



**Figure 16.** Test Setup for the DRF1400 Reference Design

Figure 16 illustrates the DRF1400 Reference Design bench set up. The +15V DC support power input is shown in the upper left, note the CMC. The +≈10V DC Low Side supply is on the lower left, also note the CMC. Above and to the right of center is the +≈10V DC High Side supply. All three of these supplies are wired with a Common Mode Choke, CMC. These CMC are absolutely essential for stable Half Bridge operation. To the left of center we see the Pre-Driver CMCs these are not only necessary but very critical for this topology. Also illustrated in Figure 16, in the upper right, is the CMC for the +HV DC supply. Here you also see CMC on this power feed. In the lower right we see the HV RF Probe. There are two important points to note with respect to the probe attachment. The first is the electrical attachment of the probe tip and the ground. The probe tip is threaded into a brass nut which has been soldered to the Pin 16, A node, F_Gnd and the ground connection is soldered to power ground. Also note that a CMC is installed on the probe cable. Failure to connect the HV RF probe in this manner will result in excessive high frequency noise on the signal and will corrupt the accuracy of a measurement.

**DC Supply**

There are power supply circuits for high side and low side driver. These supplies are electrically isolated. The high side ground is "Floating", F_GND in the schematic, while the Low side is a common ground. The Gate drivers voltage is set at 10V~10.5V, JP2 and JP3 respectively. It is very critical that all DC connections use a CMC set made from Fair-Rite's multi-apertures (30 or 73 material) for elimination of conductive noise at the operating frequency. The HV supply circuit consists of RF Choke, L1, 22 bypass capacitors, C71 through C92. The RFC is made from a T130-2 with 21 turns of 16 AWG, which has about 1K ohm inductive reactance. All capacitors must support over 1kV such as AVX 2225 X7R, min. 10% tolerance. It is critical that a Common Mode Choke (30 or 73 material) along with HV wire are on the high voltage supply lines in order to eliminate all conductive noise elements.

Primary cooling for the DRF1400 is provided via a water cooled heat sink, center. The water flow rate is ≈1GPM at full power the heat sink temperature is ≈ 35°C. Additional air cooling is provided, for PCB components by the AC fan upper right.

## PERFORMANCE (DATA SUMMARY)

### Test Set-Up

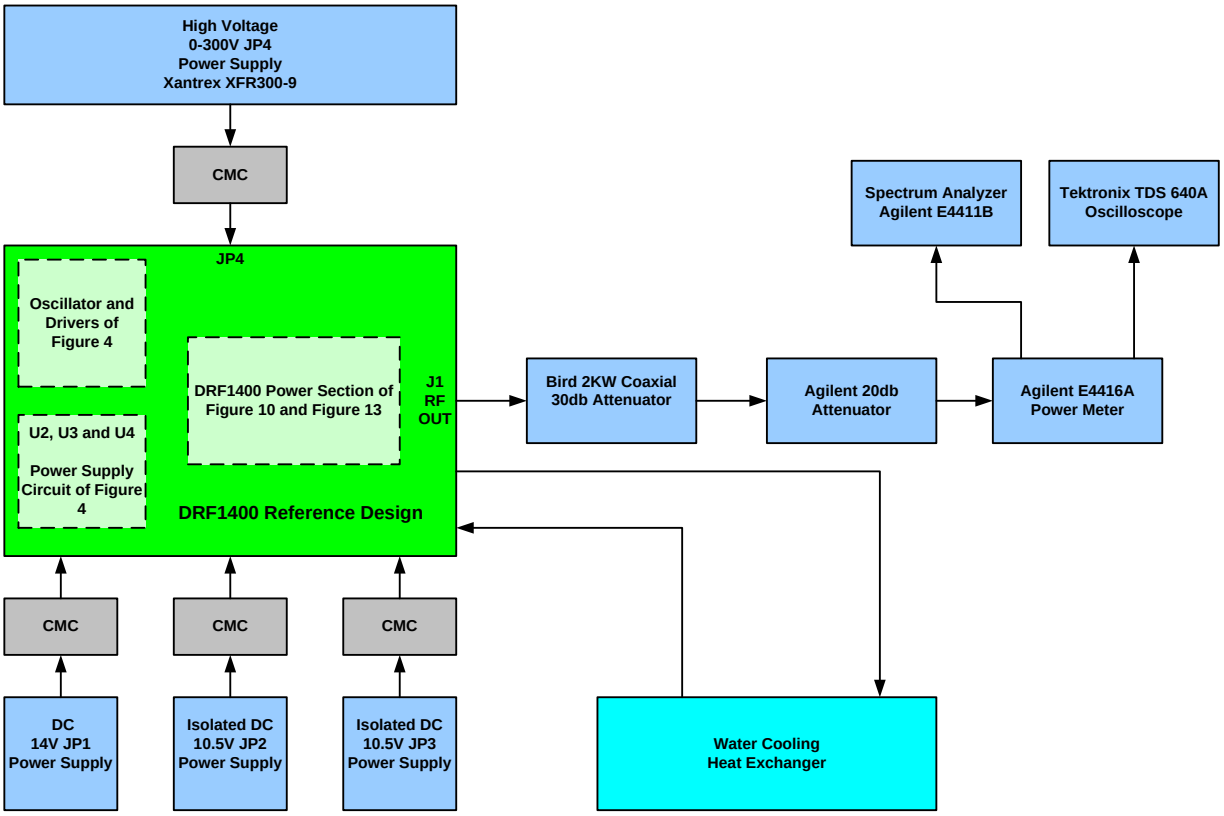



**Figure 17.** Test Set-Up Diagram

### Test Requirement

Figure 17 illustrates the DRF1400 Test Setup. All the data presented in this application note was collected using the equipment configuration illustrated. The support power supplies settings for JP1, JP2 (Isolated) and JP3 (Isolated) are noted. The High Voltage Supply, JP4 is varied from 0V to 300V in the course of data taking. Note that all Power Supplies have a CMC on the output leads. The Heat Exchanger is set at < 25°C. All adjustments on the DRF1400 have been made and checked prior to applying HV power.

Turn on power supplies and set HV of 40V for warming up for at least 30 minutes. While monitoring the RF power and waveform at output port of U1, Pin 16, ramp up HV in steps, checking all functions are in normal before increasing the HV supply. If the RF power and/or Drain waveform becomes unstable, shut-down of all power supplies and verify fault before resuming test.

**Test Results**

| Vds, V | Ids, A | Pin, W | Pout, W | Eff., % |
|---|---|---|---|---|
| 200 | 4.53 | 906 | 830 | 92 |
| 210 | 4.35 | 914 | 840 | 92 |
| 220 | 4.54 | 999 | 920 | 92 |
| 230 | 4.77 | 1097 | 1005 | 92 |
| 240 | 4.98 | 1195 | 1103 | 92 |
| 250 | 5.28 | 1320 | 1210 | 92 |
| 260 | 5.53 | 1438 | 1309 | 91 |
| 270 | 5.79 | 1563 | 1411 | 90 |
| 280 | 6.02 | 1686 | 1500 | 89 |
| 290 | 6.28 | 1821 | 1607 | 88 |
| 300 | 6.45 | 1935 | 1695 | 88 |

**Table 2.** Typical Performance Data

Table 2 shows the typical performance at increasing power levels. This step-by-step process should be observed from low power levels to the 1.7KW maximum. The table lists the input DC voltage supply (PS_HV), MOSFET drain current (Id), power in and power out with efficiency, and the voltage observed at MOSFET Output (Vds). Variation of efficiency vs. Pout is shown in Figure 18 and Drain HV vs. Pout is shown in Figure 19 on the following page. Efficiency is calculated using RF power output and DC input power of the power MOSFET. The efficiency in the table is at 13.56 MHz.

**Data Charts**

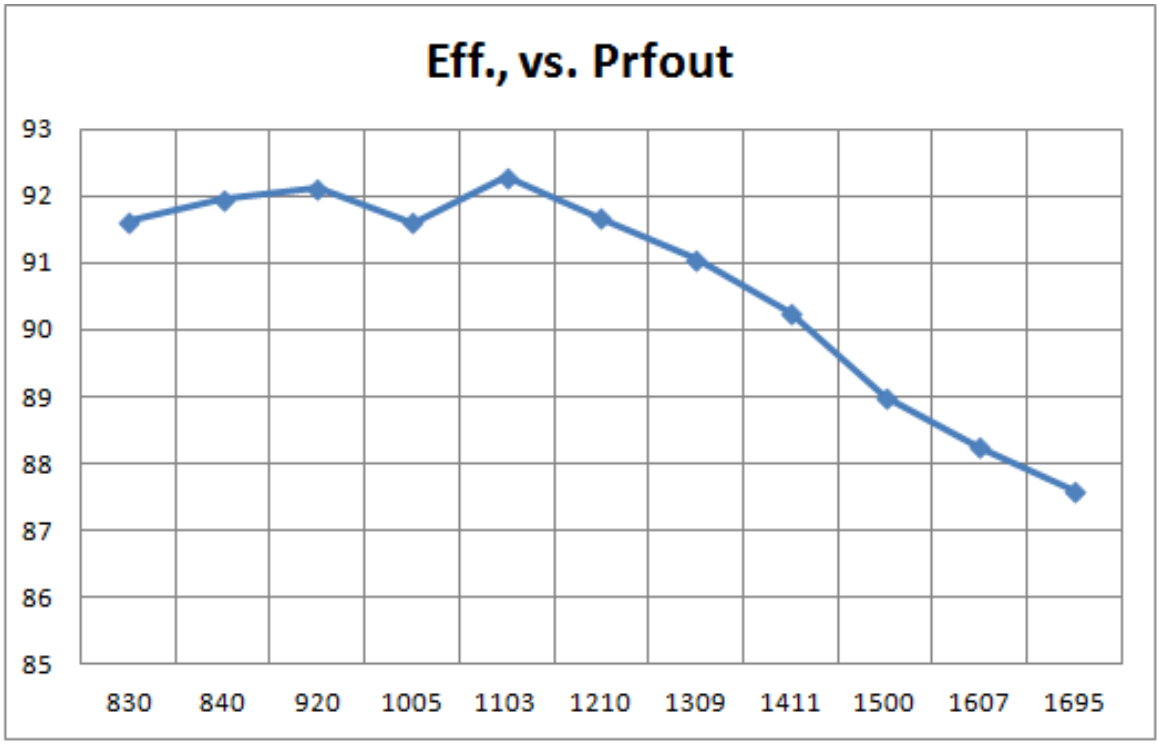



**Figure 18.** Efficiency vs. RF Pout

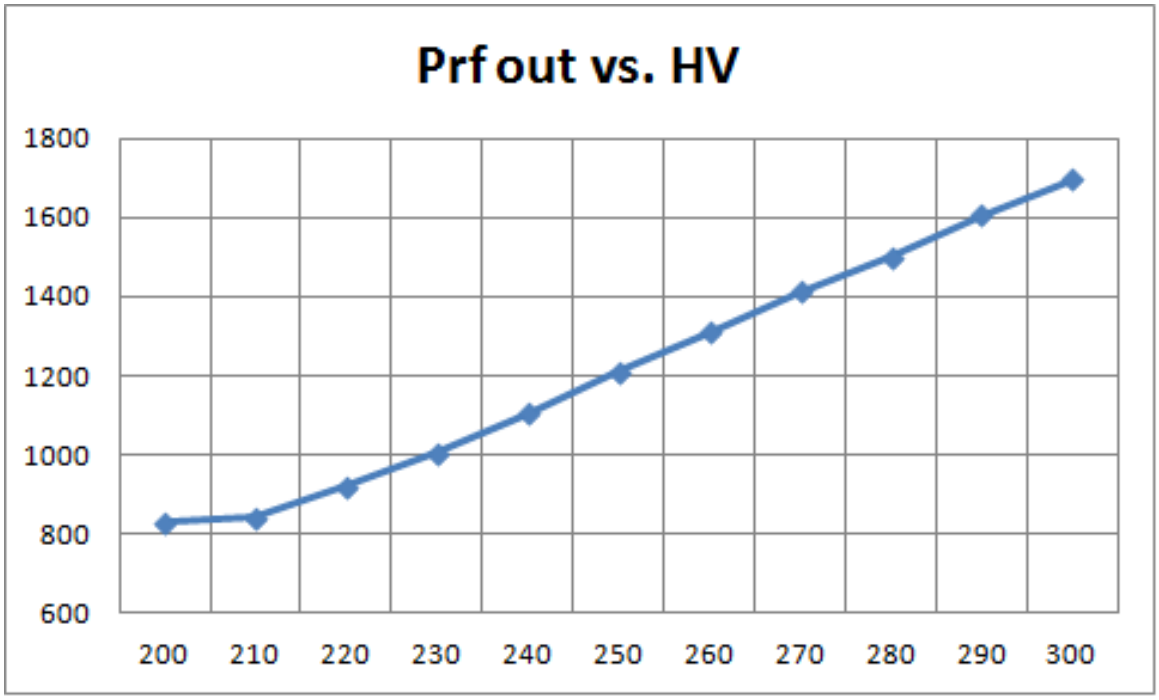


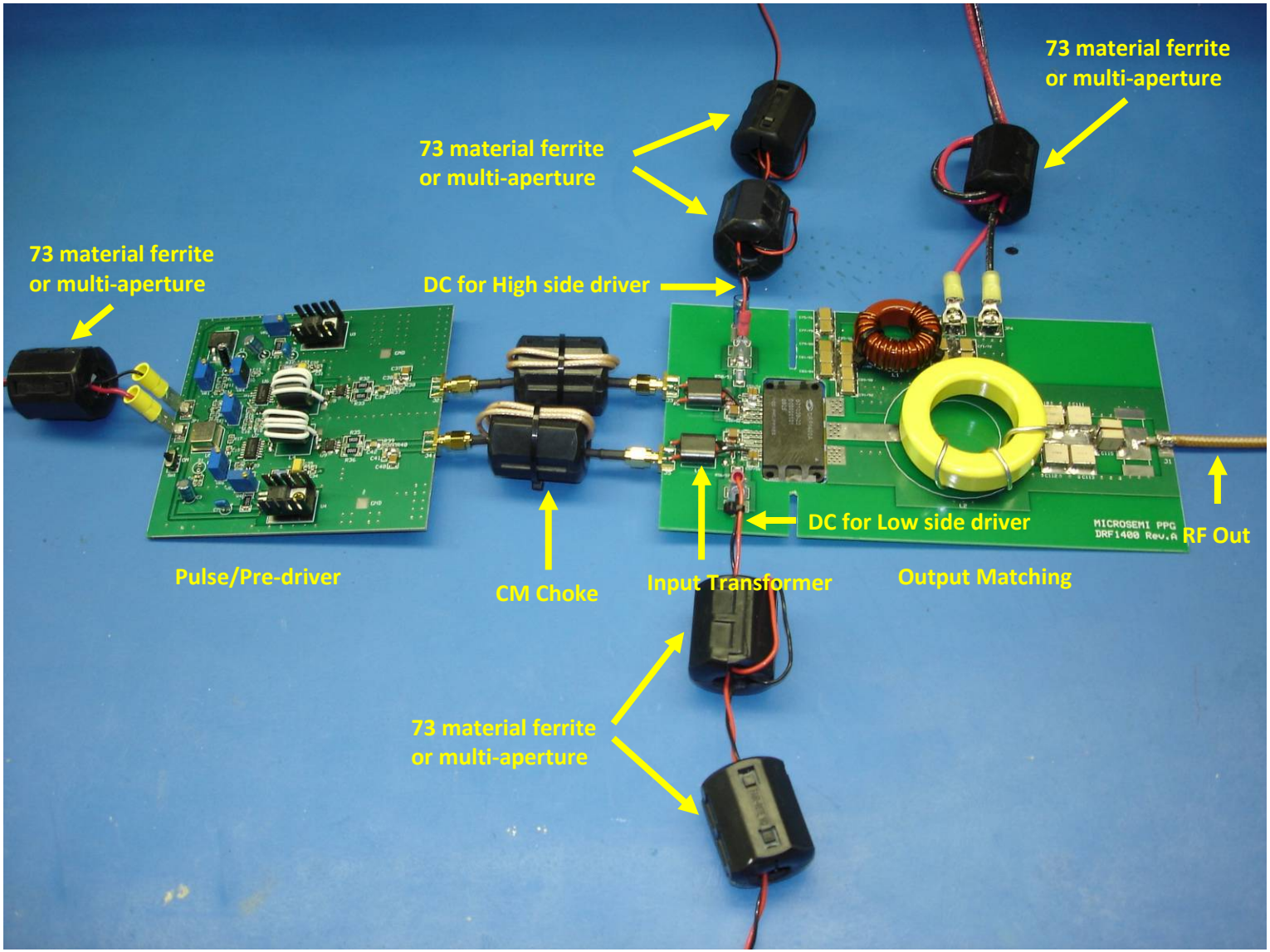

**Figure 19.** Drain HV vs. RF Pout

Measurements were taken up to 1.7KW, HV from 140V to 260V. The Drain efficiency (η) of the test board is typically 87 % at 1.7kW. More RF power can be achieved by further tuning and optimization of the output circuit.

## CONCLUSION

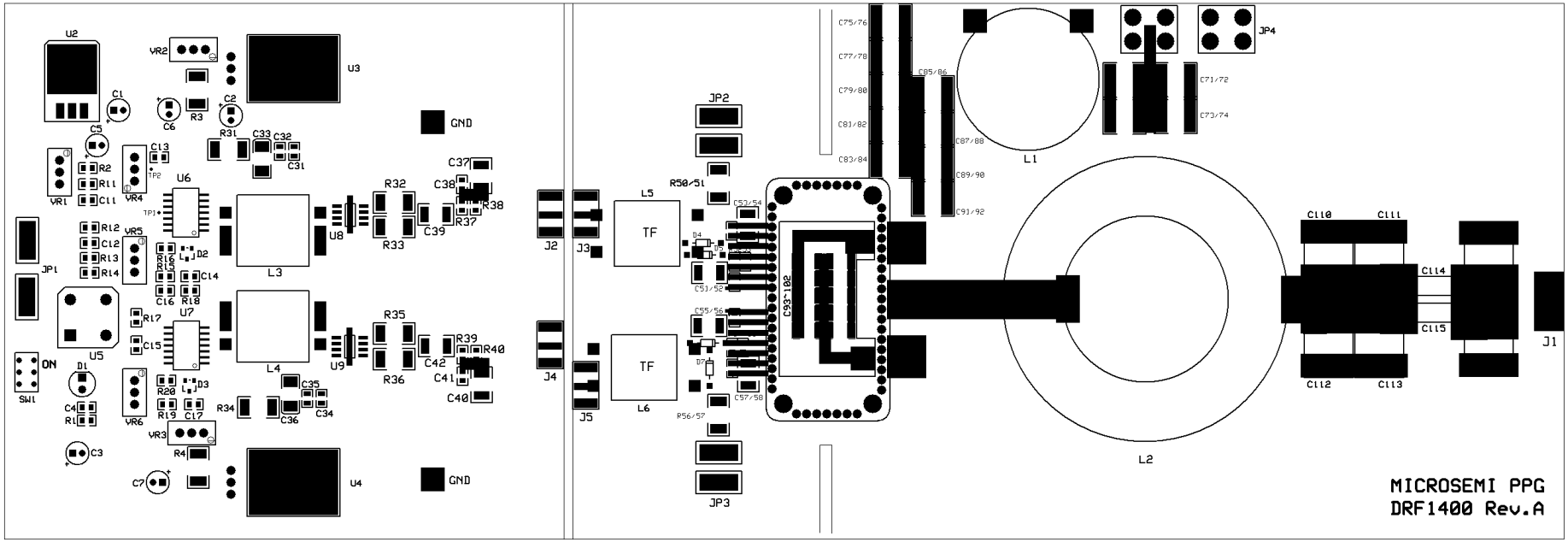
In this Application Note, technical information for design of a 1.7KW, Class- D Half Bridge, RF generator operating in 13.56 MHz is provided. Also included are critical aspects of circuit design. Some of these key aspects are isolation between High Side and Low Side drivers, suppression of conductive noise, and the bypassing capacitors on the Drain HV. The input transformer is a very critical component for Half Bridge operation. A Microsemi DRF1400 Hybrid was used to overcome layout parasitic that simplified the design and providing a single low cost, high efficiency RF generator. Transformer design can be further optimized to eliminate the peaking as shown in the Vds waveforms. The reference design minimizes design time by allowing an engineer to evaluate the performance into a 50Ω load.

# Appendix I. Whole PCB Assembly

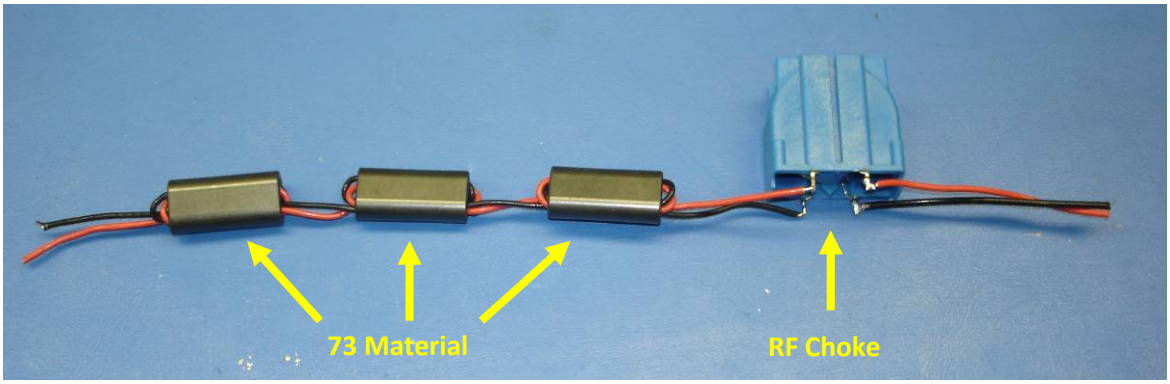


# Appendix II. PCB Lay-out

**PCB size: 4.5W * 13.1L in inch**
**PCB: FR-4, 65mil T**



# Appendix III. DC bias for High side and low side driver




Ferrite material: 73 Multi-Aperture, Fair-rite #: 2873006802 or equivalent


**Do not connect GND to "Negative" terminals for High and Low side driver to make an isolated PS.**

# Appendix IV. Parts List

| Part ID | Description | Size | Manufacturer | Manuf. PN |
|---|---|---|---|---|
| **U1** | **DRF1400** | **T4B** | **Microsemi** | **DRF1400** |
| C1-3, 5-7 | 10uF/16V(Elec cap) | 5*11 | Xicon | 140-XRL16V10-RC |
| C37,40,51-58 | 10uF/50V(Cer. Cap) | 1812 | TDK | C4532Y5V1H106Z |
| C38,41 | 0.1uF/25V(Cer. Cap) | 0805 | AVX | 0805C104KAT2A |
| C4,11,12,15,31,34 | 0.47uF/50V(Cer. Cap) | 0805 | AVX | 08055C474K4T2A |
| C39,42 | 0.47uF/50V(Cer. Cap) | 1210 | AVX | 12105C474KAT2A |
| C13,14,17 | 100pF/50V(Cer. Cap) | 0805 | Murata | GRM2165C1H101JA01D |
| C33,36 | 4.7uF/35V(Tant cap) | 6032-28 | AVX | TAJC475K035R |
| C32,35 | 1.0uF/50V(Cer. Cap) | 0805 | Taiyo Yuden | GMK212BJ105KG-T |
| C71-92 | 0.01uF/2KV | 2225 | AVX | 2225GC103KAT1A |
| C93-102 | 0.1uF/630V | 1812 | AVX | 1812CC104KAZ1A |
| C110 | 270pF | 3838 | ATC | 100E271KT |
| C111 | 22pF | 3838 | ATC | 100E220KT |
| C112 | 3p~82pF | 3838 | ATC | Tuning with 100E series |
| C113 | 270pF | 3838 | ATC | 100E271KT |
| C114 | 220pF | 3838 | ATC | 100E221KT |
| C115 | 82p~150pF | 3838 | ATC | Tuning with 100E series |
| R1 | 1.5k ohm | 0805 | ROHM | MCR10EZHF1501 |
| R2 | 100 ohm | 0805 | VISHAY | CRCW0805100RJNEA |
| R3-4 | 150 ohm | 2512 | VISHAY | CRCW2512150RJNEG |
| R11,12,17 | 3.3ohm | 0805 | SUSUMU | RL1220S-3R3-F |
| R13,14 | 1.0K ohm | 0805 | ROHM | MCR10EZHF1001 |
| R15,19 | 51.1ohm | 0805 | PANASONIC | ERJ-6ENF51R1V |
| R16,20 | 511 ohm | 0805 | ROHM | MCR10EZHF5110 |
| R3131,34,50,51,56,57 | 0.5 ohm | 2512 | PANASONIC | ERJ1TRQFR51U |
| R32,33,35,36 | 1 ohm | 2512 | VISHAY | CRCW25121R00FNEG |
| R18,37-40 | 220 ohm | 0805 | ROHM | MCR10EZHF2200 |
| R52-55 | 100 ohm | 0805 | VISHAY | CRCW0805100RJNEA |
| VR1,4-6 | POT 500ohm 1W | 3/8" sq | Vishay | T93YA501KT20 |
| VR2,3 | POT 2k ohm 1W | 3/8" sq | Vishay | T93YA202KT20 |
| D1 | LED, green | 5mm | Panasonic | LN31GPH |
| D2 | 30V/200mW(Diode Schot) | SOT23 | On Semi. | MMBD301LT1G |
| D3 | 30V/200mW(Diode Schot) | SOT23 | On Semi. | MMBD301LT1G |
| D4-7 | Zener Diode 6.8V | | FAIRCHILD | 1N5235B |
| L1 | RFChoke with 14AWG | | MICROMETALS<br>BELDEN | T130-2<br>8073(20TURNS) |
| L2 | Toroidal Inductor<br>with 12AWG | | MICROMETALS<br>Alpha | T225-6<br>289(3TURNS) |
| L3,4 | CM Choke | | FAIR-RITE<br>BELDEN | 2643375102<br>83265(4TURNS) |
| T1,2 | Transformer(TR 1:1) | | FAIR-RITE<br>ALPHA | 2843(61)000202<br>20 AWG |
| U2 | LM317 | 14SOP | | LM317 |
| U3,4 | LM338T | TO-220 | NATIONAL | LM338T/NOPB |
| U5 | 27.12M TCXO | | Ecliptek Co. | EP1100HSTSC-27.120M |
| U6,7 | Dual Flip-Flop | 14SOP | TI | SN74ACT74NSR |
| U8,9 | EL7104 | 8LDSOIC | INTERSIL | EL7104CSZ |
| SW1 | Slide Switch SPDT | | E-SWITCH | EG1271A |
| J1 | RFout port | Edge | Bomar | 161V504E |
| J2-4 | SMA, PCB mount | | Johnson/Emerson | 142-0701-801 |
| JP1-3 | DC Terminal | | Keystone | 4902 |
| JP4 | DC Terminal | | Keystone | 8191 |

# Appendix V. Test Equipment required

For testing the reference design kit, this equipment is required:

| Equipment | Spec | Quantity | Remark |
|---|---|---|---|
| HV PS | 0~400V, 15A | 1 | Sorensen DLM600-6E |
| Driver PS | 0~15V, 4A | 2 | |
| Pulse PS | 0~15V, 2A | 1 | |
| DC wires | | | |
| -. HV | AWG12 | 1 pair | "Y" terminal + wire w/ CMC |
| -. Driver | AWG20 | 2 pairs | "Snap" terminal + wire w/ 73 |
| -. pulse gen. | AWG20 | 1 pairs | "Snap" terminal + wire w/ 73 |
| | | | |
| Spec. analyzer | E4411 or Equivalent | | |
| | | | |
| RF Power meter | Agilent E4416A | 1 | |
| RF sensor | | 1 | |
| | | | |
| RF Power att. | 2kW, 30dB | 1 | Bird 8329-300 or Equivalent |
| RF mid. att. | 10W, 20dB | 2 | Agilent 8491A or Equivalent |
| or dummy load | 2kW | 1 | |
| RF Coax. cable | LMR400 | several | with n_male connector |
| | | | |
| Oscilloscope | | 1 | LeCroy 354A or Equivalent |
| HV probe | 2kV | 1 | |
| STD probe | 300V | 2 | |
| | | | |
| Heat sink | | 1 | 10", L * 8", W * 0.5", T min. |
| Chiller | | 1 | 5C ~ 25C |
| Cooling fan | | 2 | 150 CFM |

References


- Solid State Radio Engineering – Herbert L. Krauss and Charles W. Bostian
- Application Note: Simple and Inexpensive High Efficiency Power Amp using New APT MOSFET – Kenneth Dierberger 1994
- Application Note: Microsemi DRF1300 Class-D Push-Pull
- Application Note: Microsemi DRF Design Guide

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