Features

- Ultra High Performance
  - System Speeds to 100 MHz
  - Array Multipliers > 50 MHz
  - 10 ns Flexible SRAM
  - Internal Tri-state Capability in Each Cell
- FreeRAM™
  - Flexible, Single/Dual Port, Synchronous/Asynchronous 10 ns SRAM
  - 2,048 - 18,432 Bits of Distributed SRAM Independent of Logic Cells
- 128 - 384 PCI Compliant I/Os
  - 3V/5V Capability
  - Programmable Output Drive
  - Fast, Flexible Array Access Facilitates Pin Locking
  - Pin-compatible with XC4000, XC5200 FPGAs
- 8 Global Clocks
  - Fast, Low Skew Clock Distribution
  - Programmable Rising/Falling Edge Transitions
  - Distributed Clock Shutdown Capability for Low Power Management
  - Global Reset/Asynchronous Reset Options
  - 4 Additional Dedicated PCI Clocks
- Cache Logic® Dynamic Full/Partial Re-configurability In-System
  - Unlimited Re-programmability via Serial or Parallel Modes
  - Enables Adaptive Designs
  - Enables Fast Vector Multiplier Updates
  - QuickChange™ Tools for Fast, Easy Design Changes
- Pin-compatible Package Options
  - Plastic Leaded Chip Carriers (PLCC)
  - Thin, Plastic Quad Flat Packs (LQFP, TQFP, PQFP)
  - Ball Grid Arrays (BGAs)
- Industry-standard Design Tools
  - Seamless Integration (Libraries, Interface, Full Back-annotation) with Concept®, Everest, Exemplar™, Mentor®, OrCAD®, Synario™, Synopsys®, Verilog®, Veribest®, Viewlogic®, Synplicity®
  - Timing Driven Placement & Routing
  - Automatic/Interactive Multi-chip Partitioning
  - Fast, Efficient Synthesis
  - Over 75 Automatic Component Generators Create 1000s of Reusable, Fully Deterministic Logic and RAM Functions
- Intellectual Property Cores
  - Fir Filters, UARTs, PCI, FFT and Other System Level Functions
- Easy Migration to Atmel Gate Arrays for High Volume Production
- Supply Voltage 5V for AT40K, and 3.3V for AT40KLV

5K - 50K Gates Coprocessor FPGA with FreeRAM™

AT40K05
AT40K05LV
AT40K10
AT40K10LV
AT40K20
AT40K20LV
AT40K40
AT40K40LV

Summary

Rev. 0896CS–FPGA–05/02

Note: This is a summary document. A complete document is available on our web site at *www.atmel.com*.

Table 1. AT40K/AT40KLV Family[1]

Device	AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV
Usable Gates	5K - 10K	10K - 20K	20K - 30K	40K - 50K
Rows x Columns	16 x 16	24 x 24	32 x 32	48 x 48
Cells	256	576	1,024	2,304
Registers	256[1]	576[1]	1,024[1]	2,304[1]
RAM Bits	2,048	4,608	8,192	18,432
I/O (Maximum)	128	192	256	384

Note: 1. Packages with FCK will have 8 less registers.

Description

The AT40K/AT40KLV is a family of fully PCI-compliant, SRAM-based FPGAs with distributed 10 ns programmable synchronous/asynchronous, dual-port/single-port SRAM, 8 global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data), automatic component generators, and range in size from 5,000 to 50,000 usable gates. I/O counts range from 128 to 384 in industry standard packages ranging from 84-pin PLCC to 352-ball Square BGA, and support 5V designs for AT40K and 3.3V designs for AT40KLV.

The AT40K/AT40KLV is designed to quickly implement high-performance, large gate count designs through the use of synthesis and schematic-based tools used on a PC or Sun platform. Atmel's design tools provide seamless integration with industry standard tools such as Synplicity, ModelSim, Exemplar and Viewlogic.

The AT40K/AT40KLV can be used as a coprocessor for high-speed (DSP/processor-based) designs by implementing a variety of computation intensive, arithmetic functions. These include adaptive finite impulse response (FIR) filters, fast Fourier transforms (FFT), convolvers, interpolators and discrete-cosine transforms (DCT) that are required for video compression and decompression, encryption, convolution and other multimedia applications.

Fast, Flexible and Efficient SRAM

The AT40K/AT40KLV FPGA offers a patented distributed 10 ns SRAM capability where the RAM can be used without losing logic resources. Multiple independent, synchronous or asynchronous, dual-port or single-port RAM functions (FIFO, scratch pad, etc.) can be created using Atmel's macro generator tool.

Fast, Efficient Array and Vector Multipliers

The AT40K/AT40KLV's patented 8-sided core cell with direct horizontal, vertical and diagonal cell-to-cell connections implements ultra fast array multipliers without using any busing resources. The AT40K/AT40KLV's Cache Logic capability enables a large number of design coefficients and variables to be implemented in a very small amount of silicon, enabling vast improvement in system speed at much lower cost than conventional FPGAs.

Cache Logic Design

The AT40K/AT40KLV, AT6000 and FPSLIC families are capable of implementing Cache Logic (dynamic full/partial logic reconfiguration, without loss of data, on-the-fly) for building adaptive logic and systems. As new logic functions are required, they can be loaded into the logic cache without losing the data already there or disrupting the operation of the rest of the chip; replacing or complementing the active logic. The AT40K/AT40KLV can act as a reconfigurable coprocessor.

Automatic Component Generators

The AT40K/AT40KLV FPGA family is capable of implementing user-defined, automatically generated, macros in multiple designs; speed and functionality are unaffected by the macro orientation or density of the target device. This enables the fastest, most predictable and efficient FPGA design approach and minimizes design risk by reusing already proven functions. The Automatic Component Generators work seamlessly with industry standard schematic and synthesis tools to create the fastest, most efficient designs available.

The patented AT40K/AT40KLV series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 5,000 to 50,000 usable gates in the family, and have 256 to 2,304 registers. Pin locations are consistent throughout the AT40K/AT40KLV series for easy design migration in the same package footprint. The AT40K/AT40KLV series FPGAs utilize a reliable 0.6µ single-poly, CMOS process and are 100% factory-tested. Atmel's PC- and workstation-based integrated development system (IDS) is used to create AT40K/AT40KLV series designs. Multiple design entry methods are supported.

The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, efficient and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

For a complete version of this datasheet, refer to the FPGA section of the Atmel web site, www.atmel.com.

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