# Dual, Ultra-Low-Power, 12-Bit, Voltage-Output DACs

# MAX5532–MAX5535

## General Description

The MAX5532–MAX5535 are dual, 12-bit, ultra-low-power, voltage-output, digital-to-analog converters (DACs) offering rail-to-rail buffered voltage outputs. The DACs operate from a 1.8V to 5.5V supply and consume less than 5µA, making the devices suitable for low-power and low-voltage applications. A shutdown mode reduces overall current, including the reference input current, to just 0.18µA. The MAX5532–MAX5535 use a 3-wire serial interface that is compatible with SPI™, QSPI™, and MICROWIRE™.

Upon power-up, the MAX5532–MAX5535 outputs are driven to zero scale, providing additional safety for applications that drive valves or for other transducers that need to be off during power-up. The zero-scale outputs enable glitch-free power-up.

The MAX5532 accepts an external reference input and provides unity-gain outputs. The MAX5533 contains a precision internal reference and provides a buffered external reference output with unity-gain DAC outputs. The MAX5534 accepts an external reference input and provides force-sense outputs. The MAX5535 contains a precision internal reference and provides a buffered external reference output with force-sense DAC outputs.

The MAX5534/MAX5535 are available in a 4mm x 4mm x 0.8mm, 12-pin, thin QFN package. The MAX5532/MAX5533 are available in an 8-pin µMAX® package. All devices are guaranteed over the extended -40°C to +85°C temperature range.

For 10-bit compatible devices, refer to the MAX5522–MAX5525 data sheet. For 8-bit compatible devices, refer to the MAX5512–MAX5515 data sheet.

## Applications

- Portable Battery-Powered Devices
- Instrumentation
- Automatic Trimming and Calibration in Factory or Field
- Programmable Voltage and Current Sources
- Industrial Process Control and Remote Industrial Devices
- Remote Data Conversion and Monitoring
- Chemical Sensor Cell Bias for Gas Monitors
- Programmable LCD Bias

*SPI and QSPI are trademarks of Motorola, Inc.*
*MICROWIRE is a trademark of National Semiconductor Corp.*
*µMAX is a registered trademark of Maxim Integrated Products, Inc.*

## Features

- Ultra-Low 5µA Supply Current
- Shutdown Mode Reduces Supply Current to 0.18µA (max)
- Single +1.8V to +5.5V Supply
- Small 4mm x 4mm x 0.8mm Thin QFN Package
- Internal Reference Sources 8mA of Current (MAX5533/MAX5535)
- Flexible Force-Sense-Configured Rail-to-Rail Output Buffers
- Fast 16MHz, 3-Wire, SPI-/QSPI-/MICROWIRE-Compatible Serial Interface
- TTL- and CMOS-Compatible Digital Inputs with Hysteresis
- Glitch-Free Outputs During Power-Up

## Ordering Information

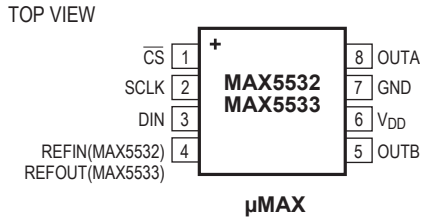
| PART | TEMP RANGE | PIN-PACKAGE | PKG CODE |
|---|---|---|---|
| **MAX5532**EUA | -40°C to +85°C | 8 µMAX | U8C-3 |
| **MAX5533**EUA | -40°C to +85°C | 8 µMAX | U8C-3 |
| **MAX5534**ETC | -40°C to +85°C | 12 Thin QFN-EP* | T1244-4 |
| **MAX5535**ETC | -40°C to +85°C | 12 Thin QFN-EP* | T1244-4 |

**EP = Exposed paddle (internally connected to GND).*

## Selector Guide

| PART | OUTPUTS | REFERENCE | TOP MARK |
|---|---|---|---|
| MAX5532EUA | Unity gain | External | — |
| MAX5533EUA | Unity gain | Internal | — |
| MAX5534ETC | Force sense | External | AACM |
| MAX5535ETC | Force sense | Internal | AACN |

## Pin Configurations




**µMAX**

*Pin Configurations continued at end of data sheet.*

*19-3062; Rev 2; 3/20*

## Absolute Maximum Ratings

$V_{DD}$ to GND .....-0.3V to +6V
OUTA, OUTB to GND.....-0.3V to ($V_{DD}$ + 0.3V)
FBA, FBB to GND .....-0.3V to ($V_{DD}$ + 0.3V)
SCLK, DIN, $\overline{CS}$ to GND.....-0.3V to ($V_{DD}$ + 0.3V)
REFIN, REFOUT to GND.....-0.3V to ($V_{DD}$ + 0.3V)
Continuous Power Dissipation ($T_A$ = +70°C)
12-Pin Thin QFN (derate 16.9mW/°C above +70°C).....1349mW
8-Pin µMAX (derate 5.9mW/°C above +70°C).....471mW

Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Electrical Characteristics

($V_{DD}$ = +1.8V to +5.5V, OUT_ unloaded, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **STATIC ACCURACY (MAX5532/MAX5534 EXTERNAL REFERENCE)** | | | | | | |
| Resolution | N | | 12 | | | Bits |
| Integral Nonlinearity (Note 1) | INL | $V_{DD}$ = 5V, $V_{REF}$ = 4.096V | | ±4 | ±8 | LSB |
| | | $V_{DD}$ = 1.8V, $V_{REF}$ = 1.024V | | ±4 | ±8 | |
| Differential Nonlinearity (Note 1) | DNL | Guaranteed monotonic, $V_{DD}$ = 5V, $V_{REF}$ = 4.096V | | ±0.2 | ±1 | LSB |
| | | Guaranteed monotonic, $V_{DD}$ = 1.8V, $V_{REF}$ = 1.024V | | ±0.2 | ±1 | |
| Offset Error (Note 2) | $V_{OS}$ | $V_{DD}$ = 5V, $V_{REF}$ = 4.096V | | ±1 | ±20 | mV |
| | | $V_{DD}$ = 1.8V, $V_{REF}$ = 1.024V | | ±1 | ±20 | |
| Offset-Error Temperature Drift | | | | ±2 | | µV/°C |
| Gain Error (Note 3) | GE | $V_{DD}$ = 5V, $V_{REF}$ = 4.096V | | ±2 | ±4 | LSB |
| | | $V_{DD}$ = 1.8V, $V_{REF}$ = 1.024V | | ±2 | ±4 | |
| Gain-Error Temperature | | | | ±4 | | ppm/°C |
| Power-Supply Rejection Ratio | PSRR | 1.8V ≤ $V_{DD}$ ≤ 5.5V | | 85 | | dB |
| **STATIC ACCURACY (MAX5533/MAX5535 INTERNAL REFERENCE)** | | | | | | |
| Resolution | N | | 12 | | | Bits |
| Integral Nonlinearity (Note 1) | INL | $V_{DD}$ = 5V, $V_{REF}$ = 3.9V | | ±4 | ±8 | LSB |
| | | $V_{DD}$ = 1.8V, $V_{REF}$ = 1.2V | | ±4 | ±8 | |
| Differential Nonlinearity (Note 1) | DNL | Guaranteed monotonic, $V_{DD}$ = 5V, $V_{REF}$ = 3.9V | | ±0.2 | ±1 | LSB |
| | | Guaranteed monotonic, $V_{DD}$ = 1.8V, $V_{REF}$ = 1.2V | | ±0.2 | ±1 | |
| Offset Error (Note 2) | $V_{OS}$ | $V_{DD}$ = 5V, $V_{REF}$ = 3.9V | | ±1 | ±20 | mV |
| | | $V_{DD}$ = 1.8V, $V_{REF}$ = 1.2V | | ±1 | ±20 | |
| Offset-Error Temperature Drift | | | | ±2 | | µV/°C |
| Gain Error (Note 3) | GE | $V_{DD}$ = 5V, $V_{REF}$ = 3.9V | | ±2 | ±4 | LSB |
| | | $V_{DD}$ = 1.8V, $V_{REF}$ = 1.2V | | ±2 | ±4 | |

## Electrical Characteristics (continued)

($V_{DD}$ = +1.8V to +5.5V, OUT_ unloaded, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Gain-Error Temperature Coefficient | | | | ±4 | | ppm/°C |
| Power-Supply Rejection Ratio | PSRR | 1.8V ≤ $V_{DD}$ ≤ 5.5V | | 85 | | dB |
| **REFERENCE INPUT (MAX5532/MAX5534)** | | | | | | |
| Reference-Input Voltage Range | $V_{REFIN}$ | | 0 | | $V_{DD}$ | V |
| Reference-Input Impedance | $R_{REFIN}$ | Normal operation | 4.1 | | | MΩ |
| | | In shutdown | | 2.5 | | GΩ |
| **REFERENCE OUTPUT (MAX5533/MAX5535)** | | | | | | |
| Initial Accuracy | $V_{REFOUT}$ | No external load, $V_{DD}$ = 1.8V | 1.197 | 1.214 | 1.231 | V |
| | | No external load, $V_{DD}$ = 2.5V | 1.913 | 1.940 | 1.967 | |
| | | No external load, $V_{DD}$ = 3V | 2.391 | 2.425 | 2.459 | |
| | | No external load, $V_{DD}$ = 5V | 3.828 | 3.885 | 3.941 | |
| Output-Voltage Temperature Coefficient | $V_{TEMPCO}$ | $T_A$ = -40°C to +85°C (Note 4) | | 12 | 30 | ppm/°C |
| Line Regulation | | $V_{REFOUT}$ < $V_{DD}$ - 200mV (Note 5) | | 2 | 200 | µV/V |
| Load Regulation | | 0 ≤ $I_{REFOUT}$ ≤ 1mA, sourcing, $V_{DD}$ = 1.8V, $V_{REF}$ = 1.2V | | 0.3 | 2 | µV/µA |
| | | 0 ≤ $I_{REFOUT}$ ≤ 8mA, sourcing, $V_{DD}$ = 5V, $V_{REF}$ = 3.9V | | 0.3 | 2 | |
| | | -150µA ≤ $I_{REFOUT}$ ≤ 0, sinking | | 0.2 | | |
| Output Noise Voltage | | 0.1Hz to 10Hz, $V_{REF}$ = 3.9V | | 150 | | $µV_{P-P}$ |
| | | 10Hz to 10kHz, $V_{REF}$ = 3.9V | | 600 | | |
| | | 0.1Hz to 10Hz, $V_{REF}$ = 1.2V | | 50 | | |
| | | 10Hz to 10kHz, $V_{REF}$ = 1.2V | | 450 | | |
| Short-Circuit Current (Note 6) | | $V_{DD}$ = 5V | | 30 | | mA |
| | | $V_{DD}$ = 1.8V | | 14 | | |
| Capacitive Load Stability Range | | (Note 7) | | 0 to 10 | | nF |
| Thermal Hysteresis | | (Note 8) | | 200 | | ppm |
| Reference Power-Up Time (from Shutdown) | | REFOUT unloaded, $V_{DD}$ = 5V | | 5.4 | | ms |
| | | REFOUT unloaded, $V_{DD}$ = 1.8V | | 4.4 | | |
| Long-Term Stability | | | | 200 | | ppm/ 1khrs |

## Electrical Characteristics (continued)

($V_{DD}$ = +1.8V to +5.5V, OUT_ unloaded, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DAC OUTPUTS (OUTA, OUTB)** | | | | | | | |
| Capacitive Driving Capability | $C_L$ | | | | 1000 | | pF |
| Short-Circuit Current (Note 6) | | $V_{DD}$ = 5V, $V_{OUT}$ set to full scale, OUT shorted to GND, source current | | | | 65 | mA |
| | | $V_{DD}$ = 5V $V_{OUT}$ set to 0V, OUT shorted to $V_{DD}$, sink current | | | | 65 | |
| | | $V_{DD}$ = 1.8V, $V_{OUT}$ set to full scale OUT shorted to GND, source current | | | | 14 | |
| | | $V_{DD}$ = 1.8V, $V_{OUT}$ set to 0V, OUT shorted to $V_{DD}$, sink current | | | | 14 | |
| DAC Power-Up Time | | Coming out of shutdown (MAX5532/MAX5534) | $V_{DD}$ = 5V | | 3 | | ms |
| | | | $V_{DD}$ = 1.8V | | 3.8 | | |
| | | Coming out of standby (MAX5533/MAX5535) | $V_{DD}$ = 1.8V to 5.5V | | 0.4 | | |
| Output Power-Up Glitch | | $C_L$ = 100pF | | | 10 | | mV |
| FB_ Input Current | | | | | 10 | | pA |
| **DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$)** | | | | | | | |
| Input High Voltage | $V_{IH}$ | 4.5V ≤ $V_{DD}$ ≤ 5.5V | | 2.4 | | | V |
| | | 2.7V < $V_{DD}$ ≤ 3.6V | | 2.0 | | | |
| | | 1.8V ≤ $V_{DD}$ ≤ 2.7V | | 0.7 x $V_{DD}$ | | | |
| Input Low Voltage | $V_{IL}$ | 4.5V ≤ $V_{DD}$ ≤ 5.5V | | | | 0.8 | V |
| | | 2.7V < $V_{DD}$ ≤ 3.6V | | | | 0.6 | |
| | | 1.8V ≤ $V_{DD}$ ≤ 2.7V | | | | 0.3 x $V_{DD}$ | |
| Input Leakage Current | $I_{IN}$ | (Note 9) | | | ±0.05 | ±0.5 | µA |
| Input Capacitance | $C_{IN}$ | | | | 10 | | pF |
| **DYNAMIC PERFORMANCE** | | | | | | | |
| Voltage-Output Slew Rate | SR | Positive and negative (Note 10) | | | 10 | | V/ms |
| Voltage-Output Settling Time | | 0.1 to 0.9 of full scale to within 0.5 LSB (Note 10) | | | 660 | | µs |
| Output Noise Voltage | | 0.1Hz to 10Hz | $V_{DD}$ = 5V | | 80 | | $µV_{P-P}$ |
| | | | $V_{DD}$ = 1.8V | | 55 | | |
| | | 10Hz to 10kHz | $V_{DD}$ = 5V | | 620 | | |
| | | | $V_{DD}$ = 1.8V | | 476 | | |

## Electrical Characteristics (continued)

($V_{DD}$ = +1.8V to +5.5V, OUT_ unloaded, $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **POWER REQUIREMENTS** | | | | | | | |
| Supply Voltage Range | $V_{DD}$ | | | 1.8 | | 5.5 | V |
| Supply Current (Note 9) | $I_{DD}$ | MAX5533/MAX5535 | $V_{DD}$ = 5V | | 7.0 | 8.0 | µA |
| | | | $V_{DD}$ = 3V | | 6.4 | 8.0 | |
| | | | $V_{DD}$ = 1.8V | | 7.0 | 8.0 | |
| | | MAX5532/MAX5534 | $V_{DD}$ = 5V | | 3.8 | 5.0 | |
| | | | $V_{DD}$ = 3V | | 3.8 | 5.0 | |
| | | | $V_{DD}$ = 1.8V | | 4.7 | 6.0 | |
| Standby Supply Current | $I_{DDSD}$ | MAX5533/MAX5535 (Note 9) | $V_{DD}$ = 5V | | 3.3 | 4.5 | µA |
| | | | $V_{DD}$ = 3V | | 2.8 | 4.0 | |
| | | | $V_{DD}$ = 1.8V | | 2.4 | 3.5 | |
| Shutdown Supply Current | $I_{DDPD}$ | (Note 9) | | | 0.05 | 0.25 | µA |

## Timing Characteristics

($V_{DD}$ = +4.5V to +5.5V, $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **TIMING CHARACTERISTICS ($V_{DD}$ = 4.5V to 5.5V )** | | | | | | |
| Serial Clock Frequency | $f_{SCLK}$ | | 0 | | 16.7 | MHz |
| DIN to SCLK Rise Setup Time | $t_{DS}$ | | 15 | | | ns |
| DIN to SCLK Rise Hold Time | $t_{DH}$ | | 0 | | | ns |
| SCLK Pulse-Width High | $t_{CH}$ | | 24 | | | ns |
| SCLK Pulse-Width Low | $t_{CL}$ | | 24 | | | ns |
| $\overline{CS}$ Pulse-Width High | $t_{CSW}$ | | 100 | | | ns |
| SCLK Rise to $\overline{CS}$ Rise Hold Time | $t_{CSH}$ | | 0 | | | ns |
| $\overline{CS}$ Fall to SCLK Rise Setup Time | $t_{CSS}$ | | 20 | | | ns |
| SCLK Fall to $\overline{CS}$ Fall Setup | $t_{CSO}$ | | 0 | | | ns |
| $\overline{CS}$ Rise to SCLK Rise Hold Time | $t_{CS1}$ | | 20 | | | ns |

## Timing Characteristics

($V_{DD}$ = +1.8V to +5.5V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

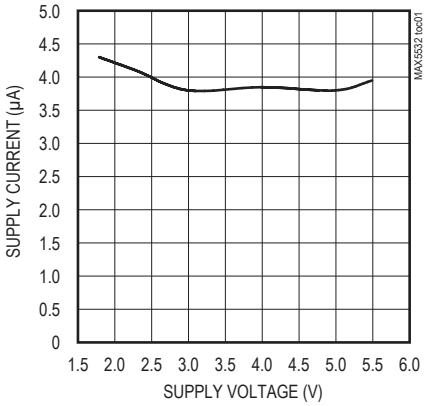
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **TIMING CHARACTERISTICS ($V_{DD}$ = 1.8V to 5.5V )** | | | | | | |
| Serial Clock Frequency | $f_{SCLK}$ | | 0 | | 10 | MHz |
| DIN to SCLK Rise Setup Time | $t_{DS}$ | | 24 | | | ns |
| DIN to SCLK Rise Hold Time | $t_{DH}$ | | 0 | | | ns |
| SCLK Pulse-Width High | $t_{CH}$ | | 40 | | | ns |
| SCLK Pulse-Width Low | $t_{CL}$ | | 40 | | | ns |
| $\overline{CS}$ Pulse-Width High | $t_{CSW}$ | | 150 | | | ns |
| SCLK Rise to $\overline{CS}$ Rise Hold Time | $t_{CSH}$ | | 0 | | | ns |
| $\overline{CS}$ Fall to SCLK Rise Setup Time | $t_{CSS}$ | | 30 | | | ns |
| SCLK Rise to $\overline{CS}$ Fall Setup | $t_{CSO}$ | | 0 | | | ns |
| $\overline{CS}$ Rise to SCK Rise Hold Time | $t_{CS1}$ | | 30 | | | ns |

**Note 1:** Linearity is tested within codes 96 to 4080.
**Note 2:** Offset is tested at code 96.
**Note 3:** Gain is tested at code 4095. For the MAX5534/MAX5535, FB_ is connected to its respective OUT_.
**Note 4:** Guaranteed by design. Not production tested.
**Note 5:** $V_{DD}$ must be a minimum of 1.8V.
**Note 6:** Outputs can be shorted to $V_{DD}$ or GND indefinitely, provided that package power dissipation is not exceeded.
**Note 7:** Optimal noise performance is at 2nF load capacitance.
**Note 8:** Thermal hysteresis is defined as the change in the initial +25°C output voltage after cycling the device from $T_{MAX}$ to $T_{MIN}$.
**Note 9:** All digital inputs at $V_{DD}$ or GND.
**Note 10:** Load = 10kΩ in parallel with 100pF, $V_{DD}$ = 5V, $V_{REF}$ = 4.096V (MAX5532/MAX5534) or $V_{REF}$ = 3.9V (MAX5533/MAX5535).

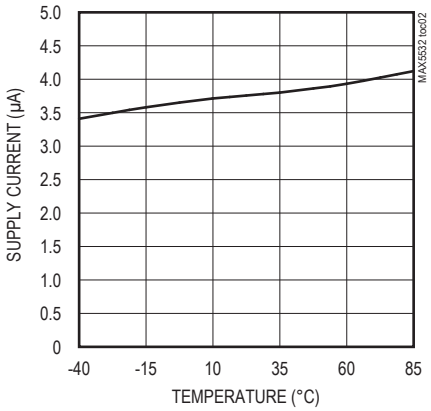
## Typical Operating Characteristics

($V_{DD}$ = 5.0V, $V_{REF}$ = 4.096V (MAX5532/MAX5534), $V_{REF}$ = 3.9V (MAX5533/MAX5535), $T_A$ = +25°C, unless otherwise noted.)

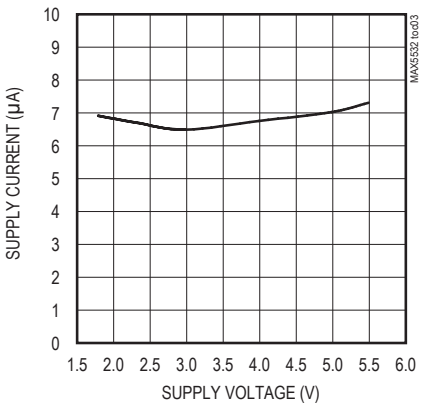
**SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX5532/MAX5534)**



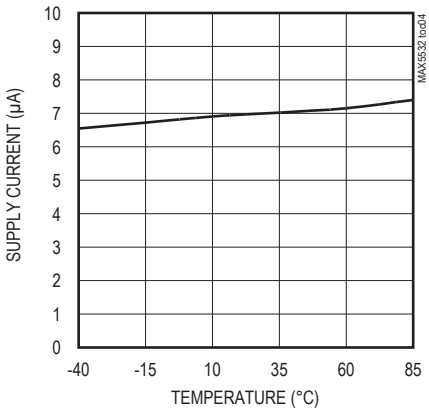

**SUPPLY CURRENT vs. TEMPERATURE (MAX5532/MAX5534)**



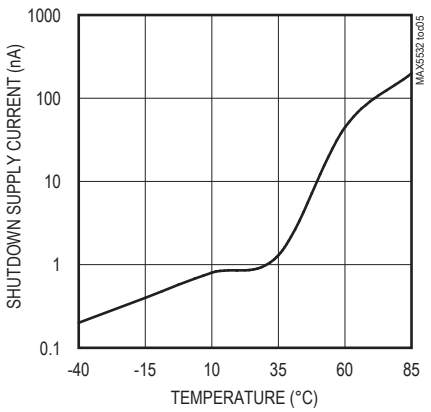

**SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX5533/MAX5535)**



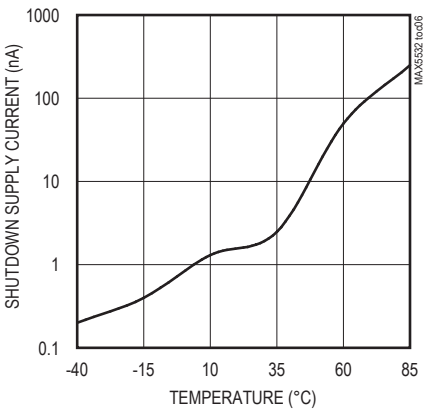

**SUPPLY CURRENT vs. TEMPERATURE (MAX5533/MAX5535)**



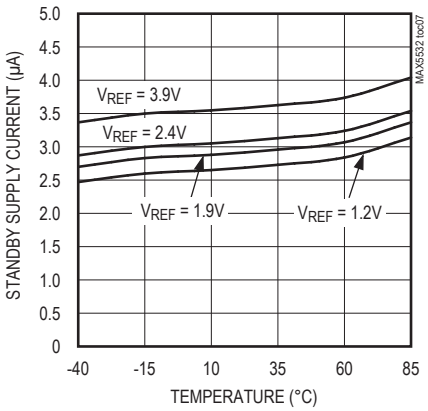

**SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE (MAX5532/MAX5534)**



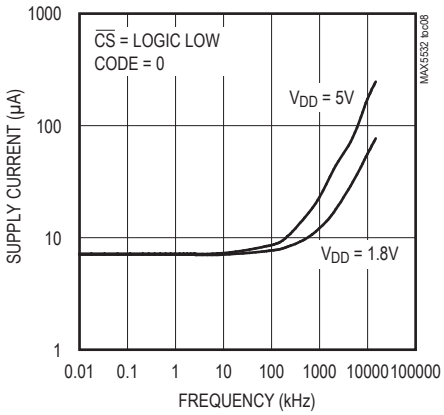

**SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE (MAX5533/MAX5535)**



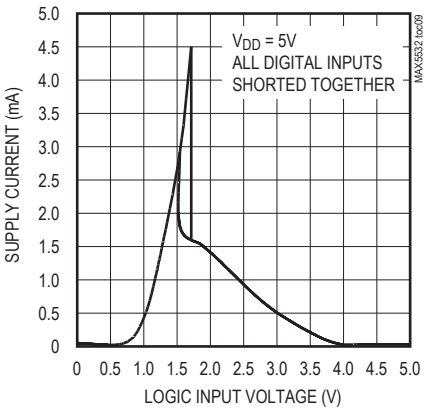

**STANDBY SUPPLY CURRENT vs. TEMPERATURE (MAX5533/MAX5535)**




**SUPPLY CURRENT vs. CLOCK FREQUENCY**



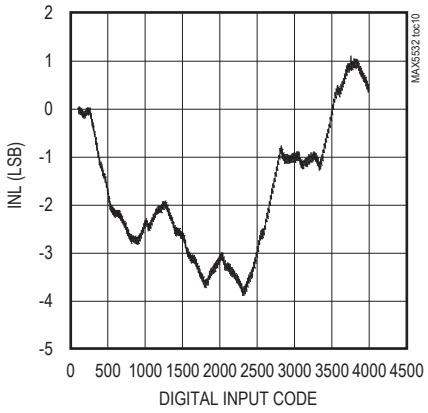

**SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE**



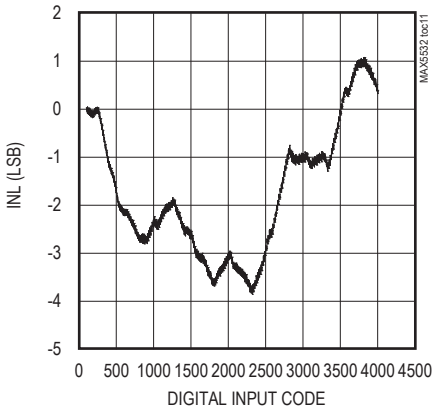
## Typical Operating Characteristics (continued)

($V_{DD}$ = 5.0V, $V_{REF}$ = 4.096V (MAX5532/MAX5534), $V_{REF}$ = 3.9V (MAX5533/MAX5535), $T_A$ = +25°C, unless otherwise noted.)

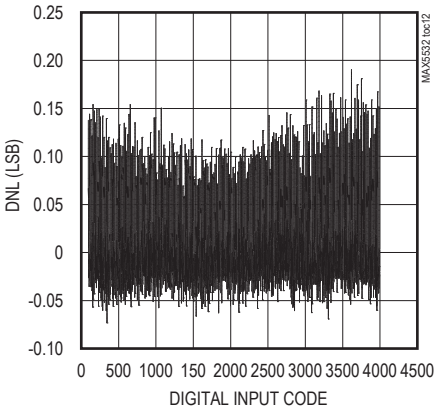
**INL vs. INPUT CODE**
**($V_{DD}$ = $V_{REF}$ = 1.8V)**



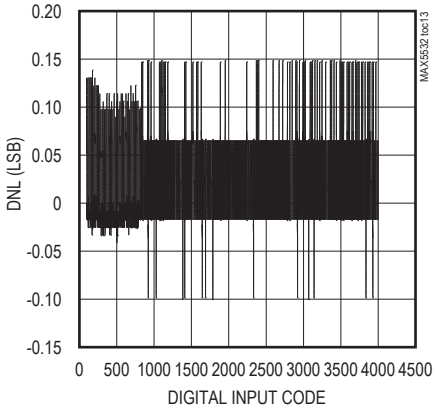

**INL vs. INPUT CODE**
**($V_{DD}$ = $V_{REF}$ = 5V)**



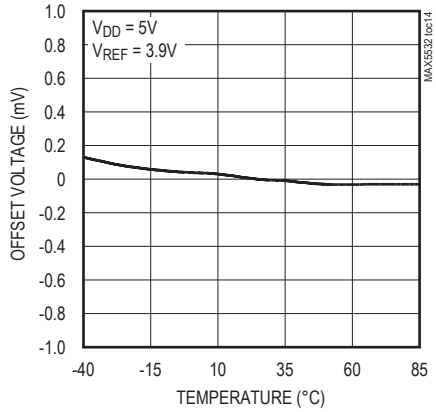

**DNL vs. INPUT CODE**
**($V_{DD}$ = $V_{REF}$ = 1.8V)**



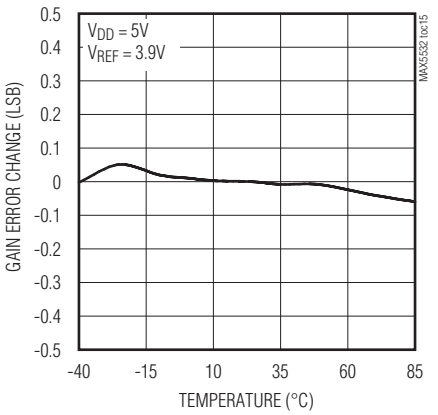

**DNL vs. INPUT CODE**
**($V_{DD}$ = $V_{REF}$ = 5V)**



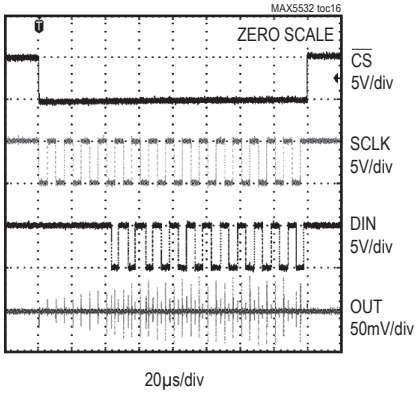

**OFFSET VOLTAGE vs. TEMPERATURE**



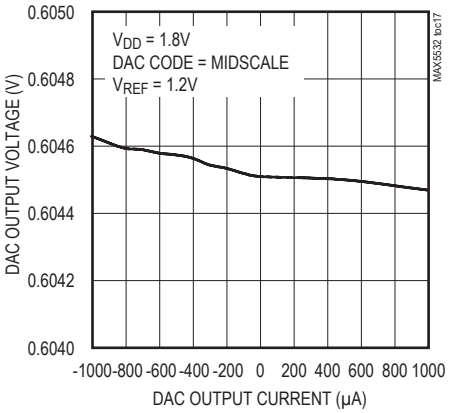

**GAIN ERROR CHANGE vs. TEMPERATURE**



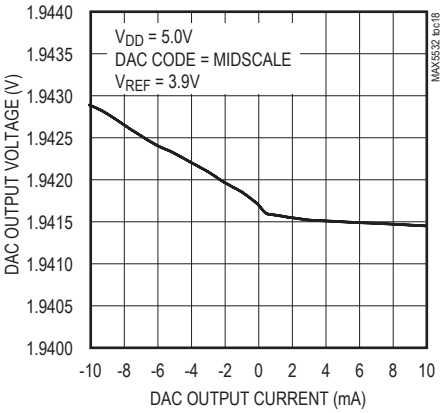

**DIGITAL FEEDTHROUGH RESPONSE**




**DAC OUTPUT LOAD REGULATION**
**vs. OUTPUT CURRENT**



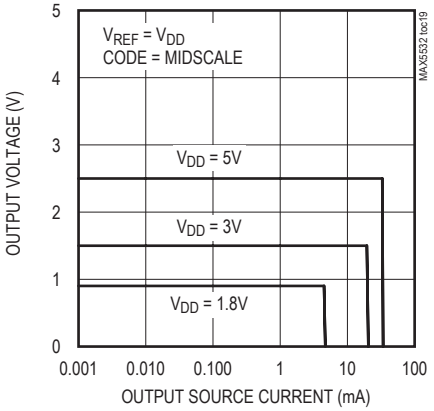

**DAC OUTPUT LOAD REGULATION**
**vs. OUTPUT CURRENT**



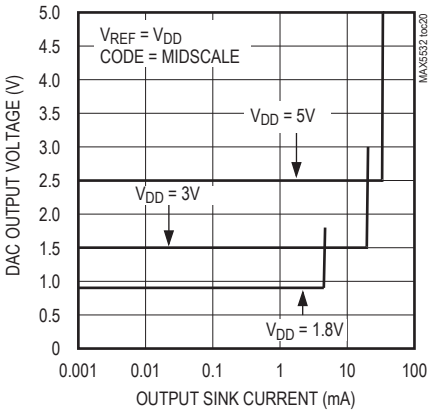
## Typical Operating Characteristics (continued)

($V_{DD}$ = 5.0V, $V_{REF}$ = 4.096V (MAX5532/MAX5534), $V_{REF}$ = 3.9V (MAX5533/MAX5535), $T_A$ = +25°C, unless otherwise noted.)

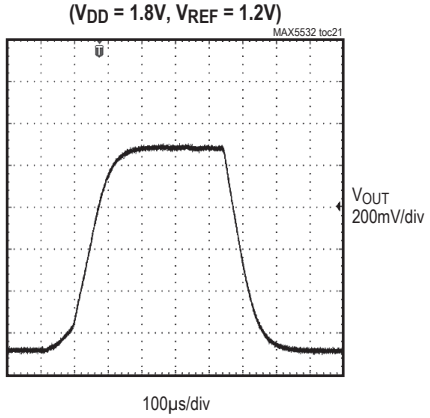
**DAC OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT**



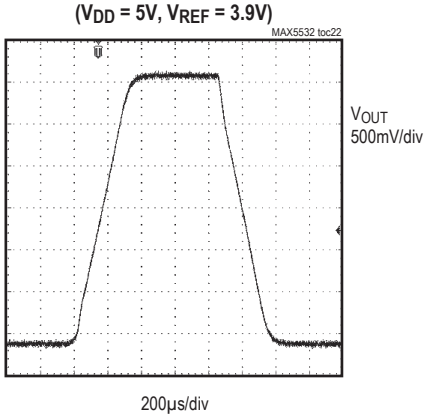

**DAC OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT**



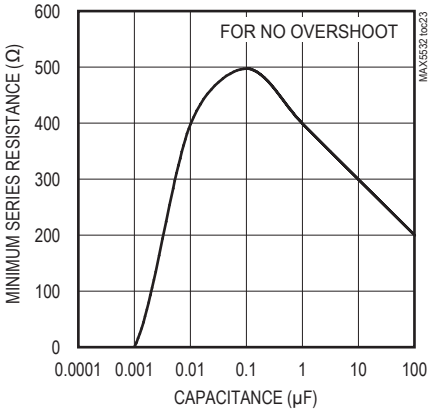

**OUTPUT LARGE-SIGNAL STEP RESPONSE ($V_{DD}$ = 1.8V, $V_{REF}$ = 1.2V)**



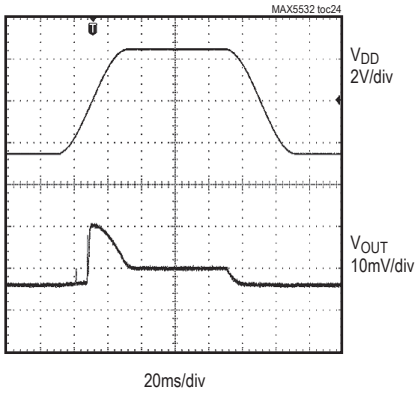

**OUTPUT LARGE-SIGNAL STEP RESPONSE ($V_{DD}$ = 5V, $V_{REF}$ = 3.9V)**



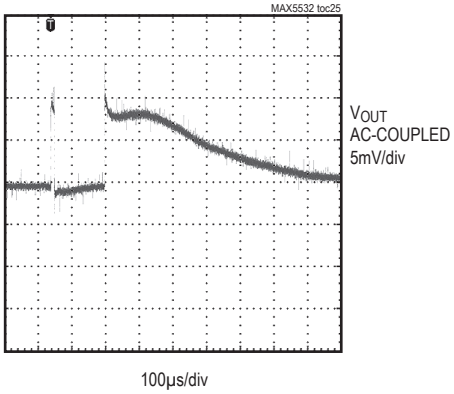

**OUTPUT MINIMUM SERIES RESISTANCE vs. LOAD CAPACITANCE**



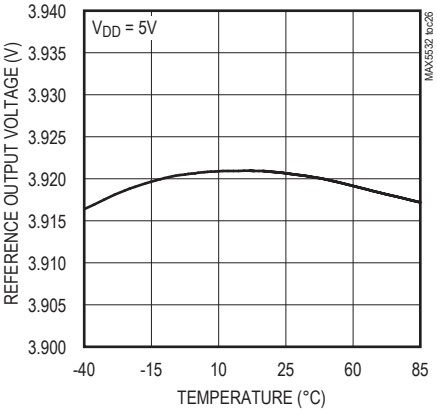

**POWER-UP OUTPUT VOLTAGE GLITCH**



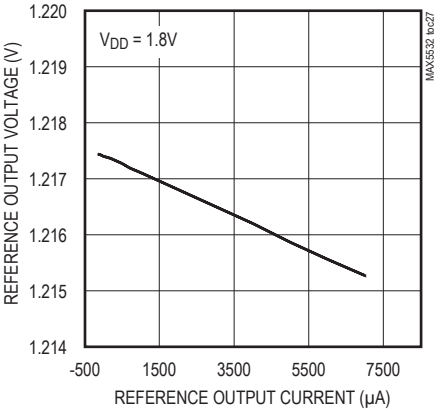

**MAJOR CARRY OUTPUT VOLTAGE GLITCH (CODE 7FFh TO 800h) ($V_{DD}$ = 5V, $V_{REF}$ = 3.9V)**




**REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE**



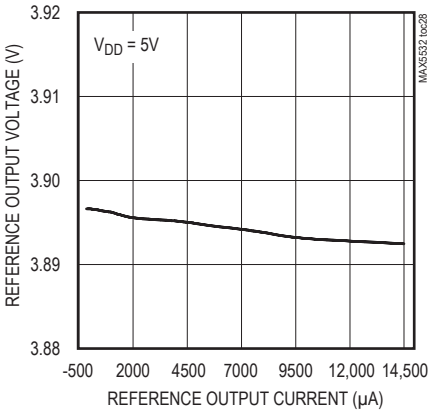

**REFERENCE OUTPUT VOLTAGE vs. REFERENCE OUTPUT CURRENT**



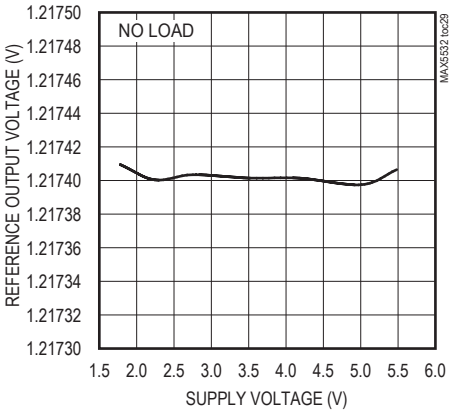
## Typical Operating Characteristics (continued)

($V_{DD}$ = 5.0V, $V_{REF}$ = 4.096V (MAX5532/MAX5534), $V_{REF}$ = 3.9V (MAX5533/MAX5535), $T_A$ = +25°C, unless otherwise noted.)

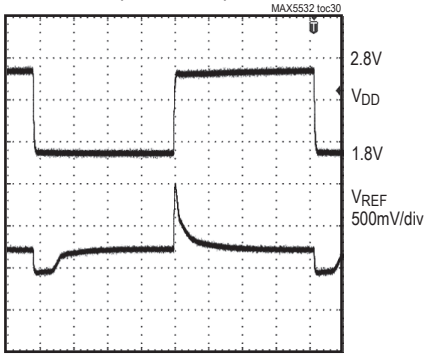
**REFERENCE OUTPUT VOLTAGE vs. REFERENCE OUTPUT CURRENT**



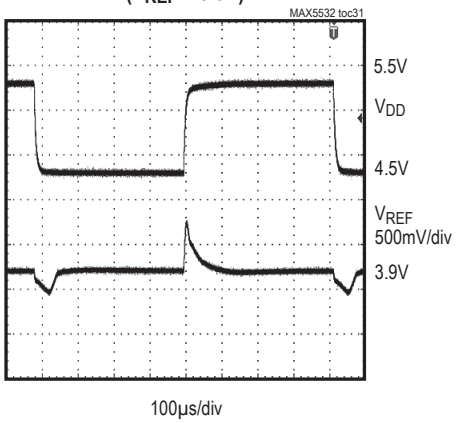

**REFERENCE OUTPUT VOLTAGE vs. SUPPLY VOLTAGE**



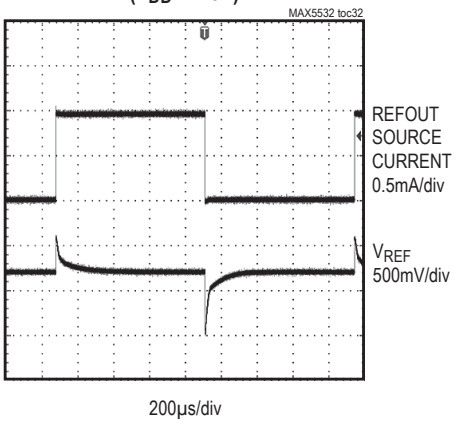

**REFERENCE LINE-TRANSIENT RESPONSE ($V_{REF}$ = 1.2V)**



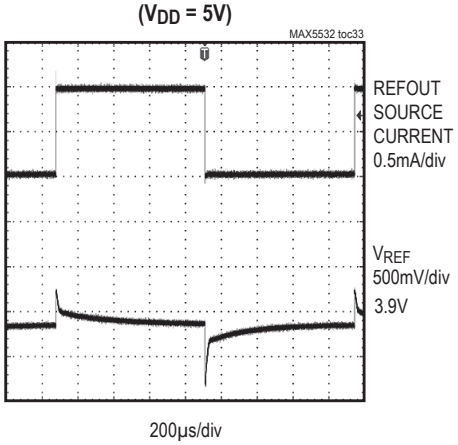

**REFERENCE LINE-TRANSIENT RESPONSE ($V_{REF}$ = 3.9V)**



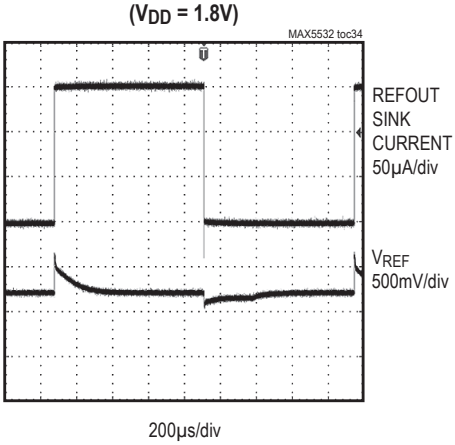

**REFERENCE LOAD TRANSIENT ($V_{DD}$ = 1.8V)**




**REFERENCE LOAD TRANSIENT ($V_{DD}$ = 5V)**



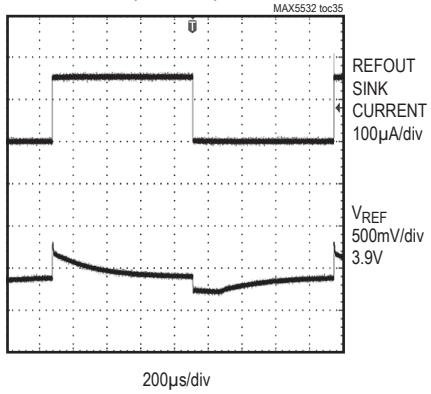

**REFERENCE LOAD TRANSIENT ($V_{DD}$ = 1.8V)**



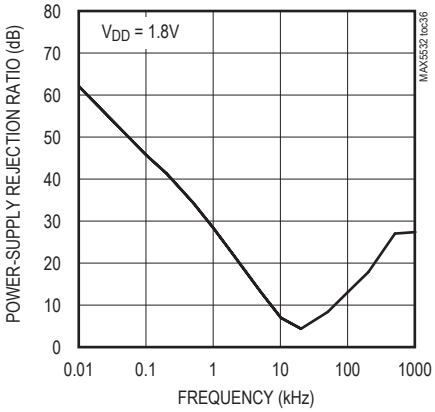
## Typical Operating Characteristics (continued)

($V_{DD}$ = 5.0V, $V_{REF}$ = 4.096V (MAX5532/MAX5534), $V_{REF}$ = 3.9V (MAX5533/MAX5535), $T_A$ = +25°C, unless otherwise noted.)

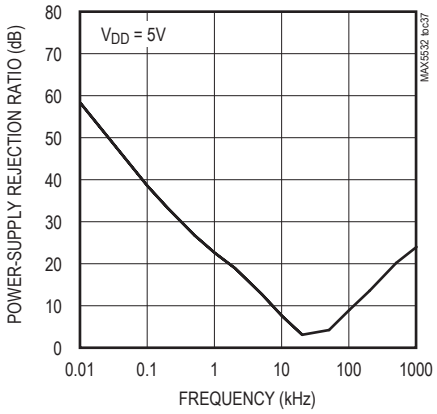
**REFERENCE LOAD TRANSIENT ($V_{DD}$ = 5V)**



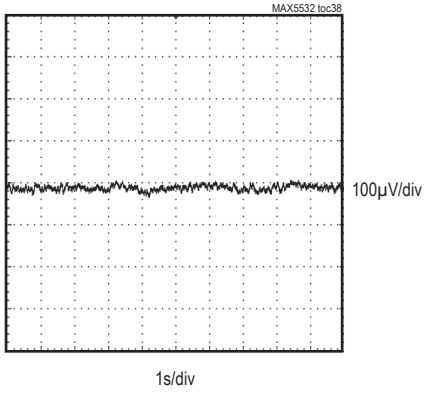

**REFERENCE PSRR vs. FREQUENCY**



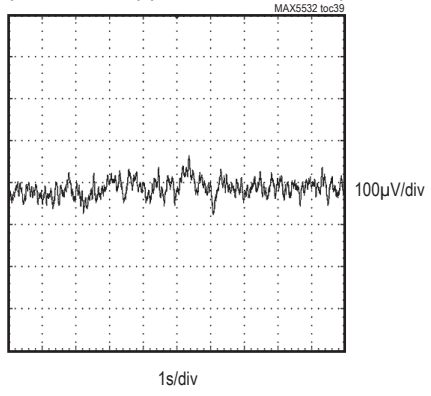

**REFERENCE PSRR vs. FREQUENCY**



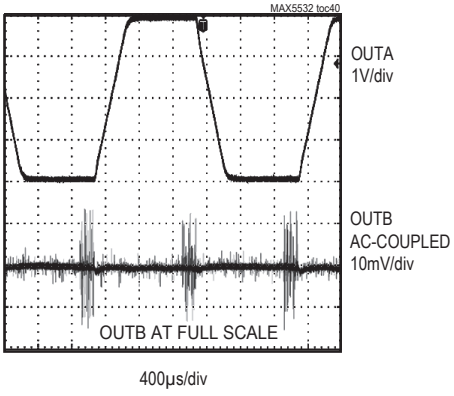

**REFERENCE OUTPUT NOISE (0.1Hz TO 10Hz) ($V_{DD}$ = 1.8V, $V_{REF}$ = 1.2V)**




**REFERENCE OUTPUT NOISE (0.1Hz TO 10Hz) ($V_{DD}$ = 5V, $V_{REF}$ = 3.9V)**



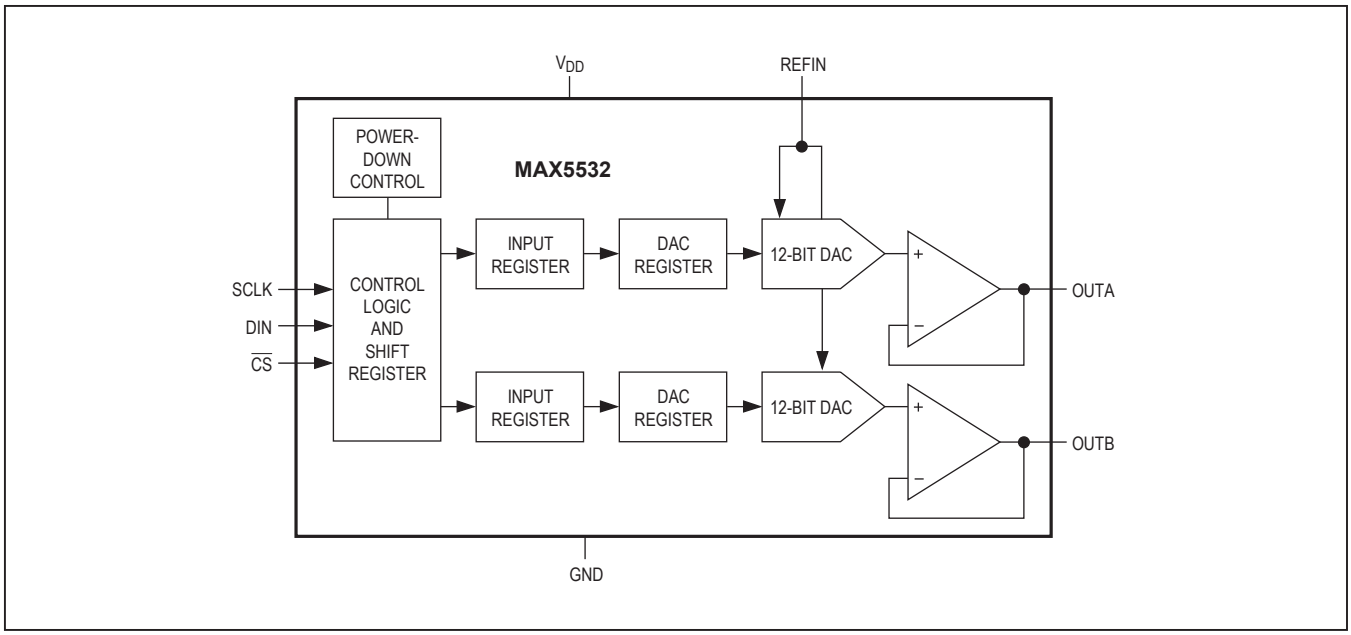

**DAC-TO-DAC CROSSTALK**



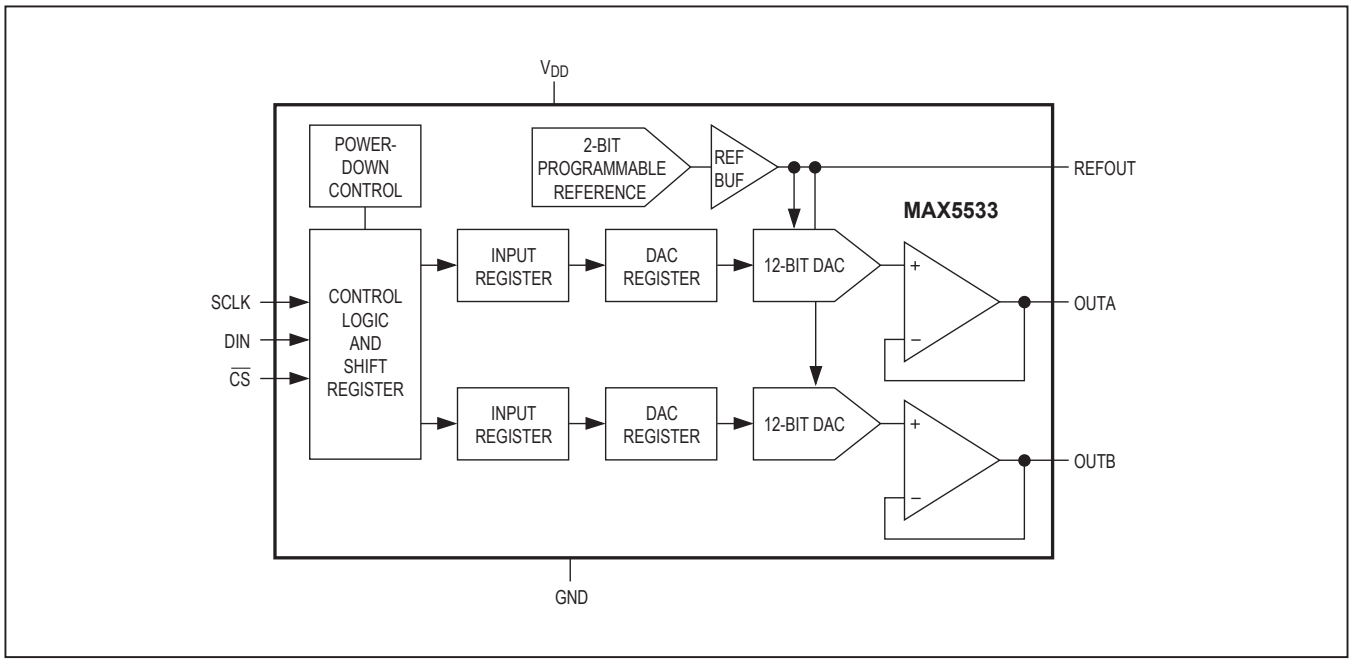
## Pin Description

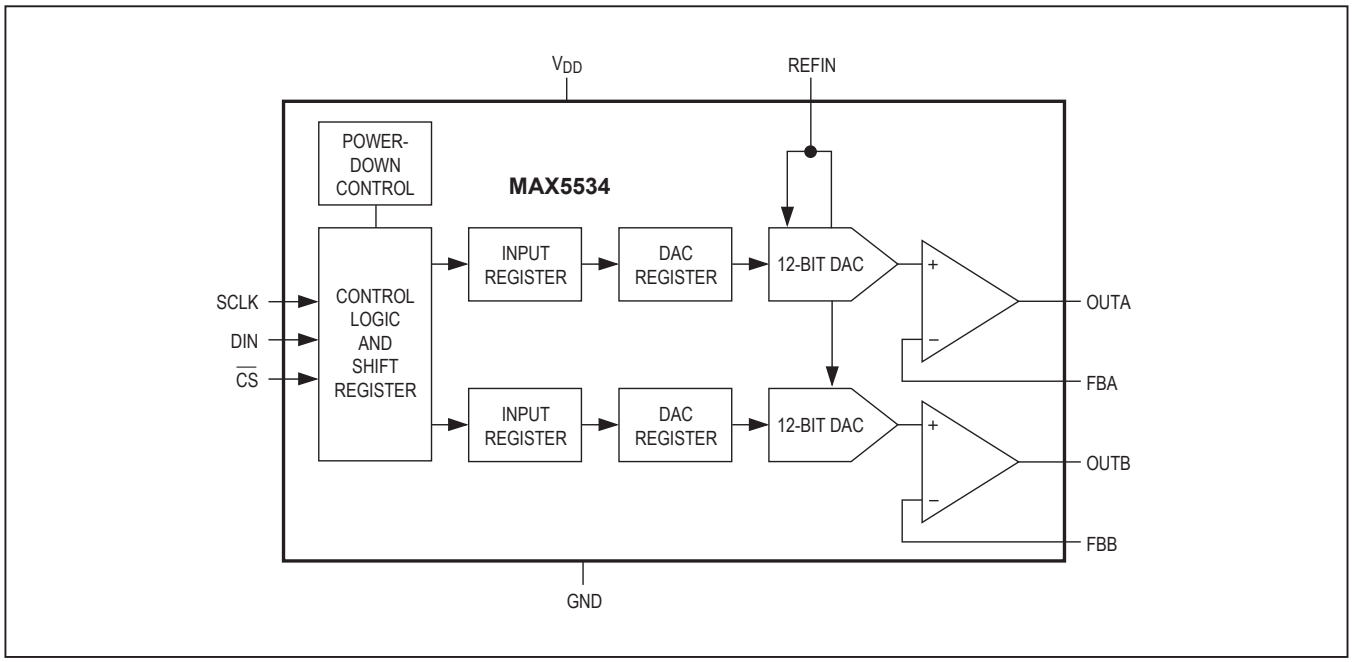
| PIN | | | | NAME | FUNCTION |
|---|---|---|---|---|---|
| MAX5532 | MAX5533 | MAX5534 | MAX5535 | | |
| 1 | 1 | 1 | 1 | $\overline{CS}$ | Active-Low Digital Chip-Select Input |
| 2 | 2 | 2 | 2 | SCLK | Serial-Interface Clock Input |
| 3 | 3 | 3 | 3 | DIN | Serial-Interface Data Input |
| 4 | — | 4 | — | REFIN | Reference Input |
| — | 4 | — | 4 | REFOUT | Reference Output |
| — | — | 5, 11 | 5, 11 | N.C. | No Connection. Leave N.C. inputs unconnected (floating) or connected to GND. |
| — | — | 6 | 6 | FBB | Channel B Feedback Input |
| 5 | 5 | 7 | 7 | OUTB | Channel B Analog Voltage Output |
| 6 | 6 | 8 | 8 | $V_{DD}$ | Power Input. Connect $V_{DD}$ to a 1.8V to 5.5V power supply. Bypass $V_{DD}$ to GND with a 0.1µF capacitor. |
| 7 | 7 | 9 | 9 | GND | Ground |
| 8 | 8 | 10 | 10 | OUTA | Channel A Analog Voltage Output |
| — | — | 12 | 12 | FBA | Channel A Feedback Input |
| — | — | EP | EP | Exposed Paddle | Exposed Paddle. Connect EP to GND. |

## Functional Diagrams

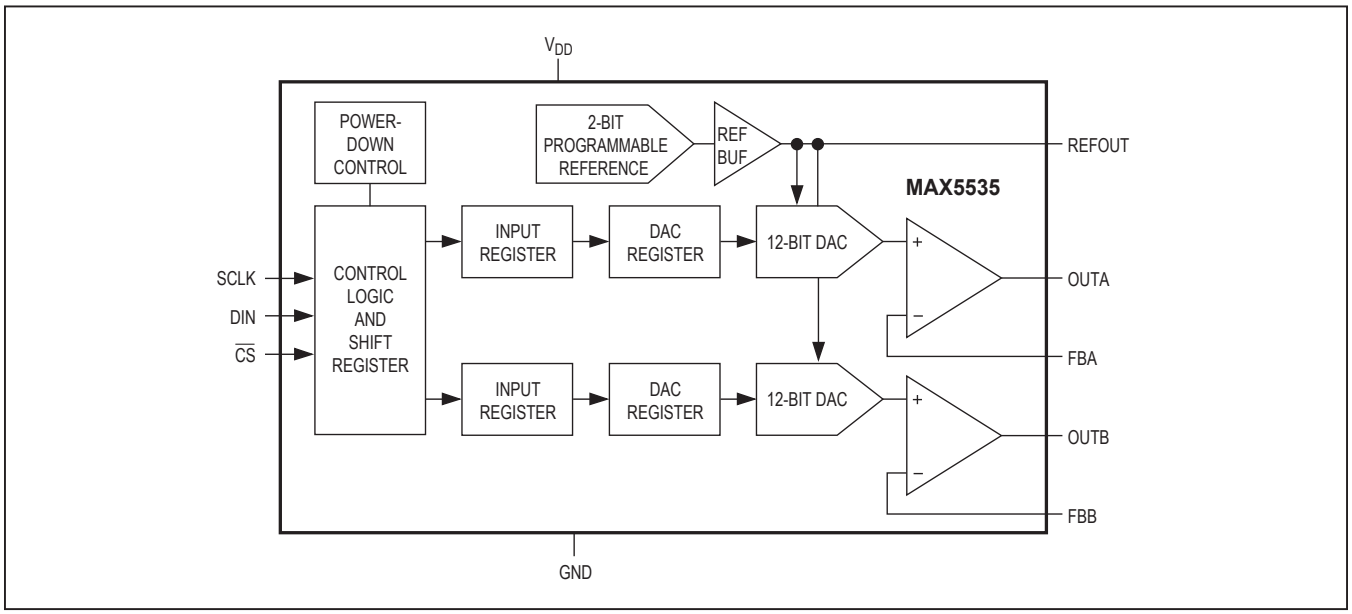


## Functional Diagrams (continued)



## Functional Diagrams (continued)




## Detailed Description

The MAX5532–MAX5535 dual, 12-bit, ultra-low-power, voltage-output DACs offer rail-to-rail buffered voltage outputs. The DACs operate from a 1.8V to 5.5V supply and require only 5µA (max) supply current. These devices feature a shutdown mode that reduces overall current, including the reference input current, to just 0.18µA (max). The MAX5533/MAX5535 include an internal reference that saves additional board space and can source up to 8mA, making it functional as a system reference. The 16MHz, 3-wire serial interface is compatible with SPI, QSPI, and MICROWIRE protocols. When $V_{DD}$ is applied, all DAC outputs are driven to zero scale with virtually no output glitch. The MAX5532/MAX5533 output buffers are configured in unity gain and come in µMAX packages. The MAX5534/MAX5535 output buffers are configured in force sense allowing users to externally set voltage gains on the output (an output-amplifier inverting input is available). The MAX5534/MAX5535 come in 4mm x 4mm thin QFN packages.

### Digital Interface

The MAX5532–MAX5535 use a 3-wire serial interface that is compatible with SPI/QSPI/MICROWIRE protocols (Figures 1 and 2).

The MAX5532–MAX5535 include a single, 16-bit, input shift register. Data loads into the shift register through the serial interface. $\overline{CS}$ must remain low until all 16 bits are clocked in. The 16 bits consist of 4 control bits (C3–C0) and 12 data bits (D11–D0) (Table 1). Following the control bits, the data loads MSB first, D11–D0. The control bits C3–C0 control the MAX5532–MAX5535, as outlined in Table 2.

Each DAC channel includes two registers: an input register and a DAC register. The input register holds input data. The DAC register contains the data updated to the DAC output.

The double-buffered register configuration allows any of the following:

- Loading the input registers without updating the DAC registers
- Updating the DAC registers from the input registers
- Updating all the input and DAC registers simultaneously

## Table 1. Serial Write Data Format

| CONTROL | | | | DATA BITS | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSB | | | | | | | | | | | | | | | LSB |
| C3 | C2 | C1 | C0 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

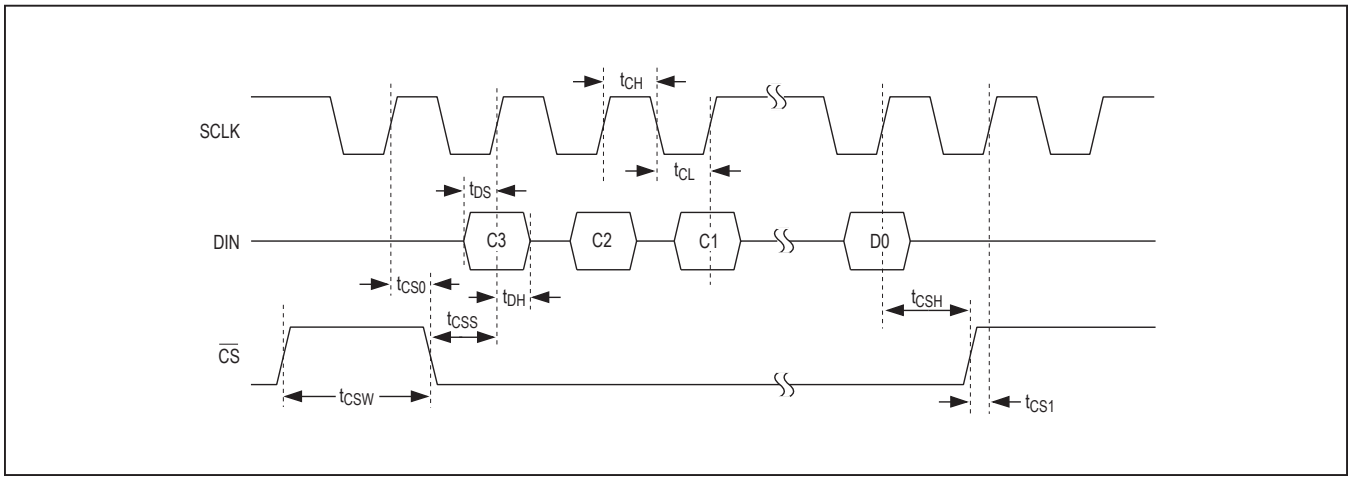



*Figure 1. Timing Diagram*

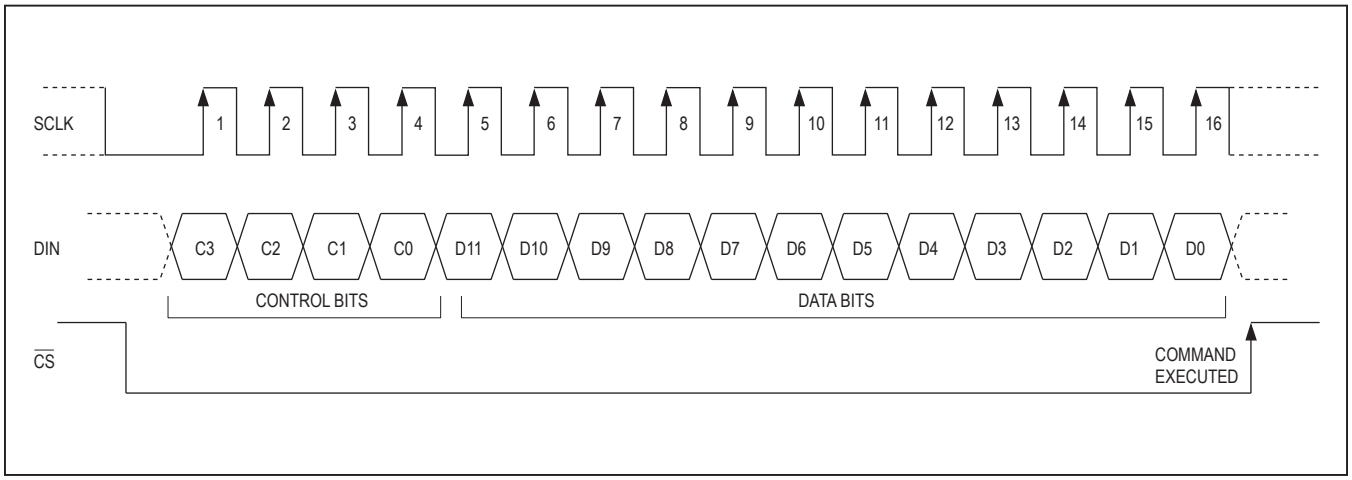



*Figure 2. Register Loading Diagram*

## Table 2. Serial-Interface Programming Commands

| CONTROL BITS | | | | INPUT DATA | FUNCTION |
|---|---|---|---|---|---|
| C3 | C2 | C1 | C0 | D11–D0 | |
| 0 | 0 | 0 | 0 | XXXXXXXXXXXX | No operation; command is ignored. |
| 0 | 0 | 0 | 1 | 12-bit data | Load input register A from shift register; DAC registers unchanged; DAC outputs unchanged. |
| 0 | 0 | 1 | 0 | 12–bit data | Load input register B from shift register; DAC registers unchanged; DAC outputs unchanged. |
| 0 | 0 | 1 | 1 | — | Command reserved. Do not use. |
| 0 | 1 | 0 | 0 | — | Command reserved. Do not use. |
| 0 | 1 | 0 | 1 | — | Command reserved. Do not use. |
| 0 | 1 | 1 | 0 | — | Command reserved. Do not use. |
| 0 | 1 | 1 | 1 | — | Command reserved. Do not use. |
| 1 | 0 | 0 | 0 | 12-bit data | Load DAC registers A and B from respective input registers; DAC outputs A and B updated; MAX5533/MAX5535 enter normal operation if in standby or shutdown; MAX5532/MAX5534 enter normal operation if in shutdown. |
| 1 | 0 | 0 | 1 | 12-bit data | Load input register A and DAC register A from shift register; DAC output A updated; Load DAC register B from input register B; DAC output B updated; MAX5533/MAX5535 enter normal operation if in standby or shutdown; MAX5532/MAX5534 enter normal operation if in shutdown. |
| 1 | 0 | 1 | 0 | 12-bit data | Load input register B and DAC register B from shift register; DAC output B updated; Load DAC register A from input register A; DAC output A updated; MAX5533/MAX5535 enter normal operation if in standby or shutdown; MAX5532/MAX5534 enter normal operation if in shutdown. |
| 1 | 0 | 1 | 1 | — | Command reserved. Do not use. |
| 1 | 1 | 0 | 0 | D11, D10, XXXXXXXXXX | MAX5533/MAX5535 enter standby*, MAX5532/MAX5534 enter shutdown. For the MAX5533/MAX5535, D11 and D10 configure the internal reference voltage (Table 3). |
| 1 | 1 | 0 | 1 | D11, D10, XXXXXXXXXX | MAX5532–MAX5535 enter normal operation; DAC outputs reflect existing contents of DAC registers. For the MAX5533/MAX5535, D11 and D10 configure the internal reference voltage (Table 3). |
| 1 | 1 | 1 | 0 | D11, D10, XXXXXXXXXX | MAX5532–MAX5535 enter shutdown; DAC outputs set to high impedance. For the MAX5533/MAX5535, D11 and D10 configure the internal reference voltage (Table 3). |
| 1 | 1 | 1 | 1 | 12-bit data | Load input registers A and B and DAC registers A and B from shift register; DAC outputs A and B updated; MAX5533/MAX5535 enter normal operation if in standby or shutdown; MAX5532/MAX5534 enter normal operation if in shutdown. |

*X = Don't care.*

**Standby mode can be entered from normal operation only. It is not possible to enter standby mode from shutdown.*

## Power Modes

The MAX5532–MAX5535 feature two power modes to conserve power during idle periods. In normal operation, the device is fully operational. In shutdown mode, the device is completely powered down, including the internal voltage reference in the MAX5533/MAX5535. The MAX5533/MAX5535 also offer a standby mode in which all circuitry is powered down except the internal voltage reference. Standby mode keeps the reference powered up while the remaining circuitry is shut down, allowing it to be used as a system reference. It also helps reduce the wake-up delay by not requiring the reference to power up when returning to normal operation.

### Shutdown Mode

The MAX5532–MAX5535 feature a software-programmable shutdown mode that reduces the supply current and the reference input current to 0.18µA (max). Writing an input control word with control bits C[3:0] = 1110 (Table 2) places the device in shutdown mode. In shutdown, the MAX5532/MAX5534 reference input and DAC output buffers go high impedance. Placing the MAX5533/MAX5535 into shutdown turns off the internal reference and the DAC output buffers go high impedance. The serial interface still remains active for all devices.

Table 2 shows several commands that bring the MAX5532–MAX5535 back to normal operation. The power-up time from shutdown is required before the DAC outputs are valid.

**Note:** For the MAX5533/MAX5535, standby mode cannot be entered directly from shutdown mode. The device must be brought into normal operation first before entering standby mode.

### Standby Mode (MAX5533/MAX5535 Only)

The MAX5533/MAX5535 feature a software-programmable standby mode that reduces the typical supply current to 3µA (max). Standby mode powers down all circuitry except the internal voltage reference. Place the device in standby mode by writing an input control word with control bits C[3:0] = 1100 (Table 2). The internal reference and serial interface remain active while the DAC output buffers go high impedance.

For the MAX5533/MAX5535, standby mode cannot be entered directly from shutdown mode. The device must be brought into normal operation first before entering standby mode. To enter standby from shutdown, issue the command to return to normal operation followed immediately by the command to go into standby.

Table 2 shows several commands that bring the MAX5533/MAX5535 back to normal operation. When transitioning from standby mode to normal operation, only the DAC power-up time is required before the DAC outputs are valid.

## Reference Input

The MAX5532/MAX5534 accept a reference with a voltage range extending from 0 to $V_{DD}$. The output voltage ($V_{OUT}$) is represented by a digitally programmable voltage source as:

$$V_{OUT} = (V_{REF} \times N / 4096) \times gain$$

where N is the numeric value of the DAC's binary input code (0 to 4095), $V_{REF}$ is the reference voltage, gain is the externally set voltage gain for the MAX5534, and gain is one for the MAX5532.

In shutdown mode, the reference input enters a high-impedance state with an input impedance of 2.5GΩ (typ).

## Reference Output

The MAX5533/MAX5535 internal voltage reference is software configurable to one of four voltages. Upon power-up, the default reference voltage is 1.214V. Configure the reference voltage using D10 and D11 data bits (Table 3) when the control bits are as follows C[3:0] = 1100, 1101, or 1110 (Table 2). $V_{DD}$ must be kept at a minimum of 200mV above $V_{REF}$ for proper operation.

## Table 3. Reference Output Voltage Programming

| D11 | D10 | REFERENCE VOLTAGE (V) |
|---|---|---|
| 0 | 0 | 1.214 |
| 0 | 1 | 1.940 |
| 1 | 0 | 2.425 |
| 1 | 1 | 3.885 |

## Applications Information

### 1-Cell and 2-Cell Circuits

See Figure 3 for an illustration of how to power the MAX5532–MAX5535 with either one lithium-ion battery or two alkaline batteries. The low current consumption of the devices make the MAX5532–MAX5535 ideal for battery-powered applications.

### Programmable Current Source

See the circuit in Figure 4 for an illustration of how to configure the MAX5534/MAX5535 as a programmable current source for driving an LED. The MAX5534/MAX5535 drive a standard NPN transistor to program the current source. The current source ($I_{LED}$) is defined in the equation in Figure 4.

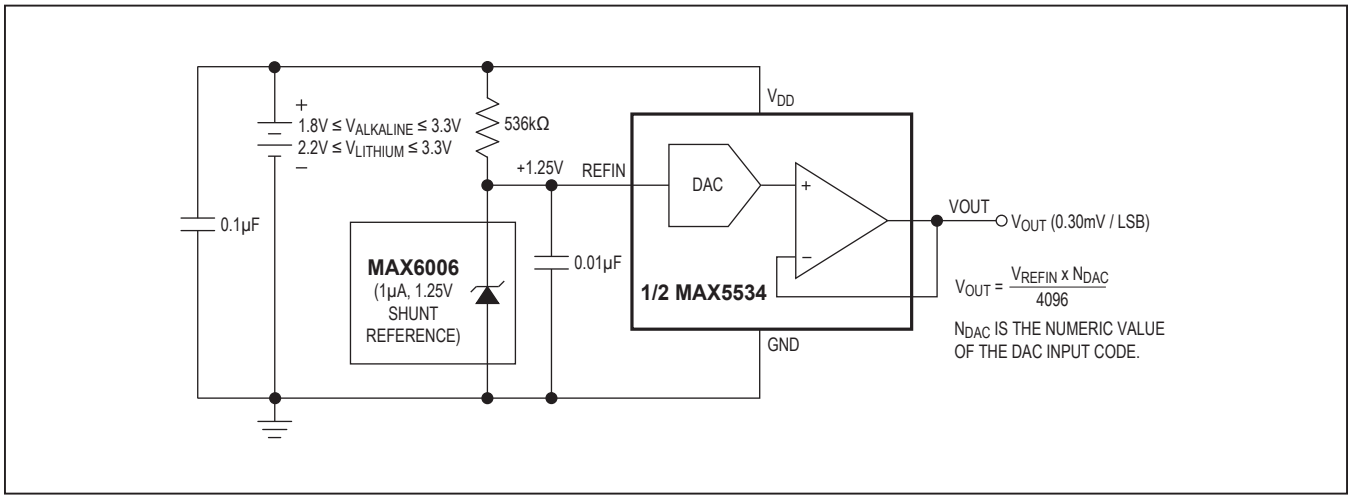



*Figure 3. Portable Application Using Two Alkaline Cells or One Lithium Coin Cell*

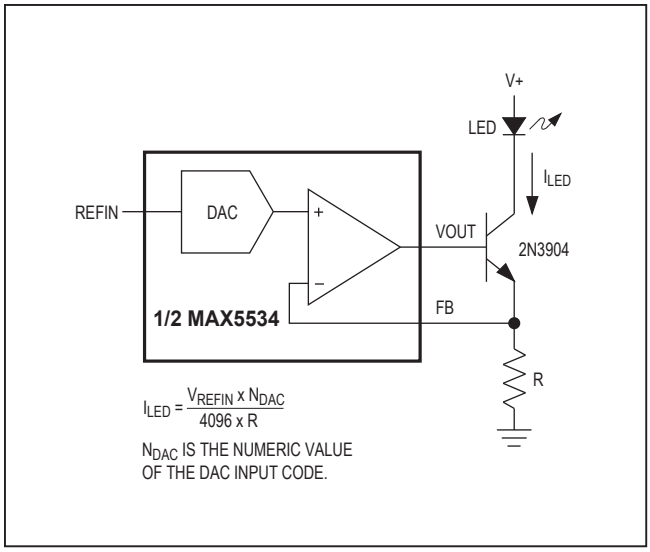



*Figure 4. Programmable Current Source Driving an LED*

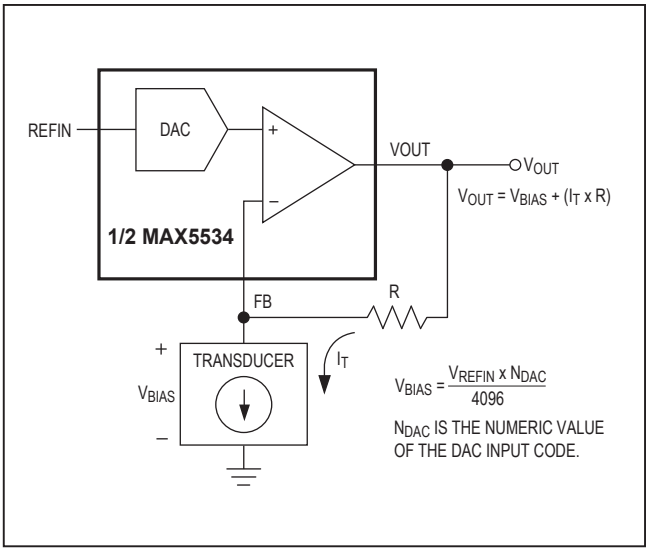



*Figure 5. Transimpedance Configuration for a Voltage-Biased Current-Output Transducer*

### Voltage Biasing a Current-Output Transducer

See the circuit in Figure 5 for an illustration of how to configure the MAX5534/MAX5535 to bias a current-output transducer. In Figure 5, the output voltage of the MAX5534/MAX5535 is a function of the voltage drop across the transducer added to the voltage drop across the feedback resistor R.

### Unipolar Output

Figure 6 shows the MAX5534 in a unipolar output configuration with unity gain. Table 4 lists the unipolar output codes.

### Bipolar Output

The MAX5534 output can be configured for bipolar operation as shown in Figure 7. The output voltage is given by the following equation:

$$V_{OUT\_} = V_{REFIN} \times [(N_A - 2048) / 2048]$$

where $N_A$ represents the decimal value of the DAC's binary input code. Table 5 shows the digital codes (offset binary) and the corresponding output voltage for the circuit in Figure 7.

### Configurable Output Gain

The MAX5534/MAX5535 have force-sense outputs, which provide a connection directly to the inverting terminal of the output op-amp, yielding the most flexibility. The advantage of the force-sense output is that specific gains can be set externally for a given application. The gain error for the MAX5534/MAX5535 is specified in a unity-gain configuration (op-amp output and inverting terminals connected), and additional gain error results from external resistor tolerances. Another advantage of the force-sense DAC is that it allows many useful circuits to be created with only a few simple external components.

An example of a custom fixed gain using the MAX5534/MAX5535 force-sense output is shown in Figure 8. In this example, R1 and R2 set the gain for $V_{OUTA}$.

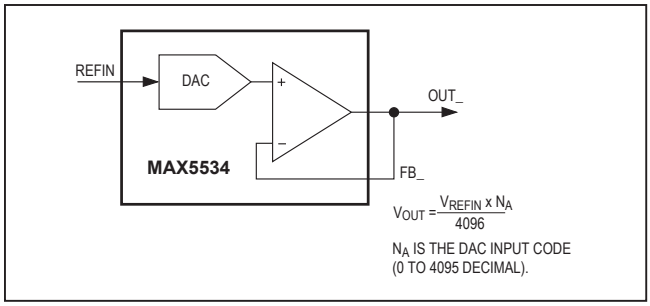



*Figure 6. Unipolar Output Circuit*

$$V_{OUTA} = [(V_{REFIN} \times N_A) / 4096] \times [1 + (R2 / R1)]$$

where $N_A$ represents the numeric value of the DAC input code.

### Self-Biased Two-Electrode Potentiostat Application

See the circuit in Figure 10 for an illustration of how to use the MAX5535 to bias a two-electrode potentiostat on the input of an ADC.

### Power Supply and Bypassing Considerations

Bypass the power supply with a 0.1µF capacitor to GND. Minimize lengths to reduce lead inductance. If noise becomes an issue, use shielding and/or ferrite beads to increase isolation. For the thin QFN package, connect the exposed pad to ground.

## Layout Considerations

Digital and AC transient signals coupling to GND can create noise at the output. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane. Wire-wrapped boards and sockets are not recommended. For optimum system performance, use printed circuit (PC) boards. Good PC board ground layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Reduce crosstalk by keeping analog lines away from digital lines.

## Table 4. Unipolar Code Table (Gain = +1)

| DAC CONTENTS | | | ANALOG OUTPUT |
|---|---|---|---|
| MSB | | LSB | |
| 1111 | 1111 | 1111 | $+V_{REF}$ (4095/4096) |
| 1000 | 0000 | 0001 | $+V_{REF}$ (2049/4096) |
| 1000 | 0000 | 0000 | $+V_{REF}$ (2048/4096) = $+V_{REF}$ / 2 |
| 0111 | 1111 | 1111 | $+V_{REF}$ (2047/4096) |
| 0000 | 0000 | 0001 | $+V_{REF}$ (1/4096) |
| 0000 | 0000 | 0000 | 0V |

## Table 5. Bipolar Code Table (Gain = +1)

| DAC CONTENTS | | | ANALOG OUTPUT |
|---|---|---|---|
| MSB | | LSB | |
| 1111 | 1111 | 1111 | $+V_{REF}$ (2047/2048) |
| 1000 | 0000 | 0001 | $+V_{REF}$ (1/2048) |
| 1000 | 0000 | 0000 | 0V |
| 0111 | 1111 | 1111 | $-V_{REF}$ (1/2048) |
| 0000 | 0000 | 0001 | $-V_{REF}$ (2047/2048) |
| 0000 | 0000 | 0000 | $-V_{REF}$ (2048/2048) = $-V_{REF}$ |

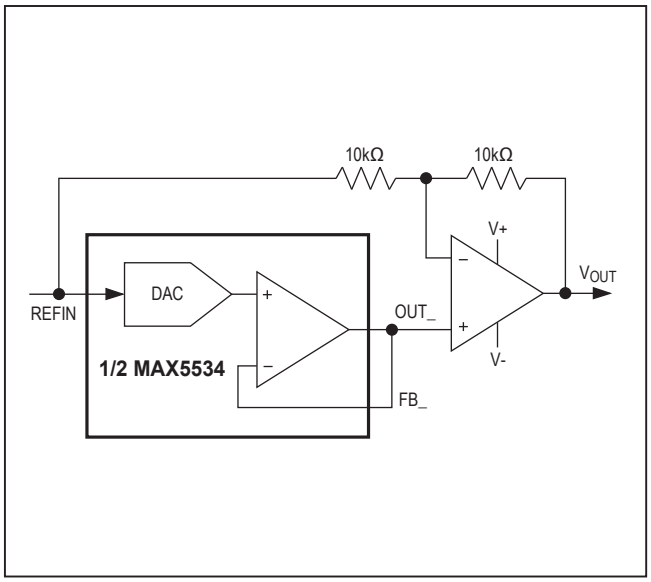



*Figure 7. Bipolar Output Circuit*

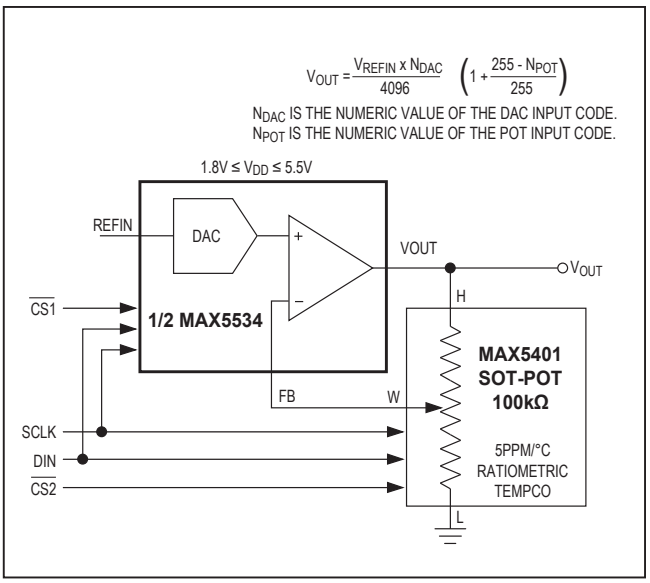



*Figure 9. Software-Configurable Output Gain*

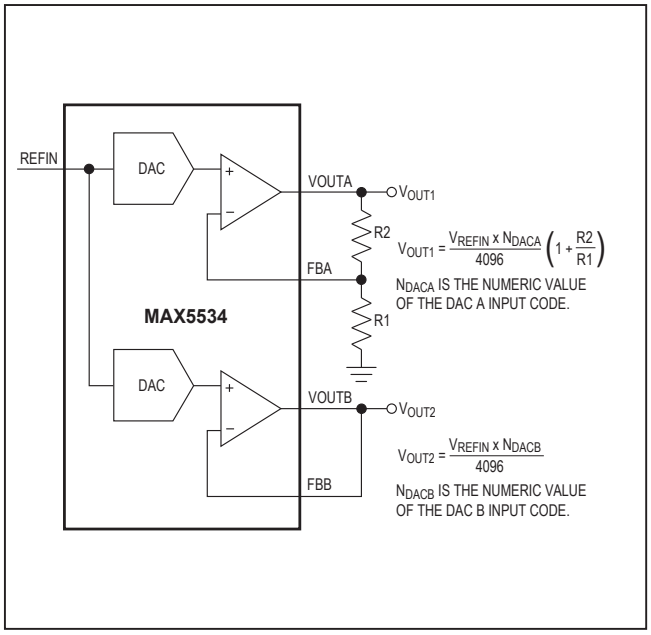



*Figure 8. Separate Force-Sense Outputs Create Unity and Greater-than-Unity DAC Gains Using the Same Reference*

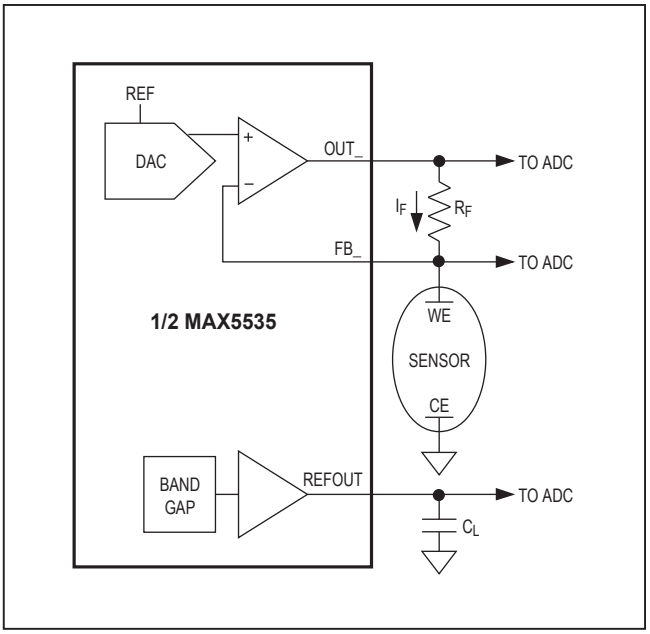



*Figure 10. Self-Biased Two-Electrode Potentiostat Application*

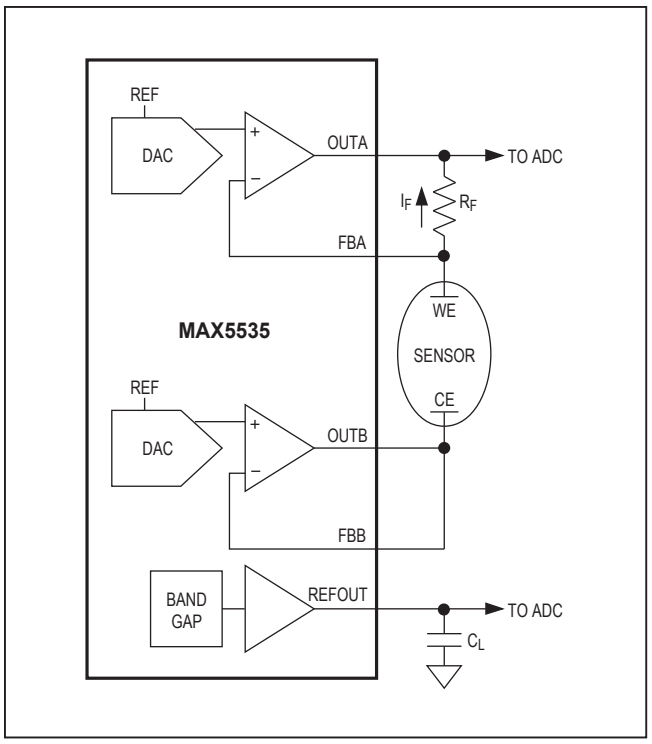
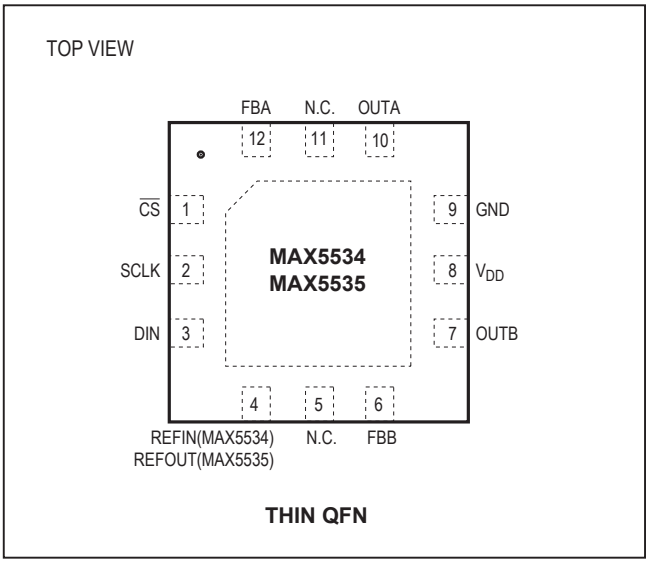



*Figure 11. Driven Two-Electrode Potentiostat Application*

## Pin Configurations (continued)



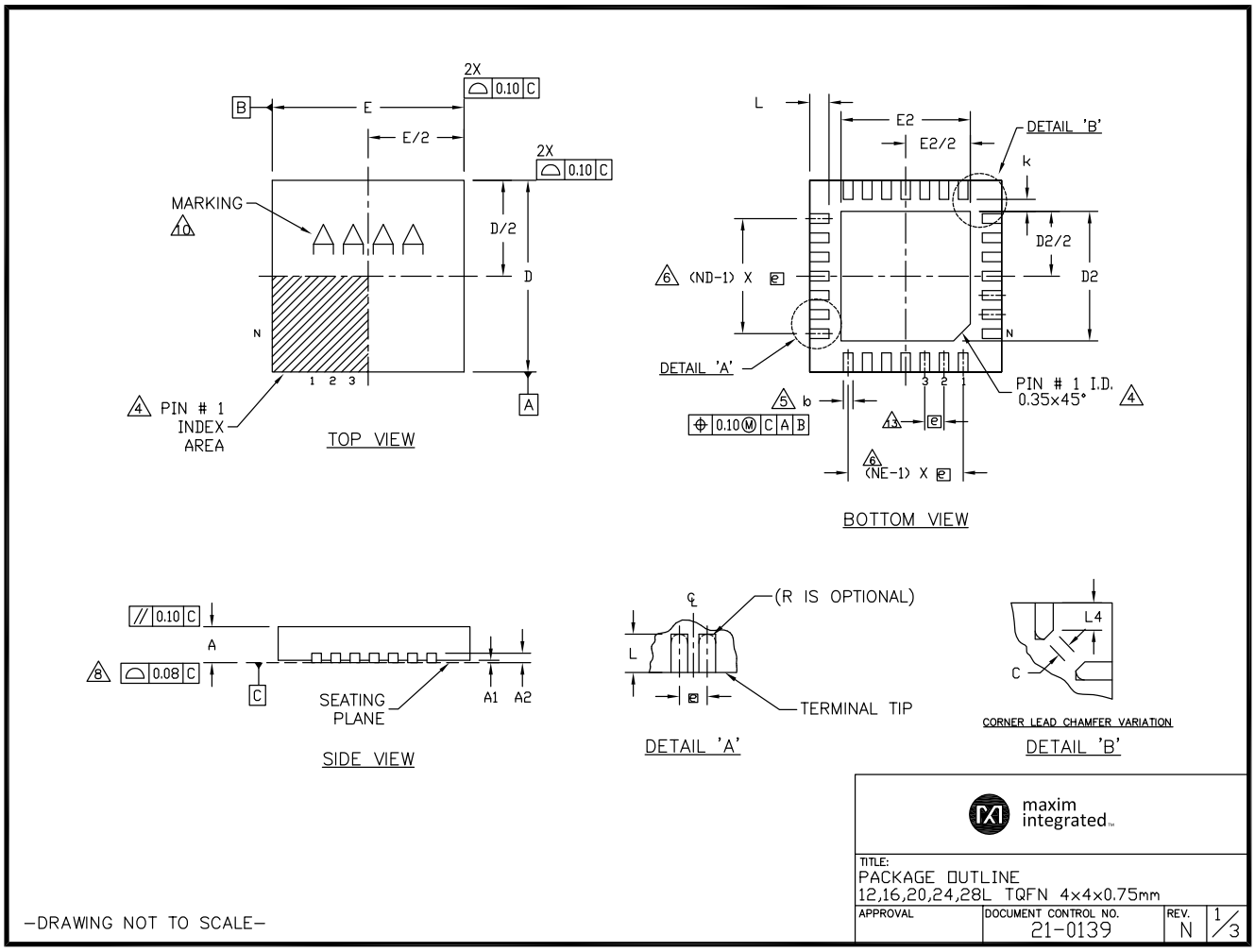

## Chip Information

TRANSISTOR COUNT: 10,688

PROCESS: BiCMOS

## Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



## Package Information (continued)

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**COMMON DIMENSIONS**

| PKG | 12L 4x4 | | | 16L 4x4 | | | 20L 4x4 | | | 24L 4x4 | | | 28L 4x4 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REF. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| A1 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 |
| A2 | 0.20 REF | | | 0.20 REF | | | 0.20 REF | | | 0.20 REF | | | 0.20 REF | | |
| b | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.20 | 0.25 | 0.30 | 0.18 | 0.23 | 0.30 | 0.15 | 0.20 | 0.25 |
| D | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 |
| E | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 |
| e | 0.80 BSC. | | | 0.65 BSC. | | | 0.50 BSC. | | | 0.50 BSC. | | | 0.40 BSC. | | |
| k | 0.25 | – | – | 0.25 | – | – | 0.25 | – | – | 0.25 | – | – | 0.25 | – | – |
| L | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 | 0.30 | 0.40 | 0.50 |
| N | 12 | | | 16 | | | 20 | | | 24 | | | 28 | | |
| ND | 3 | | | 4 | | | 5 | | | 6 | | | 7 | | |
| NE | 3 | | | 4 | | | 5 | | | 6 | | | 7 | | |
| Jedec Var. | WGGB | | | WGGC | | | WGGD-1 | | | WGGD-2 | | | WGGE | | |

**EXPOSED PAD VARIATIONS**

| PKG. CODES | D2 | | | E2 | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| T1244-3 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T1244-4 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T1644-3 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T1644-4 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T2044-2 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T2044-3 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T2444-2 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T2444-3 | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 |
| T2444-4 | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 |
| T2444-4C | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 |
| T2444N-4 | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 |
| T2444M-1 | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 |
| T2444MK-1 | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 |
| T2844-1 | 2.50 | 2.60 | 2.70 | 2.50 | 2.60 | 2.70 |
| T2844-1C | 2.50 | 2.60 | 2.70 | 2.50 | 2.60 | 2.70 |
| T2844N-1 | 2.65 | 2.70 | 2.75 | 2.65 | 2.70 | 2.75 |

**DIMENSION VARIATIONS**

| PKG. CODE | D2 | | | E2 | | | L | | | R (LEAD TIP RADIUS) |
|---|---|---|---|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | |
| T2044-4 | 2.85 | 2.90 | 2.95 | 2.85 | 2.90 | 2.95 | 0.25 | 0.30 | 0.35 | 0.125 REF |
| T2044-5 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 | 0.35 | 0.40 | 0.45 | 0.203 REF |

**CORNER LEAD CHAMFER VARIATION**

| PKG. CODES | C | L4 |
|---|---|---|
| T2444-2 | 0.120 X 45° REF | 0.31 REF |
| T2444-3 | 0.120 X 45° REF | 0.31 REF |
| T2444-4 | 0.120 X 45° REF | 0.31 REF |
| T2444-4C | 0.120 X 45° REF | 0.31 REF |
| T2444M-1 | 0.120 X 45° REF | 0.31 REF |
| T2444MK-1 | 0.120 X 45° REF | 0.31 REF |
| T2444N-4 | 0.120 X 45° REF | 0.31 REF |

maxim integrated

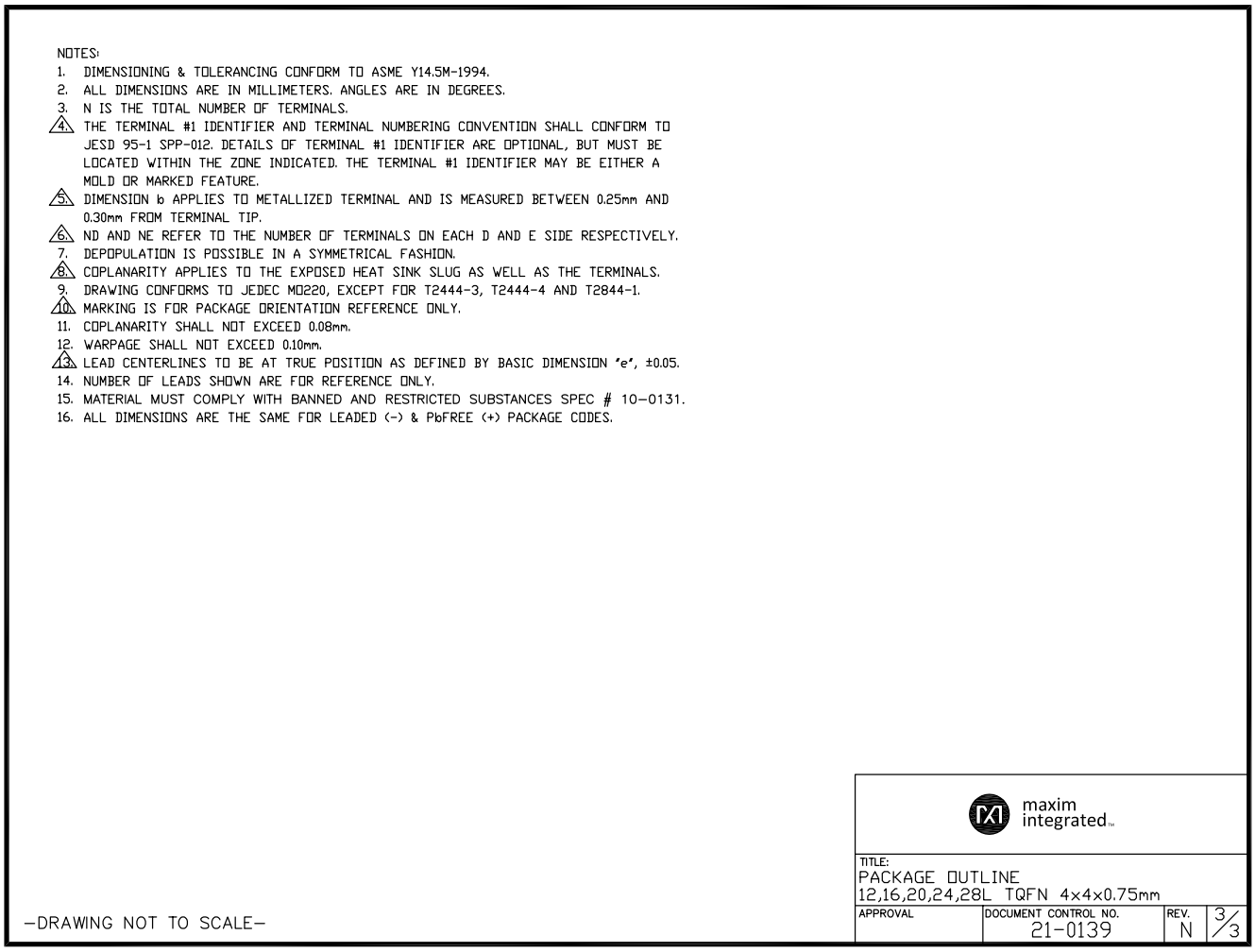
TITLE:
PACKAGE OUTLINE
12,16,20,24,28L TQFN 4x4x0.75mm

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0139 | N | 2/3 |

–DRAWING NOT TO SCALE–

## Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
16. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-

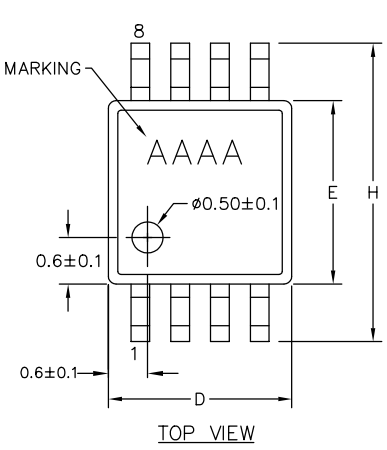
maxim integrated

TITLE:
PACKAGE OUTLINE
12,16,20,24,28L TQFN 4x4x0.75mm

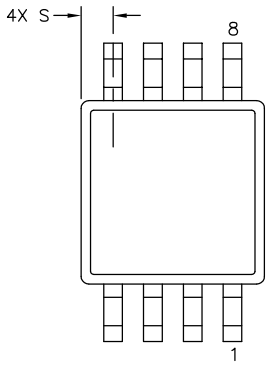
| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0139 | N | 3/3 |

## Package Information (continued)

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

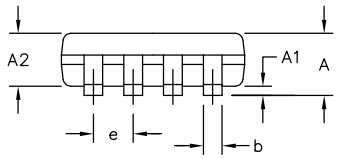



TOP VIEW

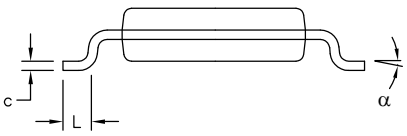



BOTTOM VIEW

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | – | 0.043 | – | 1.10 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| A2 | 0.030 | 0.037 | 0.75 | 0.95 |
| b | 0.010 | 0.014 | 0.25 | 0.36 |
| c | 0.005 | 0.007 | 0.13 | 0.18 |
| D | 0.114 | 0.122 | 2.90 | 3.10 |
| e | 0.0256 BSC | | 0.65 BSC | |
| E | 0.114 | 0.122 | 2.90 | 3.10 |
| H | 0.188 | 0.198 | 4.78 | 5.03 |
| L | 0.016 | 0.026 | 0.41 | 0.66 |
| α | 0° | 6° | 0° | 6° |
| S | 0.0207 BSC | | 0.5250 BSC | |
| PKG. CODES: U8–1; U8–3; U8CN–1 | | | | |




FRONT VIEW




SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COMPLIES TO JEDEC MO–187, LATEST REVISION, VARIATION AA.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (–) AND PbFREE (+) PKG. CODES.

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TITLE:
PACKAGE OUTLINE, 8L uMAX/uSOP

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21–0036 | L | 1/1 |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 1 | 1/07 | — | 1, 6, 14, 21, 24 |
| 2 | 3/20 | Changed DAC power-up time unit from µs to ms in the *Electrical Characteristics* table | 4 |

# Mouser Electronics

Authorized Distributor

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Maxim Integrated:

MAX5532EUA+ MAX5533EUA+ MAX5532EUA+T MAX5533EUA+T MAX5534ETC+ MAX5534ETC+T MAX5535ETC+ MAX5535ETC+T