MAX40662

Quad Transimpedance Amplifier with Input Current Clamp and Multiplexer for LiDAR

General Description

The MAX40662 is a 4-channel transimpedance amplifier for optical distance measurement receivers in light detection and ranging (LiDAR) applications. Low noise, high gain, low group delay, and fast recovery from overload make this quad TIA ideal for time-of-flight distance-measurement applications. The four input transimpedance stages are multiplexed to a pair of differential outputs. Important features include 2.1pA/√Hz input-referred noise density, an internal current input clamp (up to 2A for 10ns pulses), pin-selectable 25kΩ and 50kΩ transimpedance, and wide 440MHz bandwidth. An offset current input allows optional output offset adjustment to the output voltage. A low-power/standby mode can be used to help reduce average power supply current between pulses.

The MAX40662 is available in a 16-pin, 4mm x 4mm, TQFN package with side-wettable flanks and is specified over the -40°C to +125°C automotive operating temperature range.

Applications

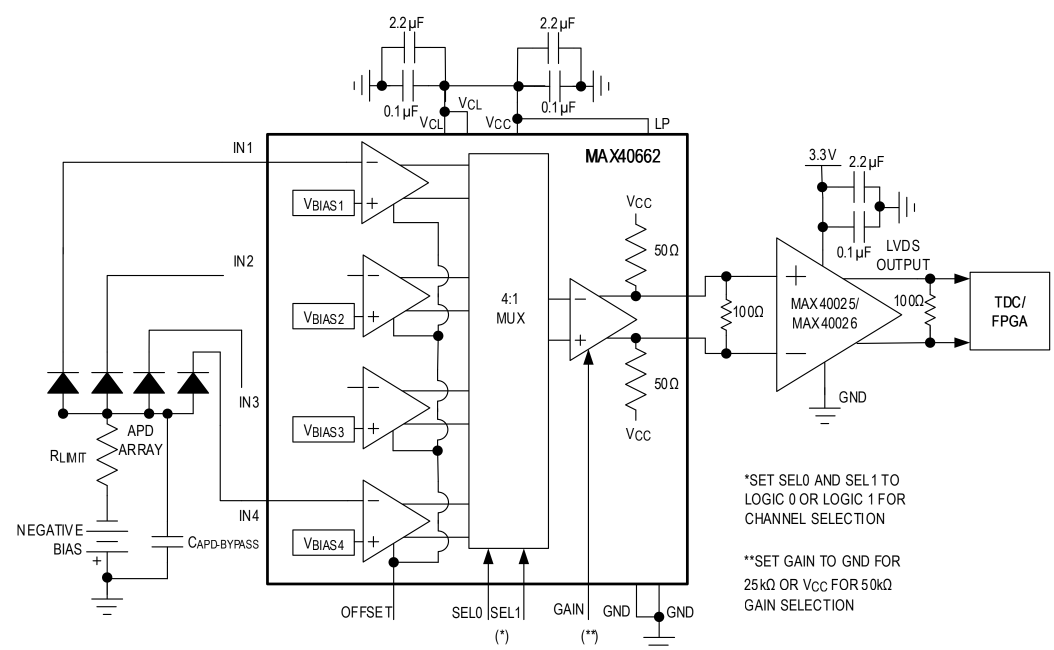
- Optical Time-of-Flight Distance Measurement
- LiDAR Receivers
- Automotive Driver Assistance Systems

Benefits and Features

- AEC-Q100
- Enables ASIL Compliance (FMEDA Available upon Request)
- Internal Multiplexer
- Bandwidth = 440MHz (typ), 300MHz (min)
- Low Noise: 2.1pA/√Hz
- Optimized for C_{IN} = 0.5pF to 5pF
- Two Pin-Selectable Transimpedance Values
  - 25kΩ
  - 50kΩ
- OFFSET Input Enables DC Offset Cancellation from Photodiode at IN_ Input
- LP Input Reduce Power Dissipation between Pulses
- Internal Clamps for Input Current up to 2A for 10ns Pulses
- 3.3V Operation
- 16-Pin, 4mm x 4mm TQFN Package with Side-Wettable Flanks

***Ordering Information** appears at end of data sheet.*

Typical Application Circuit



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Absolute Maximum Ratings

Supply Voltage .... -0.3V to +3.6V
Current into IN1, IN2, IN3, IN4 (10ns pulse width, 0.5% duty cycle) .... -2A
Current into IN1, IN2, IN3, IN4, OFFSET (Continuous) ....-0.4mA
Current into LP, Gain, SEL0, SEL1 (Continuous) ....-10mA to +10mA
Current into OUTP and OUTN (Continuous)..... -20mA to +20mA
Voltage at OUTN, OUTP .... V_{CC} + 0.3V
Voltage at OFFSET, LP ....-0.3V to V_{CC} + 0.3V
Operating Temperature Range ....-40°C to +125°C
Operating Junction Temperature Range (die) ....-40°C to +150°C
Storage Temperature Range ....-55°C to +150°C
Soldering Temperature (reflow) ....+260°C
Die Attach Temperature..+400°C
Continuous Power Dissipation (T_A = +125°C, derate 25mW/°C above +70°C (Multilayer Board)) 2000mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 TQFN

Package Code	T1644Y+5C
Outline Number	21-100204
Land Pattern Number	90-0070
Thermal Resistance, Four-Layer Board:	
Junction to Ambient ($θ_{JA}$)	42.71°C/W
Junction to Case ($θ_{JC}$)	4.67°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{CC} = +2.9V to +3.5V, V_{CL} = V_{CC}, 100Ω AC-coupled load between OUTN and OUTP, T_A = -40°C to +125°C, C_{IN} = 0.5pF (Note 1), Input current is defined as flowing out of IN_. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	I_{CC}	LP < 0.8V		21	27	mA
		LP > 2.0V		56	76	
Input Bias Voltage	V_{BIAS}	IN and OFFSET		0.86	1	V
Transimpedance Linearity		Applies to any selected input channel (Note 2)	-10	±2	+10	%
Transimpedance	Z_{21}	Applies to any selected input channel. GAIN = GND, I_{IN} < 2µA_{P-P}	18	25	32	kΩ
		Applies to any selected input channel. GAIN = V_{CC}, I_{IN} < 1µA_{P-P}	36	50	64	
Gain Switching Time	t_{G-SW}	GAIN = 25kΩ to 50kΩ		35		ns
OFFSET Input Transimpedance		GAIN = GND, I_{OFFSET} < 2µA_{P-P}	18	25	32	kΩ
		GAIN = V_{CC}, I_{OFFSET} < 1µA_{P-P}	36	50	64	
Overload Recovery Time		I_{IN} = 1mA		3		ns
		I_{IN} = 10mA		3		
		I_{IN} = 100mA		3		

Electrical Characteristics (continued)

(V_{CC} = +2.9V to +3.5V, V_{CL} = V_{CC}, 100Ω AC-coupled load between OUTN and OUTP, T_A = -40°C to +125°C, C_{IN} = 0.5pF (Note 1), Input current is defined as flowing out of IN_. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Logic 0	V_{IL}	GAIN, LP, SEL0, SEL1	0		0.8	V
Input Logic 1	V_{IH}	GAIN, LP, SEL0, SEL1	2.0		V_{CC}	V
Logic Input Current	I_{IL}	GAIN, LP, SEL0, SEL1		0.001	1.0	µA
	I_{IH}	GAIN, LP, SEL0, SEL1		0.001	1.0	
Standby Deassert Delay		Time from LP > V_{IL} to output common-mode voltage 90% of nominal value.		1		µs
Multiplexer Settling Time				20		ns
Output Common-Mode Voltage			V_{CC} - 1.15	V_{CC} - 0.78	V_{CC} - 0.45	V
Differential Output Offset	ΔV_{OUT}	I_{IN} = 0mA, GAIN = GND		-200		mV
		I_{IN} = 0mA, GAIN = V_{CC}		-400		
Output Impedance	Z_{OUT}	Single ended	40	50	60	Ω
Maximum Differential Output Voltage Swing	$V_{OUT(MAX)}$	I_{IN} = 0µA to -200µA pulse, GAIN = GND	475	880	1290	mV_{P-P}
		I_{IN} = 0µA to -200µA pulse, GAIN = V_{CC}	500	990	1490	
Input Resistance	R_{IN}	Small signal		98		Ω
Bandwidth	BW	GAIN = GND (Note 3)	300	420	540	MHz
		GAIN = V_{CC} (Note 3)	300	440	580	
Adjacent Channel Isolation		100MHz, I_{IN} = 2µA_{P-P}, GAIN = V_{CC}		45		dB
		100MHz, I_{IN} = 2µA_{P-P}, GAIN = GND		45		
Non-Adjacent Channel Isolation		100MHz, I_{IN} = 2µA_{P-P}, GAIN = V_{CC}		60		dB
		100MHz, I_{IN} = 2µA_{P-P}, GAIN = GND		60		
Input Noise Density		f = 10MHz		2.1		pA/√Hz
		f = 10MHz, C_{IN} = 5pF		2.5		
Output Noise Density		C_{IN} = 0.5pF, f = 10MHz, GAIN = GND		54		nV/√Hz
		C_{IN} = 0.5pF, f = 10MHz, GAIN = V_{CC}		92		
Output Integrated Noise		C_{IN} = 0.5pF, 0.1MHz to 100MHz, GAIN = GND		0.6		mV_{RMS}
		C_{IN} = 0.5pF, 0.1MHz to 100MHz, GAIN = V_{CC}		1.1		
		C_{IN} = 0.5pF, 0.1MHz to 200MHz, GAIN = GND		1		
		C_{IN} = 0.5pF, 0.1MHz to 200MHz, GAIN = V_{CC}		1.8		

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

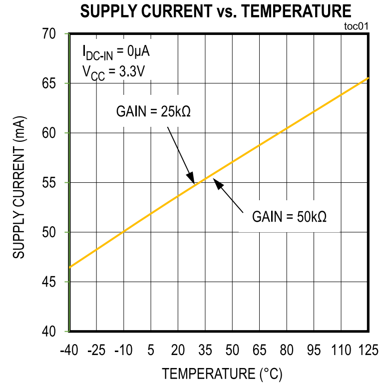
Note 2: Linearity is calculated as follows: For 25kΩ transimpedance, Linearity = (Large signal gain at 20µA – Large signal gain at 2µA)/Large signal gain at 2µA, where large signal gain at X is (V_{OUT} at I_IN = X - V_{OUT} at I_IN = 0). For 50kΩ transimpedance, Linearity = (Large signal gain at 10µA – Large signal gain at 1µA)/Large signal gain at 1µA, where large signal gain at X is (V_{OUT} at I_IN = X - V_{OUT} at I_IN = 0)

Note 3: -3dB bandwidth is measured relative to the gain at 10MHz.

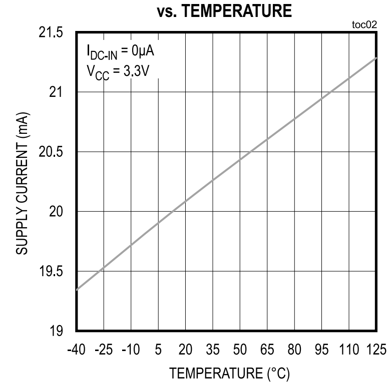
Typical Operating Characteristics

(V_{CC} = +3.3V, V_{CL} = V_{CC}, 100Ω AC-coupled load between OUTN and OUTP, T_A = +25°C, C_{IN} = 0.5pF)

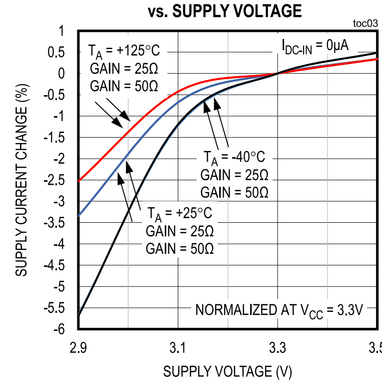
SUPPLY CURRENT vs. TEMPERATURE



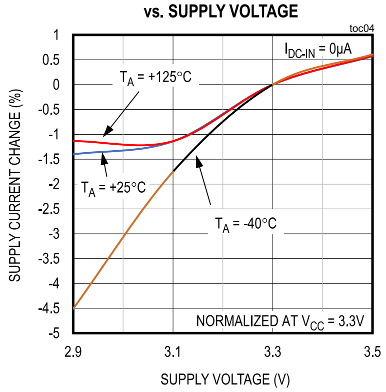
LOW-POWER STANDBY SUPPLY CURRENT vs. TEMPERATURE



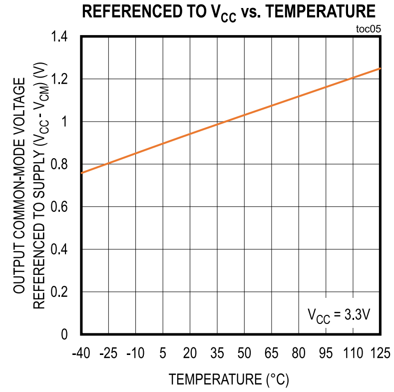
ACTIVE SUPPLY CURRENT vs. SUPPLY VOLTAGE



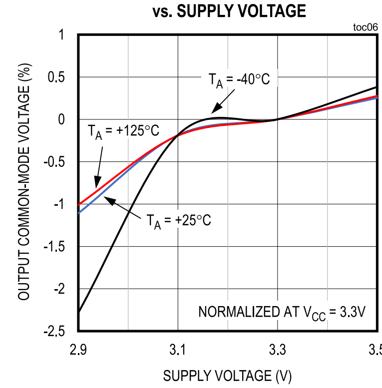
LOW-POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE



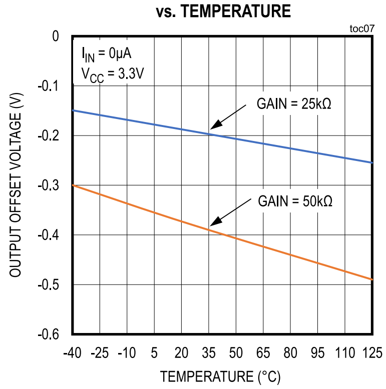
OUTPUT COMMON-MODE VOLTAGE REFERENCED TO V_{CC} vs. TEMPERATURE



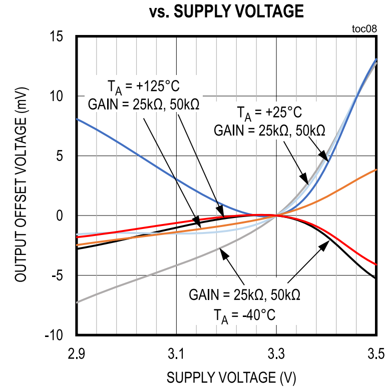
OUTPUT COMMON-MODE VOLTAGE vs. SUPPLY VOLTAGE



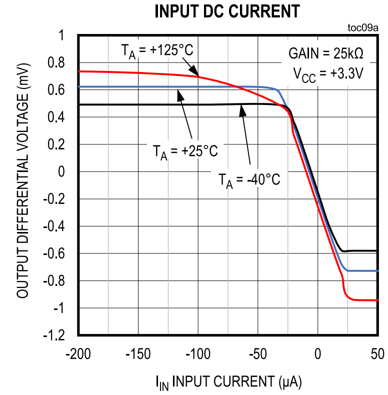
OUTPUT OFFSET VOLTAGE vs. TEMPERATURE



OUTPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE

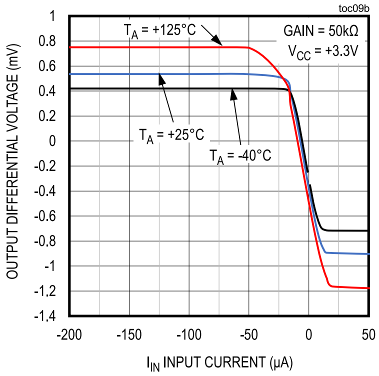


OUTPUT DIFFERENTIAL VOLTAGE vs. INPUT DC CURRENT

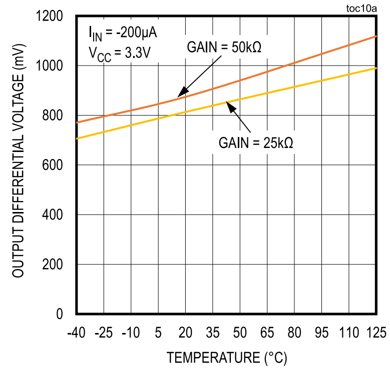


Typical Operating Characteristics (continued)

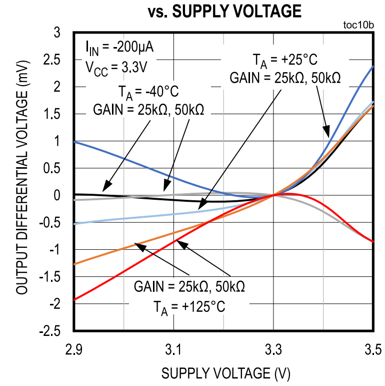
(V_{CC} = +3.3V, V_{CL} = V_{CC}, 100Ω AC-coupled load between OUTN and OUTP, T_A = +25°C, C_{IN} = 0.5pF)



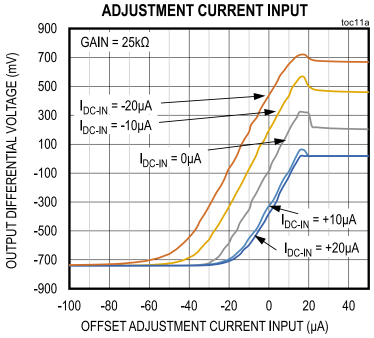
OUTPUT DIFFERENTIAL VOLTAGE vs. INPUT DC CURRENT



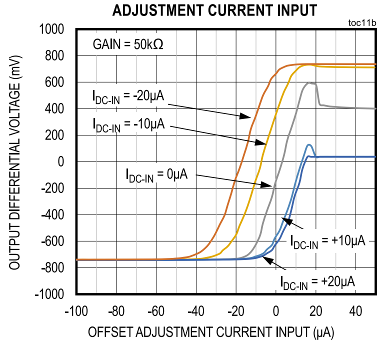
OUTPUT DIFFERENTIAL VOLTAGE vs. TEMPERATURE



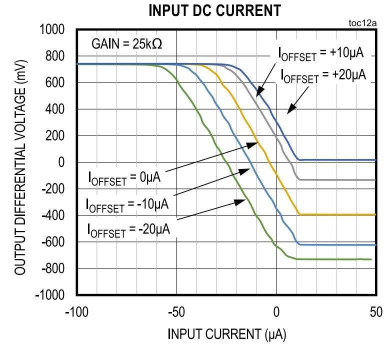
OUTPUT DIFFERENTIAL VOLTAGE vs. SUPPLY VOLTAGE



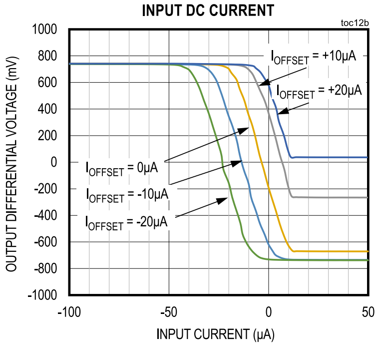
OUTPUT DIFFERENTIAL VOLTAGE vs. OFFSET ADJUSTMENT CURRENT INPUT



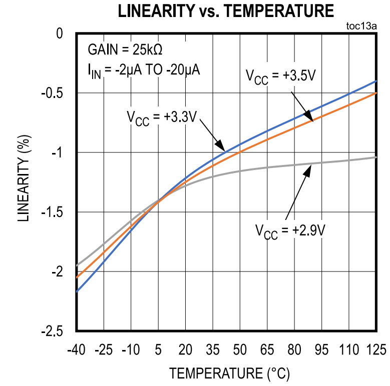
OUTPUT DIFFERENTIAL VOLTAGE vs. OFFSET ADJUSTMENT CURRENT INPUT



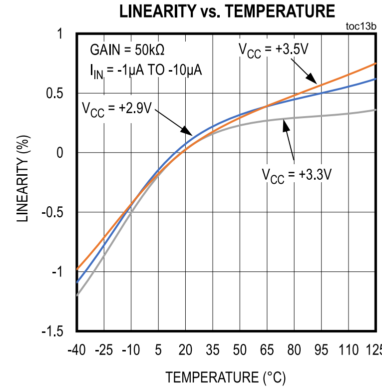
OUTPUT DIFFERENTIAL VOLTAGE vs. INPUT DC CURRENT



OUTPUT DIFFERENTIAL VOLTAGE vs. INPUT DC CURRENT



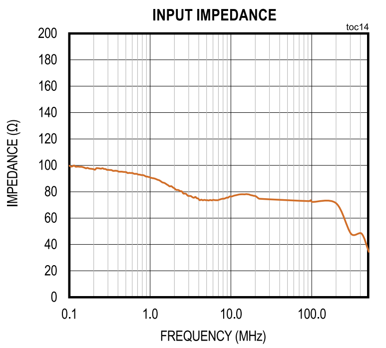
LINEARITY vs. TEMPERATURE

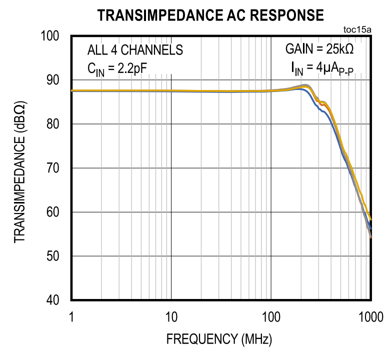


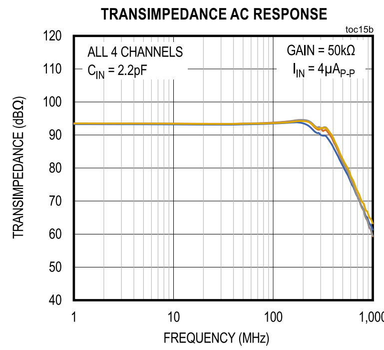
LINEARITY vs. TEMPERATURE

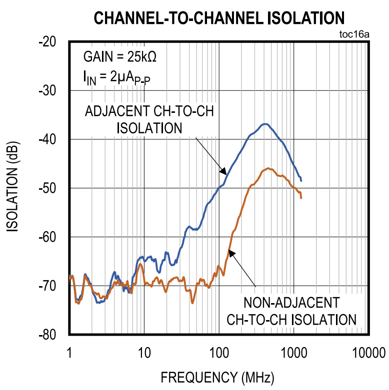
Typical Operating Characteristics (continued)

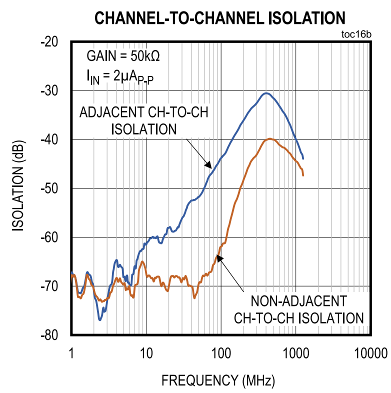
(V_{CC} = +3.3V, V_{CL} = V_{CC}, 100Ω AC-coupled load between OUTN and OUTP, T_A = +25°C, C_{IN} = 0.5pF)

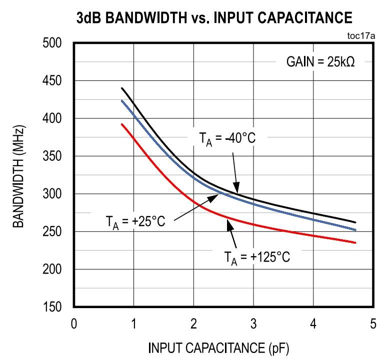


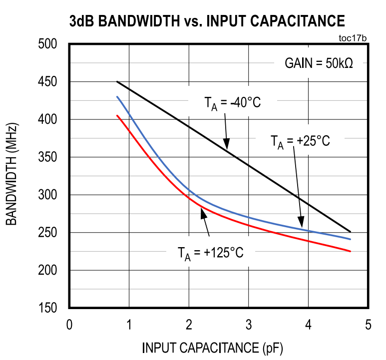


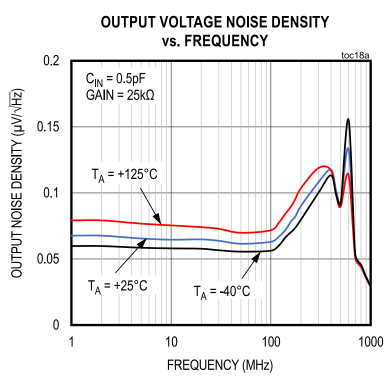


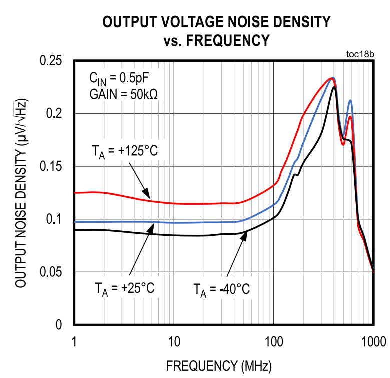






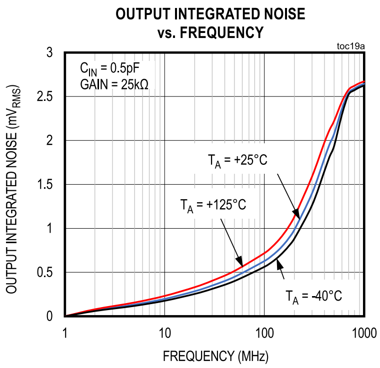


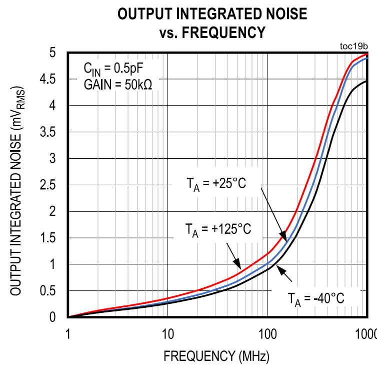


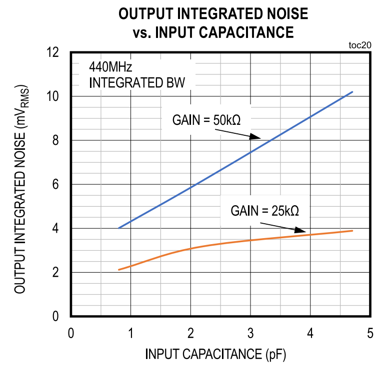


Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_{CL} = V_{CC}, 100Ω AC-coupled load between OUTN and OUTP, T_A = +25°C, C_{IN} = 0.5pF)

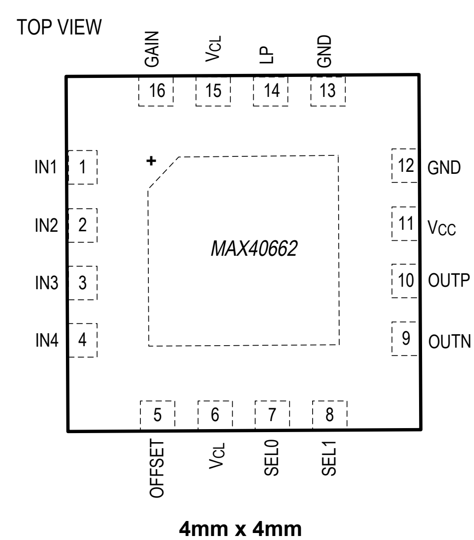






Pin Configuration

TQFN



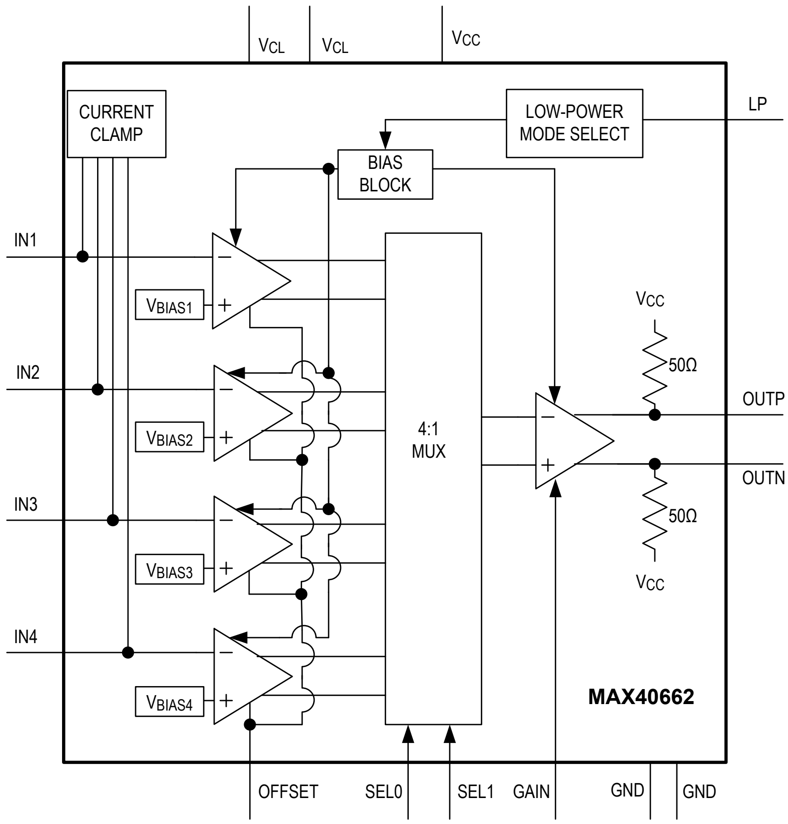
Pin Description

PIN	NAME	FUNCTION
1	IN1	Channel 1 Signal Input. Connect to photodiode anode.
2	IN2	Channel 2 Signal Input. Connect to photodiode anode.
3	IN3	Channel 3 Signal Input. Connect to photodiode anode.

Pin Description (continued)

PIN	NAME	FUNCTION
4	IN4	Channel 4 Signal Input. Connect to photodiode anode.
5	OFFSET	Offset Adjustment Input. Draw current from this input to adjust the effective input offset current for all the channels that alter output offset voltage.
6, 15	V_{CL}	Power Supply Connection for Input Current Clamp. Connect to V_{CC}.
7	SEL0	Channel Select Input. Use SEL0 and SEL1 to select the active channel as shown in the *Multiplexer* section.
8	SEL1	Channel Select Input. Use SEL0 and SEL1 to select the active channel as shown in the *Multiplexer* section.
9	OUTN	Negative 50Ω Output. Increasing input current causes OUTN voltage to decrease.
10	OUTP	Positive 50Ω Output. Increasing input current causes OUTP voltage to increase.
11	V_{CC}	+3.3V Supply Voltage
12, 13	GND	Circuit Ground
14	LP	Enable/Low-Power Input. Logic-high = normal operation. Logic-low = low-power standby.
16	GAIN	Gain Select Input. Connect to GND for gain = 25kΩ; connect to V_{CC} for gain = 50kΩ.
EP	EP	Exposed Pad (GND). This pad must be connected to ground.

Functional Diagram



Detailed Description

Operation

A typical TIA amplifies the current out of the photodiode (APD) by letting it pass into its input and through a feedback resistor, but the MAX40662 provides current out of the IN pins when the APD is reverse-biased and under optical illumination. When an APD with a negative bias voltage is connected to one of the four TIA inputs, the signal current flows out of the amplifier's summing node. The input current flows through an internal load resistor to develop a voltage.

An internal clamp circuit protects against input currents as high as 2A for a 10ns pulse at 0.5% duty cycle. (Longer pulses or higher duty cycles will reduce this value.) The clamp circuit also maintains very fast overload recovery times (about 2ns) for input currents up to 100mA (see the *Block Diagram*).

Gain Stages

Each input stage has a transimpedance of 12.5kΩ. The input stage outputs are then applied to the input of the multiplexer, and the selected output signal is then applied to the input of the second stage.

The second gain stage post multiplexer provides additional gain of 4 or 2 depending on the logic level on GAIN pin and converts the selected transimpedance amplifier's single-ended output into a differential signal. This stage is designed to drive a 100Ω differential load between OUT+ and OUT-. For optimum supply noise rejection, the outputs should be terminated with differential loads. The single-ended outputs do not drive a DC-coupled grounded load. The outputs should be AC-coupled or terminated to V_{CC}. If a single-ended output is required, both the used and unused outputs should be terminated in a similar manner.

Inputs to TIA

The MAX40662 input structure is designed in such a way that any optical illumination with proper biasing on the APD would allow current to flow out of the IN pins into the respective APDs. Each input pin has an internal DC bias of 0.86V on it.

OFFSET Inputs

The OFFSET pin is an input pin. The offset input current for any channel, I_{OFFSET}, is the current flowing from the OFFSET pin. This current affects the TIA's output voltage with a polarity opposite that of the current flowing from IN, so it may be used to effectively apply an offset to the output voltage. The OFFSET pin is biased internally to the same voltage as the IN_ pins at 0.86V.

Multiplexer

The SEL1 and SEL0 logic inputs select the input channel whose output will be passed to the second gain stage. The active channel is selected as shown in the following table.

Table 1. Channel Selection Using SEL1 and SEL0

SEL1:SEL0	SELECTED INPUT CHANNEL
00	1
01	2
10	3
11	4

LP Input

The low power (LP) input accepts a logic signal that can be used to put the circuit into a low-power mode, thereby reducing the supply current from 56mA to 21mA (typ). Driving this input with a logic-high enables the circuit, while a logic-low disables the circuit and places it into the low-power mode.

Applications Information

Photodiode

Noise performance and bandwidth are adversely affected by capacitance on a TIA's input node. Although the MAX40662 is less sensitive than most TIAs to input capacitance, it is good practice to minimize any unnecessary capacitance. The MAX40662 is optimized for 0.5pF to 5pF of capacitance on the input. Selecting low-capacitance photodiodes helps to minimize the total input capacitance on the input pin. Assembling the TIA in die form using chip and wire technology provides the lowest capacitance inputs and the best possible performance.

Supply Filter

Sensitive optical receivers require wideband power supply decoupling. Power supply bypassing should provide low impedance between V_{CC} and ground for frequencies between 10kHz and 700MHz. Isolate the amplifiers from noise sources with LC supply filters and shielding.

Place a supply filter as close to the MAX40662 supply pin as possible, and it is a good practice to use multiple bypass capacitors like 100pF, 2.2nF, and 1µF in parallel.

AC or DC-Coupling on Input

Coupling choice of electrical signal from APD to the TIA is a major design decision a system designer has to make based on the trade-offs.

The DC-coupled input design, as shown in Figure 1, is the least complicated and takes minimum number of components that serves best in saving PCB space and cost. In DC-coupled mode, input channel switching times are rapid on the order of <20ns and saturation recovery times are minimal. However, photodiode dark currents and ambient light DC components will be fed to the output of the TIA.

For that reason, AC-coupling on the input, as shown in Figure 2, is preferred to block DC components and preserve dynamic range of the TIA. However, in AC-coupled mode, there is additional delay in channel switching time depending on the value of input capacitor as that introduces RC delay. Channel switching also introduces multiplexer switching glitch, and the input signal cannot be read until this switch glitch is settled. An AC-coupling capacitor of 100pF is a good starting point and can be adjusted based on timing requirements of the design.

Input Capacitance and Its Effect

In TIAs, bandwidth, noise, and rise time of the output pulse depend on the input capacitance presented by the APD. The more the capacitance on the input, noise increases, bandwidth and the output pulse rise time reduces. As a result, an APD with a smaller input capacitance need to be chosen and also the input's trace parasitic capacitance need to be minimized.

The MAX40662 has a unique architecture that does not have a huge effect on the bandwidth based on the input capacitance, but the noise goes up and output pulse rise time slows down as expected. From the bandwidth information shown in *Typical Operating Characteristics* section, one can estimate output rise time for a given input capacitance from the below relationship:

$$t_R = 0.35/BW$$

As a result of preserving higher bandwidth compared to a traditional TIA at higher input capacitance, integrated output noise of the MAX40662 output is slightly higher due to having wide bandwidth output signal.

Input Dynamic Range of MAX40662

The MAX40662 offers linear input current range of 40µA and 20µA for 25kΩ and 50kΩ transimpedance settings, respectively. Input currents any higher would saturate the output and will have no pulse stretching for currents all the way till 100mA. Each input has an independent current clamps that can handle current as high as 100mA. Input current as high as 2A is also supported, but at 10ns pulse width and 0.5% duty cycle.

Layout Considerations

Some critical layout guidelines are listed below:

- A differential microstrip is the recommended layout for MAX40662 outputs with terminations close to the outputs. Care must be taken to avoid unwanted stubs by removing ground below the traces that are not part of the 50Ω termination line leading into input pins. The parasitic capacitance created between traces and ground slow down and even distort the signals by creating reflections on the path.
- The input trace connecting the photodiode to IN_ of the MAX40662 should be as short as possible and have ground etched/removed underneath. This will reduce/avoid unwanted parasitic capacitance created in the PCB. Having longer trace lengths will increase the parasitic inductance in signal trace paths.
- As there ought to be four input traces in design, it is critical to include a ground isolation between them to minimize channel-to-channel coupling.
- Use a PCB with a low-impedance ground plane.
- Mount one or more 10nF ceramic capacitors between GND and V_{CC} as close to the pins as possible. Multiple bypass capacitors help to reduce the effect of trace impedance and capacitor ESR.
- Choose bypass capacitors for minimum inductance and ESR.
- Use a 100Ω termination resistor for the output connected directly between OUTP and OUTN after the AC-coupling capacitors, if practical. If the destination inputs cannot be located adjacent to the outputs, use a 100Ω microstrip between the output pins and the termination resistor, which should be close to the inputs of the destination component. This will avoid the creation of stub beyond the termination resistor, which will cause reflections. The added length of the differential trace has less degrading effects than added stub length.
- Minimize any parasitic layout inductance.
- It is recommended to use higher performance substrate materials (e.g., Rogers).

Slew Rate on the Supply Ramp

The ramp rate of the supply needs to be 50μs or more to make sure the core clamp is not triggered during power-up. If the supply ramp is faster than 50μs, then the core clamp triggers and there will be excess current consumption for about 6μs.

Typical Application Circuits

DC-Coupled Receiver

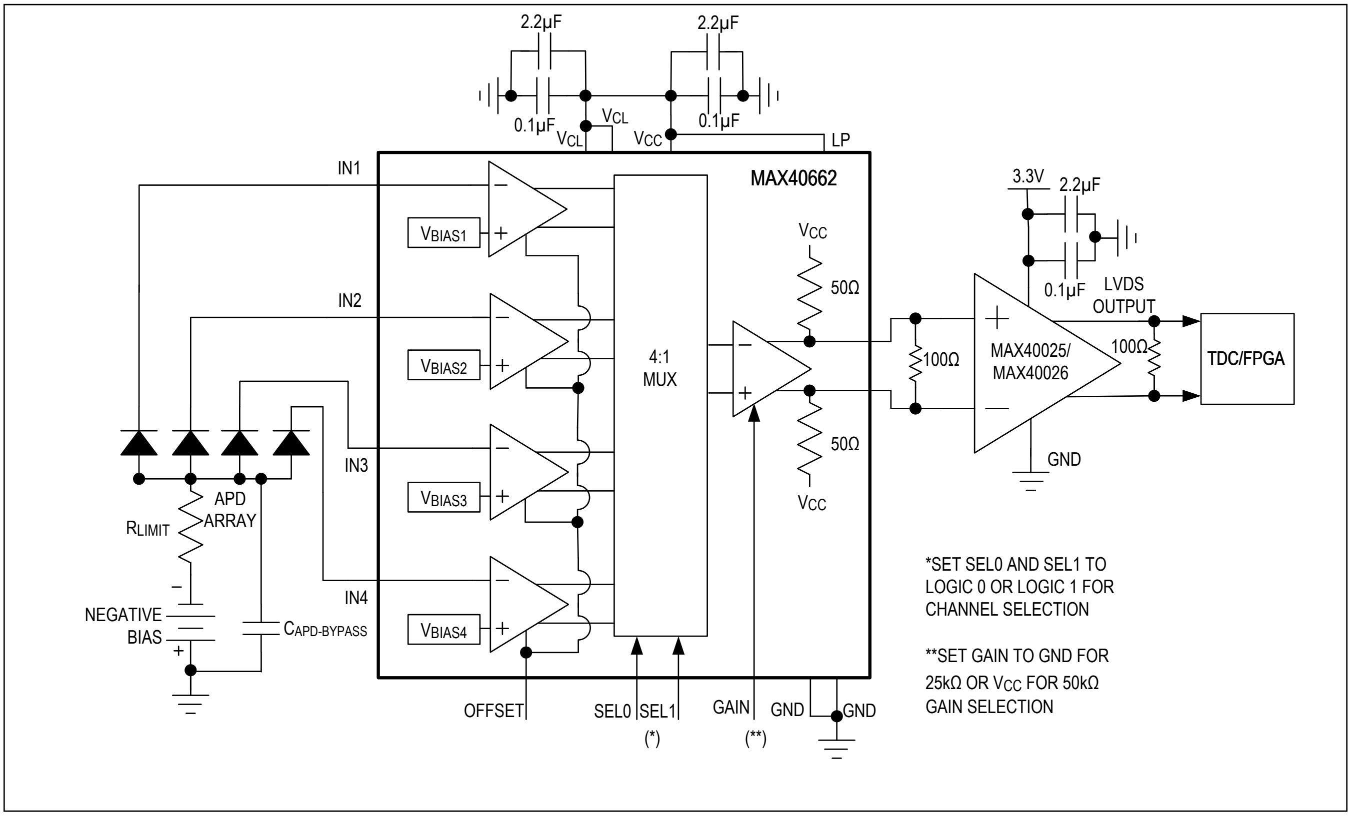


Figure 1. Typical Application with DC-Coupled Negative Bias APD Receiver TIA

In Figure 1, a typical application circuit with the MAX40662 is shown in DC-coupled mode with negative bias on APD.

A 4-APD array in a receiver is shown for simplicity to match the 4-channel inputs on the MAX40662. In reverse-bias condition, based on the amount of light incident on the APDs, current flows out of the IN pin of the TIA and flows through the respective APD.

R_{LIMIT} helps in limiting the AC currents through the APD under extreme optical illumination and at the same time isolates the high negative bias voltage on the input pins of the MAX40662 in case of a short fault on the APD.

The DC-coupled and negative bias APD receiver test setup shown in Figure 1 is the most convenient setup, as it requires the least amount of components and, at the same time, provides rapid saturation recovery time and faster channel switching through the 4:1 multiplexer.

Typical Application Circuits (continued)

AC-Coupled Negative Bias APD Receiver TIA

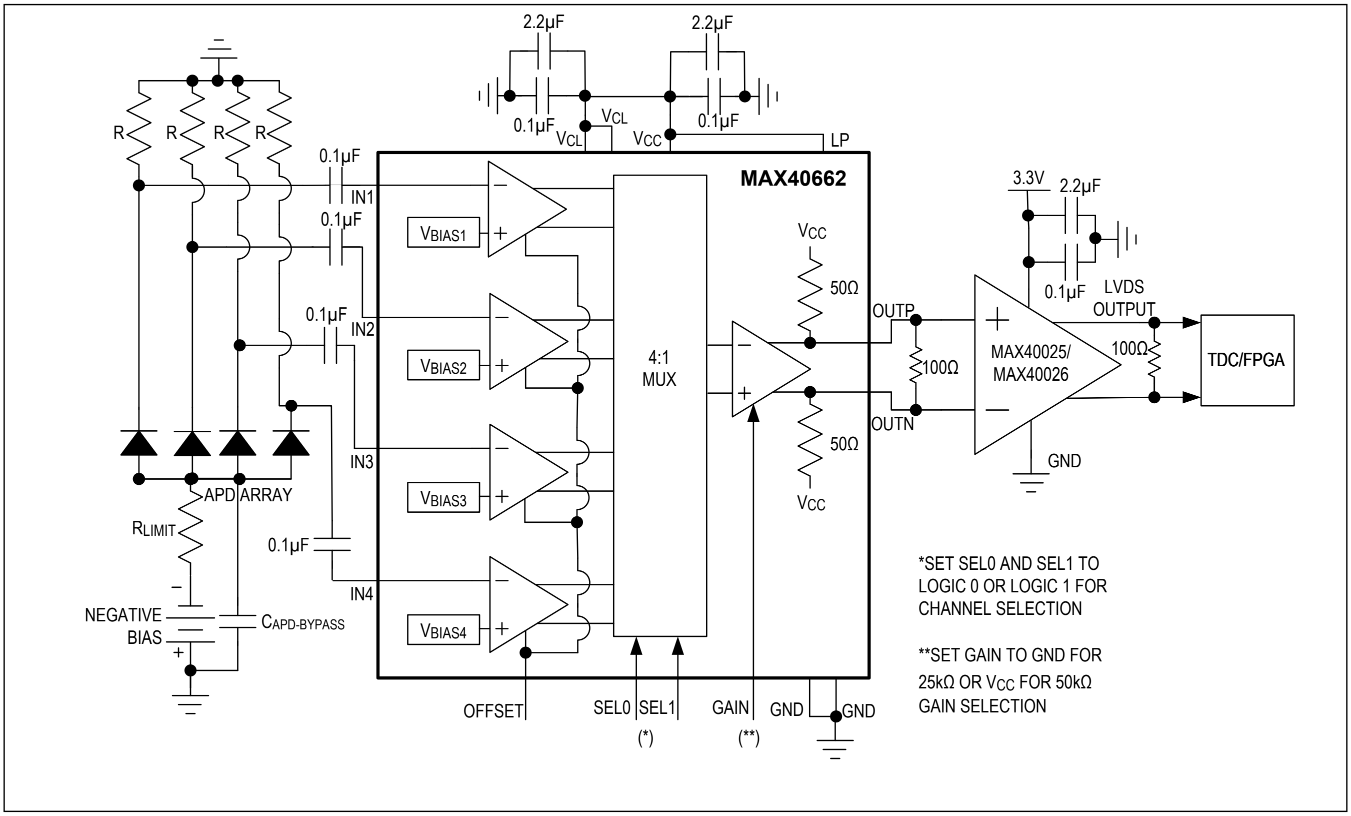


Figure 2. AC-Coupled Negative Bias APD Receiver TIA

In Figure 2, a typical application circuit with the MAX40662 is shown in AC-coupled mode with negative bias on the APD.

A 4-APD array in a receiver is shown for simplicity to match the 4-channel inputs on the MAX40662. In a reverse-bias condition, based on the amount of light incident on the APDs, current flows out of the IN pin of the TIA and flows through the respective APD. Four resistors on each APD cathode establish a DC-biasing point to the APD, as there are DC-blocking capacitors on the inputs of TIA.

R_{LIMIT} helps in limiting the AC currents through the APD under extreme optical illumination. In terms of sizing the biasing resistor vs. R_{LIMIT}, it must be experimented during prototype stage based on the application requirement as biasing resistors and input-coupling capacitors form an RC time constant. Also, R_{LIMIT} needs to be much smaller compared to the biasing resistor in order to provide a low impedance path for AC currents to flow through the APDs.

Typical Application Circuits (continued)

AC-Coupled Positive Bias APD Receiver TIA

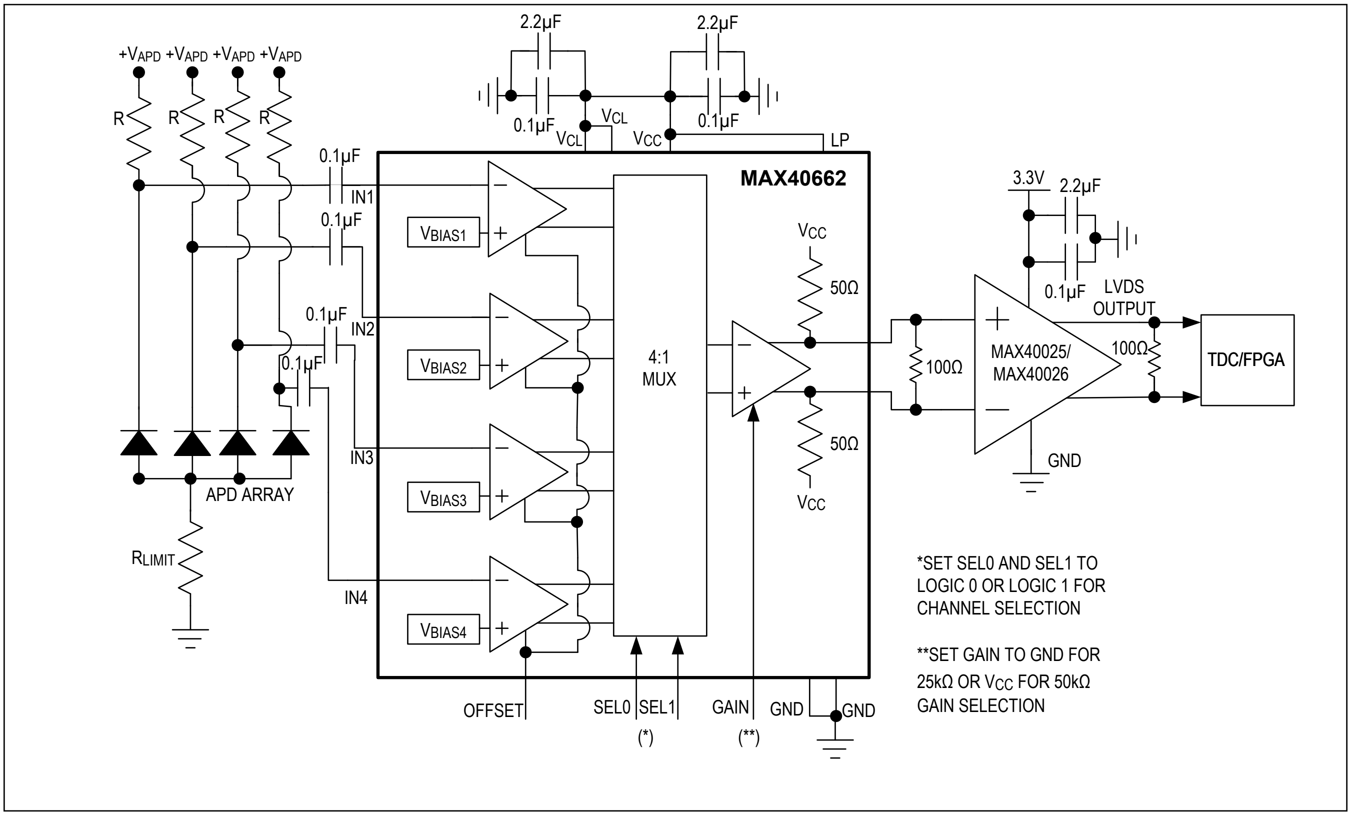


Figure 3. AC-Coupled Positive Bias APD Receiver TIA

In Figure 3, a typical application circuit with the MAX40662 is shown in AC-coupled mode with positive bias on the APD. This setup is mainly preferred if there is no negative bias available in the system.

A 4-APD array in a receiver is shown for simplicity to match the 4-channel inputs on the MAX40662. In reverse-bias condition, based on the amount of light incident on the APDs, current flows out of the IN pin of the TIA and flows through the respective APD. Four resistors on each APD cathode establish a DC-biasing point to the APD, as there are DC-blocking capacitors on the inputs of the TIA.

R_{LIMIT} helps in limiting the AC currents through the APD under extreme optical illumination. In terms of sizing the biasing resistor vs R_{LIMIT}, it must be experimented during prototype stage based on the application requirement as biasing resistors and input-coupling capacitors form an RC time constant. Also, R_{LIMIT} needs to be much smaller compared to the biasing resistor in order to provide a low-impedance path for the AC currents to flow through the APDs.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE	TOP MARK
MAX40662ATE/VY+T	-40°C to +125°C	16 TQFN	MAX40662A E/V YWW NEAA +

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape-and-reel.

/V Denotes an automotive-qualified part.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/20	Initial release	—
1	9/20	Added TOCs	9, 10, 11