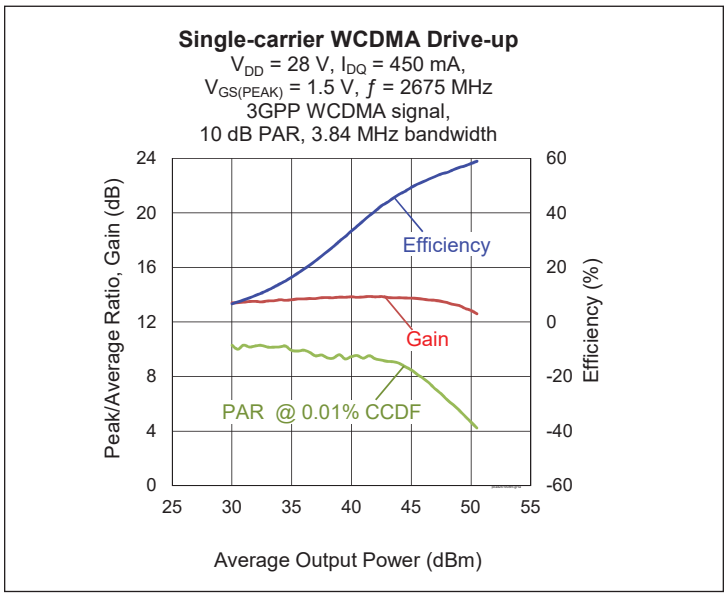
PXAE261908NF

Thermally-Enhanced High Power RF LDMOS FET
240 W, 28 V, 2515 – 2675 MHz

Description

The PXAE261908NF is a 240-watt (P_{3dB}) LDMOS FET intended for use in multi-standard cellular power amplifier applications in the 2515 to 2675 MHz frequency band. Features include input and output matching, high gain and a thermally-enhanced package with earless flange. Manufactured with an advanced LDMOS process, this device provides excellent thermal performance and superior reliability.

PXAE261908NF
Package PG-HBSOF-6-3



Features

- Broadband internal input and output matching
- Asymmetric Doherty design
  - Main: P_{3dB} = 90 W typical
  - Peak: P_{3dB} = 180 W typical
- Typical pulsed CW performance, 2675 MHz, 28 V
  - Output power at P_{1dB} = 51 W
  - Output power at P_{3dB} = 240 W
  - Gain = 11.8 dB
  - Efficiency = 60%
- Capable of handling 10:1 VSWR at 28 V, 32 W (CW) output power
- Integrated ESD protection
- Human Body Model, Class 2 (per ANSI/ESDA/JEDEC JS-001)
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in the Doherty test fixture)
V_{DD} = 28 V, I_{DQ} = 450 mA, $V_{GS(PEAK)}$ = 1.5 V, P_{OUT} = 32 W avg, f = 2675 MHz, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	12.8	13.5	—	dB
Drain Efficiency	η_D	45	47.5	—	%
Adjacent Channel Power Ratio	ACPR	—	–28	–26	dBc
Output PAR at 0.01% probability on CCDF	OPAR	7.6	8	—	dB

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RoHS compliant

Rev. 04, 2023-07-24

DC Characteristics

Characteristic		Conditions	Symbol	Min	Typ	Max	Unit
Drain-source Breakdown Voltage		V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current		V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1	µA
		V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10	µA
Gate Leakage Current		V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1	µA
On-state Resistance	(main)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.08	—	Ω
	(peak)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.03	—	Ω
Operating Gate Voltage	(main)	V_{DS} = 28 V, I_{DQ} = 450 mA	V_{GS}	2.7	3	3.3	V
	(peak)	V_{DS} = 28 V, I_{DQ} = 0 mA	V_{GS}	—	1.5	—	V

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	65	V
Gate-source Voltage	V_{GS}	–6 to +10	V
Operating Voltage	V_{DD}	0 to +32	V
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C

Thermal Characteristics

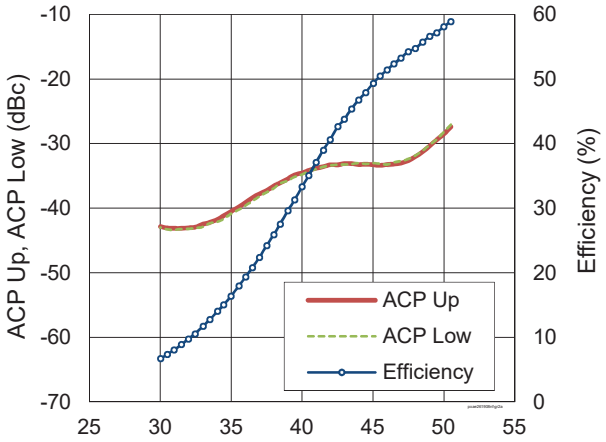
Characteristic		Symbol	Value	Unit
Thermal Resistance	(main, T_{CASE} = 70°C, 32 W CW)	$R_{\theta JC}$	0.96	°C/W
	(peak, T_{CASE} = 70°C, 56 W CW)	$R_{\theta JC}$	0.36	°C/W

Ordering Information

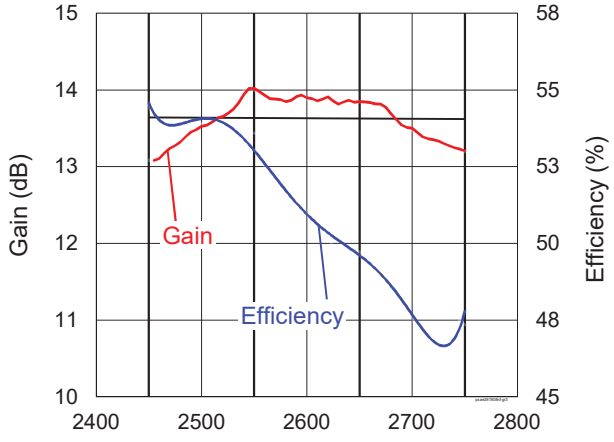
Type and Version	Order Code	Package	Shipping
PXAE261908NF V1 R5	PXAE261908NF-V1-R5	PG-HBSOF-6-3	Tape & Reel, 500 pcs

Typical Performance (data taken in the production test fixture)

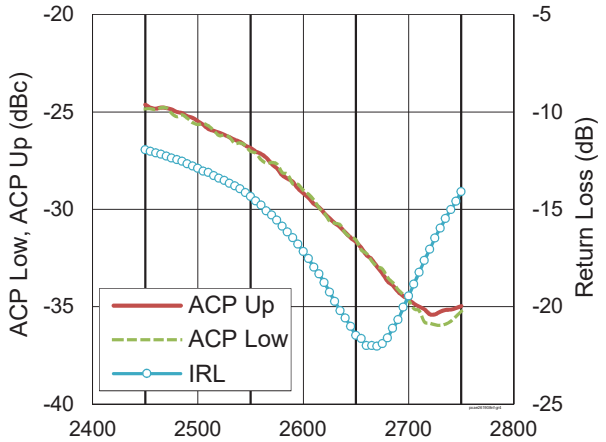
Single-carrier WCDMA Drive-up
V_{DD} = 28 V, $I_{DQ(MAIN)}$ = 450 mA,
$V_{GS(PEAK)}$ = 1.5 V, f = 2675 MHz
3GPP WCDMA signal,
10 dB PAR, 3.84 MHz bandwidth



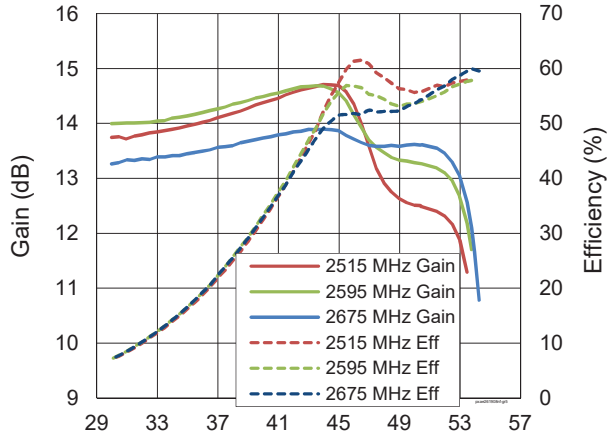
Single-carrier WCDMA Broadband
V_{DD} = 28 V, I_{DQ} = 450 mA,
$V_{GS(PEAK)}$ = 1.5 V P_{OUT} = 45.05 dBm,
3GPP WCDMA signal
10 dB PAR, 3.84 MHz bandwidth



Single-carrier WCDMA Broadband
V_{DD} = 28 V, I_{DQ}= 450 mA,
$V_{GS(PEAK)}$ = 1.5 V, P_{OUT} = 45.05 dBm,
3GPP WCDMA signal
10 dB PAR, 3.84 MHz bandwidth

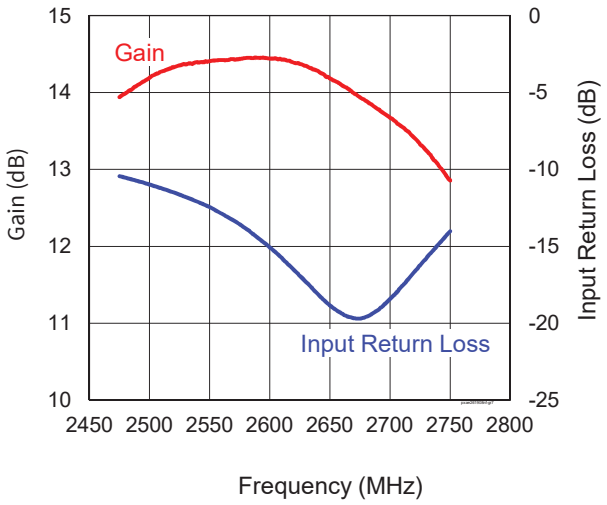


Pulsed CW Performance
V_{DD} = 28 V, I_{DQ} = 450 mA, $V_{GS(PEAK)}$ = 1.5 V

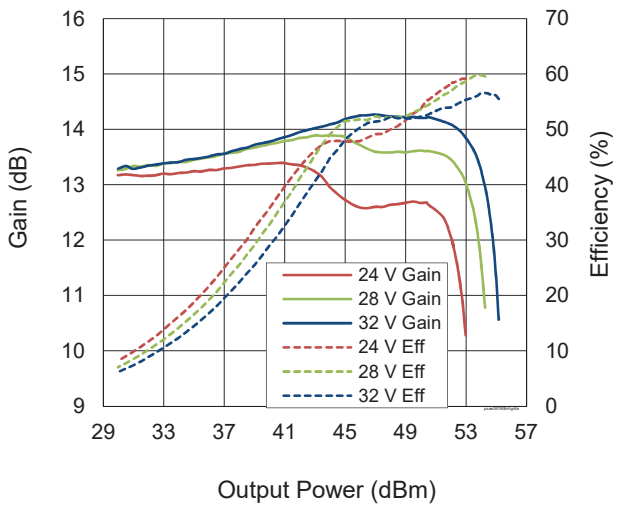


Typical Performance (cont.)

CW Performance Small Signal
Gain and Input Return Loss
V_{DD} = 28 V,
I_{DQ} = 450 mA, $V_{GS(PEAK)}$ = 1.5 V



Pulsed CW Performance
at various V_{DD}
I_{DQ} = 450 mA, $V_{GS(PEAK)}$ = 1.5 V, f = 2675 MHz



Load Pull

Main Side (Doherty) Load Pull Performance – Pulsed CW signal: 10 µsec pulse width, 10% duty cycle, 28 V, I_{DQ} = 460 mA, class AB

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{3dB} [W]	η_D [%]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{3dB} [W]	η_D [%]
2515	4.7 – j16.2	3.4 – j6.1	16.4	49.30	85	55.4	5.6 – j4.0	18.1	48.14	65	63.0
2595	7.5 – j18.4	3.3 – j6.3	16.4	49.30	85	54.8	5.6 – j4.7	18.2	48.15	65	62.0
2675	12.4 – j22.5	3.3 – j6.5	16.7	48.70	74	49.3	5.5 – j4.7	18.6	47.70	59	56.0

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	η_D [%]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	η_D [%]
2515	4.7 – j16.2	3.3 – j6.4	14.2	50.04	101	55.3	5.7 – j4.1	16.1	48.80	76	63.0
2595	7.5 – j18.4	3.0 – j6.8	14.0	50.11	103	54.0	5.4 – j4.8	16.1	48.90	78	62.0
2675	12.4 – j22.5	3.3 – j7.1	14.4	49.60	91	49.3	5.4 – j4.2	16.7	48.30	68	56.0

Tables continued nex page

Load Pull (cont.)

Peak Side Doherty Load Pull Performance – Pulsed CW signal: 10 µsec pulse width, 10% duty cycle, V_{DD} = 28 V, I_{DQ} = 10 mA, class B

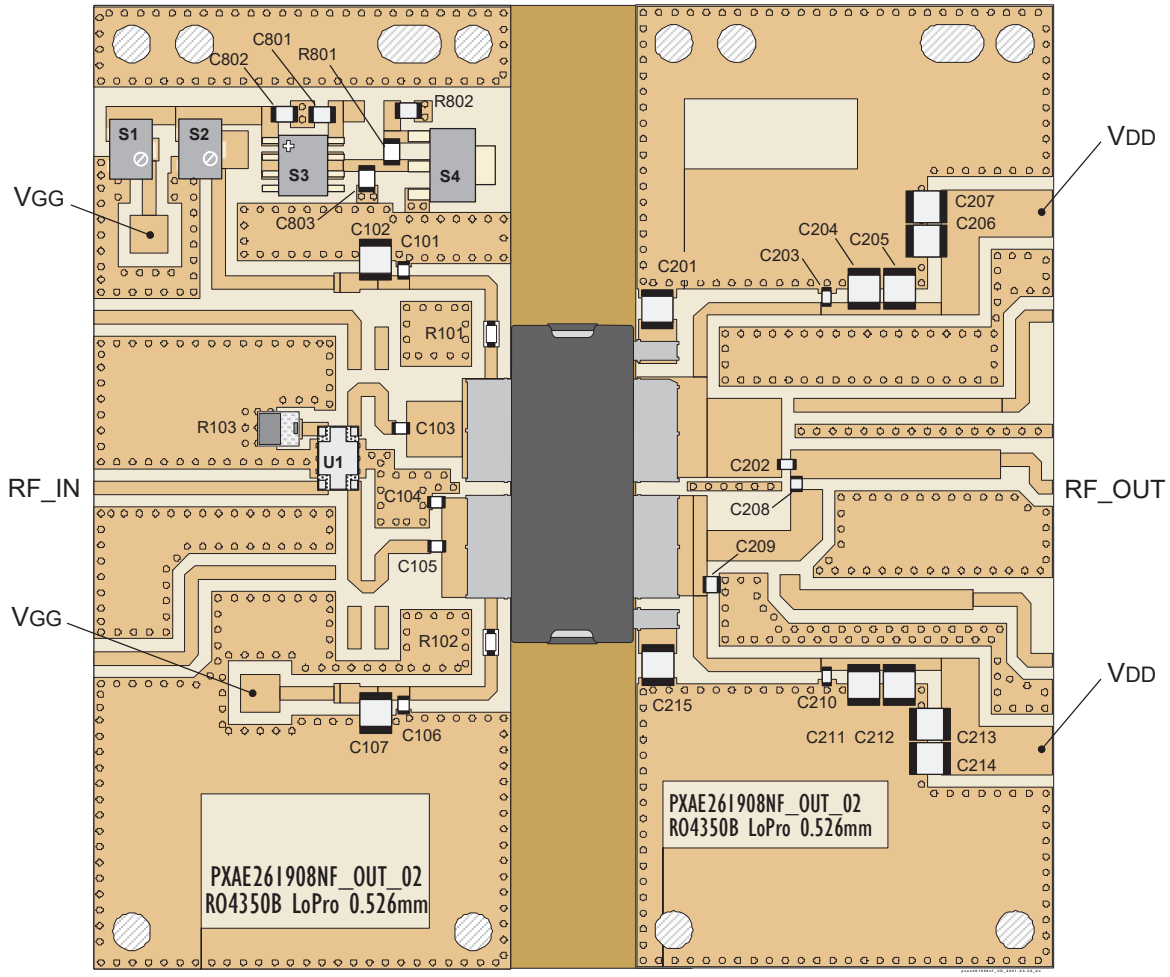
		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{1dB} [W]	η_D [%]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{3dB} [W]	η_D [%]
2515	3.0 – j13.2	4.4 – j7.1	14.2	52.50	178	58.2	4.7 – j3.6	15.4	51.00	126	66.0
2595	3.4 – j14.5	4.7 – j8.1	14.1	52.33	171	53.4	4.4 – j4.1	15.7	50.90	123	64.0
2675	6.3 – j15.0	5.8 – j8.7	14.4	52.20	166	52.7	4.7 – j5.0	15.8	51.00	126	60.0

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	η_D [%]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	η_D [%]
2515	3.0 – j13.2	4.9 – j8.1	11.8	53.12	205	55.5	5.0 – j3.9	13.4	51.80	151	65.0
2595	3.4 – j14.5	5.7 – j8.7	12.0	53.00	200	53.3	4.8 – j4.8	13.5	52.00	158	63.0
2675	6.3 – j15.0	6.3 – j8.9	12.3	52.80	191	52.4	4.7 – j5.4	13.6	51.90	155	60.0

See next page for evaluation circuit information.

Evaluation Circuit, 2515 – 2675 MHz

DUT	PXAE261908NF V1
Test Fixture Part No.	LTA/PXAE261908NF-V1
PCB	Rogers 4350B LoPro , 0.526 mm [0.0207"] thick, 1 oz. copper, ε_r = 3.66



Evaluation circuit assembly diagram (not to scale)

Bias Sequencing

Bias ON

1. Ensure RF is turned off
2. Apply pinch-off voltage of 0 V to the gate
3. Apply nominal drain voltage
4. Bias gate to desired quiescent drain current
5. Apply RF

Bias OFF

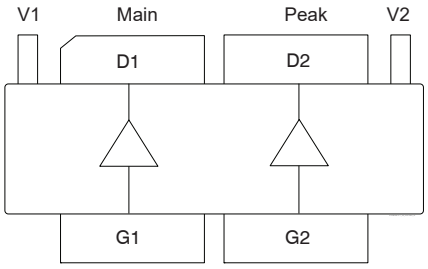
1. Turn RF off
2. Appliy pinch-off voltage of 0 V to the gate
3. Turn off drain voltage
4. Turn off gate voltage

Evaluation Circuit (cont.)

Components Table

Component	Description	Manufacturer	P/N
Input			
C101, C103, C105, C106	Capacitor, 20 pF	ATC	ATC800A200JT250T
C102, C107	Capacitor, 10 µF, 50 V	Taiyo Yuden	UMK325C7106MM-T
C104	Capacitor, 0.6 pF	ATC	ATC800A0R6CT250T
R101, R102	Resistor, 2.49 ohms	Vishay Dale	CRCW12062R49FKEA
R103	Resistor, 50 ohms	RICHARDSON	C8A50Z4A
U1	Hybrid coupler	ANAREN	X3C35P1-02S
C801,C802, C803	Capacitor, 1,000 pF	Murata Electronics	GRM188R72A102KA01D
R801	Chip resistor, 1.2K ohms	Panasonic Electronic Components	ERJ-3GEYJ122V
R802	Chip resistor, 1.3K ohms	Panasonic Electronic Components	ERJ-3GEYJ132V
S1, S2	Variable resistor, 2K ohms	Bourns Inc.	3224W-1-202E
S3	Voltage regulator	Texas Instruments	LM78L05ACM
S4	Transistor	Diodes Incorporated	BCP5616TA
Output			
C201, C204, C205, C206, C207, C211, C212, C213, C214, C215	Capacitor, 10 µF, 50 V	Taiyo Yuden	UMK325C7106MM-T
C202	Capacitor, 3.9 pF	ATC	ATC800A3R9CT250T
C203, C208, C210	Capacitor, 20 pF	ATC	ATC800A200JT250T
C209	Capacitor, 1.0 pF	ATC	ATC100B1R0CW500XB

Pinout Diagram (top view)



Pin	Description
D1	Drain Device 1 (Main)
D2	Drain Device 2 (Peak)
G1	Gate Device 1(Main)
G2	Gate Device 2 (Peak)
S	Source (flange)
V1, V2	Drain video decoupling, no DC Bias

Package Outline Specifications

Package PG-HBSOF-6-3

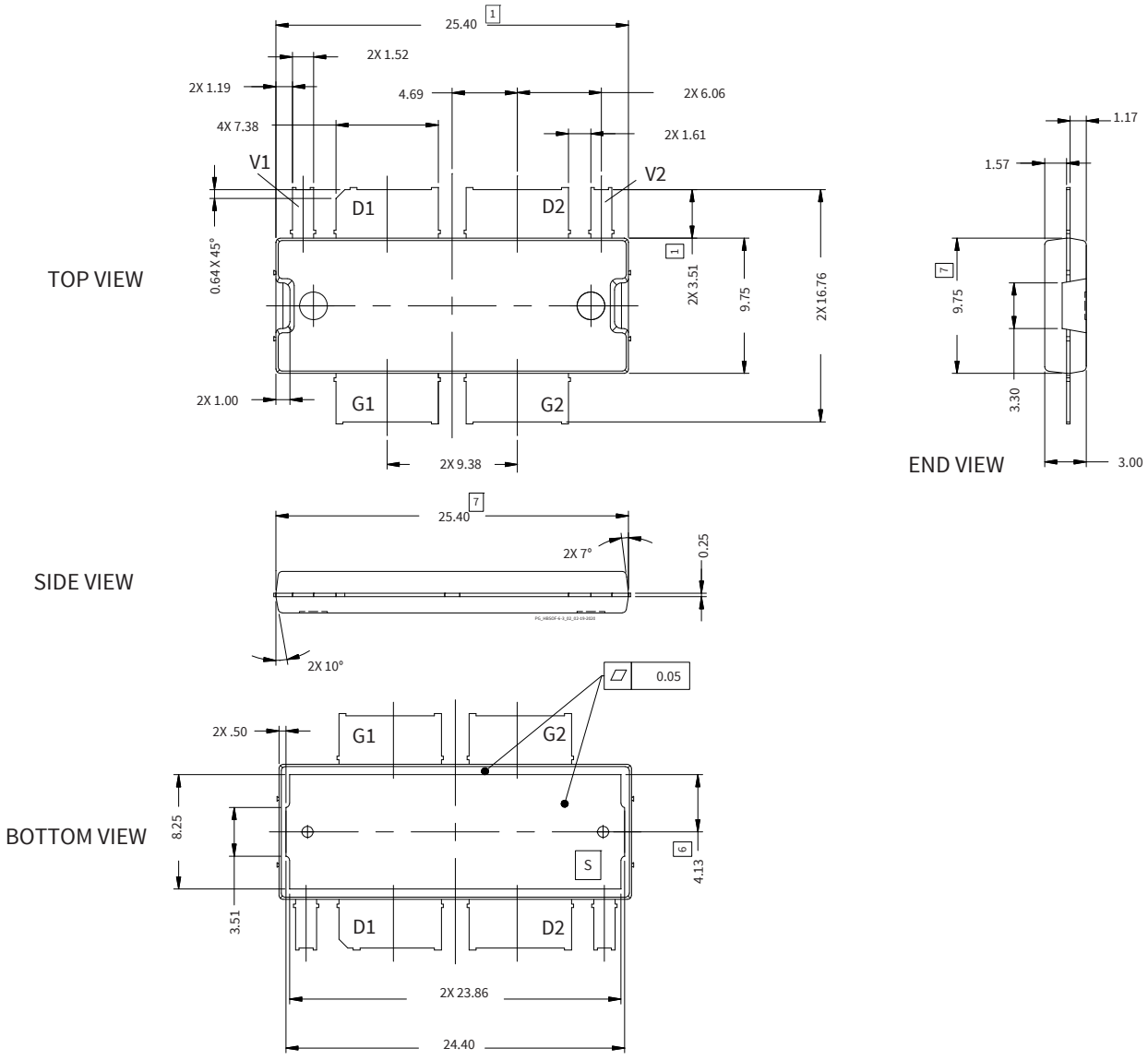


Diagram Notes–unless otherwise specified:

1. Mold/dam bar/metal protusion of 0.30 mm max per side not included.
2. Metal protrusion are connected to source and shall not exceed 0.10 mm max.
3. Fillets and radii: all radii are 0.3 mm max.
4. Interpret dimensions and tolerances per ISO 8015.
5. Dimensions are mm.
6. Exposed metal surface is tin-plated, may not be covered by mold compound.
7. Does not include mold/dam bar/metal protusion.
8. All tolerances ± 0.1 mm unless specified otherwise.
9. All metal surfaces pre-plated, except area of cut.
10. Lead thickness: 0.25 mm.
11. Pins: D1, D2 = drain; G1, G2 = gate; S = source; V1, V2 = drain video decoupling, not for DC bias.

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