

## PTRA084808NF

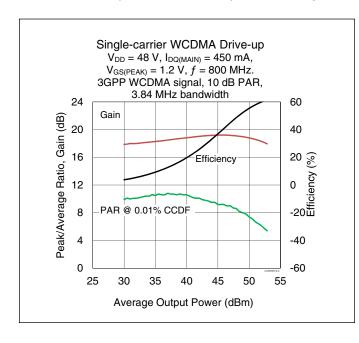
Thermally-Enhanced High Power RF LDMOS FET 550 W, 48 V, 734 - 821 MHz

## **Description**

The PTRA084808NF is a 550-watt LDMOS FET intended for use in multi-standard cellular power amplifier applications in the 734 to 821 MHz frequency band. Features include input matching, high gain and thermally-enhanced package with earless flanges. Manufactured with an advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



Package Types: PG-HBSOF-6-2 PN: PTRA084808NF



#### **Features**

- Broadband internal matching
- Asymmetric design

  - Main: P<sub>1dB</sub> = 200 W typical Peak: P<sub>1dB</sub> = 350 W typical
- Typical pulsed CW performance (class AB), 800 MHz, 48 V, 10 μs pulse width, 10% duty cycle, Doherty configuration
  - Output power at P<sub>3dB</sub> = 550 W
  - Efficiency = 56%
  - Gain = 18.5 dB
- Capable of handling 10:1 VSWR @ 48 V, 89 W (CW) output power
- Integrated ESD protection
- Human Body Model Class 1C (per ANSI/ESDA/ JEDEC JS-001)
- Low thermal resistance
- Pb-free and RoHS compliant

#### **RF Characteristics**

**Single-carrier WCDMA Specifications** (tested in the Doherty test fixture)

 $V_{DD} = 48 \text{ V}, I_{DO} = 450 \text{ mA}, V_{GS(PEAK)} = 1.2 \text{ V}, P_{OUT} = 87 \text{ W avg}, f = 800 \text{ MHz}. 3GPP signal, channel bandwidth} = 3.84 \text{ MHz}, f = 800 \text{ MHz}$ peak/average = 10 dB @ 0.01% CCDF.

Characteristic	Symbol	Min.	Тур.	Max.	Unit
Gain	G <sub>ps</sub>	17.5	18.2	_	dB
Drain Efficiency	$\eta_{D}$	52.5	55	_	%
Adjacent Channel Power Ratio	ACPR	_	-30	-27.5	dBc
Output PAR @ 0.01% CCDF	OPAR	6.5	7	_	dB

All published data at T<sub>CASE</sub> = 25°C unless otherwise indicated ESD: Electrostatic discharge sensitive device—observe handling precautions!





## **DC Characteristics** (each side)

Characteristic	Symbol	Min.	Тур.	Max.	Unit	Conditions
Drain-Source Breakdown Voltage	V <sub>BR(DSS)</sub>	105	_	_	V	$V_{GS} = 0 \text{ V}, I_{DS} = 10 \text{ mA}$
Drain Leakage Current		_	_	1	μΑ	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$
Drain Leakage Current	DSS	_	_	10		V <sub>DS</sub> = 105 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	I <sub>GSS</sub>	_	_	1		V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 0 V
On-State Resistance (main)		_	0.08	_		
On-State Resistance (peak)	R <sub>DS(on)</sub>	_	0.05	_	Ω	$V_{GS} = 10 \text{ V}, V_{DS} = 0.1 \text{ V}$
Operating Gate Voltage (main)		3	3.5	4	.,	V <sub>DS</sub> = 48 V, I <sub>DQ</sub> = 0.45 A
Operating Gate Voltage (peak)	$V_{GS}$	_	2	_	V	V <sub>DS</sub> = 48 V, I <sub>DQ</sub> = 0 A

## **Maximum Ratings**

Parameter	Symbol	Value	Unit	
Drain-source Voltage	V <sub>DSS</sub>	105		
Gate-source Voltage	V <sub>GS</sub>	V <sub>GS</sub> -6 to +12		
Operating Voltage	V <sub>DD</sub>	0 to +55		
Junction Temperature	T <sub>J</sub>	225	0.0	
Storage Temperature Range	T <sub>STG</sub>	-65 to +150	°C	

<sup>1.</sup> Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range  $(V_{DD})$  specified above.

### **Thermal Characteristics**

Characteristics	Symbol	Value	Unit	Conditions
Thermal Resistance	$R_{ heta JC}$	0.51	°C/W	T <sub>CASE</sub> = 70°C, 87 W (CW), 48 V, I <sub>DQ</sub> = 450 mA, 800 MHz

## **Moisture Sensitivity Level**

Level	Test Signal	Package Temperature	Unit		
3	IPC/JEDEC J-STD-020	260	°C		

## **Ordering Information**

Type and Version	Order Code	Package and Description	Shipping		
PTRA084808NF V1 R5	PTRA084808NF-V1-R5	PG-HBSOF-6-2, plastic overmold	Tape & Reel, 500 pcs		

<sup>2.</sup> Parameters values can be affected by end application and product usage. Values may change over time.

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### **Typical Performance** (data taken in the production test fixture)

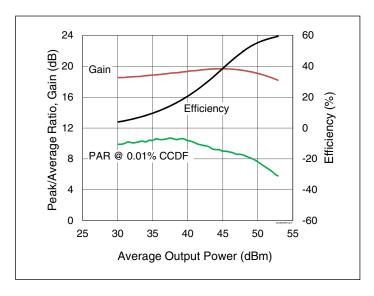


Figure 1. Single-carrier WCDMA Drive-up

 $V_{DD}=48$  V,  $I_{DQ(MAIN)}=450$  mA,  $V_{GS(PEAK)}=1.2$  V, f=770 MHz. 3GPP WCDMA signal, 10 dB PAR, 3.84 MHz bandwidth

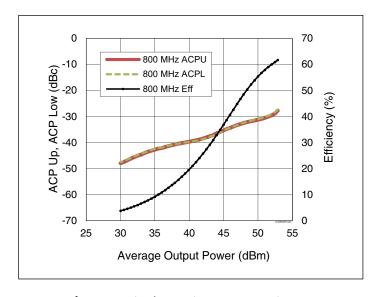


Figure 3. Single-carrier WCDMA Drive-up

 $V_{DD} = 48 \text{ V}, I_{DQ(MAIN)} = 450 \text{ mA}, \ V_{GS(PEAK)} = 1.2 \text{ V}, f = 800 \text{ MHz}, \ 3GPP WCDMA signal, 10 dB PAR,} \ 3.84 \text{ MHz bandwidth}$ 

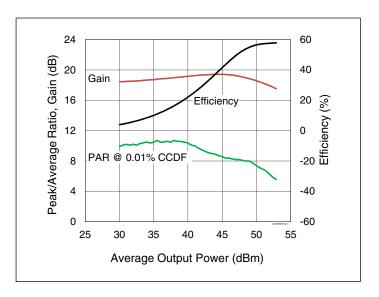
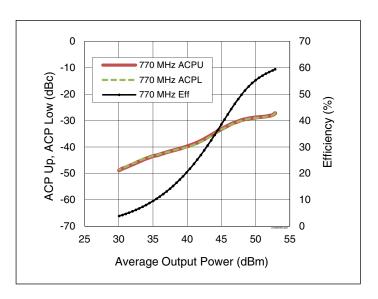


Figure 2. Single-carrier WCDMA Drive-up

 $V_{DD}=48~V,~I_{DQ(MAIN)}=450~mA, \ V_{GS(PEAK)}=1.2~V,~f=740~MHz. \ 3GPP~WCDMA~signal,~10~dB~PAR, \ 3.84~MHz~bandwidth$ 



**Figure 4.** Single-carrier WCDMA Drive-up

 $V_{DD}$  = 48 V,  $I_{DQ(MAIN)}$  = 450 mA,  $V_{GS(PEAK)}$  = 1.2 V, f = 770 MHz. 3GPP WCDMA signal, 10 dB PAR, 3.84 MHz bandwidth



### **Typical Performance (cont.)**

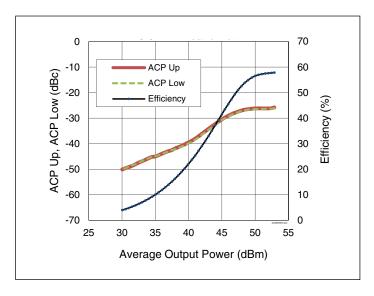


Figure 5. Single-carrier WCDMA Drive-up

$$\begin{split} &\mathbf{V}_{\mathrm{DD}} = 48~\mathrm{V,~I}_{\mathrm{DQ(MAIN)}} = 450~\mathrm{mA,} \\ &\mathbf{V}_{\mathrm{GS(PEAK)}} = 1.2~\mathrm{V,~} f = 740~\mathrm{MHz.} \\ &3\mathrm{GPP~WCDMA~signal,~} 10~\mathrm{dB~PAR,} \end{split}$$
3.84 MHz bandwidth

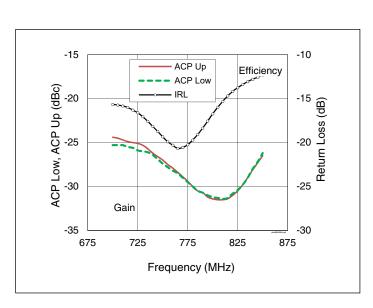


Figure 7. Single-carrier WCDMA Broadband

$$\begin{split} &V_{DD}=48~V,~I_{DQ(MAIN)}=450~mA,\\ &V_{GS(PEAK)}=1.2~V,~P_{OUT}=49.4~dBm,\\ &3GPP~WCDMA~signal,~10~dB~PAR \end{split}$$

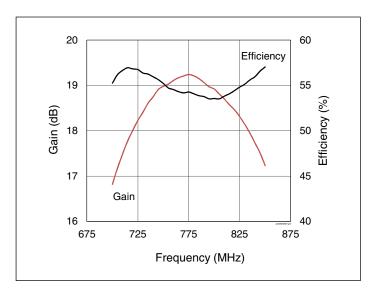


Figure 6. Single-carrier WCDMA Broadband

$$\begin{split} &V_{\text{DD}}=48~\text{V, I}_{\text{DQ(MAIN)}}=450~\text{mA},\\ &V_{\text{GS(PEAK)}}=1.2~\text{V, P}_{\text{OUT}}=49.4~\text{dBm,}\\ &3\text{GPP WCDMA signal, 10 dB PAR} \end{split}$$

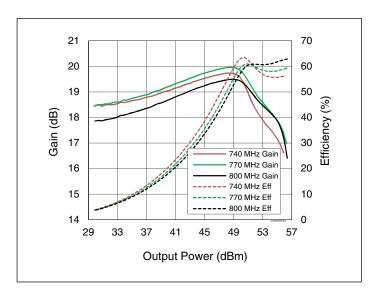
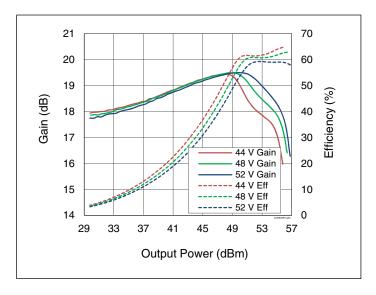


Figure 8. CW Performance

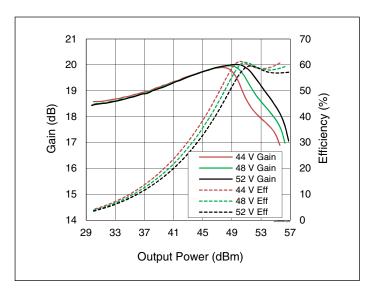
 $V_{DD} = 48 \text{ V}, \ I_{DQ(MAIN)} = 450 \text{ mA}, \\ V_{GS(PEAK)} = 1.2 \text{ V}$ 

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## **Typical Performance (cont.)**

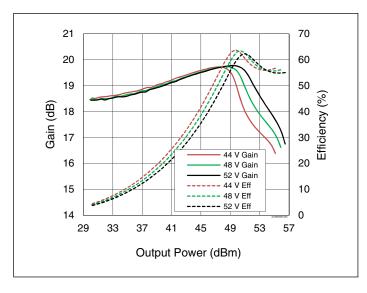


**Figure 9.** CW Performance at various V<sub>DD</sub> 
$$\begin{split} I_{DQ(MAIN)} = 450 \text{ mA}, \ V_{GS(PEAK)} = 1.2 \text{ V}, \\ f = 800 \text{ MHz} \end{split}$$



**Figure 10.** CW Performance at various V<sub>DD</sub>

$$I_{DQ(MAIN)} = 450 \text{ mA}, V_{GS(PEAK)} = 1.2 \text{ V},$$
  
 $f = 770 \text{ MHz}$ 



**Figure 11.** CW Performance at various V<sub>DD</sub>

$$I_{DQ(MAIN)} = 450 \text{ mA}, V_{GS(PEAK)} = 1.2 \text{ V},$$

$$f = 740 \text{ MHz}$$

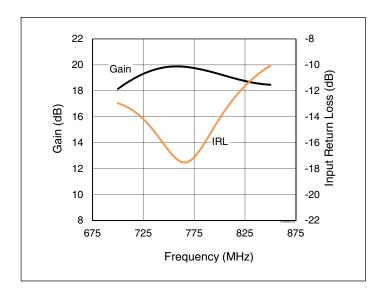


Figure 12. CW Performance Small Signal

$$V_{DD} = 48 \text{ V}, \ I_{DQ(MAIN)} = 450 \text{ mA}, \\ V_{GS(PEAK)} = 1.2 \text{ V}$$



### **Load Pull Performance**

Main side pulsed CW signal: 10  $\mu sec$ , 10% duty cycle,  $V_{DD}$  = 48 V,  $I_{DQ}$  = 390 mA, class AB

			$P_{1dB}$									
			Max C	Output Po	wer		Max Drain Efficiency					
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	Р <sub>оит</sub> [dBm]	P <sub>OUT</sub> [W]	ηD [%]	Zl [Ω]	Gain [dB]	Р <sub>оит</sub> [dBm]	P <sub>OUT</sub> [W]	ηD [%]	
730	2.00 – j3.64	1.96 – j0.96	20.5	53.53	225	56.4	4.71 + j0.66	22.1	51.59	144	66.1	
760	2.18 – j4.45	1.97 – j0.37	20.8	53.39	218	58.2	4.83 + j2.41	22.5	50.75	119	67.5	
780	2.23 - j4.48	1.75 – j0.81	20.5	53.18	208	52.8	4.95 + j1.41	22.9	51.00	126	66.9	
805	2.91 – j5.23	1.75 – j0.81	20.7	53.23	210	54.1	3.29 + j1.34	22.4	51.59	144	67.4	
820	2.96 – j5.44	1.96 – j0.96	21.2	53.12	205	55.8	3.43 + j0.83	22.7	51.79	151	67.6	

			P <sub>3dB</sub>									
			Max C	Output Po	wer		Max Drain Efficiency					
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P <sub>OUT</sub> [dBm]	P <sub>OUT</sub> [W]	ηD [%]	Zl [Ω]	Gain [dB]	P <sub>OUT</sub> [dBm]	P <sub>OUT</sub> [W]	ηD [%]	
730	2.00 – j3.64	1.96 – j0.96	18.5	54.48	281	60.9	5.35 + j1.53	20.2	51.79	151	67.9	
760	2.18 – j4.45	2.00 – j0.39	18.8	54.23	265	62.2	4.77 + j1.31	20.5	52.01	159	69.6	
780	2.23 – j4.48	1.56 – j1.27	18.2	54.11	258	53.7	4.29 + j1.74	20.6	51.82	152	69.3	
805	2.91 – j5.23	1.99 – j0.95	19.0	54.06	255	59.4	3.29 + j1.34	20.4	52.24	167	69.2	
820	2.96 – j5.44	1.99 – j1.26	19.2	53.99	251	58.1	3.60 + j1.21	20.8	52.16	164	69.8	

**Peak side pulsed CW signal:** 10  $\mu$ sec, 10% duty cycle,  $V_{DD}$  = 48 V,  $V_{GSPK}$  = 2.2 V, class C

			P <sub>1dB</sub>									
			Max C	Output Po	wer		Max Drain Efficiency					
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	Р <sub>оит</sub> [dBm]	P <sub>OUT</sub> [W]	ηD [%]	Zl [Ω]	Gain [dB]	Р <sub>оит</sub> [dBm]	P <sub>OUT</sub> [W]	ηD [%]	
730	1.79 – j3.78	1.06 – j0.36	17.2	55.63	366	63.4	1.16 + j1.09	18.1	52.87	194	78.4	
760	2.22 – j4.57	1.05 – j0.36	17.2	55.58	361	64.3	0.87 + j0.93	18.2	52.54	179	77.8	
780	2.24 – j4.52	1.14 – j0.55	17.1	55.52	356	62.0	0.89 + j0.86	18.2	52.45	176	76.4	
805	2.57 – j5.09	1.33 – j0.81	17.0	55.28	337	61.2	1.30 + j0.58	18.0	53.22	210	74.0	
820	3.79 – j5.33	1.13 – j0.67	17.4	55.35	343	62.9	1.10 + j0.75	17.9	52.45	176	74.4	

			P <sub>3dB</sub>									
			Max (	Output Po	wer		Max Drain Efficiency					
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P <sub>OUT</sub> [dBm]	P <sub>OUT</sub> [W]	ηD [%]	Zl [Ω]	Gain [dB]	Р <sub>оит</sub> [dBm]	P <sub>OUT</sub> [W]	ηD [%]	
730	1.79 – j3.78	1.06 – j0.36	15.2	56.36	433	65.0	1.12 + j0.79	16.2	54.27	267	77.7	
760	2.22 – j4.57	1.33 – j0.44	15.3	56.34	431	68.4	1.42 + j0.90	15.9	54.04	254	76.2	
780	2.24 - j4.52	1.16 – j0.62	15.0	56.36	433	64.0	1.31 + j0.54	16.0	54.53	284	75.9	
805	2.57 – j5.09	1.34 – j0.81	15.0	56.09	406	63.3	1.39 + j0.47	15.9	54.28	268	74.0	
820	3.79 – j5.33	1.21 – j0.71	15.3	56.08	406	64.4	1.25 + j0.46	16.0	54.14	259	74.1	

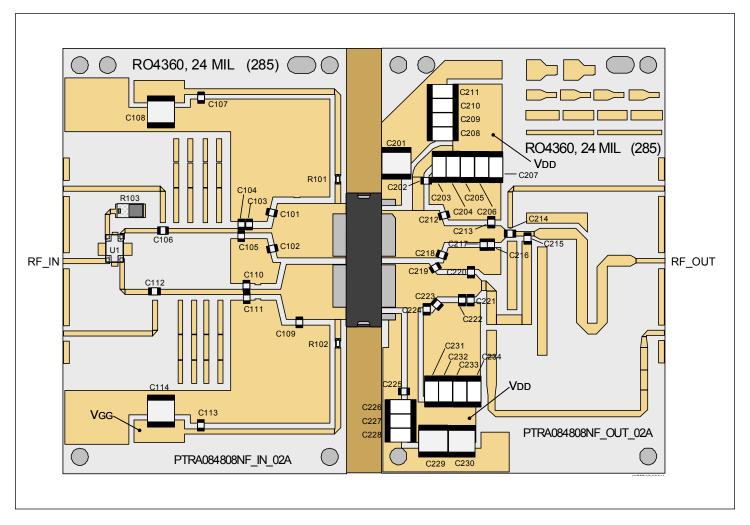
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## Evaluation Board, 734 to 821 MHz

Evaluation Board Part Number	LTA/PTRA084808NF-V1
PCB Information	Rogers 4360, 0.609 mm [0.024"] thick, 2 oz. copper, $\varepsilon_r$ = 6.15



Reference circuit assembly diagram (not to scale)

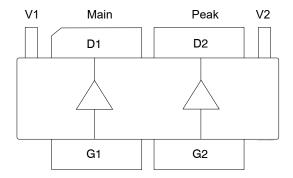


## **Components Information**

Component	Description	Manufacturer	P/N	
Input				
C101, C102	Capacitor, 2.7 pF	ATC	ATC600F2R7CT250	
C103	Capacitor, 1.4 pF	ATC	ATC600F1R4CT250	
C104	Capacitor, 3.9 pF	ATC	ATC600F3R9CT250	
C105	Capacitor, 1.0 pF	ATC	ATC600F1R0CT250	
C106	Capacitor, 68 pF	ATC	ATC600F680JT250	
C107, C113	Capacitor, 82 pF	ATC	ATC600F820JT250	
C108, C114	Capacitor, 10 μF, 100V	TDK Corporation	C5750X7S2A106M230KB	
C109	Capacitor, 5.6 pF	ATC	ATC600F5R6CT250	
C110	Capacitor, 4.7 pF	ATC	ATC600F4R7CT250	
C111	Capacitor, 2.0 pF	ATC	ATC600F2R0CT250	
C112	Capacitor, 56 pF	ATC	ATC800A560JT250	
R101, R102	Resistor, 10 ohms	Panasonic Electronic Components	ERJ-8GEYJ100V	
R103	Resistor, 50 ohms	Anaren	C8A50Z4A	
U1	Hybrid coupler	Anaren	X3C07F1-02S	
Output				
C201, C203, C204, C205, C206, C207, C208, C209, C210, C211, C226, C227, C228, C229,C230, C231, C232, C233, C234	Capacitor, 10 μF, 100V	TDK Corporation	C5750X7S2A106M230KB	
C202, C215	Capacitor, 82 pF	ATC	ATC600F820JT250	
C212	Capacitor, 10 pF	ATC	ATC600F100JT250	
C213	Capacitor, 6.8 pF	ATC	ATC600F6R8CT250	
C214	Capacitor, 47 pF	ATC	ATC600F470JT250	
C216, C222	Capacitor, 1.0 pF	ATC	ATC600F1R0CT250	
C217	Capacitor, 3.9 pF	ATC	ATC600F3R9CT250	
C218	Capacitor, 5.6 pF	ATC	ATC600F5R6CT250	
C219, C223	Capacitor, 12 pF	ATC	ATC600F120JT250	
C220, C221	Capacitor, 1.5 pF	ATC	ATC600F1R5CT250	
C224	Capacitor, 2.0 pF	ATC	ATC600F2R0CT250	
C225	Capacitor, 100 pF	ATC	ATC600F101JT250	



## **Pinout Diagram** (top view)



Pin	Description
D1	Drain Device 1 (Main)
D2	Drain Device 2 (Peak)
G1	Gate Device 1 (Main)
G2	Gate Device 2 (Peak)
S	Source (flange)
V1	Drain video decoupling, no DC bias
V2	NC (not connected to ground)

See next page for package mechanical specifications.



### Package Outline Specifications - Package PG-HBSOF-6-2 (top and side views)

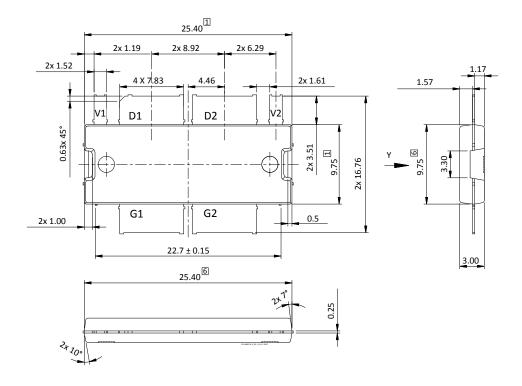


Diagram Notes—unless otherwise specified:

- 1. Mold/dam bar/metal protrusion of 0.30 mm max per side not included.
- 2. Metal protrusions are connected to source and shall not exceed 0.10 mm max.
- 3. Fillets and radii: all radii are 0.3 mm max.
- 4. Interpret dimensions and tolerances per ISO 8015.
- 5. Dimensions are mm.
- 6. Does not include mold/dam bar and metal protrusion.
- 7. Exposed metal surface is tin-plated, may not be covered by mold compound.
- 8. All tolerances  $\pm$  0.1 mm unless specified otherwise.
- 9. All metal surfaces are tin-plated, except area of cut.
- 10. Lead thickness: 0.25 mm.
- 11. Pins: D1, D2 = drain; G1, G2 = gate; S = source, V1, V2 = no DC bias, NC or connect to GRD



### Package Outline Specifications (cont.) - Package PG-HBSOF-6-2 (bottom view)

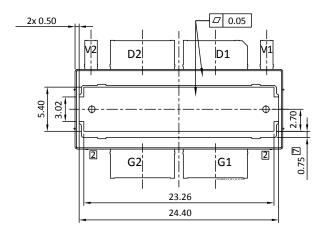


Diagram Notes—unless otherwise specified:

- 1. Mold/dam bar/metal protrusion of 0.30 mm max per side not included.
- 2. Metal protrusions are connected to source and shall not exceed 0.10 mm max.
- 3. Fillets and radii: all radii are 0.3 mm max.
- 4. Interpret dimensions and tolerances per ISO 8015.
- 5. Dimensions are mm.
- 6. Does not include mold/dam bar and metal protrusion.
- 7. Exposed metal surface is tin-plated, may not be covered by mold compound.
- 8. All tolerances  $\pm$  0.1 mm unless specified otherwise.
- 9. All metal surfaces are tin-plated, except area of cut.
- 10. Lead thickness: 0.25 mm.
- 11. Pins: D1, D2 = drain; G1, G2 = gate; S = source, V1, V2 = no DC bias, NC or connect to GRD



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