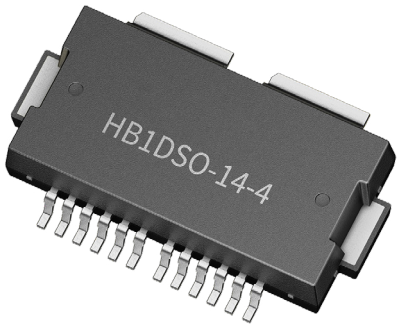
PTGA090304MD

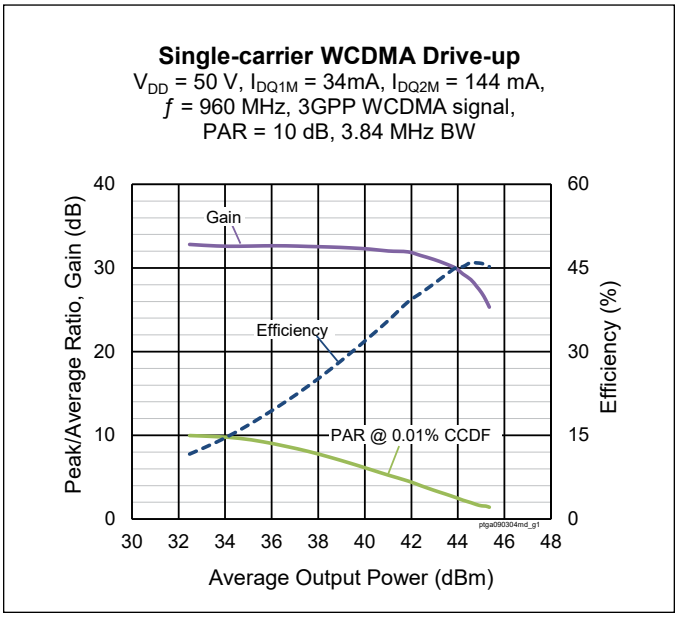
Wideband LDMOS Two-stage Integrated Power Amplifier
2 X 15 W, 48 V, 575 – 960 MHz



Package Types: PG-HB1DSO-14-4

Description

The PTGA090304MD is a wideband, two-stage, LDMOS integrated power amplifier. Fabricated with 50 V LDMOS process, it incorporates internal matching for operation from 575 MHz to 960 MHz, and dual independent outputs of 15 W each. It is available in a 14-lead plastic overmold package with gull wing leads.



Features

- On-chip matching for broadband operation
- Designed for ultra wideband performance
- Typical CW performance, 960 MHz, 50 V, combined outputs
  - Output power at P_{1dB} = 45 dBm
  - Output power at P_{3dB} = 45.9 dBm
  - Linear Gain at P_{1dB} = 31 dB
  - Efficiency at P_{1dB} = 48.1%
- Capable of handling 10:1 VSWR @50 V, 30 W CW output power
- Integrated ESD protection
- Human Body Model Class 1C (per ANSI/ESDA/JEDEC JS-001)
- Integrated temperature compensation
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in the Class AB production test fixture, combined outputs)
V_{DD} = 50 V, I_{DQ1M} = 34 mA, I_{DQ2M} = 144 mA, P_{OUT} = 3.9 W avg, f = 960 MHz, 3GPP WCDMA signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Gain	G_{ps}	30.2	32	—	dB
Drain Efficiency	η_D	17.5	19	—	%
Adjacent Channel Power Ratio	ACPR	—	–44	–46.5	dBc
Output PAR at 0.01% probability on CCDF	OPAR	8.5	9	—	dB

Note:
All published data at T_{CASE} = 25°C unless otherwise indicated
ESD: Electrostatic discharge sensitive device—observe handling precautions!

RoHS compliant

Typical Performance, 920 – 960 MHz (tested in the narrowband test fixture)

V_{DD} = 50 V, I_{DQ1M} = 34 mA, I_{DQ2M} = 144 mA, 3GPP WCDMA signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Freq [MHz]	Gain [dB]	RL [dB]	Eff [%]	P_{OUT} [dBm]	ACPL [dBc]	ACPU [dBc]	ACP max [dBc]
920	32.9	–37.1	19.8	35.9	–44.7	–44.6	–44.64
940	32.8	–43.6	19.4	35.9	–44.4	–44.1	–44.05
960	32.6	–38.9	19.2	35.9	–43.8	–43.9	–43.75

Typical Broadband Performance, 575 – 960 MHz (tested in the broadband test fixture)

V_{DD} = 50 V, I_{DQ1M} = 34 mA, I_{DQ2M} = 144 mA, 3GPP WCDMA signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Freq [MHz]	Gain [dB]	RL [dB]	Eff [%]	P_{OUT} [dBm]	PAR [dB]	ACPL [dBc]	ACPU [dBc]	ACP max [dBc]
575	29.1	–22.3	17.7	35.9	9.2	–37.5	–37.3	–37.30
590	30.1	–22.7	17.8	35.9	9.2	–39.4	–39.5	–39.41
660	32.0	–24.8	18.1	35.9	9.3	–44.5	–45.1	–44.54
746	30.8	–28.0	17.1	35.9	9.5	–45.6	–45.8	–45.57
860	30.2	–23.4	15.8	35.9	9.5	–45.0	–45.5	–45.05
960	30.4	–26.9	15.0	35.9	9.4	–44.0	–44.0	–43.98

DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	105	—	—	V	V_{GS} = 0 V, I_{DS} = 136 µA
Drain Leakage Current – Stage 1	I_{DSS}	—	—	0.1	µA	V_{DS} = 50 V, V_{GS} = 0 V
		—	—	1.0		V_{DS} = 105 V, V_{GS} = 0 V
Drain Leakage Current –Stage 2		—	—	0.1		V_{DS} = 50 V, V_{GS} = 0 V
		—	—	1.0		V_{DS} = 105 V, V_{GS} = 0 V
Gate Leakage Current – Stage 1	I_{GSS}	—	—	0.1		V_{GS} = 1 V, V_{DS} = 0 V
Gate Leakage Current – Stage 2		—	—			
On-State Resistance – Stage 1	$R_{DS(on)}$	—	22.5	—	Ω	V_{GS} = 10 V, V_{DS} = 0.1 V, I_D = 24 mA
On-State Resistance – Stage 2		—	2.6	—		V_{GS} = 10 V, V_{DS} = 0.1 V, I_D = 136 mA
Operating Gate Voltage – Stage 1	V_{GS1}	—	3.9	—	V	V_{DS} = 50 V, I_{DQ1M} = 34 mA
Operating Gate Voltage – Stage 2	V_{GS2}	—	3.8	—		V_{DS} = 50 V, I_{DQ2M} = 144 mA
Fixture Operating Gate Voltage – Stage 1	V_{GS1}	—	5.8	—		V_{DS} = 50 V, I_{DQ1M} = 34 mA
Fixture Operating Gate Voltage – Stage 2	V_{GS2}	—	5.7	—		V_{DS} = 50 V, I_{DQ2M} = 144 mA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	105	V
Gate-Source Voltage	V_{GS}	–6 to +12	
Operating Voltage	V_{DD}	0 to +55	
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	

1. Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range (V_{DD}) specified above.
2. Parameters values can be affected by end application and product usage. Values may change over time.

Thermal Characteristics

Parameter	Symbol	Value	Unit	Conditions
Thermal Resistance – Stage 1	$R_{\theta JC}$	7.8	°C/W	T_{CASE} = 70°C, 4 W WCDMA
Thermal Resistance – Stage 2		3.3		T_{CASE} = 70°C, 4 W WCDMA

Moisture Sensitivity Level

Level	Test Standard	Package Temperature	Unit
3	IPC/JEDEC J-STD-020	260	°C

Ordering Information

Type and Version	Order Code	Package Description	Shipping
PTGA090304MD V2 R5	PTGA090304MD-V2-R5	PG-HB1DSO-14-4	Tape & Reel, 500 pcs

Evaluation Boards

Order Code	Frequency	Description
LTN/PTGA090304MD-V2	920 – 960 MHz	Class AB with combined outputs, R04350
LTN/PTGA090304MD-E2	728 – 768 MHz	Class AB with combined outputs, R04350
LTN/PTGA090304MD-E3	575 – 960 MHz	Class AB with combined outputs, R04350

Typical Performance, 920 – 960 MHz (data taken in test fixture)

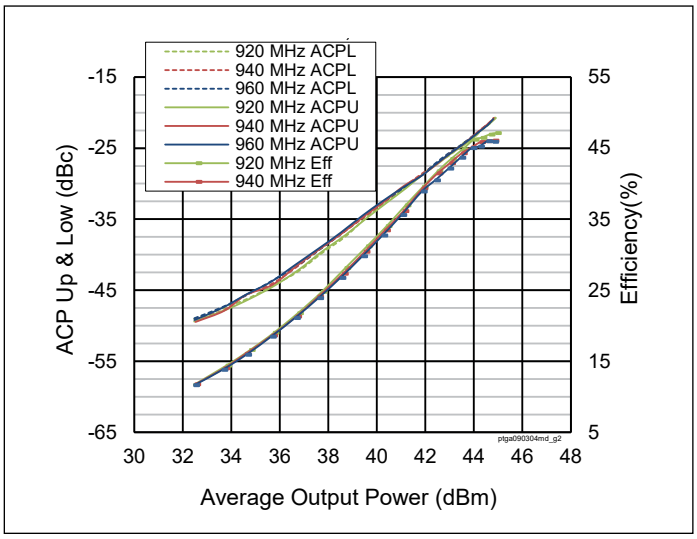


Figure 1. Single-carrier WCDMA 3GPP Drive-up

V_{DD} = 50 V, I_{DQ1M} = 34 mA, I_{DQ2M} = 144 mA,
f = 920-960 MHz, 3GPP WCDMA signal,
PAR = 10 dB, BW = 3.84 MHz

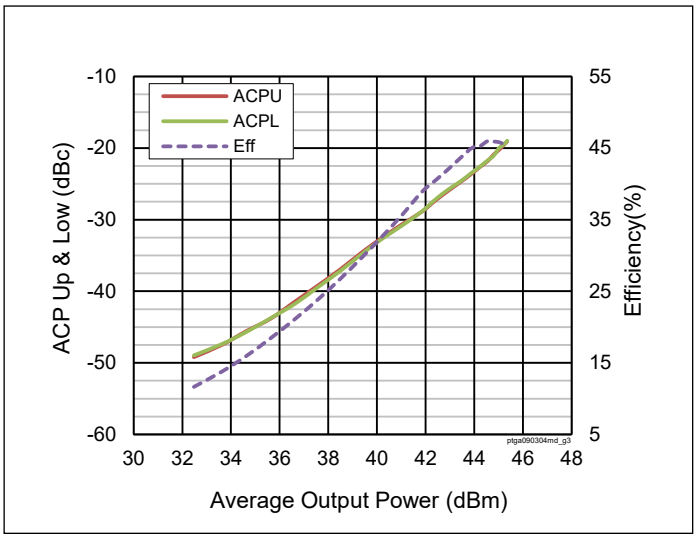


Figure 2. Single-carrier WCDMA Drive-up

V_{DD} = 50 V, I_{DQ1} = 34 mA, I_{DQ2} = 144 mA,
f = 960 MHz, 3GPP WCDMA signal,
PAR = 10 dB, 3.84 MHz BW

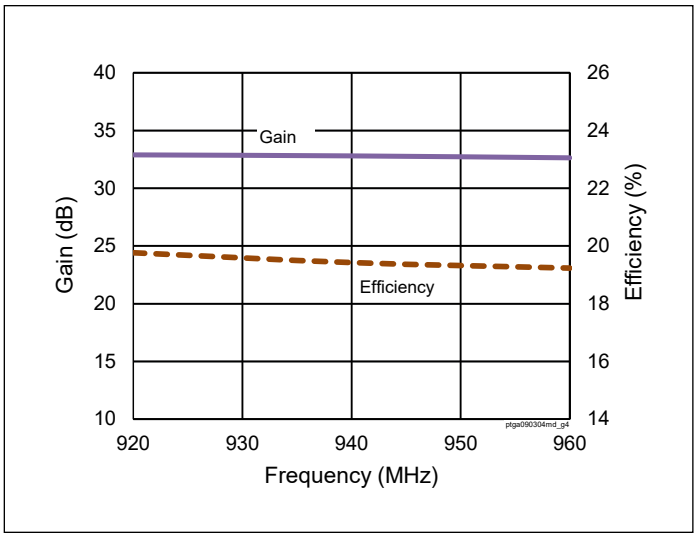


Figure 3. Single-carrier WCDMA Broadband Performance

V_{DD} = 50 V, I_{DQ1M} = 34 mA, I_{DQ2M} = 144 mA,
P_{OUT} = 35.9 dBm, 3GPP WCDMA signal,
PAR = 10 dB

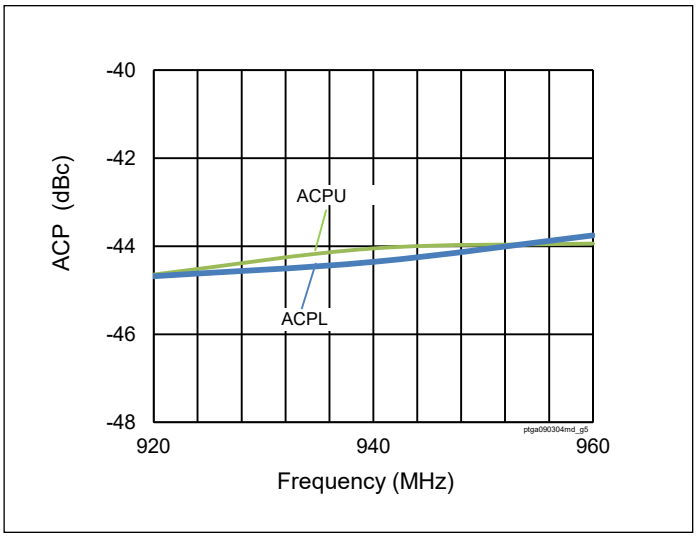


Figure 4. Single-carrier WCDMA Broadband Performance

V_{DD} = 50 V, I_{DQ1M} = 34 mA, I_{DQ2M} = 144 mA,
P_{OUT} = 35.9 dBm, 3GPP WCDMA signal,
PAR = 10 dB

Typical Performance, 920 – 960 MHz (data taken in test fixture)

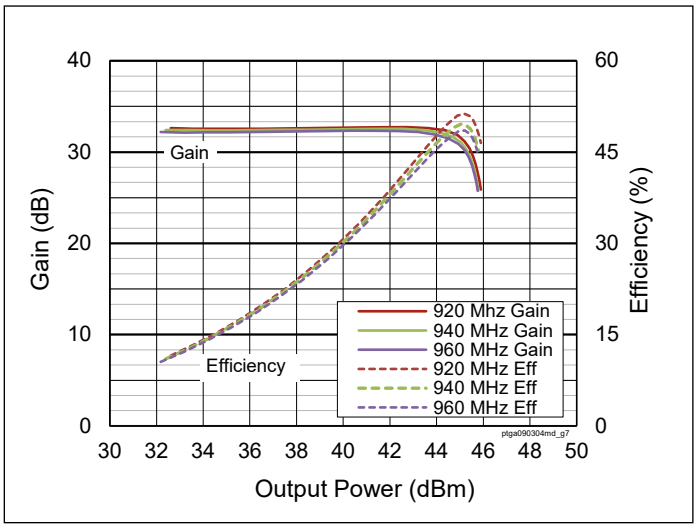


Figure 5. CW Performance

V_{DD} = 50 V, I_{DQ1M} = 34 mA, I_{DQ2M} = 144 mA

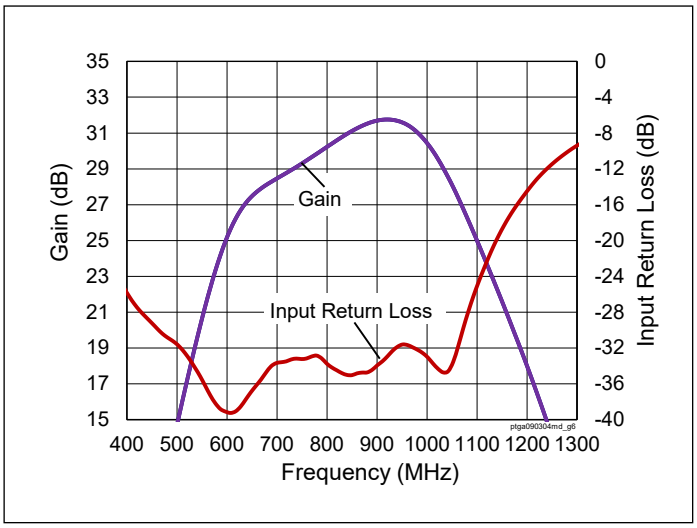


Figure 6. Small Signal CW Gain & Return Loss

V_{DD} = 50 V, I_{DQ1} = 34 mA, I_{DQ2} = 144 mA

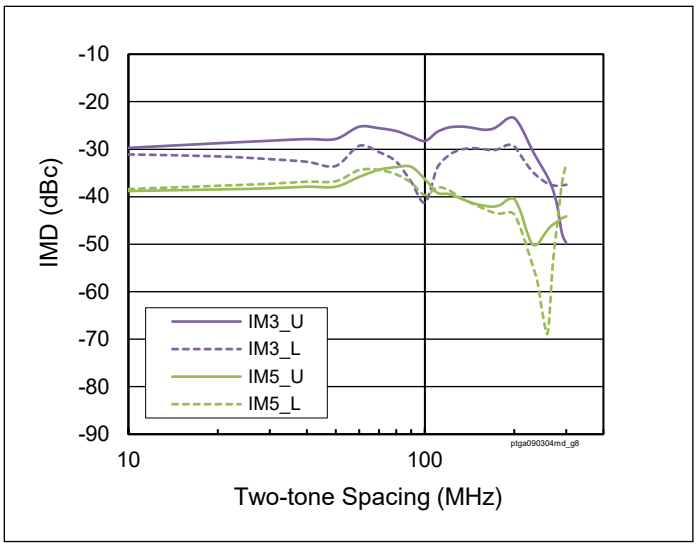
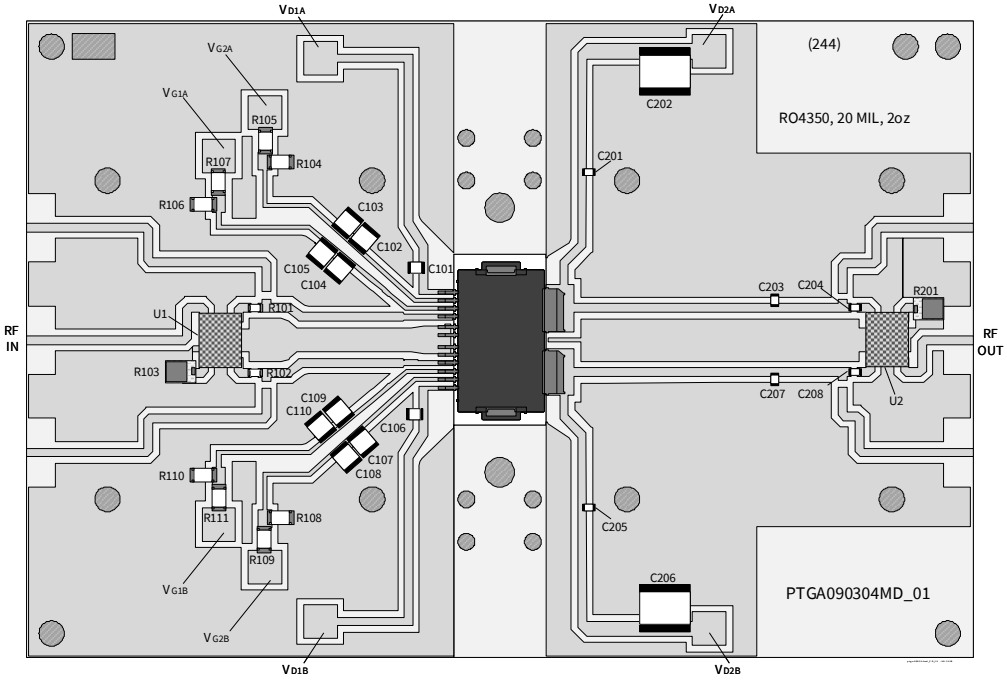


Figure 7. IMD versus two-tone spacing

V_{DD} = 50 V, I_{DQ1M} = 34 mA, I_{DQ2M} = 144 mA,
($f1$+$f2$)/2=Center Frequency of 940 MHz

Evaluation Board, 920 – 960 MHz



Reference circuit assembly diagram (not to scale)

Evaluation Board Part Number	LTN/PTGA090304MD-V2
PCB Information	Rogers 4350, 0.508 mm [0.020”] thick, 2 oz. copper, ε_r = 3.66, f = 920 – 960 MHz

Components Information

Component	Description	Manufacturer	P/N
C101, C106	Capacitor, 0.1 µF	TDK Corporation	C3216X7R2A104M160AA
C102, C104, C107, C109	Capacitor, 100 V, 10 µF	Murata Electronics North America	GRM32EC72A106KE05L
C103, C105, C108, C110	Capacitor, 4.7 µF	Murata Electronics North America	GRM32ER71H475KA88L
C201, C204, C205, C208	Capacitor, 100 pF	ATC	ATC800A101JT250T
C202, C206	Capacitor, 100 V, 10 µF	TDK Corporation	C5750X7S2A106M230KB
C203, C207	Capacitor, 0.1 pF	ATC	ATC800A0R1CT250T
R101, R102	Resistor, 0 ohms	Panasonic Electronic Components	ERJ-3GEY0R00V
R103, R201	Resistor, 50 ohms	Anaren	C8A50Z4A
R104, R106, R108, R110	Resistor, 4.3K ohms	Panasonic Electronic Components	ERJ-8GEYJ432V
R105, R107, R109, R111	Resistor, 1K ohms	Panasonic Electronic Components	ERJ-8GEYJ102V
U1, U2	Hybrid coupler	Anaren	X3C07P1-03S

Typical Broadband Performance, 575 – 960 MHz (data taken in test fixture)

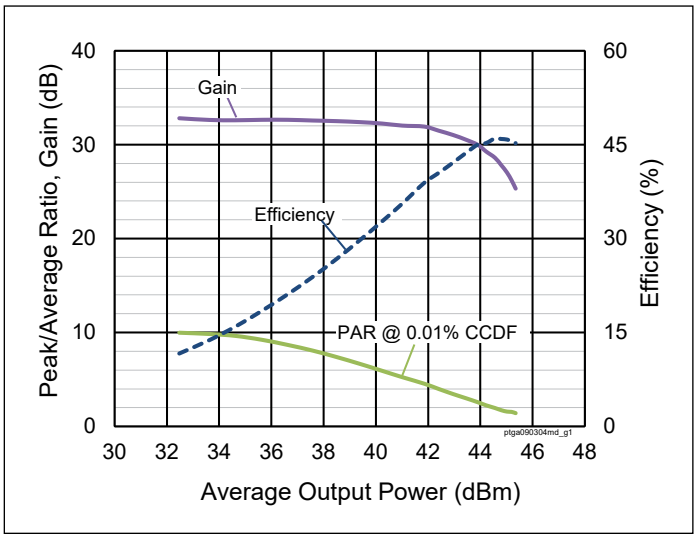


Figure 8. Single-carrier WCDMA Drive-up

V_{DD} = 50 V, I_{DQ1M} = 34mA, I_{DQ2M} = 144 mA,
f = 960 MHz, 3GPP WCDMA signal,
PAR = 10 dB, 3.84 MHz BW

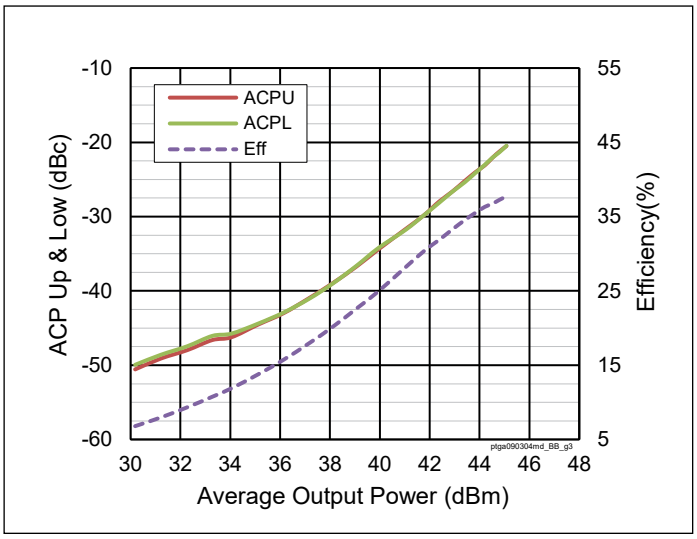


Figure 9. Single-carrier WCDMA Drive-up

V_{DD} = 50 V, I_{DQ1} = 34 mA, I_{DQ2} = 144 mA,
f = 960 MHz, 3GPP WCDMA signal,
PAR = 10 dB, 3.84 MHz BW

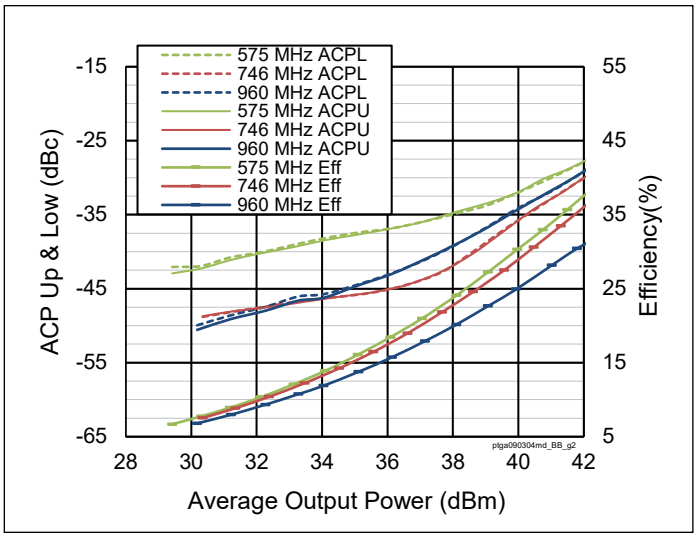


Figure 10. Single-carrier WCDMA 3GPP Drive-up

V_{DD} = 50 V, I_{DQ1M} = 34mA, I_{DQ2M} = 144 mA,
f = 575-960 MHz, 3GPP WCDMA signal,
PAR = 10 dB, BW = 3.84 MHz

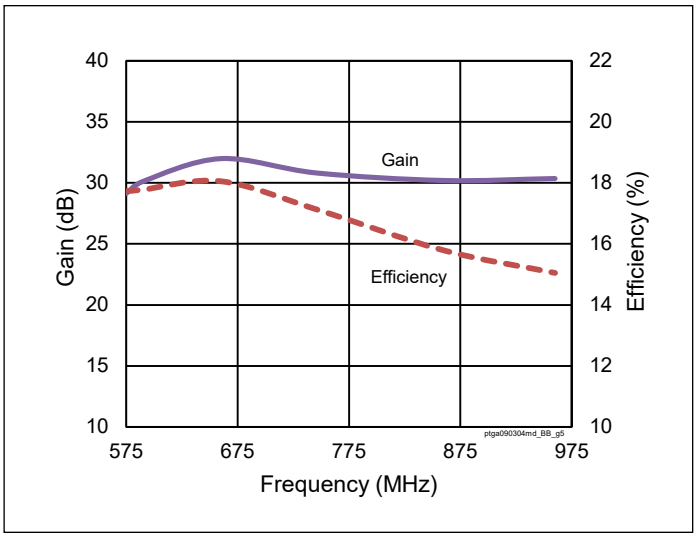


Figure 11. Single-carrier WCDMA Broadband Performance

V_{DD} = 50 V, I_{DQ1M} = 34 mA, I_{DQ2M} = 144 mA,
P_{OUT} = 35.9 dBm, 3GPP WCDMA signal,
PAR = 10 dB

Typical Broadband Performance, 575 – 960 MHz (data taken in test fixture)

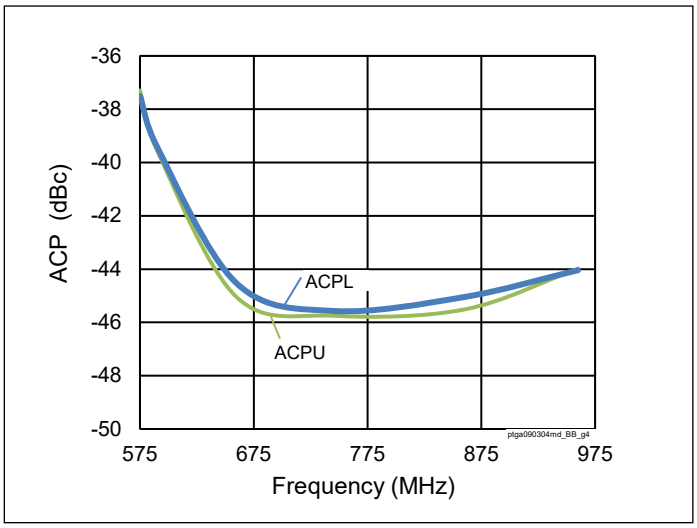


Figure 12. Single-carrier WCDMA Broadband Performance

V_{DD} = 50 V, I_{DQ1M} = 34 mA, I_{DQ2M} = 144 mA,
P_{OUT} = 35.9 dBm, 3GPP WCDMA signal,
PAR = 10 dB

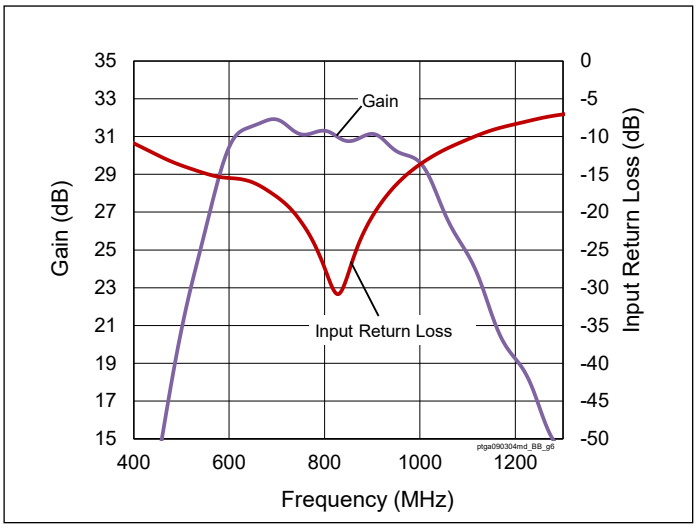


Figure 6. Small Signal CW Gain & Input Return Loss

V_{DD} = 50 V, I_{DQ1} = 34 mA, I_{DQ2} = 144 mA

Load Pull Performance

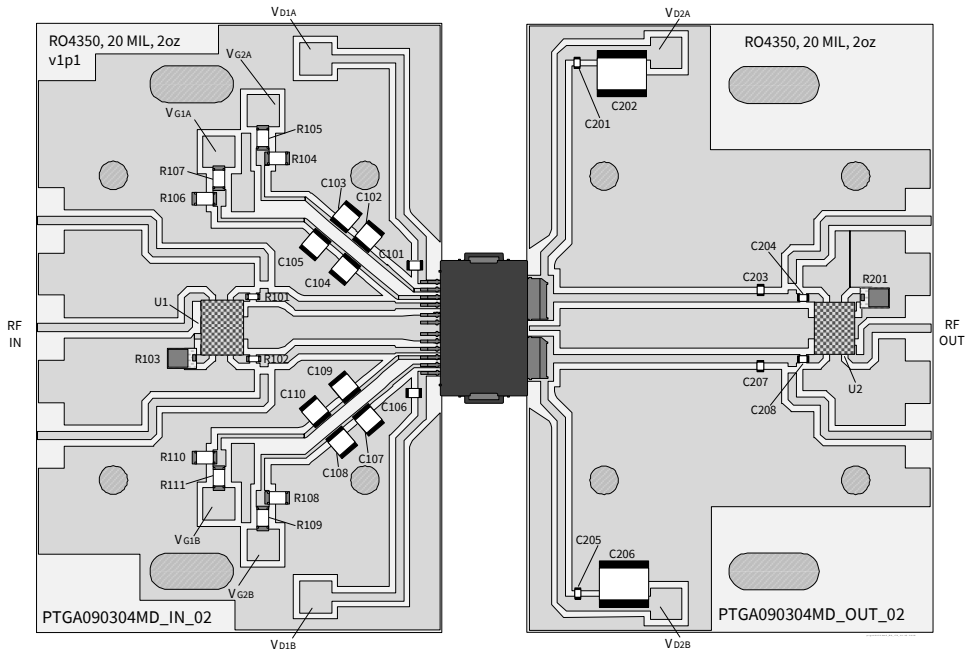
CW signal: 50 V, I_{DQ} = 17 mA, 72 mA

		P_{1dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Z_s [W]	Z_l[W]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Z_l[W]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
575	50+j0.00	29.6+j22.6	30.0	42.9	19.3	61.6	13.6+j32.8	34.0	40.4	10.9	72.5
746	50+j0.00	20.8+j18.8	31.3	43.1	20.4	57.1	9+j23.5	34.2	41.0	12.5	66.9
920	50+j0.00	13.8+j16.6	31.6	43.1	20.6	56.3	7+j20.3	34.4	41.3	13.4	68.6
940	50+j0.00	15.4+j16.8	31.4	43.1	20.5	55.3	5.8+j20	35.2	40.5	11.3	70.1
960	50+j0.00	15.6+j16.8	31.7	43.2	20.8	57.6	6+j20	35.8	40.7	11.8	77.5

		P_{3dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Z_s [W]	Z_l[W]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Z_l[W]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
575	50+j0.00	29.2+j20.1	27.7	43.5	22.3	60.8	14+j32.8	31.9	41.0	12.5	71.2
746	50+j0.00	18.1+j16.5	29.3	43.8	24.0	58.1	9.5+j23.9	32.1	41.6	14.5	65.4
920	50+j0.00	14.2+j16.6	29.5	43.8	24.1	56.4	6.6+j20	32.5	41.8	15.0	66.2
940	50+j0.00	15.7+j16.5	29.3	43.8	23.9	54.9	5.4+j20	33.4	40.9	12.4	68.1
960	50+j0.00	15.8+j16.5	29.6	43.9	24.5	57.5	6+j20	33.8	41.3	13.5	75.5

*Please note max PAE contours not closed

Evaluation Board, 575 – 960 MHz



Reference circuit assembly diagram (not to scale)

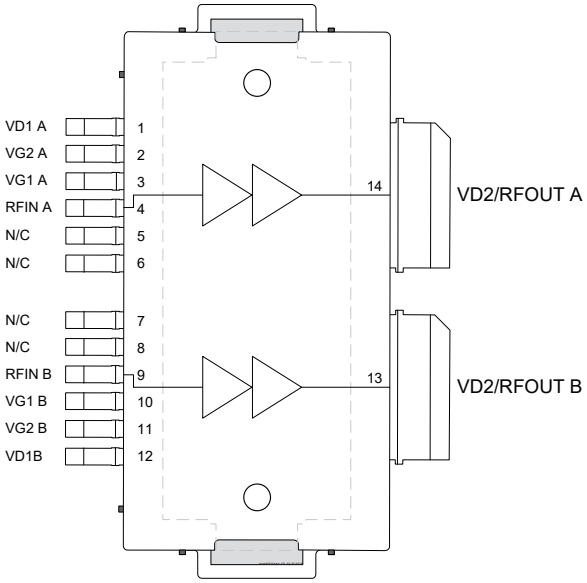
Evaluation Board Part Number	LTN/PTGA090304MD-E3
PCB Information	Rogers 4350, 0.508 mm [0.020”] thick, 2 oz. copper, ε_r = 3.66, f = 575 – 960 MHz

Reference Circuit, 575 – 960 MHz (cont.)

Components Information

Component	Description	Manufacturer	P/N
Input			
C101, C106	Capacitor, 0.1 µF	TDK Corporation	C3216X7R2A104M160AA
C102, C104, C107, C109	Capacitor, 10 µF, 100 V	Murata Electronics North America	GRM32EC72A106KE05L
C103, C105, C108, C110	Capacitor, 4.7 µF	Murata Electronics North America	GRM32ER71H475KA88L
R101, R102	Resistor, 0.0 ohms	Panasonic Electronic Components	ERJ-3GEY0R00V
R103	Resistor, 50 ohms	Anaren	C8A50Z4A
R104, R106, R108, R110	Resistor, 4.3K ohms	Panasonic Electronic Components	ERJ-8GEYJ432V
R105, R107, R109, R111	Resistor, 1K ohms	Panasonic Electronic Components	ERJ-8GEYJ102V
U1	Hybrid Coupler	Anaren	X3C07P1-03S
Output			
C201, C204, C205, C208	Capacitor, 100 pF	ATC	ATC800A101JT250T
C202, C206	Capacitor, 10 µF, 100 V	TDK Corporation	C5750X7S2A106M230KB
C203, C207	Capacitor, 1.1 pF	ATC	ATC800A1R1CT250T
R201	Resistor, 50 ohms	Anaren	C8A50Z4A
U2	Hybrid Coupler	Anaren	X3C07P1-03S

Pinout Diagram (top view)



Source: plated copper heat slug on backside of package

Lead connections for PTGA090304MD

Package Outline Specifications – Package PG-HB1DSO-14-4

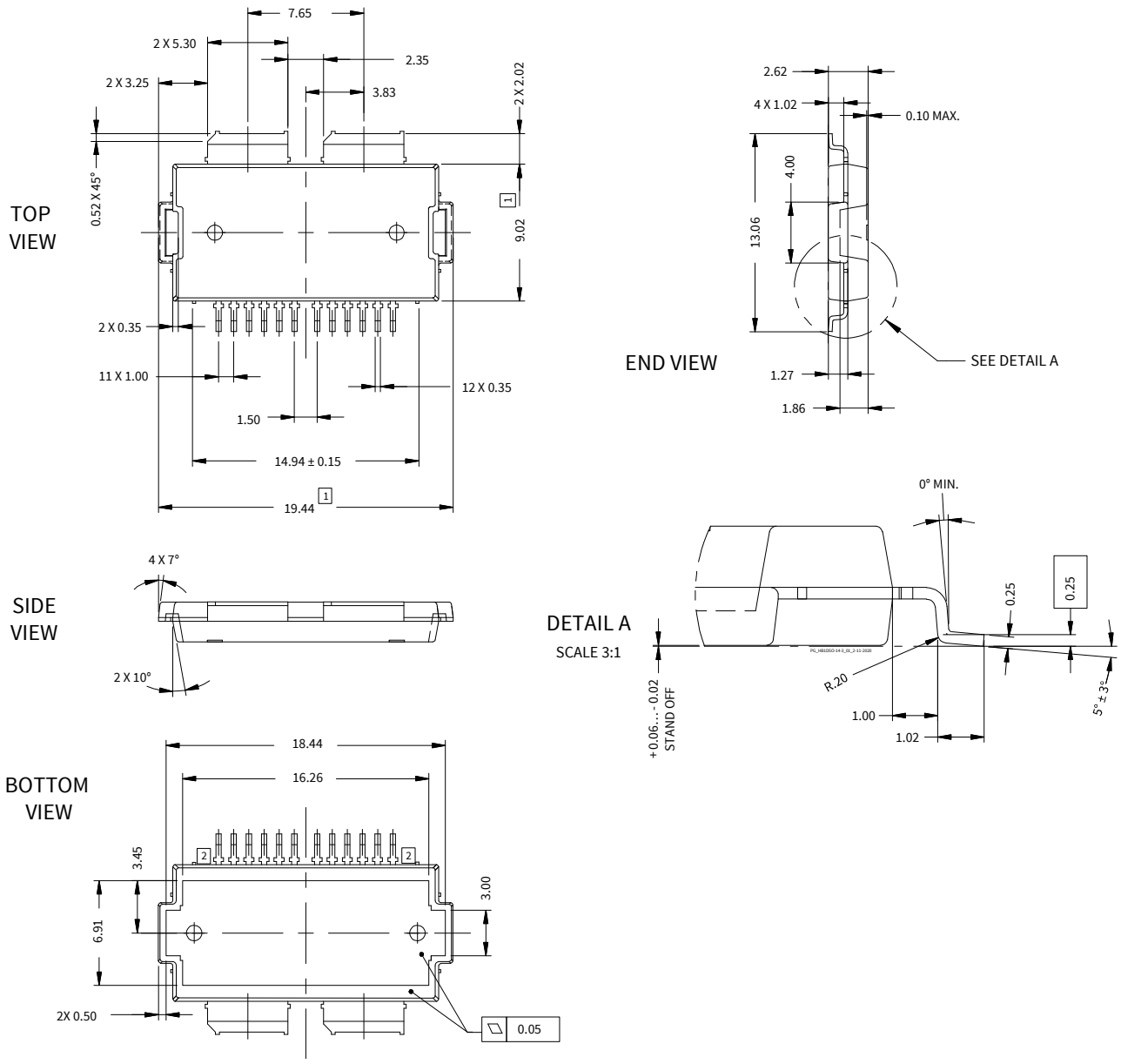


Diagram Notes–unless otherwise specified:

1. Mold/Dam Bar/Metal protusion of 0.30 mm max per side not included.
2. Metal protrusion are connected to source and shall not exceed 0.10 mm max.
3. Fillets and radii: all radii are 0.3 mm max.
4. Interpret dimensions and tolerances per ISO 8015.
5. Dimensions are mm.
6. All tolerances ± 0.1 mm unless specified otherwise.
7. All metal surfaces are tin-plated, except area of cut.
8. Lead thickness: 0.25 mm.

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