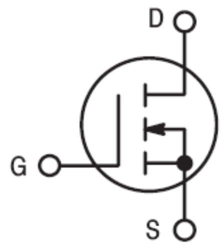
MRF173

The RF MOSFET Line
80W, 175MHz, 28V

M/A-COM Products
Released - Rev. 07.07

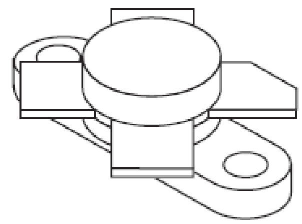
Designed for broadband commercial and military applications up to 200 MHz frequency range. The high–power, high–gain and broadband performance of this device make possible solid state transmitters for FM broadcast or TV channel frequency bands.

N–Channel enhancement mode MOSFET



- Guaranteed performance at 150 MHz, 28 V:
  - Output power = 80 W
  - Gain = 11 dB (13 dB typ.)
  - Efficiency = 55% min. (60% typ.)
- Low thermal resistance
- Ruggedness tested at rated output power
- Nitride passivated die for enhanced reliability
- Low noise figure — 1.5 dB typ at 2.0 A, 150 MHz
- Excellent thermal stability; suited for Class A operation

Product Image



CASE 211–11, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage	V_{DGO}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	9.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	220 1.26	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Temperature Range	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.8	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{DS} = 0 V, V_{GS} = 0 V) I_D = 50 mA	$V_{(BR)DSS}$	65	—	—	V
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	2.0	mA
Gate–Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0 V)	I_{GSS}	—	—	1.0	µA
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 50 mA)	$V_{GS(th)}$	1.0	3.0	6.0	V
Drain–Source On–Voltage ($V_{DS(on)}$, V_{GS} = 10 V, I_D = 3.0 A)	$V_{DS(on)}$	—	—	1.4	V
Forward Transconductance (V_{DS} = 10 V, I_D = 2.0 A)	g_{fs}	1.8	2.2	—	mhos

(continued)

NOTE — CAUTION — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

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ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	—	110	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{oss}	—	105	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{rss}	—	10	—	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DD} = 28 V, f = 150 MHz, I_{DQ} = 50 mA)	NF	—	1.5	—	dB
Common Source Power Gain (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	G_{ps}	11	13	—	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	η	55	60	—	%
Electrical Ruggedness (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA) Load VSWR 30:1 at all phase angles	ψ	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	Z_{in}	—	2.99–j4.5	—	Ohms
Series Equivalent Output Impedance (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	Z_{out}	—	2.68–j1.3	—	Ohms

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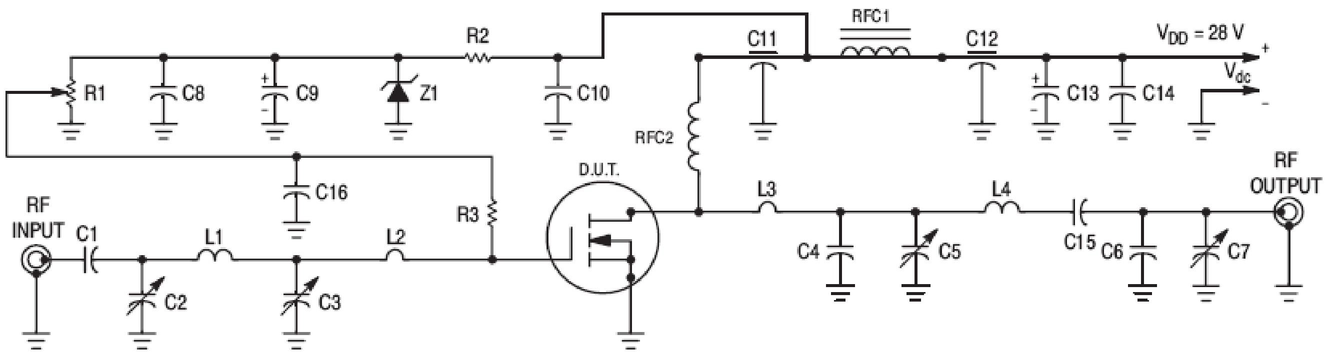

C1, C15 — 470 pF Unelco
C2, C3, C5 — 9–180 pF, Arco 463
C4, C6 — 15 pF, Unelco
C7 — 5–80 pF, Arco 462
C8, C10, C14, C16 — 0.1 μF
C9, C13 — 50 μF, 50 Vdc
C11, C12 — 680 pF, Feed Through
L1 — #16 AWG, 1–1/4 Turns, 0.3″ ID
L2 — #16 AWG Hairpin 1″ long
L3 — #14 AWG Hairpin 0.8″ long
L4 — #14 AWG Hairpin 1.1″ long
RFC1 — Ferroxcube VK200–19/4B
RFC2 — 18 Turns #18 AWG Enameled, 0.3″ ID
R1 — 10 kΩ, 10 Turns Bourns
R2 — 1.8 kΩ, 1/4 W
R3 — 10 kΩ, 1/2 W
Z1 — 1N5925A Motorola Zener

Figure 1. 150 MHz Test Circuit

TYPICAL CHARACTERISTICS

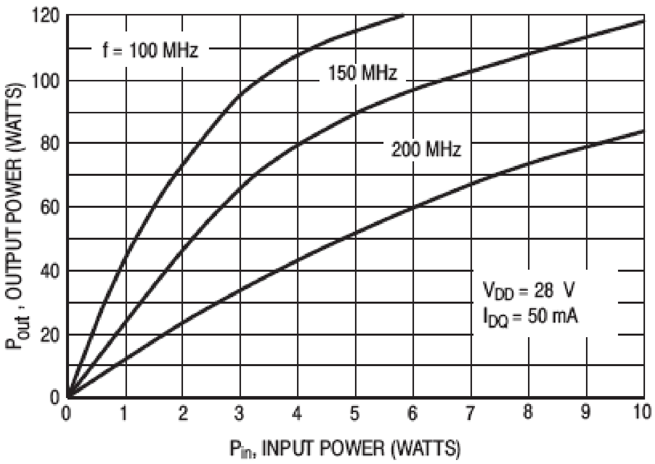

Figure 2. Output Power versus Input Power

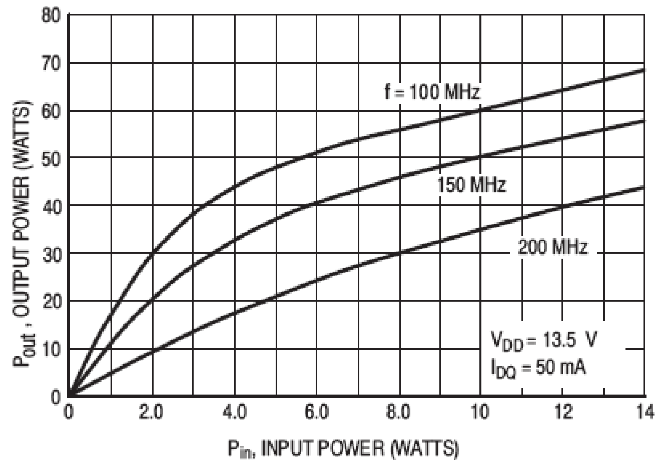

Figure 3. Output Power versus Input Power

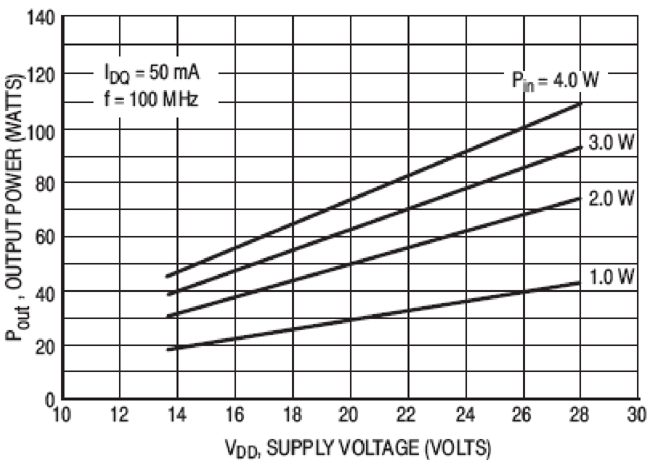

Figure 4. Output Power versus Supply Voltage

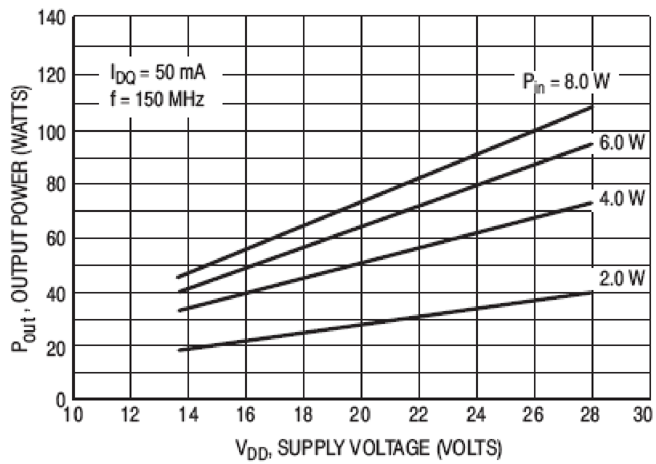

Figure 5. Output Power versus Supply Voltage

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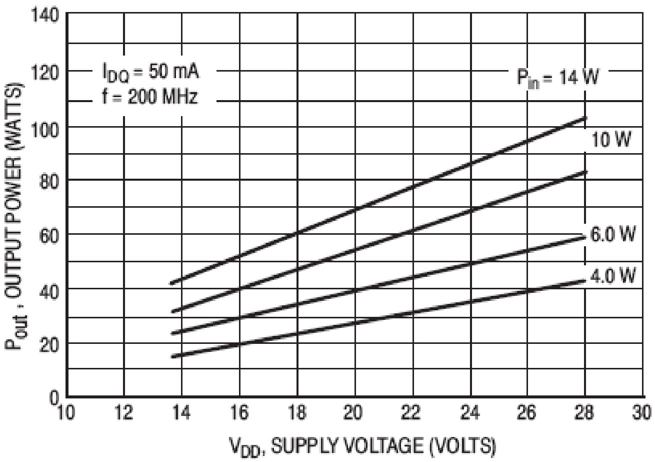

Figure 6. Output Power versus Supply Voltage

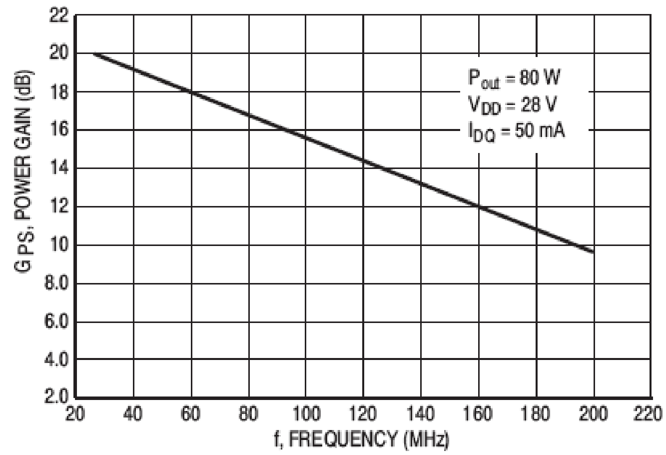

Figure 7. Power Gain versus Frequency

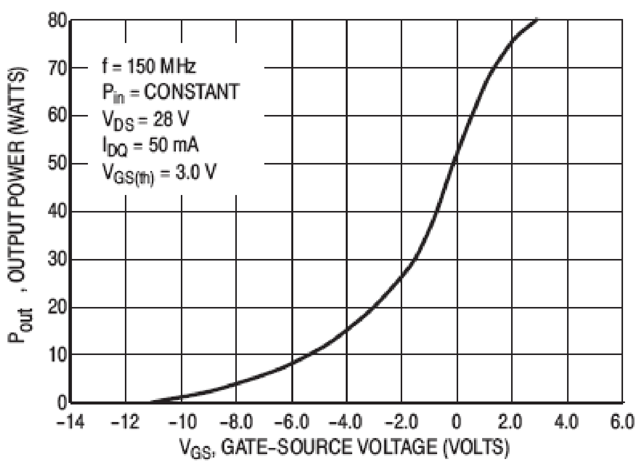

Figure 8. Output Power versus Gate Voltage

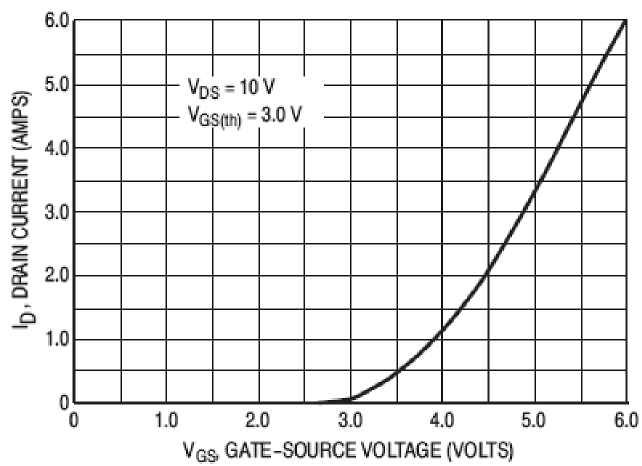

Figure 9. Drain Current versus Gate Voltage

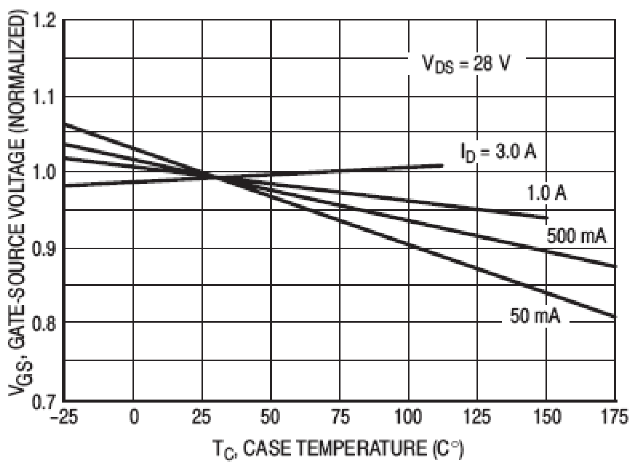

Figure 10. Gate–Source Voltage versus Case Temperature

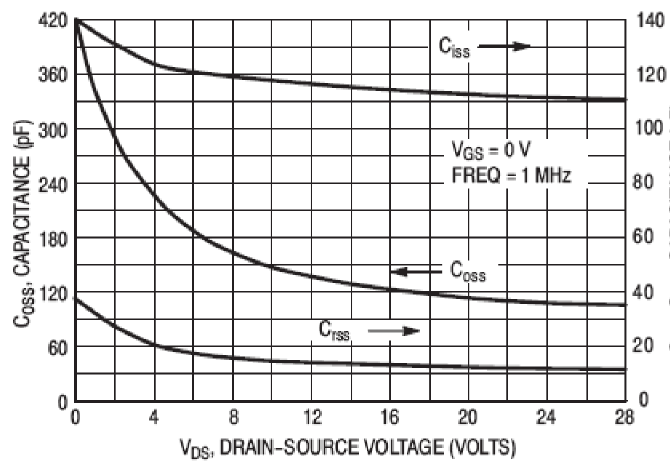

Figure 11. Capacitance versus Drain Voltage

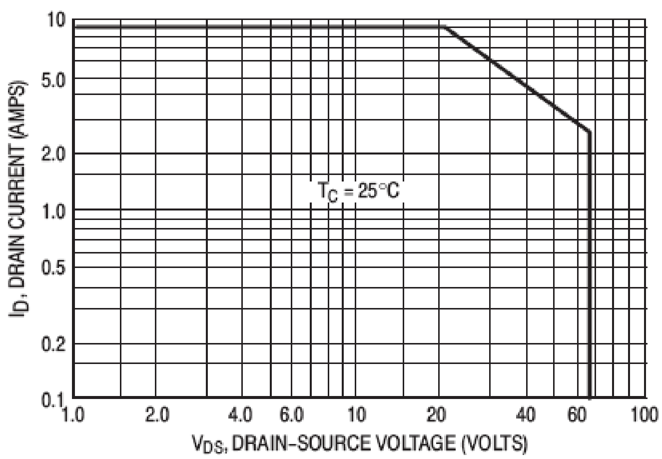

Figure 12. DC Safe Operating Area

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Table 1. Common Source S–Parameters (V_{DS} = 12.5 V, I_D = 4 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
30	0.879	–170	8.09	92	0.014	23	0.839	–174
40	0.883	–173	6.19	87	0.016	24	0.839	–179
50	0.885	–174	4.94	84	0.016	28	0.853	–178
60	0.885	–175	4.21	81	0.017	30	0.845	180
70	0.888	–176	3.57	77	0.017	34	0.849	179
80	0.888	–177	3.06	77	0.017	37	0.852	–179
90	0.888	–178	2.71	76	0.018	42	0.842	–179
100	0.890	–178	2.45	72	0.019	43	0.858	180
110	0.888	–179	2.28	70	0.020	46	0.859	179
120	0.892	–179	2.02	69	0.021	50	0.872	–180
130	0.893	–179	1.84	67	0.022	52	0.870	–179
140	0.894	–180	1.73	66	0.023	55	0.880	–180
150	0.896	–180	1.58	64	0.024	55	0.887	180
160	0.896	180	1.51	61	0.026	56	0.863	180
170	0.898	179	1.38	60	0.026	60	0.850	179
180	0.899	179	1.28	58	0.028	60	0.871	179
190	0.899	179	1.25	57	0.030	62	0.890	178
200	0.902	179	1.15	55	0.030	63	0.884	178
210	0.902	179	1.12	53	0.032	63	0.899	178
220	0.904	178	1.08	51	0.034	65	0.893	178
230	0.907	178	0.97	49	0.037	65	0.941	176
240	0.907	178	0.95	48	0.037	65	0.884	176
250	0.909	178	0.90	49	0.039	67	0.896	177
260	0.911	177	0.85	48	0.039	68	0.888	176
270	0.909	177	0.83	46	0.042	68	0.895	176
280	0.913	177	0.78	45	0.044	69	0.893	175
290	0.914	177	0.74	42	0.044	69	0.882	174
300	0.915	176	0.74	42	0.047	72	0.877	175
310	0.917	176	0.70	41	0.048	73	0.909	176
320	0.916	176	0.69	39	0.052	71	0.912	175
330	0.917	176	0.65	37	0.055	71	0.885	173
340	0.919	176	0.65	38	0.055	70	0.898	173
350	0.919	175	0.62	36	0.057	72	0.887	174
360	0.920	175	0.60	37	0.059	72	0.918	172
370	0.921	175	0.57	35	0.061	71	0.929	172
380	0.923	175	0.56	34	0.063	71	0.900	172
390	0.925	175	0.54	36	0.065	71	0.907	171
400	0.926	174	0.51	34	0.067	75	0.902	173
410	0.927	174	0.51	33	0.070	73	0.942	170
420	0.929	174	0.49	31	0.071	71	0.926	169
430	0.929	173	0.46	32	0.072	72	0.901	170
440	0.930	173	0.45	32	0.076	73	0.904	170

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Table 1. Common Source S–Parameters (V_{DS} = 12.5 V, I_D = 4 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
450	0.932	173	0.45	29	0.079	75	0.924	170
460	0.932	172	0.44	30	0.082	71	0.938	167
470	0.933	172	0.42	30	0.081	73	0.908	168
480	0.931	172	0.42	29	0.086	72	0.933	168
490	0.931	171	0.41	28	0.089	72	0.926	167
500	0.931	171	0.41	27	0.092	71	0.936	167

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Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 4 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
30	0.840	–163	11.48	92	0.016	20	0.718	–169
40	0.849	–167	8.80	86	0.017	22	0.713	–174
50	0.853	–170	6.99	82	0.017	24	0.748	–174
60	0.854	–171	5.92	79	0.017	23	0.746	–175
70	0.859	–172	5.00	74	0.018	25	0.746	–175
80	0.859	–174	4.29	73	0.018	30	0.741	–174
90	0.861	–174	3.77	71	0.019	38	0.735	–174
100	0.866	–175	3.39	67	0.018	40	0.768	–176
110	0.865	–175	3.12	64	0.018	41	0.782	–177
120	0.871	–176	2.75	63	0.019	42	0.794	–175
130	0.875	–176	2.49	60	0.021	45	0.783	–172
140	0.877	–177	2.31	59	0.023	51	0.776	–175
150	0.883	–177	2.10	56	0.023	55	0.806	–176
160	0.884	–177	1.99	53	0.023	58	0.807	–176
170	0.886	–178	1.82	51	0.023	61	0.806	–176
180	0.890	–178	1.66	49	0.025	59	0.820	–175
190	0.891	–179	1.62	48	0.027	60	0.815	–176
200	0.896	–179	1.47	46	0.030	63	0.819	–177
210	0.898	–179	1.41	43	0.031	67	0.842	–178
220	0.901	–179	1.36	41	0.032	70	0.855	–178
230	0.905	–180	1.22	38	0.033	70	0.906	–178
240	0.906	–180	1.19	38	0.034	67	0.845	–178
250	0.909	180	1.11	39	0.037	68	0.831	–178
260	0.913	180	1.03	37	0.038	70	0.837	–180
270	0.912	179	0.10	35	0.041	72	0.859	179
280	0.916	179	0.93	34	0.042	74	0.876	178
290	0.918	179	0.88	31	0.041	73	0.865	179
300	0.919	178	0.87	31	0.044	74	0.837	–180
310	0.922	178	0.83	31	0.046	74	0.863	180
320	0.922	178	0.80	27	0.051	73	0.879	177
330	0.924	177	0.75	26	0.054	74	0.878	176
340	0.926	177	0.74	27	0.053	74	0.897	177
350	0.926	177	0.71	24	0.054	77	0.879	179

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 4 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
360	0.927	177	0.68	26	0.056	75	0.888	177
370	0.929	177	0.64	24	0.058	73	0.893	175
380	0.931	176	0.62	23	0.062	72	0.885	174
390	0.934	176	0.60	25	0.064	74	0.903	174
400	0.934	176	0.57	22	0.065	78	0.898	177
410	0.936	175	0.56	21	0.068	77	0.931	175
420	0.938	175	0.53	20	0.070	74	0.906	173
430	0.938	174	0.51	21	0.072	73	0.885	173
440	0.939	174	0.49	21	0.075	75	0.895	172
450	0.941	174	0.48	19	0.080	78	0.923	172
460	0.941	173	0.47	19	0.082	75	0.940	171
470	0.942	173	0.45	18	0.080	75	0.904	172
480	0.940	173	0.44	18	0.083	74	0.910	171
490	0.940	172	0.43	18	0.088	72	0.906	169
500	0.940	172	0.42	17	0.092	72	0.927	168

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DESIGN CONSIDERATIONS

The MRF173 is a RF MOSFET power N–channel enhancement mode field–effect transistor (FET) designed for VHF power amplifier applications. M/A-COM RF MOSFETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V–groove power FETs.

M/A-COM Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF173 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (IDQ) is not critical for many applications. The MRF173 was characterized at IDQ = 50 mA, which is the suggested minimum value of IDQ. For special applications such as linear amplification, IDQ may have to be selected to optimize the critical parameters.

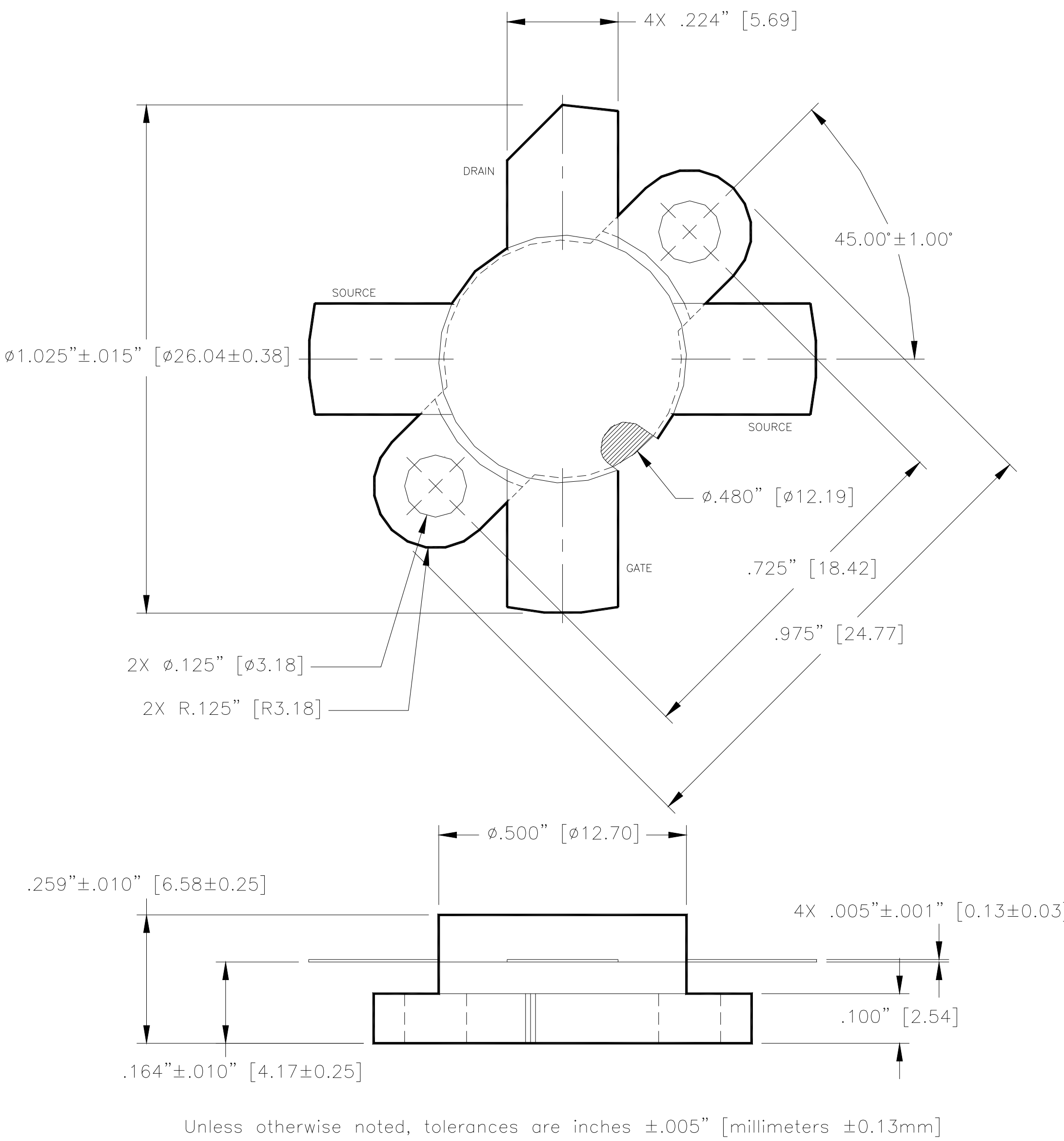
The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF173 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.
(see Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF173. See M/A-COM Application Note AN721`, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of RF MOSFETs helps ease the task of broadband network design. Both small–signal scattering parameters and large–signal impedances are provided. While the s–parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF MOS power FETs.



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