Features

- Saturated Power: 18 W
- Drain Efficiency: 70%
- Small Signal Gain: 12.5 dB
- Lead-Free Air Cavity Ceramic Package
- RoHS* Compliant

440196 440166

Applications

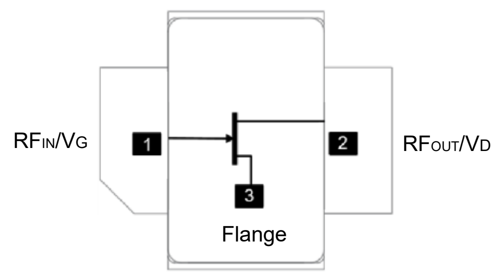
- Avionics - TACAN, DME, IFF
- Military Radio
- L, S, C-band Radar
- Electronic Warfare
- ISM
- General Amplification

Description

The MAPC-A3006-AB/AS is a 18 W packaged, unmatched transistor utilizing a high performance, 0.15 µm GaN on SiC production process. This transistor supports both defense and commercial related applications.

Offered in a thermally-enhanced flange package, the MAPC-A3006-AB/AS provides superior performance under CW operation allowing customers to improve SWaP-C benchmarks in their next generation systems.

Functional Schematic



Typical RF Performance:

- Measured at CW = P_{SAT}, defined at I_{GS} = 0.36 mA, V_{DS} = 28 V, I_{DQ} = 100 mA, T_C = 25°C

Frequency (GHz)	Output Power (dBm)	Gain (dB)	η_D (%)
3.4	43.8	14.2	74.4
3.7	42.5	12.5	70.5
4.0	42.3	12.2	56.4

Pin Configuration

Pin #	Pin Name	Function
1	RF_{IN} / V_G	RF Input / Gate
2	RF_{OUT} / V_D	RF Output / Drain
3	Flange[1]	Ground / Source

1. The flange on the package bottom must be connected to RF, DC and thermal ground.

Ordering Information

Part Number	MOQ Increment
MAPC-A3006-AB000	Bulk Quantity: Boltdown
MAPC-A3006-AS000	Bulk Quantity: Earless
MAPC-A3006-ABSB1	Sample Board: Both

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

RF Electrical Specifications: Frequency = 3.7 GHz, P_{SAT} @ I_{GS} = 0.36 mA, T_A = +25C, V_{DS} = 28 V, I_{DQ} = 100 mA, Low Power Gain tested at Input Power of 10 dBm

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Units
Saturated Power	V_{DD} = 28 V, CW	P_{SAT}	14.8	17.5	-	W
Drain Efficiency	V_{DD} = 28 V, CW	η_{SAT}	74	77	-	%
Low Power Gain	V_{DD} = 28 V, P_{IN} = 10 dBm, CW	G_{SS}	15.3	16.2	-	dB

Note: Final testing and screening for all transistor sales is performed using the MAPC-A3006-ABSB1 at 3.7 GHz.

Absolute Maximum Ratings[2,3]

Parameter	Absolute Maximum
Drain-Source Voltage	84 V
Gate Voltage	-10, +2 V
Drain Current	4.6 A
Gate Current	3.6 mA
Input Power	30.5 dBm
Storage Temperature	-55°C to +150°C
Mounting Temperature	+245°C
Junction Temperature[3,4,5]	+225°C
Operating Temperature	-40°C to +85°C

2. Exceeding any one or combination of these limits may cause permanent damage to this device.
3. MACOM does not recommend sustained operation near these survivability limits.
4. Operating at nominal conditions with $T_J \le$ +225 °C will ensure MTTF > 1 x 10^6 hours.
5. Junction Temperature (T_J) = T_C + Ɵjc * (V * I)
   Typical thermal resistance (Ɵjc) = 7.83 °C/W for CW.
   a) For T_C = +25°C,
      T_J = 91 °C @ P_{DISS} = 8.4 W
   b) For T_C = +85°C,
      T_J = 153 °C @ P_{DISS} = 8.7 W

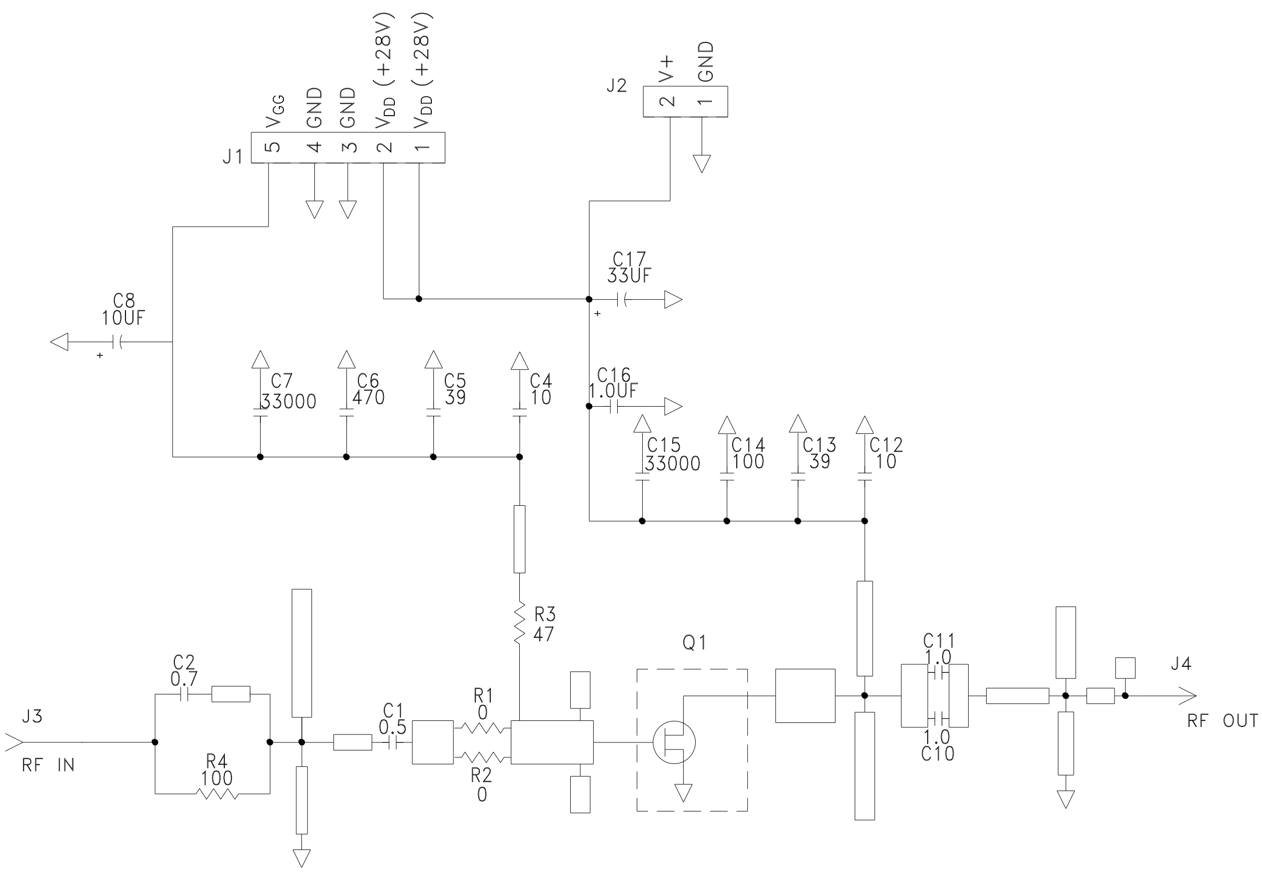
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Evaluation Test Fixture and Recommended Tuning Solution, 3.4 - 4.0 GHz



Description

Parts measured on evaluation board (20-mil thick RO4350). Matching is provided using a combination of lumped elements and transmission lines as shown in the simplified schematic above. Recommended tuning solution component placement, transmission lines, and details are shown on the next page.

Biasing Sequence

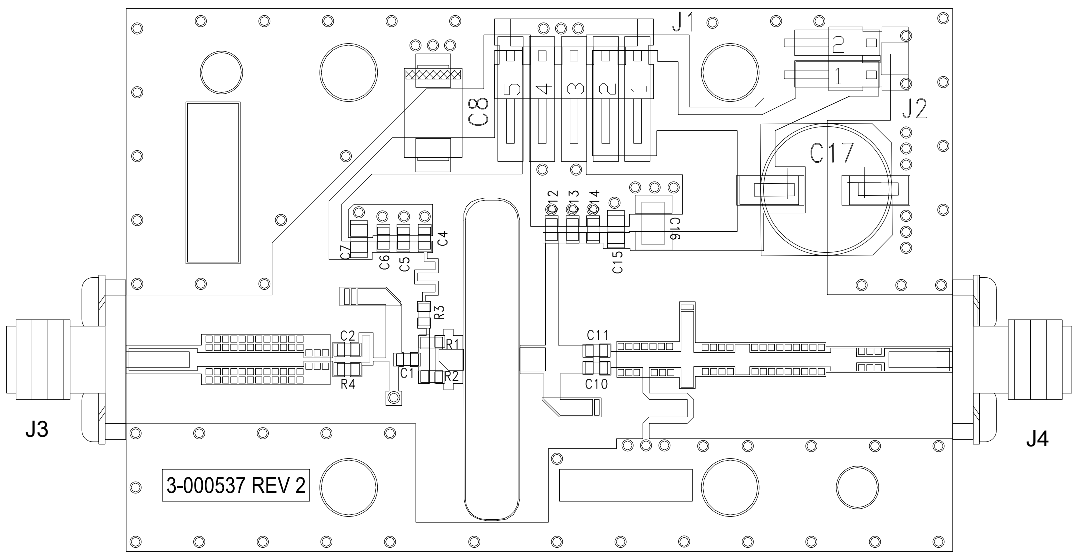
Bias ON

1. Ensure RF is turned off
2. Apply pinch-off voltage of -5 V to the gate
3. Apply nominal drain voltage
4. Bias gate to desired quiescent drain current
5. Apply RF

Bias OFF

1. Turn RF off
2. Apply pinch-off voltage of -5 V to the gate
3. Turn-off drain voltage
4. Turn-off gate voltage

Evaluation Test Fixture and Recommended Tuning Solution, 3.4 - 4.0 GHz



Assembly Parts List

Reference Designator	Description	Qty.
C1	Cap, 0.5 pF, ±0.05pF, 0603, ATC	1
C2	Cap, 0.7 pF, ±0.1pF, 0603, ATC	1
C4, C12	Cap, 10 pF, ±5%, 0603, ATC	2
C5, C13	Cap, 39 pF, ±5%, 0603, ATC	2
C6	Cap, 470 pF, ±5%, 100V, 0603	1
C7, C15	CAP, 33000 pF, 0805,100V, X7R	2
C8	Cap, 10 µF, 16V, Tantalum, 2312	1
C10, C11	Cap, 1 pF, ±0.1pF, 0603, ATC	2
C14	Cap, 100 pF, ±5%, 0603, ATC	1
C16	Cap, 1 µF, 100V, ±10%, X7R, 1210	1
C17	Cap, 33 µF, ±20%, G CASE	1
R1, R2	Res, 0 Ω, ±1%, 0603, 1/16W	2
R3	RES, 47 Ω, ±1%, 0603, 1/16W	1
R4	RES, 100 Ω, ±1%, 0603, 1/16W	1
J1	Header, 5POS, 0.1in Pitch, 105°C, 250V	1
J2	Header, 2POS, 0.1in Pitch, 105°C, 250V	1
J3, J4	SMA Connector, Panel Jack, Post Contact, DC-18GHz, 50Ω, 0.05in	2
-	PCB, RO4350B, Er = 3.48, h = 20 mil	1
Q1	MAPC-A3006-AB/AS	1

Typical Performance Curves as Measured in the 3.4 - 4.0 GHz Evaluation Test Fixture

CW, P_{SAT} @ I_{GS} = 0.36 mA, V_{DS} = 28 V, I_{DQ} = 100 mA, Frequency = 3.7 GHz (Unless Otherwise Noted)
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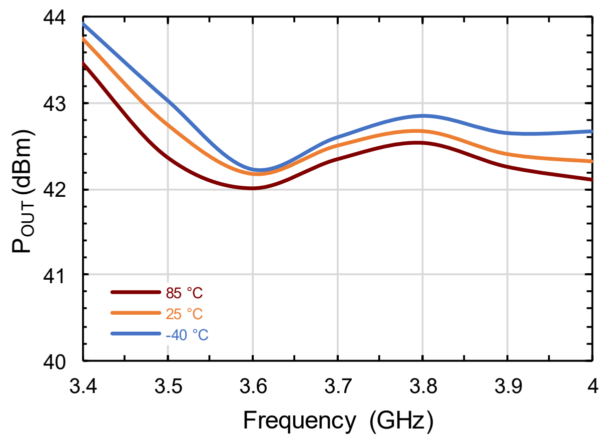
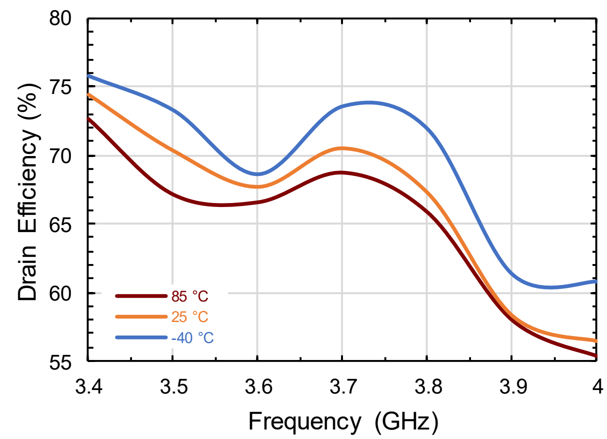
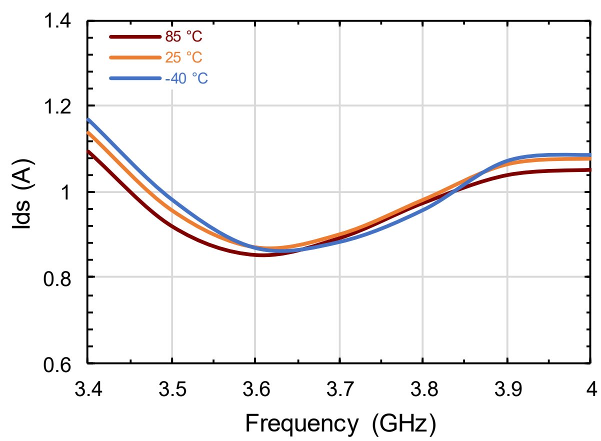
Output Power vs. Temperature and Frequency



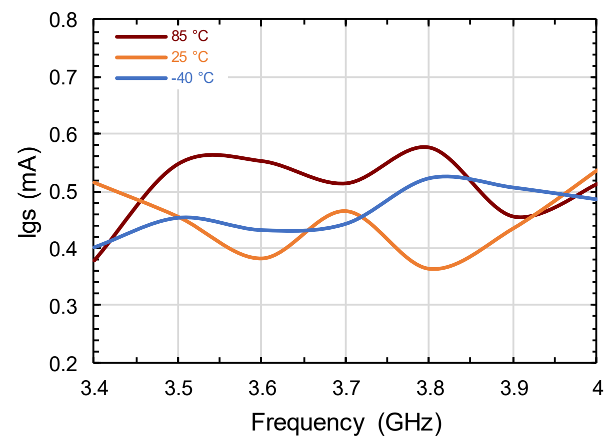
Drain Efficiency vs. Temperature and Frequency



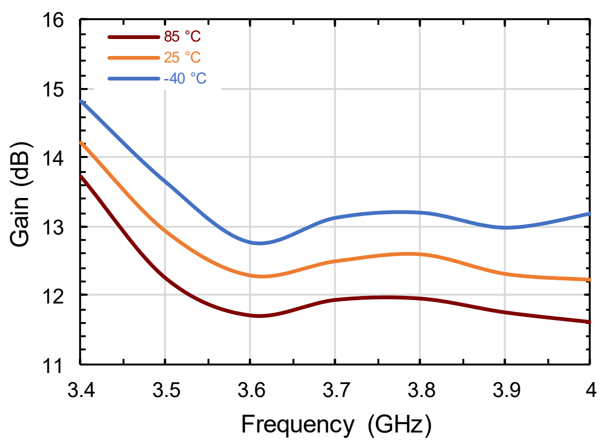
Drain Current vs. Temperature and Frequency



Gate Current vs. Temperature and Frequency



Large Signal Gain vs. Temperature and Frequency



Typical Performance Curves as Measured in the 3.4 - 4.0 GHz Evaluation Test Fixture

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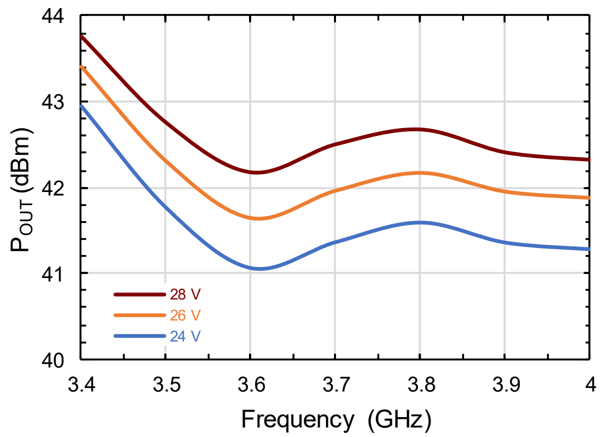
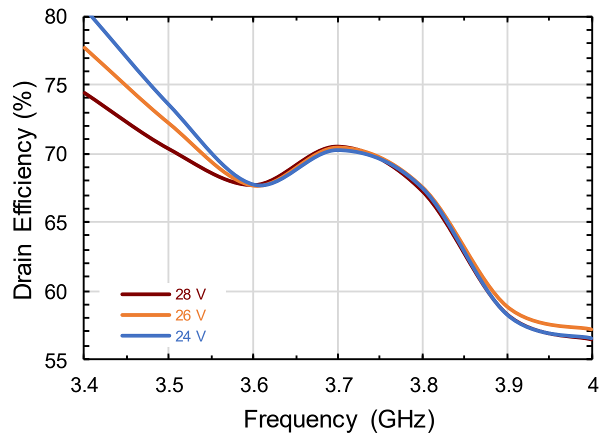
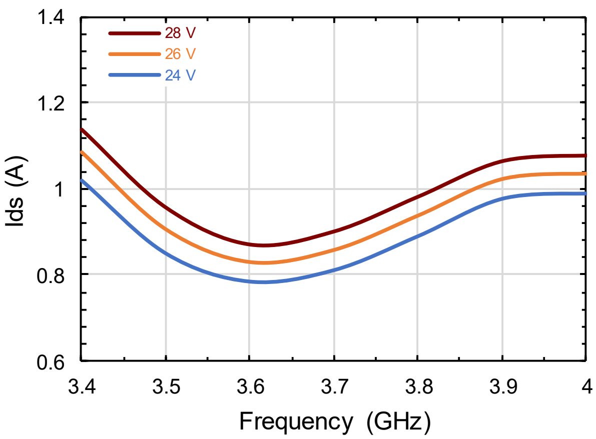
Output Power vs. V_{DS} and Frequency



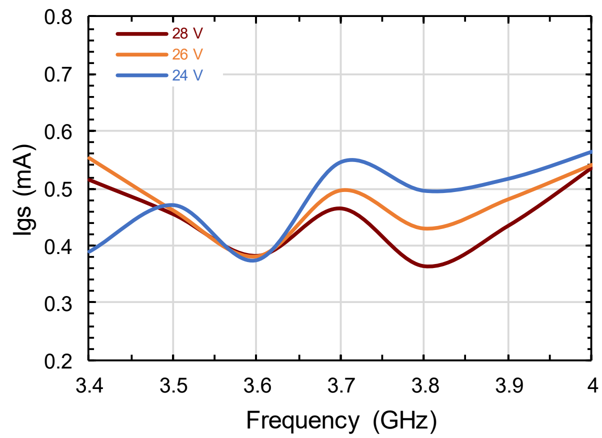
Drain Efficiency vs. V_{DS} and Frequency



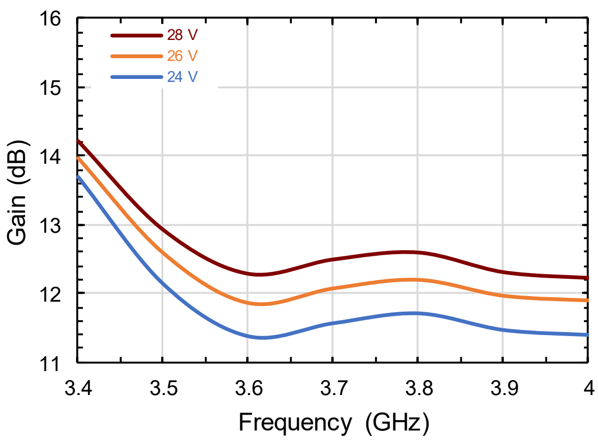
Drain Current vs. V_{DS} and Frequency



Gate Current vs. V_{DS} and Frequency



Large Signal Gain vs. V_{DS} and Frequency



Typical Performance Curves as Measured in the 3.4 - 4.0 GHz Evaluation Test Fixture

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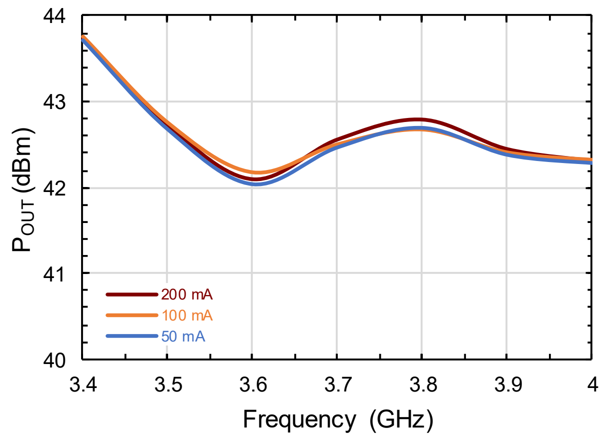
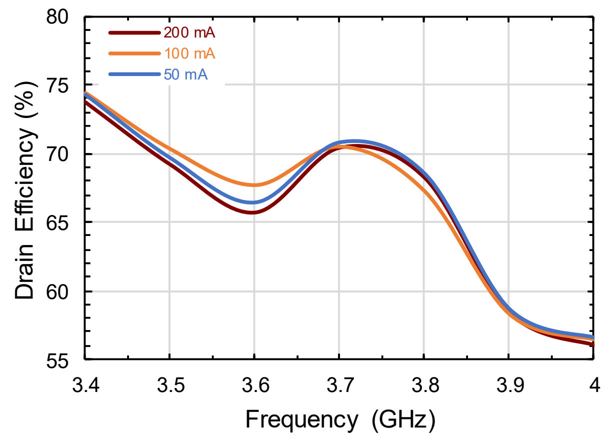
Output Power vs. I_{DQ} and Frequency



Drain Efficiency vs. I_{DQ} and Frequency



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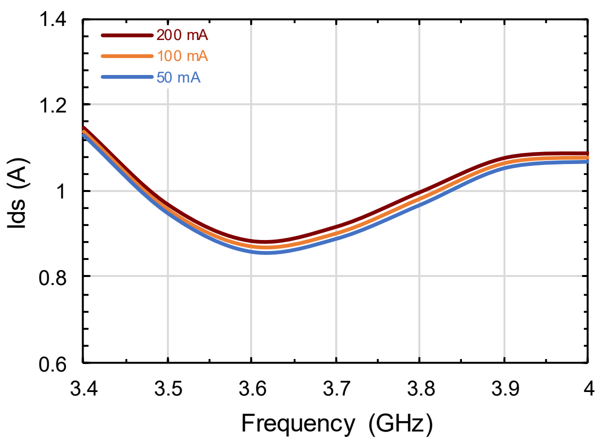

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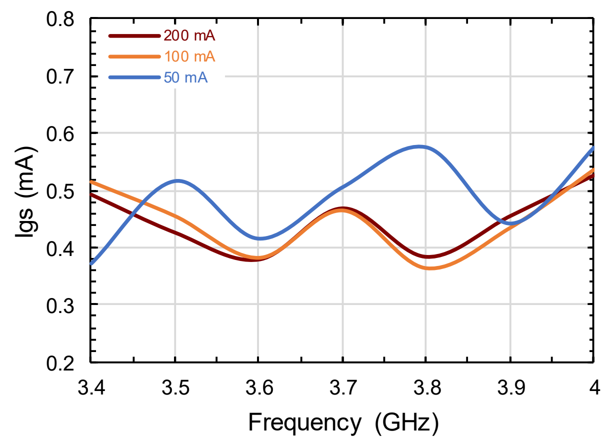

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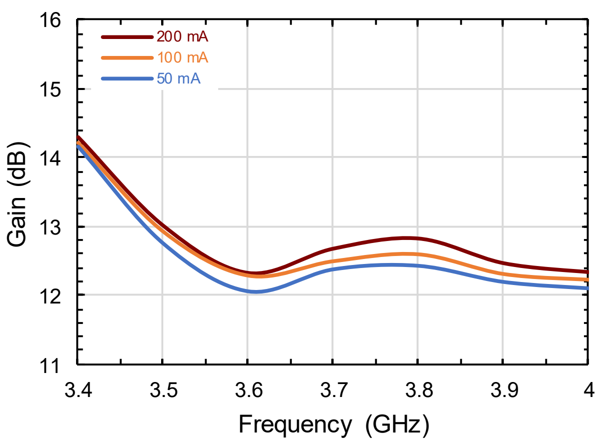

Typical Performance Curves as Measured in the 3.4 - 4.0 GHz Evaluation Test Fixture

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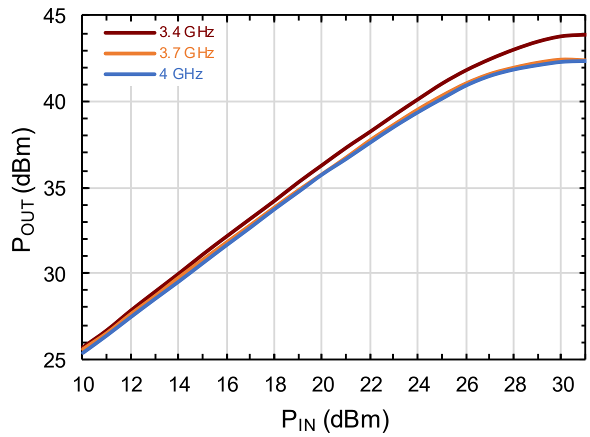
Output Power vs. Frequency and P_{IN}



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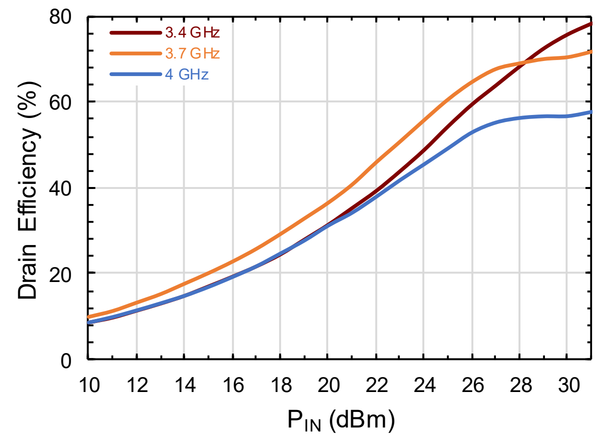

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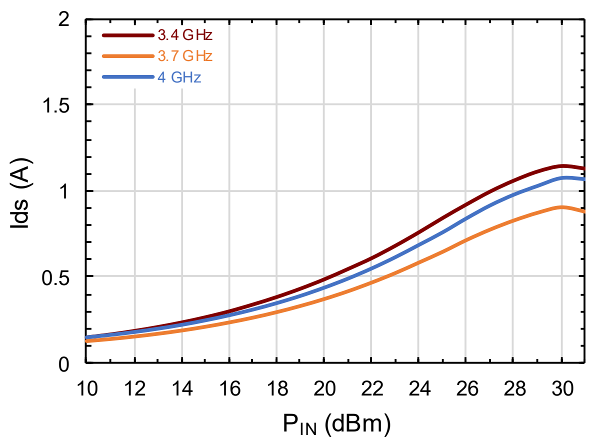

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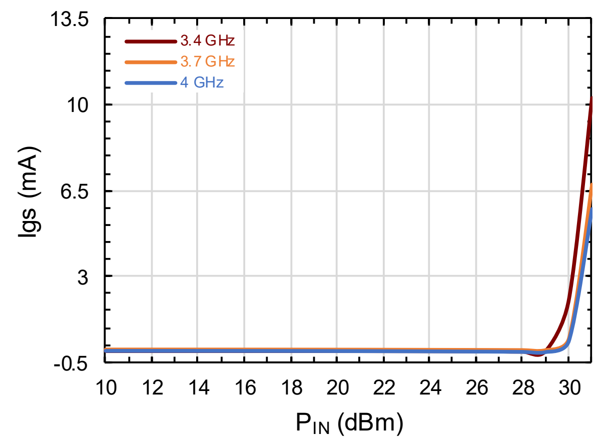

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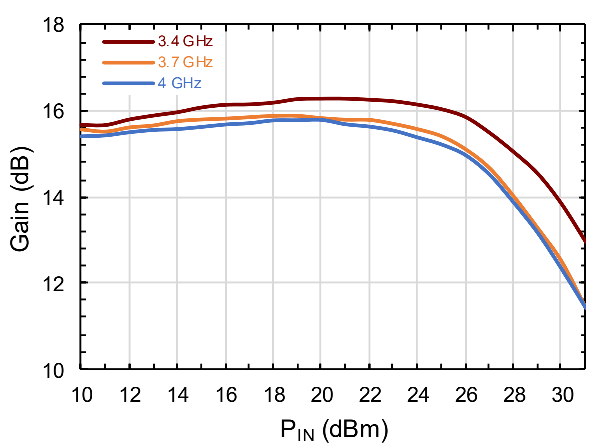

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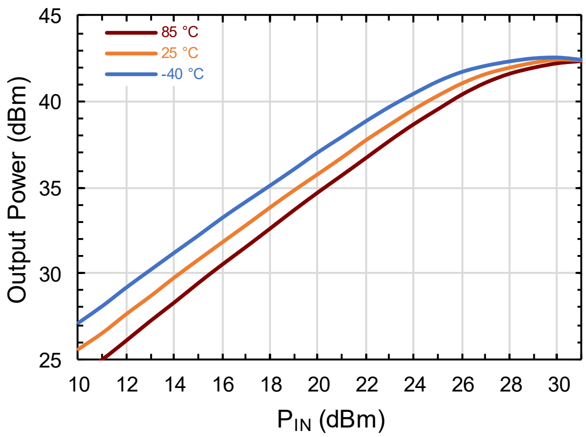
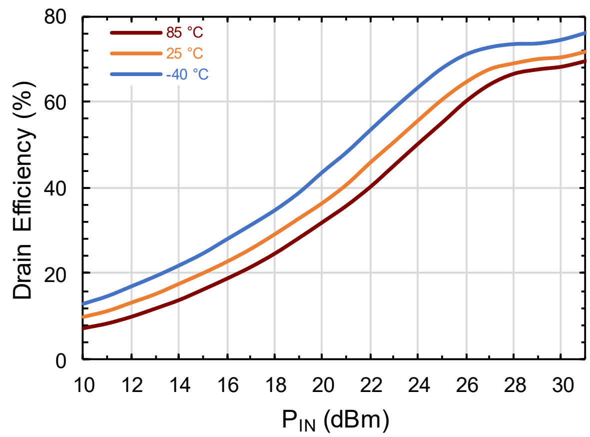


Drain Efficiency vs. Temperature and P_{IN}



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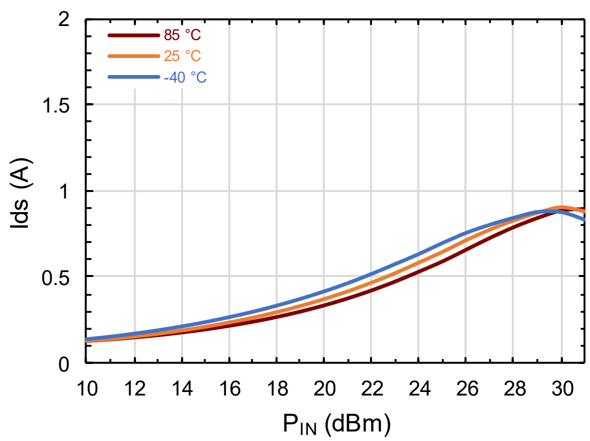
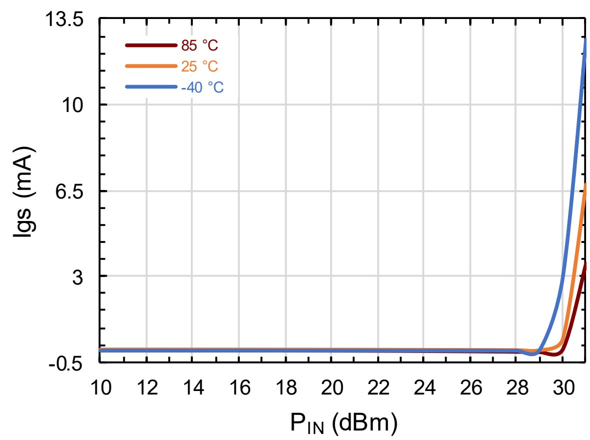


Gate Current vs. Temperature and P_{IN}



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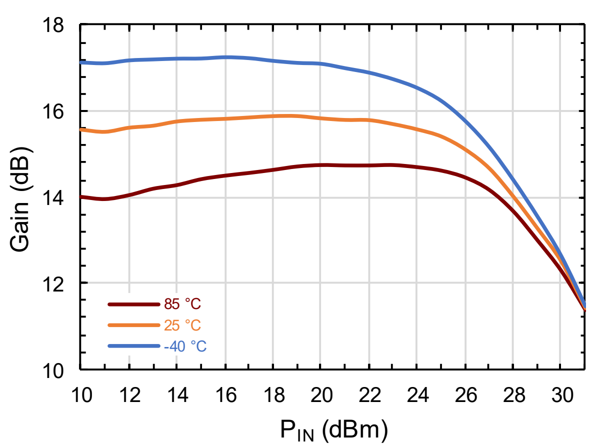

Typical Performance Curves as Measured in the 3.4 - 4.0 GHz Evaluation Test Fixture

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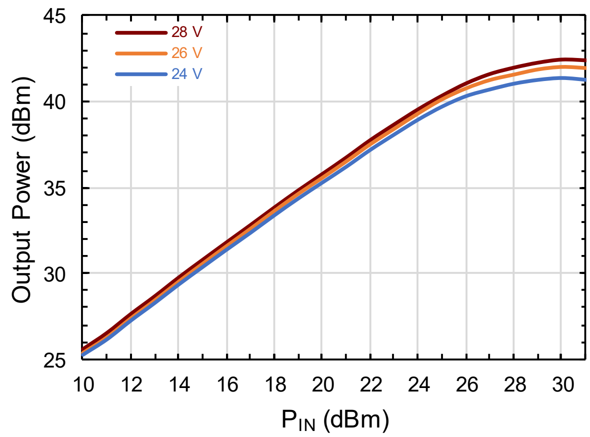
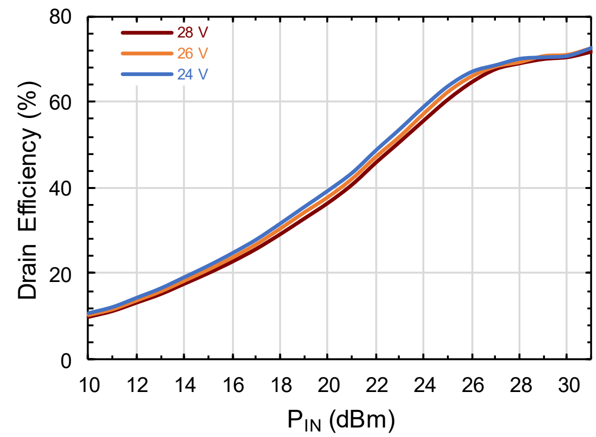


Drain Efficiency vs. V_{DS} and P_{IN}



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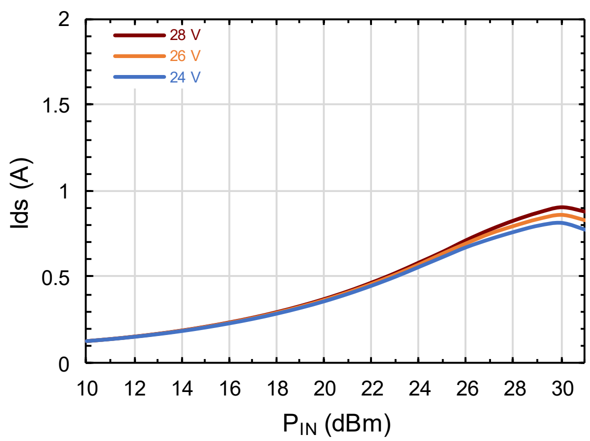

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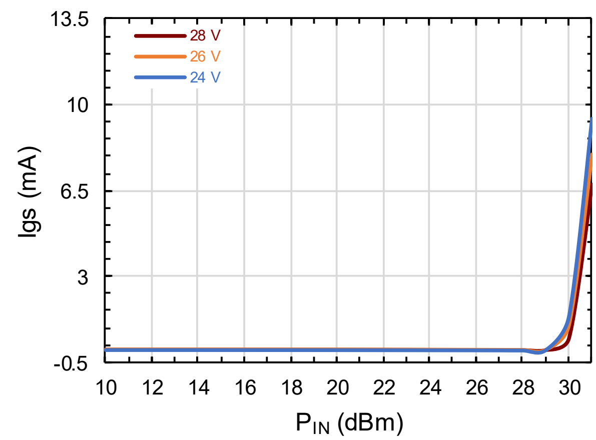

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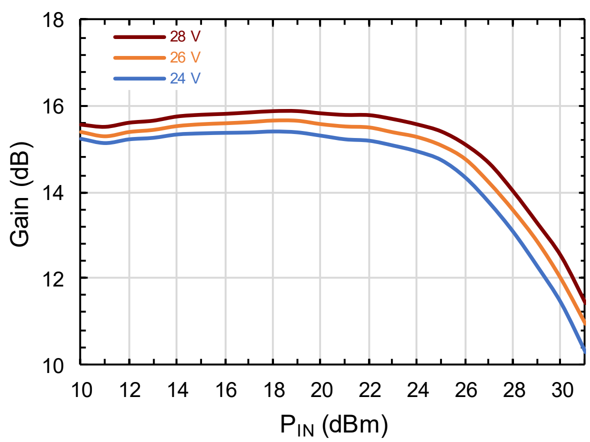

Typical Performance Curves as Measured in the 3.4 - 4.0 GHz Evaluation Test Fixture
CW, P_{SAT} @ I_{GS} = 0.36 mA, V_{DS} = 28 V, I_{DQ} = 100 mA, Frequency = 3.7 GHz (Unless Otherwise Noted)
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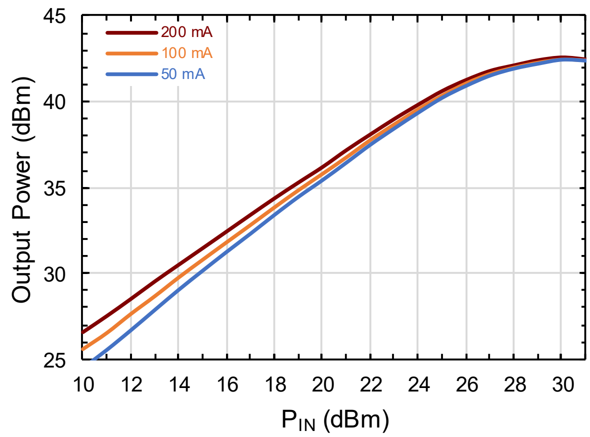
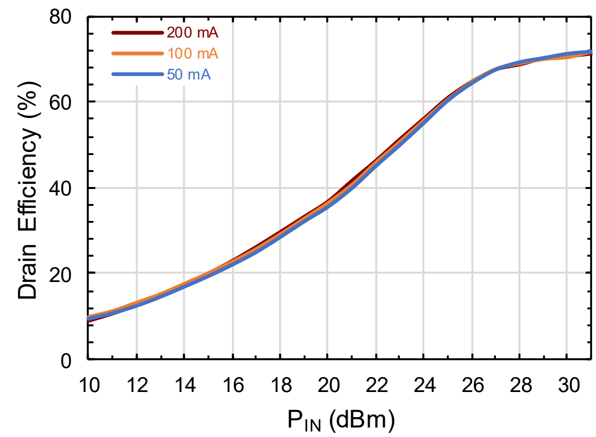
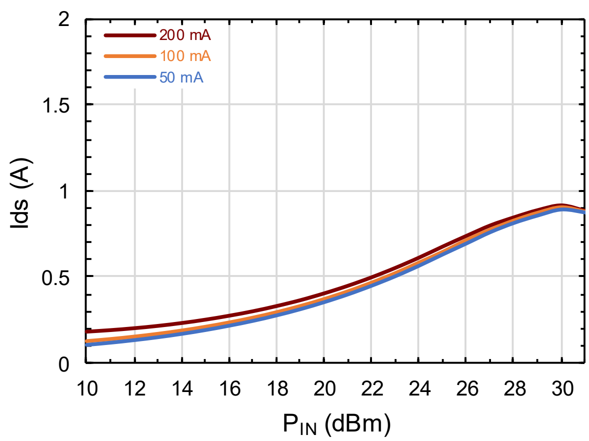


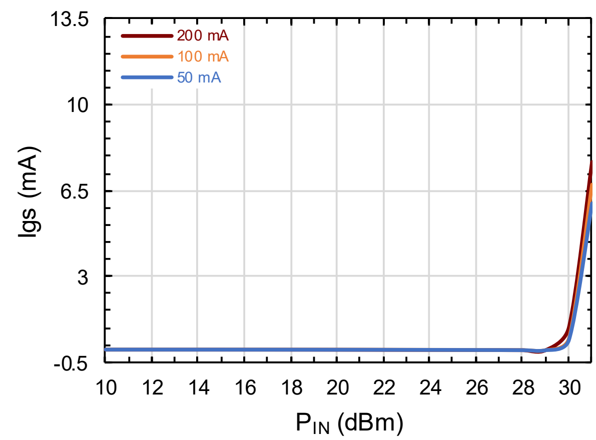
Drain Efficiency vs. I_{DQ} and P_{IN}



Drain Current vs. I_{DQ} and P_{IN}



Gate Current vs. I_{DQ} and P_{IN}



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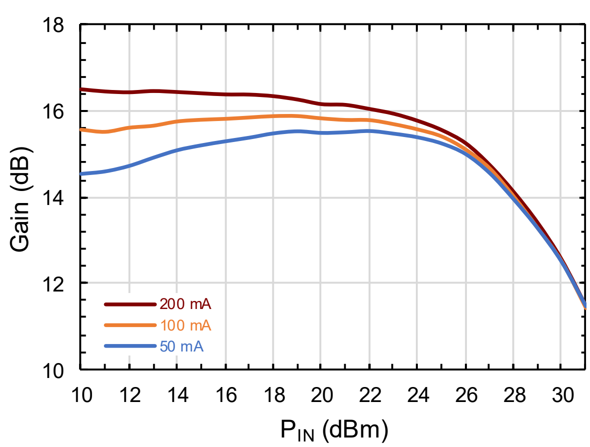

Typical Performance Curves as Measured in the 3.4 - 4.0 GHz Evaluation Test Fixture:

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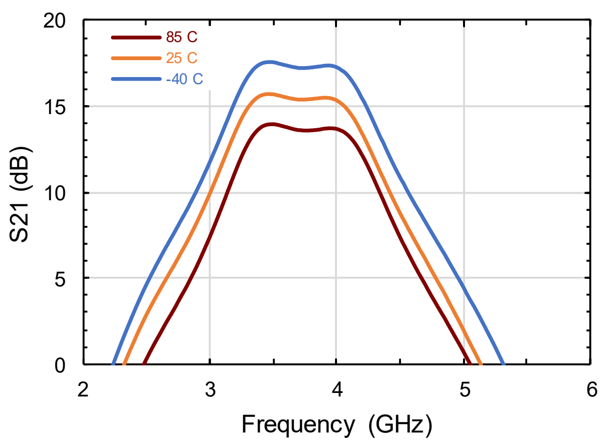
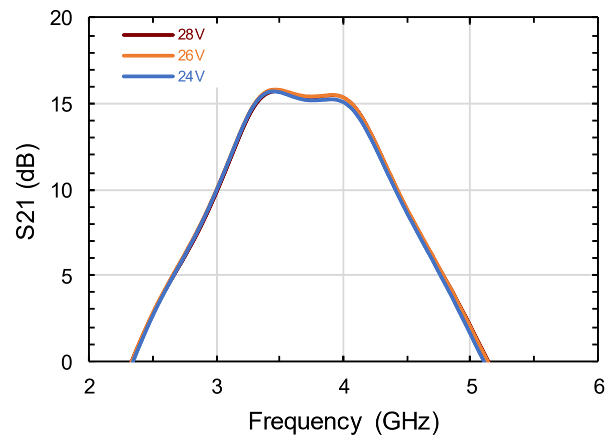
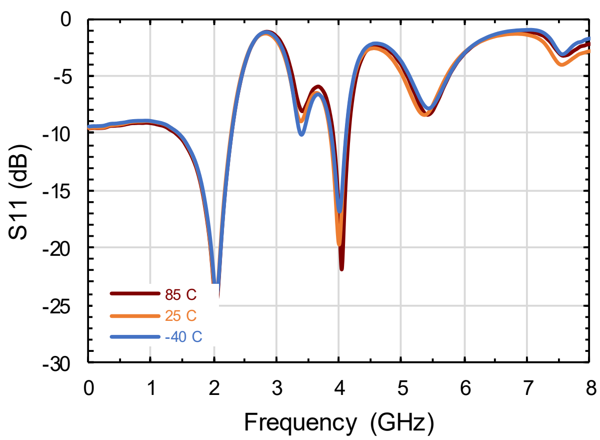
S21 vs Frequency and Temperature



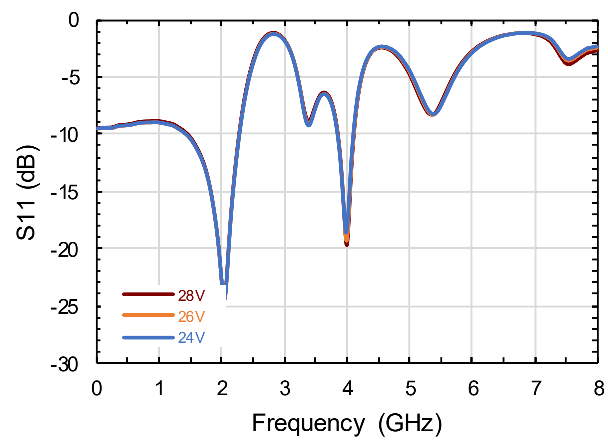
S21 vs Frequency and V_{DS}



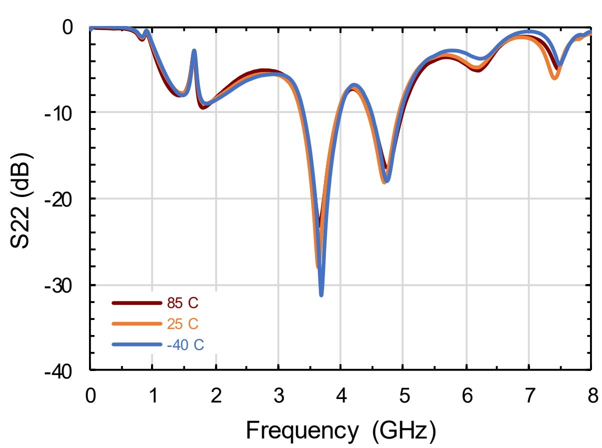
S11 vs Frequency and Temperature



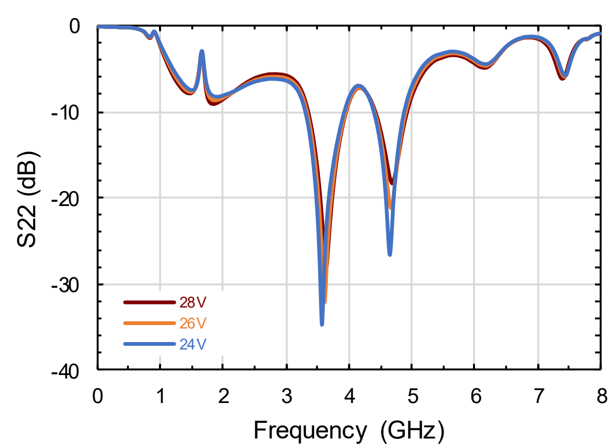
S11 vs Frequency and V_{DS}



S22 vs Frequency and Temperature



S22 vs Frequency and V_{DS}



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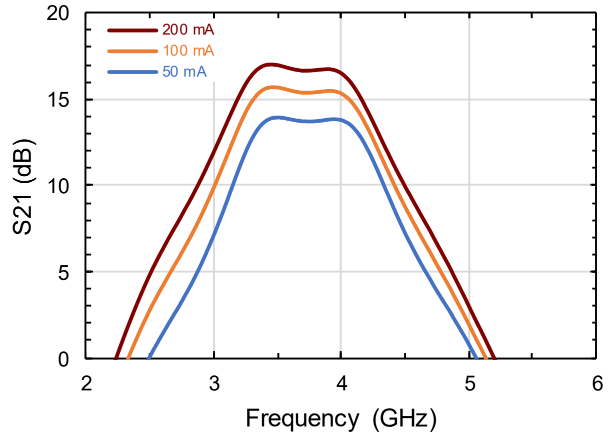
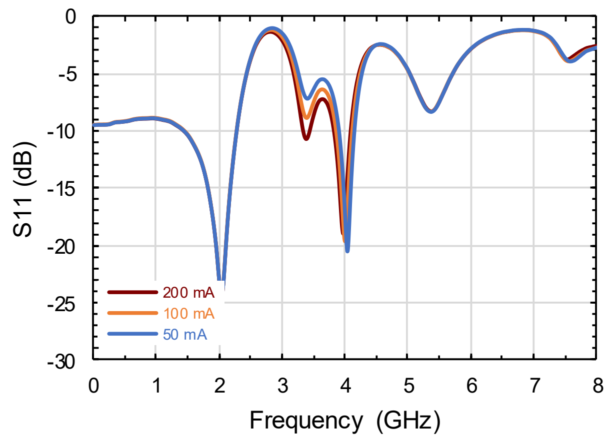
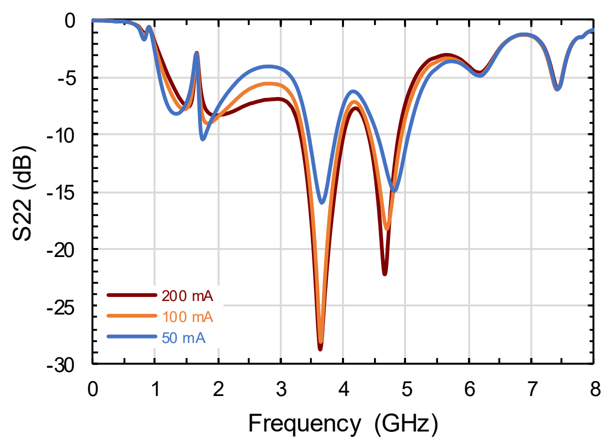
S21 vs Frequency and I_{DQ}



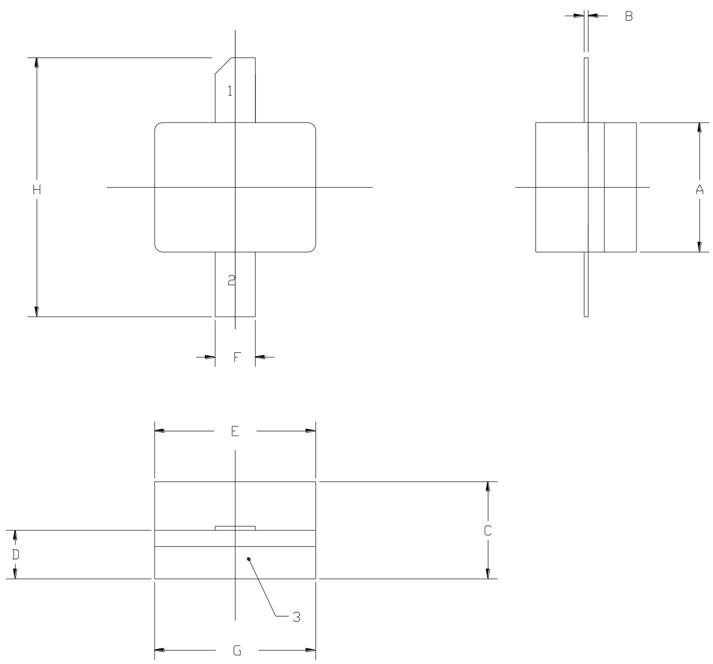
S11 vs Frequency and I_{DQ}



S22 vs Frequency and I_{DQ}



Lead-free 440196 Package Dimensions



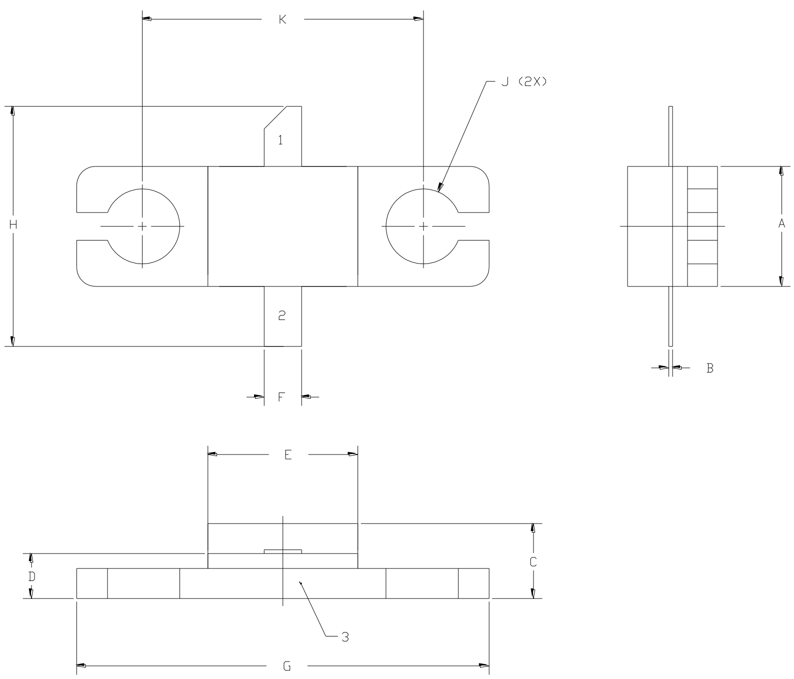
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.
5. ALL PLATED SURFACES ARE NI/AU

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.155	0.165	3.94	4.19
B	0.003	0.006	0.10	0.15
C	0.115	0.135	2.92	3.17
D	0.057	0.067	1.45	1.70
E	0.195	0.205	4.95	5.21
F	0.045	0.055	1.14	1.40
G	0.195	0.205	4.95	5.21
H	0.280	0.360	7.11	9.14

PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE

Lead-free 440166 Package Dimensions



NOTES:

1. DIMENSIONING AND TOLERANICING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.
5. ALL PLATED SURFACES ARE NI/AU

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.155	0.165	3.94	4.19
B	0.004	0.006	0.10	0.15
C	0.115	0.135	2.92	3.43
D	0.057	0.067	1.45	1.70
E	0.195	0.205	4.95	5.21
F	0.045	0.055	1.14	1.40
G	0.545	0.555	13.84	14.09
H	0.280	0.360	7.11	9.14
J	ø .100		2.54	
K	0.375		9.53	

PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE