Features

- High Gain: 28.0 dB
- P1dB: 36 dBm
- P3dB: 37 dBm
- IM3 Level: -26 dBc @ P_{OUT} = +30 dBm/tone
- Power Added Efficiency: 28% @ P3dB
- Lead-Free 5 mm AQFN 32-lead Package
- RoHS* Compliant

Applications

- Point-to-Point
- VSAT

Description

The MAAP-011361 is a 4 Watt, 4-stage power amplifier assembled in a lead-free 5 mm 32-lead air cavity QFN plastic package. This power amplifier operates from 27.5 to 30 GHz and provides 28 dB of linear gain, 4 W saturated output power and 28% efficiency while biased at 5.5 V.

The MAAP-011361 can be used as a power amplifier stage or as a driver stage in higher power applications. This device is ideally suited for VSAT and 28 GHz PTP applications.

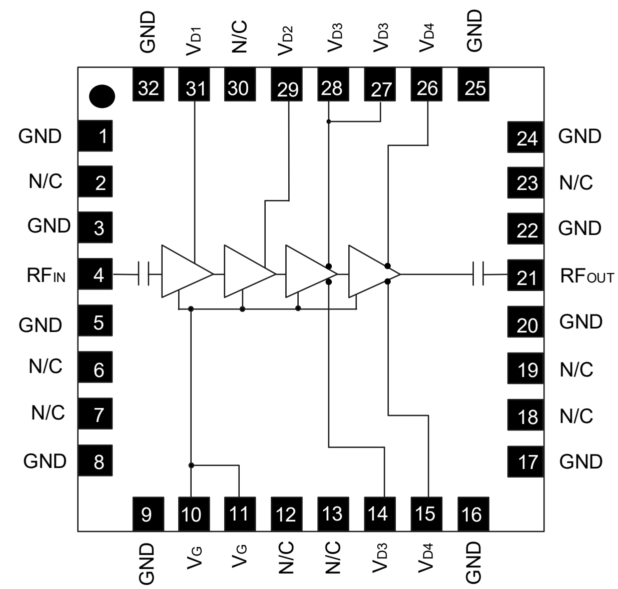
This product is fabricated using a GaAs pHEMT process which features full passivation for enhanced reliability.

Ordering Information[1,2]

Part Number	Package
MAAP-011361-TR0500	500 Part Reel
MAAP-011361-001SMB	Sample Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 3 loose parts.

Functional Schematic



Pin Configuration[3,4]

Pin #	Pin Name	Description
1, 3, 5, 8, 9, 16, 17, 20, 22, 24, 25, 32	GND	Ground
2, 6, 7, 12, 13, 18, 19, 23, 30	N/C	No Connection
4	RF_{IN}	RF Input
10, 11	V_G	Gate Voltage
14, 27, 28	V_D3	Drain Voltage 3
15, 26	V_D4	Drain Voltage 4
21	RF_{OUT}	RF Output
29	V_D2	Drain Voltage 2
31	V_D1	Drain Voltage 1

3. With exception to pin 19, MACOM recommends connecting all No Connection (N/C) pins to ground. Pin 19 should be left open circuit.
4. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: T_A = +25°C, V_D = 5.5 V, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	27.5 GHz 29.0 GHz 30.0 GHz	dB	23 23 20.5	26.5 28.0 27.5	—
Output Power (@ P3dB)	27.5 GHz 29.0 GHz 30.0 GHz	dBm	34.8 35.5 35.2	36.5 37.0 37.0	—
IM3 Level	P_{OUT} = 30 dBm / tone	dBc	—	-26	—
Power Added Efficiency	P_{IN} = 15 dBm	%	—	28	—
Input Return Loss	—	dB	—	10	—
Output Return Loss	—	dB	—	15	—
Quiescent Current	I_{DSQ} (see bias conditions, page 4)	mA	—	2400	—
Drain Current (V_{D1} + V_{D2} + V_{D3} + V_{D4})	P_{IN} = 12 dBm	mA	—	3300	—

Maximum Operating Conditions

Parameter	Rating
Input Power	$P_{IN} \leq$ 3 dB Compression
Junction Temperature[5,6]	+160°C
Operating Temperature	-40°C to +85°C

5. Operating at nominal conditions with junction temperature ≤ +160°C will ensure MTTF > 1 x 10^6 hours.
6. Junction Temperature (T_J) = T_C + Θ_{JC} * ((V * I) - (P_{OUT} - P_{IN}))
   Typical thermal resistance (Θ_{JC}) = 3.8 °C/W.
   a) For T_C = +25°C
      T_J = +75°C @ 5.5 V, 3.3 A, P_{OUT} = 37 dBm, P_{IN} = 12 dBm
   b) For T_C = +85°C
      T_J = +135°C @ 5.5 V, 3.3 A, P_{OUT} = 37 dBm, P_{IN} = 12 dBm

Absolute Maximum Ratings[7,8]

Parameter	Absolute Maximum
Input Power	18 dBm
Drain Voltage	+6 V
Gate Voltage	-3 to 0 V
Junction Temperature[9]	+175°C
Storage Temperature	-65°C to +125°C

7. Exceeding any one or combination of these limits may cause permanent damage to this device.
8. MACOM does not recommend sustained operation near these survivability limits.
9. Junction temperature directly affects device MTTF. Junction temperature should be kept as low as possible to maximize lifetime.

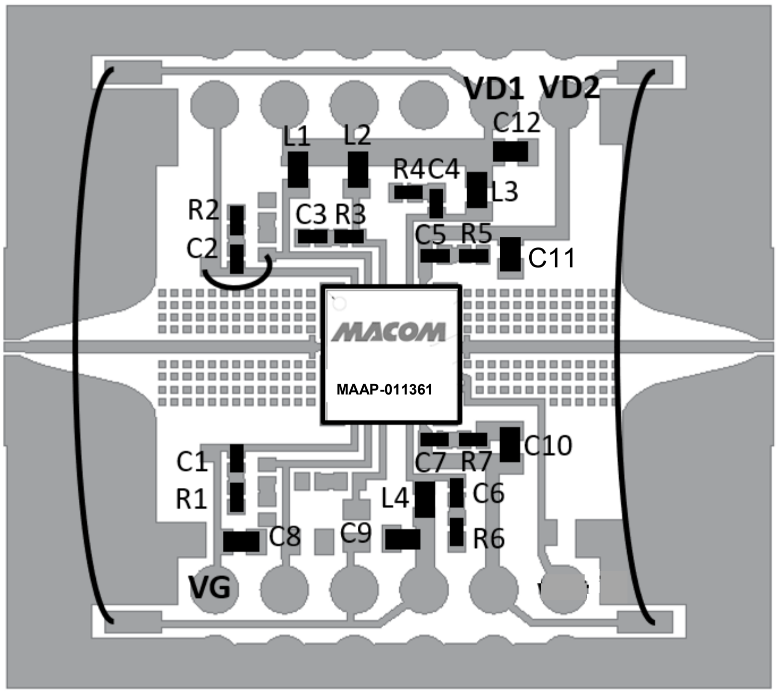
Handling Procedures

Please observe the following precautions to avoid damage:

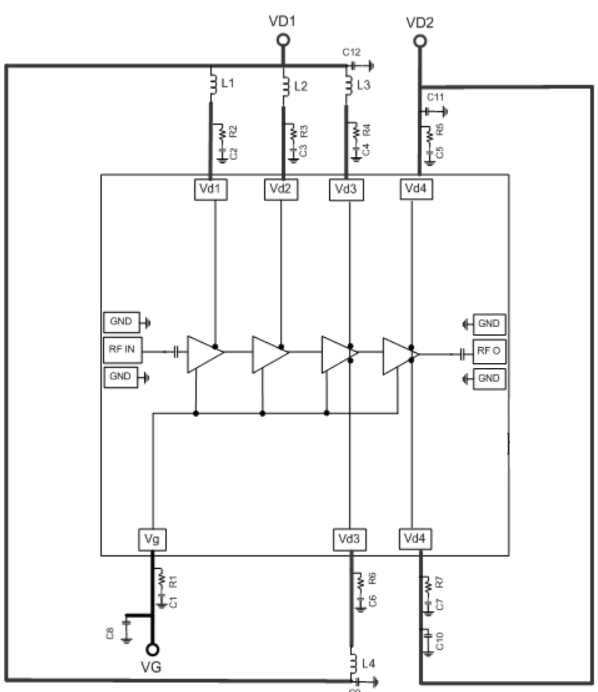
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

Sample Board Layout



Application Schematic



Parts List

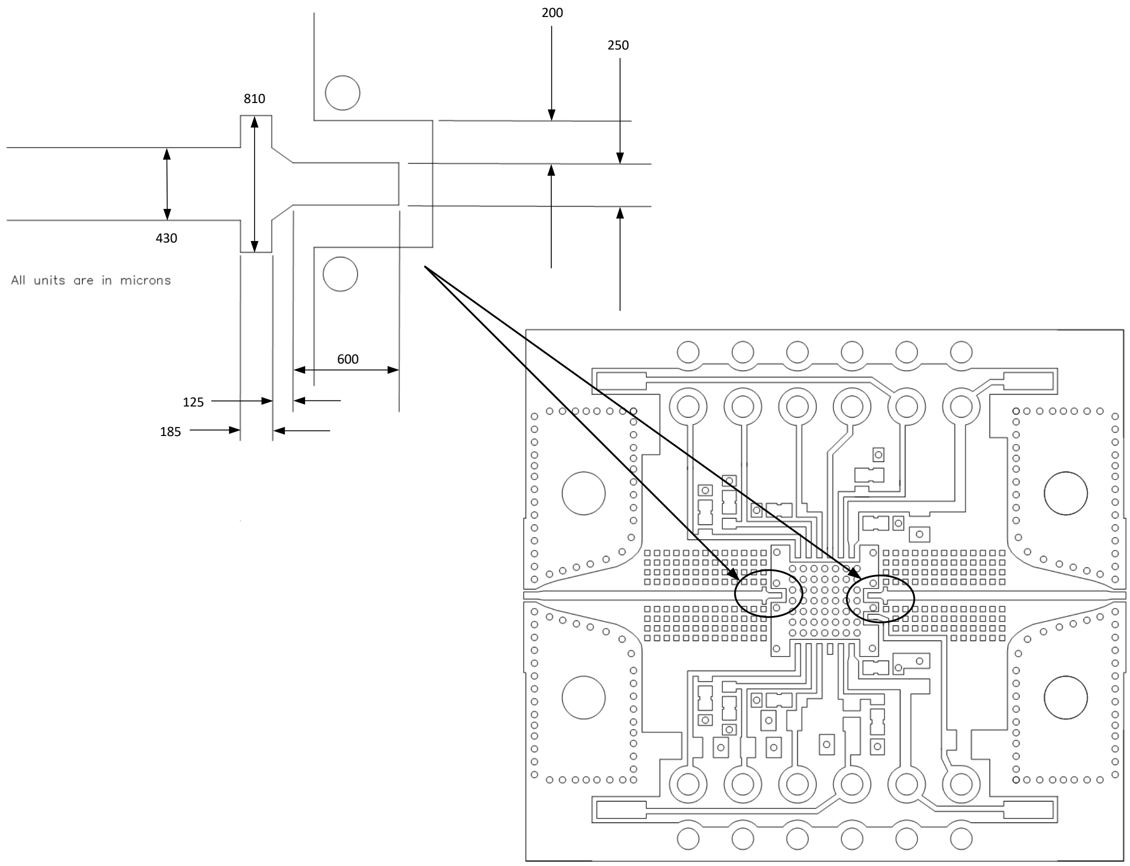
Part	Value	Case Style
C1 - C7	0.01 µF	0402
C8 - C12	22 µF	0603
R1 - R7	10 Ω	0402
L1 - L4	Ferrite bead Murata BLM18HE601SN1D	0603

Sample Board Material Specifications

Top Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Dielectric Layer: Rogers RO4003C 0.203 mm thickness
Bottom Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Finished overall thickness: 0.238 mm

Recommended PCB Layout Detail:

RF input and output pre-matching circuit patterns are identical and are designed to compensate packaging effects. Transmission line dimensions apply to a PCB with 0.203 mm thick Rogers RO4003C laminate dielectric. Performance curves shown in this data sheet were measured with these circuit patterns.



Biasing Conditions

The recommended biasing conditions are V_D = 5.5 V, I_{DSQ} = 2400 mA (controlled with V_G). The drain bias voltage range is 5 to 6 V.

V_G pins 10 and 11 are connected internally; choose either pin for layout convenience. Muting can be accomplished by setting the V_G to the pinched off voltage (V_G = -2 V).

V_D bias must be applied to V_D1, V_D2, V_D3, and V_D4 pins. V_D3 pins 27 and 28 are connected internally: choose pin 14, 27 or 28 for layout convenience. Two V_D4 pins 15 and 26 (not connected internally) are required for current symmetry.

Operating the MAAP-01361

Turn-on

1. Apply V_G (-1.5 V).
2. Apply V_D (5.5 V typical).
3. Set I_{DQ} by adjusting V_G more positive
4. Apply RF_{IN} signal.

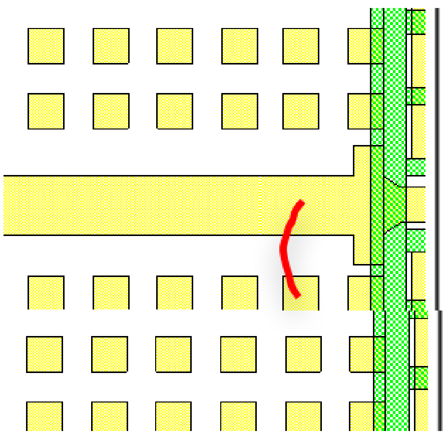
Turn-off

1. Remove RF_{IN} signal.
2. Decrease V_G to -1.5 V.
3. Decrease V_D to 0 V.

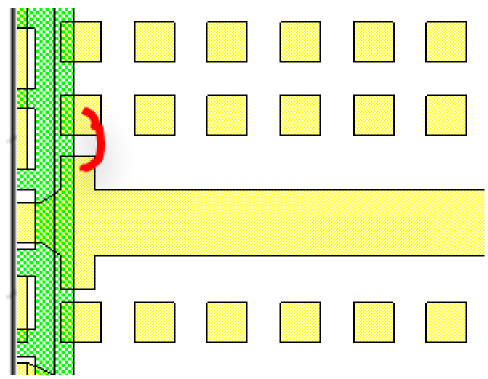
PCB Input and Output Tuning:

RF input and output pre-match bond wire tuning was used to obtain the data shown in this datasheet. This tuning is to add a small amount of capacitance to optimize the input and output match of the PA and therefore the overall RF performance. Rather than use tuning dots and bond wires on the application PCB, users can add a similar amount of capacitance in the appropriate places on the input and output RF transmission lines. The capacitance of each tuning dot is approximately 0.06 pF.

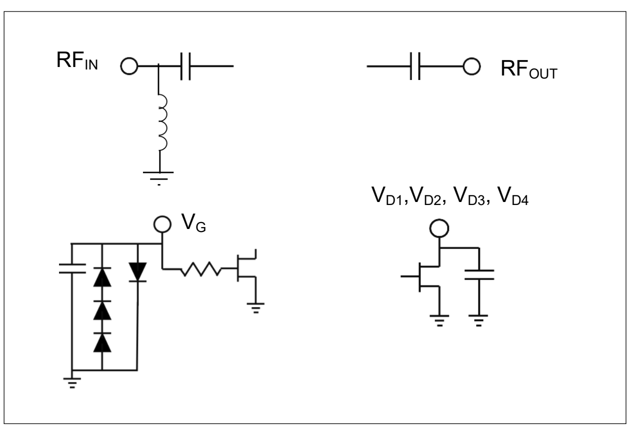
Input Tuning:



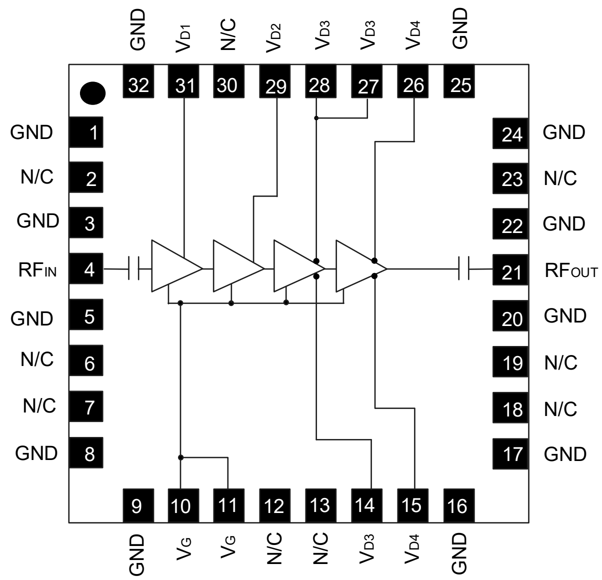
Output Tuning:



Interface Schematics



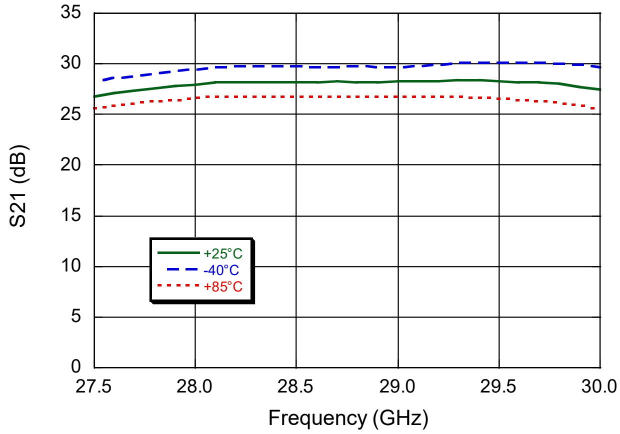
Pin Configuration and Functional Descriptions



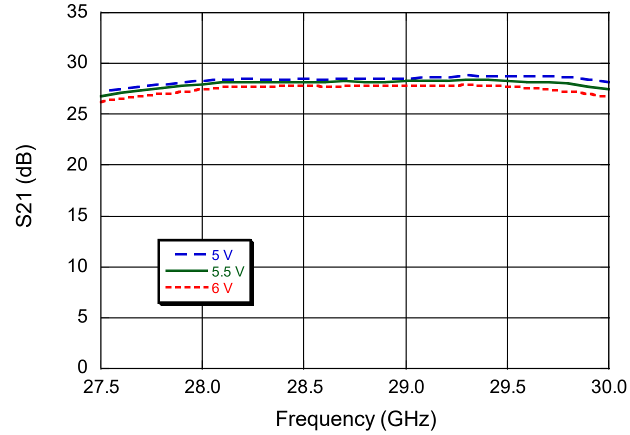
Pin #	Pin Name	Description
1,3,5,8,9,16,17, 20,22,24,25,32	GND	These pins are grounded on the package and MMIC.
2,6,7,12,13, 18,19,23,30	N/C	With exception to pin 19, these pins are not connected to anything and are recommended to be grounded in the application. Pin 19 should be left open circuit.
4	RF_{IN}	RF Signal Input. This pin is matched to 50 Ω and is AC coupled.
10,11	V_G	Power amplifier gate controls. Adjust V_G from -1.5 V to 0 V to achieve the desired quiescent current. External bypass capacitors and de-Q resistor are required as described in the applications schematic.
14,27,28	V_{D3}	Drain biases for stage 3 of the amplifier. External bypass capacitors, de-Q resistors and bead inductors are required as described in the applications schematic. There is no internal connection between pins 14 and 27-28 and so all pins need to be externally connected to the same voltage.
15,26	V_{D4}	Drain biases for stage 4 of the amplifier. External bypass capacitors, de-Q resistors and bead inductors are required as described in the applications schematic. There is no internal connection between pins 15 and 26 so both pins need to be externally connected to the same voltage.
21	RF_{OUT}	RF Signal Output. This pad is matched to 50 Ω and is AC coupled
29	V_{D2}	Drain bias for stage 2 of the amplifier. External bypass capacitors, de-Q resistor and bead inductor are required as described in the applications schematic.
31	V_{D1}	Drain bias for stage 1 of the amplifier. External bypass capacitors, de-Q resistor and bead inductor are required as described in the applications schematic.

Typical Performance Curves: V_D = 5.5 V, I_{DSQ} = 2400 mA

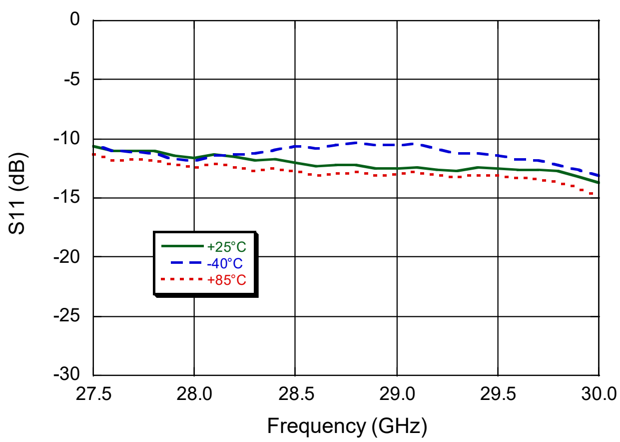
Small Signal Gain vs. Frequency over Temperature



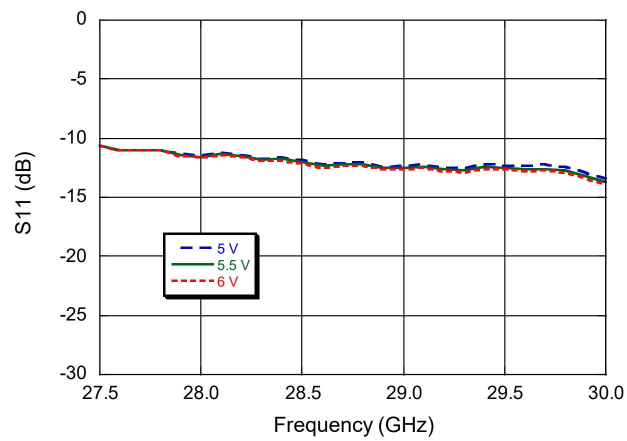
Small Signal Gain vs. Frequency over Bias Voltage



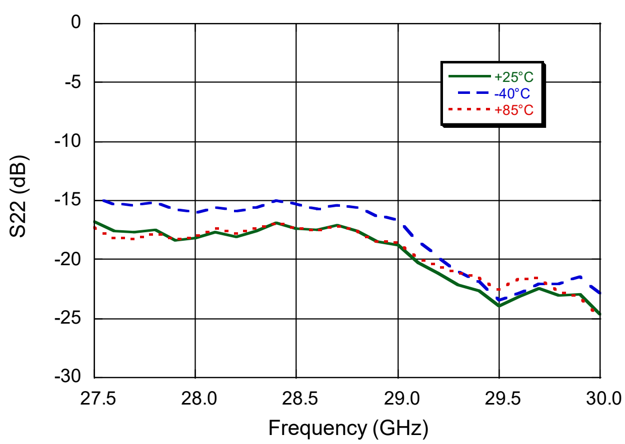
Input Return Loss vs. Frequency over Temperature



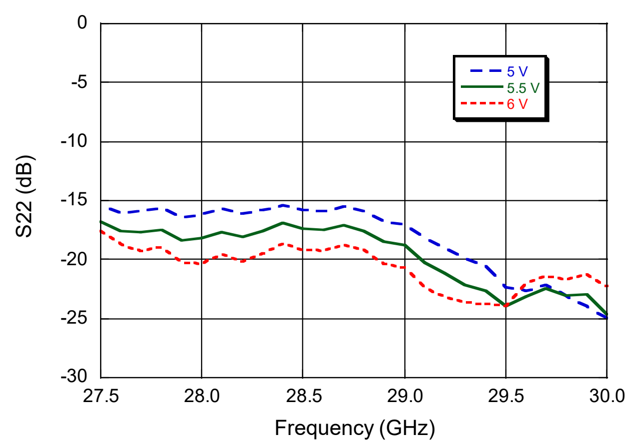
Input Return Loss vs. Frequency over Bias Voltage



Output Return Loss vs. Frequency over Temperature

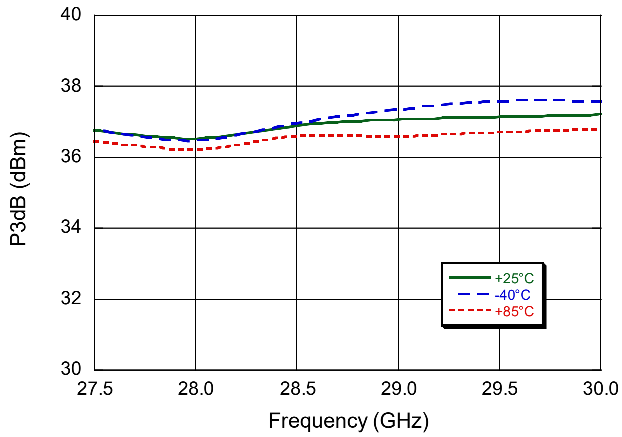


Output Return Loss vs. Frequency over Bias Voltage

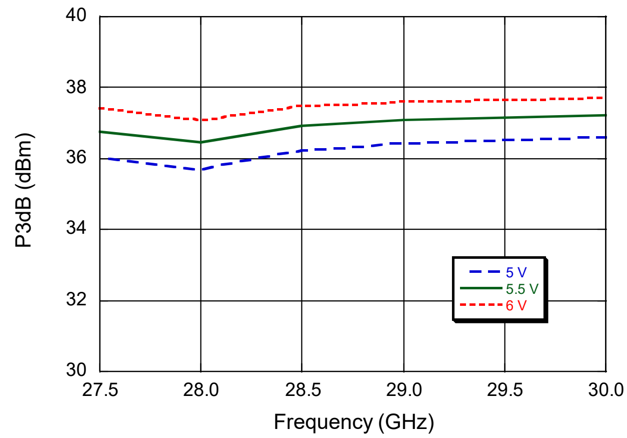


Typical Performance Curves: V_D = 5.5 V, I_{DSQ} = 2400 mA

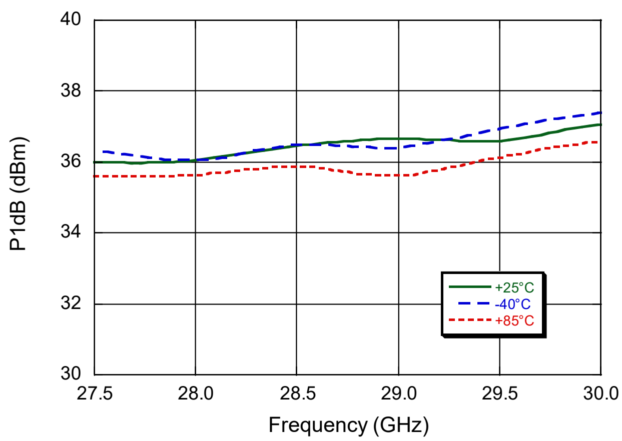
P3dB vs. Frequency over Temperature



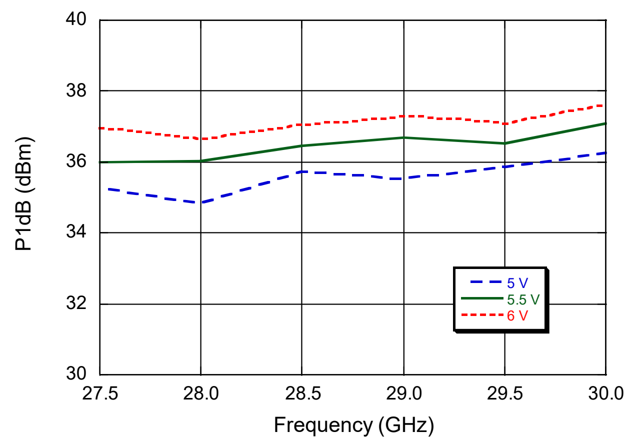
P3dB vs. Frequency over Bias Voltage



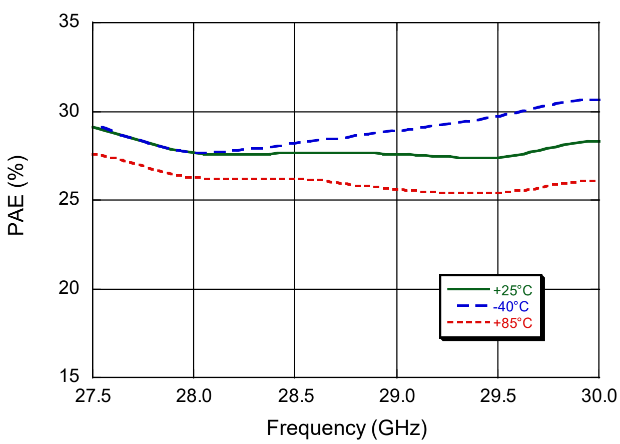
P1dB vs. Frequency over Temperature



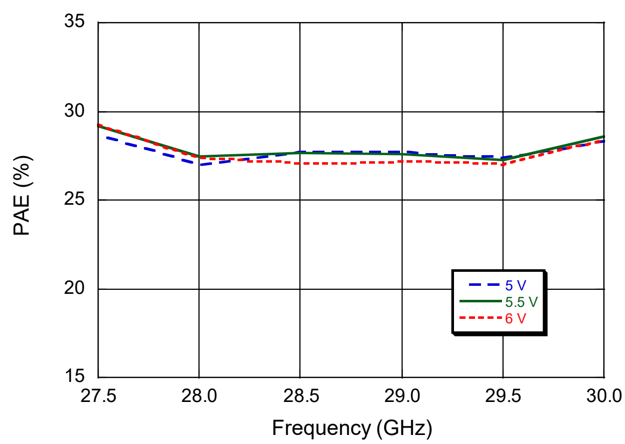
P1dB vs. Frequency over Bias Voltage



PAE@3dB vs. Frequency over Temperature

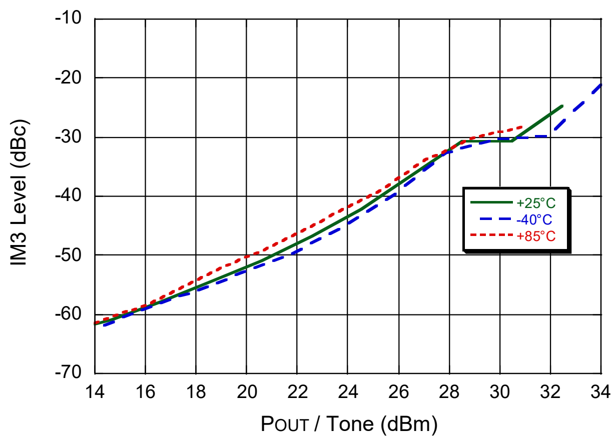


PAE@3dB vs. Frequency over Bias Voltage

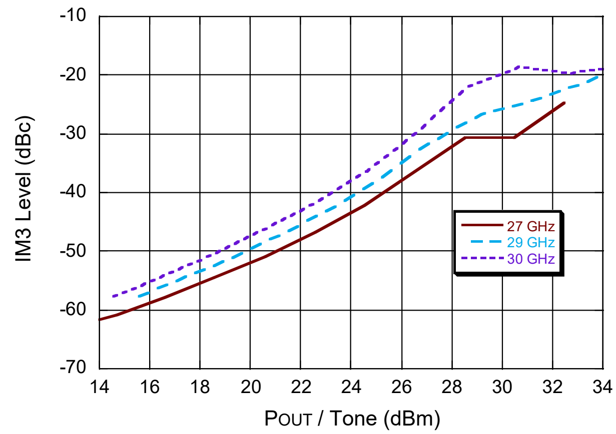


Typical Performance Curves: V_D = 5.5 V, I_{DSQ} = 2400 mA

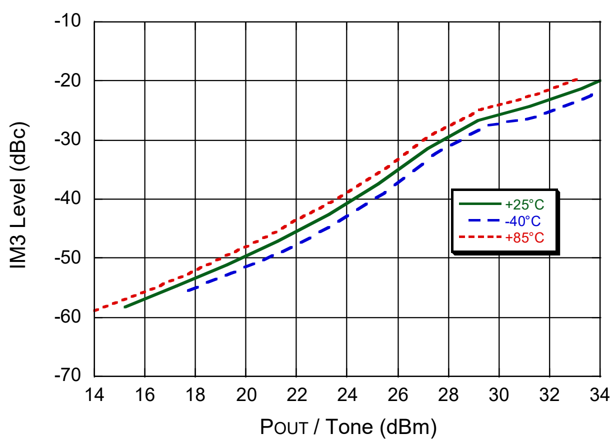
IM3 vs. Output Power (27 GHz)



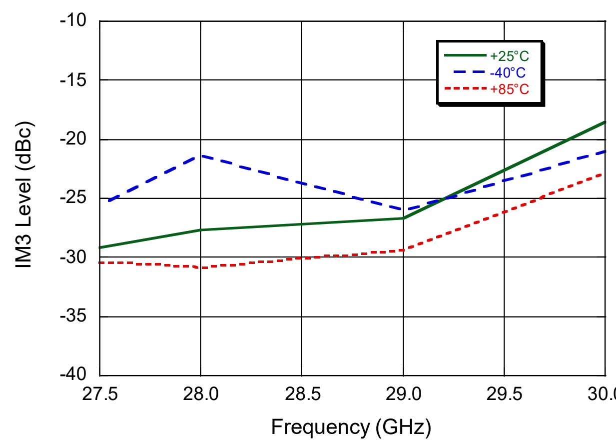
IM3 vs. Output Power @ 25˚C



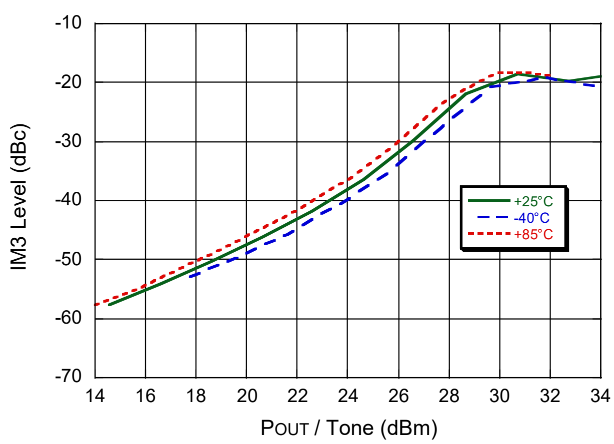
IM3 vs. Output Power (29 GHz)



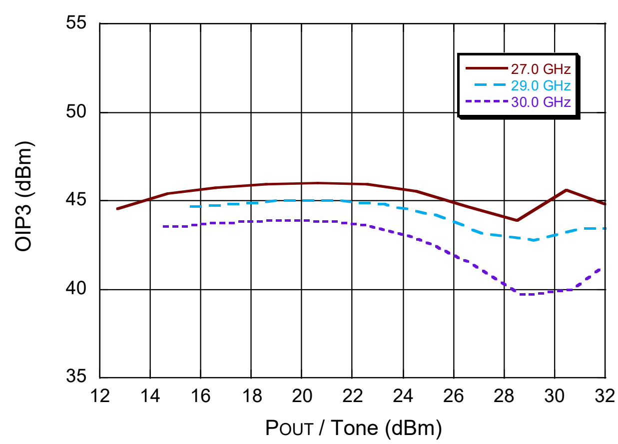
IM3 vs. Frequency @ Pout = 30 dBm/tone



IM3 vs. Output Power (30 GHz)

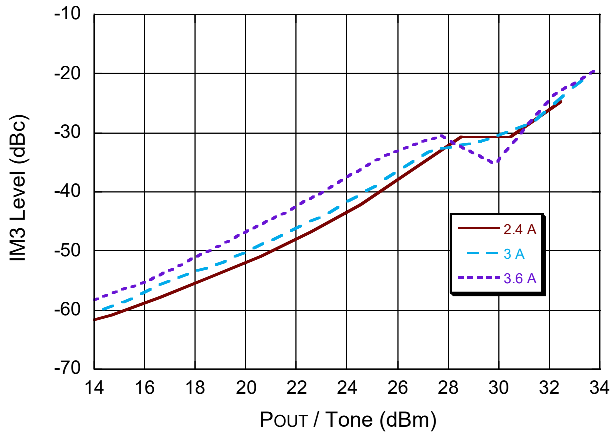


Output IP3 vs. Output Power

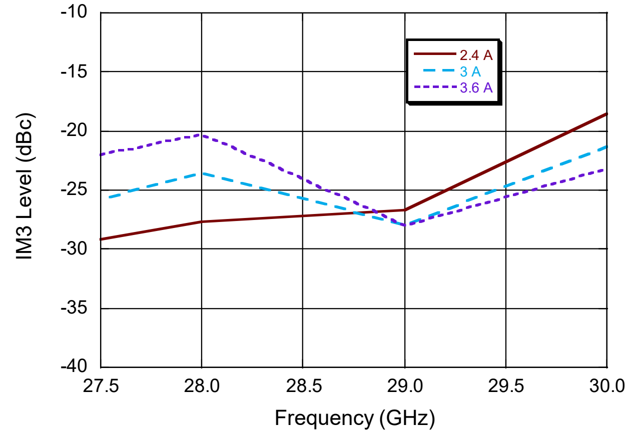


Typical Performance Curves: V_D = 5.5 V, 25°C

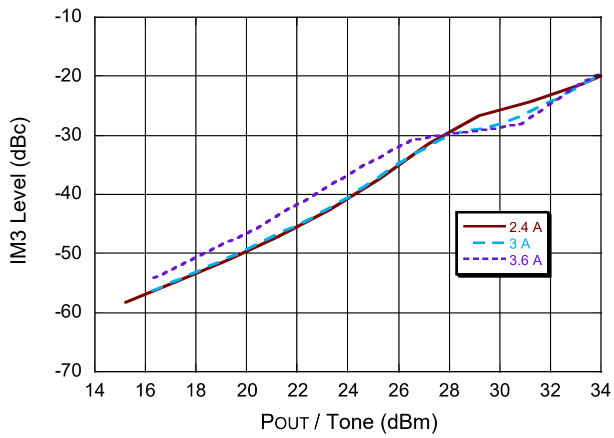
IM3 vs. Output Power @ 27 GHz, @Idsq=2.4A, 3A, and 3.6A



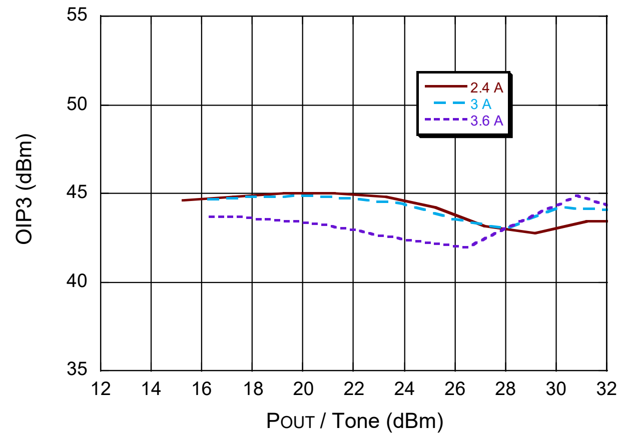
IM3 vs. Frequency by Drain Current @ Pout = 30 dBm/tone @Idsq=2.4A, 3A, and 3.6A



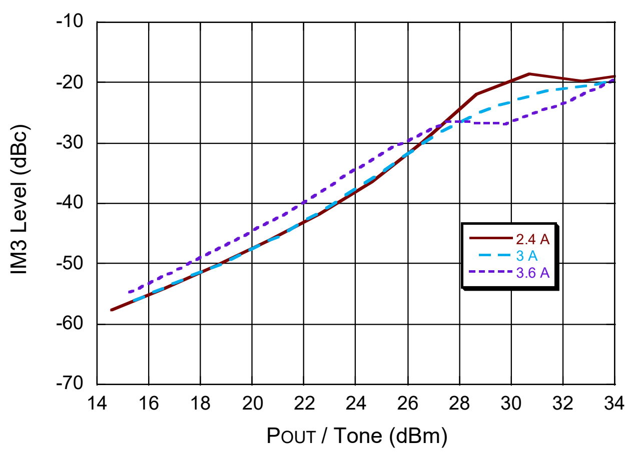
IM3 vs. Output Power @ 29 GHz, @Idsq=2.4A, 3A and 3.6A



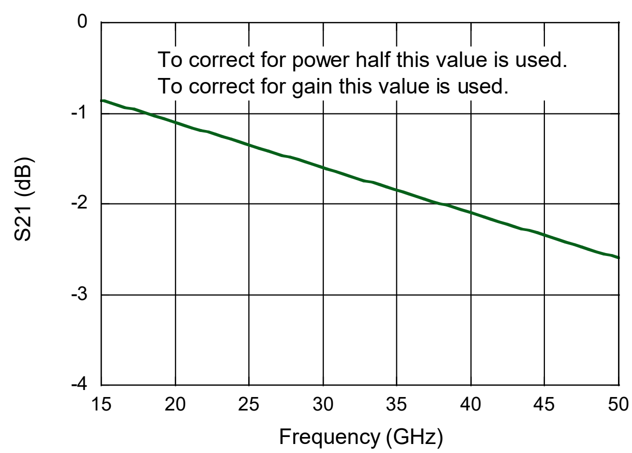
Output IP3 vs. Output Power @ 29 GHz @Idsq=2.4A, 3A, and 3.6A



IM3 vs. Output Power @ 30 GHz, @Idsq=2.4A, 3A and 3.6A

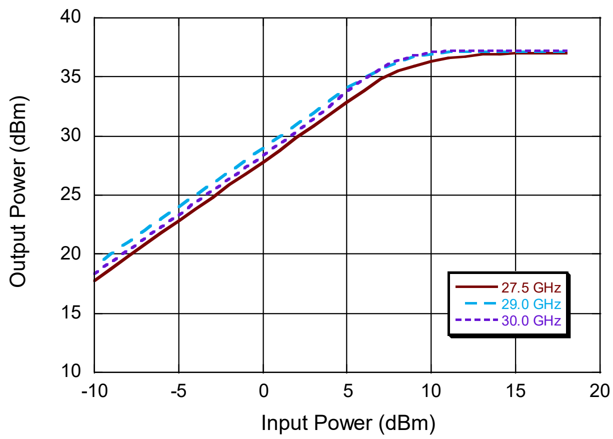


Combined Input and Output Sample Board Thru Loss

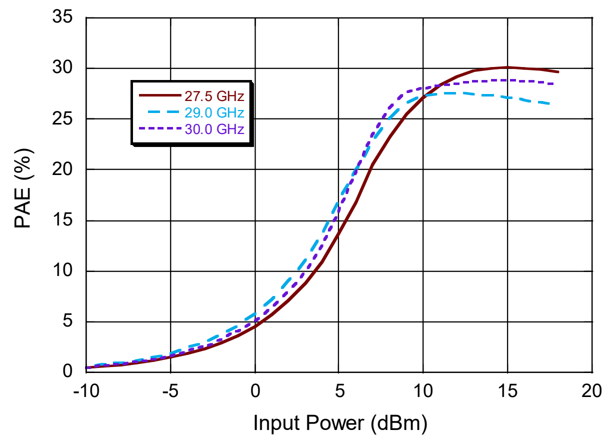


Typical Performance Curves: V_D = 5.5 V, I_{DSQ} = 2400 mA, 25°C

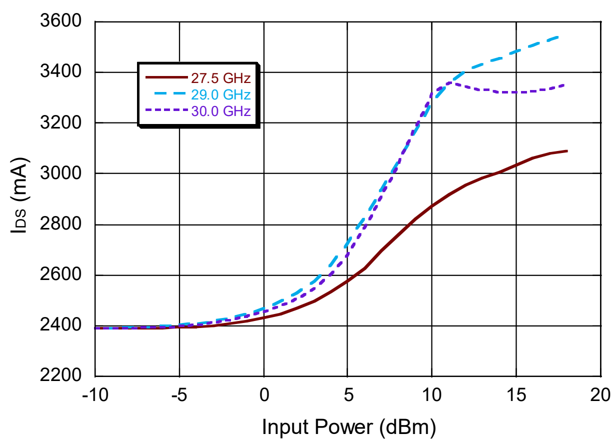
Output Power vs. Input Power



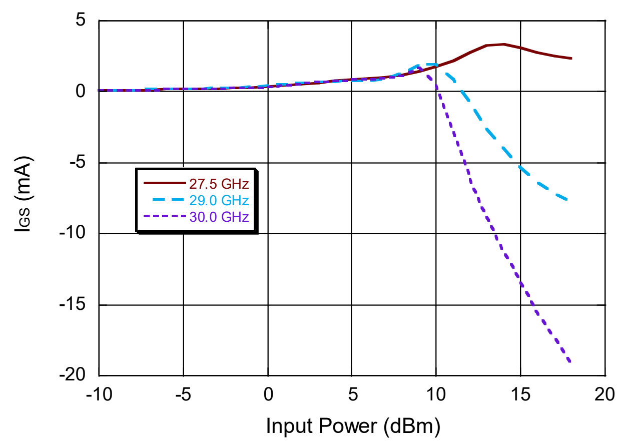
PAE vs. Input Power



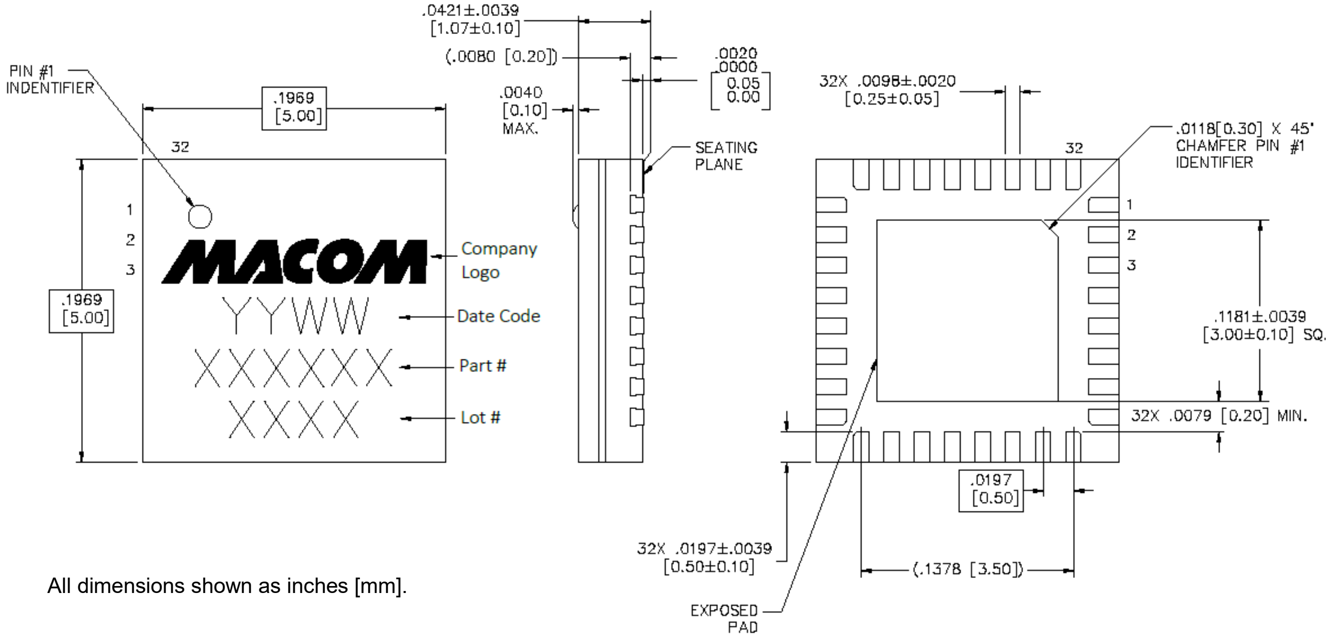
Bias Current vs. Input Power



Gate Current vs. Input Power



Lead-Free 5 mm 32-Lead AQFN Package†



All dimensions shown as inches [mm].

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.
Plating is NiPdAu.