Balanced Power Amplifier, 4 W 13.5 - 15.0 GHz

MAAP-011333-DIE

Features

- High Gain: 26 dB
- P1dB: 37 dBm at 14 GHz
- P3dB: 37.8 dBm at 14 GHz
- IM3 Level: -28 dBc @ P_{OUT} 28 dBm/tone
- Power Added Efficiency: 27% at P3dB
- Die Size: 2.5 x 3.0 x 0.1 mm
- Integrated Temperature Compensated Power Detector
- Scratch Protection Die Coating
- RoHS* Compliant

Applications

- VSAT

Description

The MAAP-011333-DIE is a balanced 4 Watts power amplifier offered as a bare die part. This power amplifier operates from 13.5 to 15 GHz and provides 26 dB of linear gain and 4 W saturated output power with 27% efficiency while biased at 6 V.

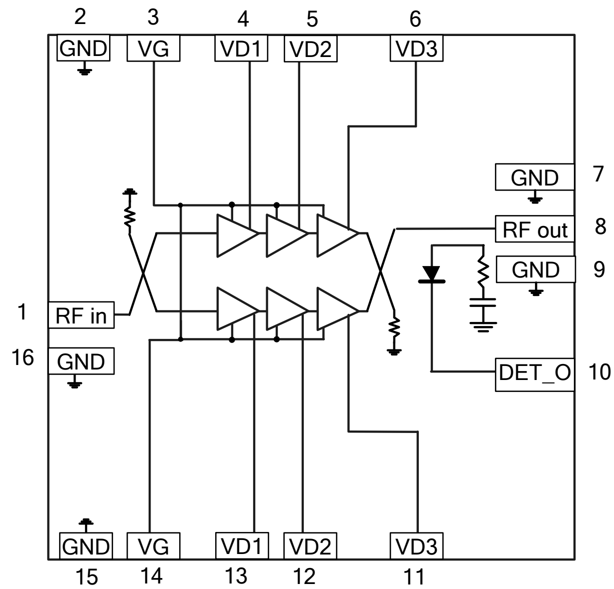
The MAAP-011333-DIE can be used as a power amplifier stage or as a driver stage in higher power applications. This device is ideally suited for linear Ku-band VSAT communications.

This product is fabricated using a GaAs pHEMT process which features full passivation and scratch protection for enhanced reliability.

Ordering Information

Part Number	Package
MAAP-011333-DIE	Gel Pack
MAAP-011333-DIESMB	Sample Board

Functional Schematic



Pin Configuration[1]

Pin #	Pin Name	Description
1	RF_{IN}	RF Input
2, 7, 9, 15, 16	GND	Ground
3, 14	V_G	Gate Voltage
4, 13	V_{D1}	Drain Voltage 1
5, 12	V_{D2}	Drain Voltage 2
6, 11	V_{D3}	Drain Voltage 3
8	RF_{OUT}	RF output
10	DET_O	Detector Output

1. Backside of die must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: Freq. = 14 GHz, T_A = +25°C, V_D = +6 V, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	P_{IN} = 0 dBm	dB	24	26	—
P_{OUT}	P_{IN} = +14 dBm	dBm	36	37.8	—
IM3 Level	P_{OUT} = 28 dBm / tone	dBc	—	28	—
Power Added Efficiency	P_{SAT} (P_{IN} = +14 dBm)	%	—	27	—
Input Return Loss	P_{IN} = -20 dBm	dB	—	17	—
Output Return Loss	P_{IN} = -20 dBm	dB	—	20	—
Quiescent Current	I_{DQ} (see bias conditions, page 4)	mA		1700	—
Current	P_{SAT} (P_{IN} = +14 dBm)	mA	—	3600	—

Maximum Operating Ratings

Parameter	Rating
Input Power	$P_{IN} \leq$ 3 dB Compression
Junction Temperature[2,3]	+160°C
Operating Temperature	-40°C to +85°C

2. Operating at nominal conditions with junction temperature ≤ +160°C will ensure MTTF > 1 x 10^6 hours.
3. Junction Temperature (T_J) = T_C + Θ_{JC} * ((V * I) - (P_{out} - P_{IN}))
Typical thermal resistance (Θ_{JC}) = 3.63 °C/W.
a) For T_C = +25°C
T_J = +86.3°C @ 6 V, 3.84 A, P_{OUT} = 37.9 dBm, P_{IN} = 15 dBm
b) For T_C = +85°C
T_J = 142.3°C @ 6 V, 3.42 A, P_{OUT} = 36.8 dBm, P_{IN} = 15 dBm

Absolute Maximum Ratings[4, 5]

Parameter	Absolute Maximum
Input Power	+30 dBm
Drain Voltage	+6.5 V
Gate Voltage	-3 to 0 V
Junction Temperature[6]	+175°C
Storage Temperature	-65°C to +150°C

4. Exceeding any one or combination of these limits may cause permanent damage to this device.
5. MACOM does not recommend sustained operation near these survivability limits.
6. Junction temperature directly effects device MTTF. Junction temperature should be kept as low as possible to maximize lifetime.

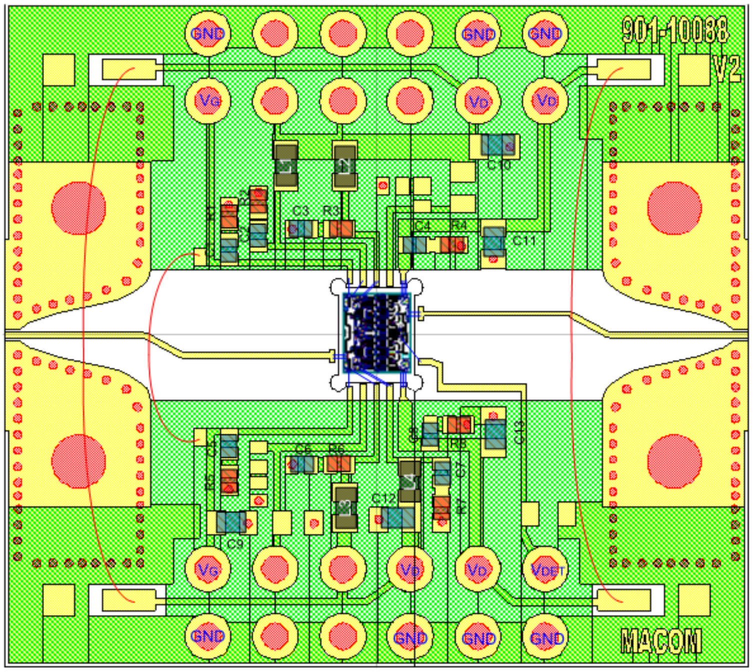
Handling Procedures

Please observe the following precautions to avoid damage:

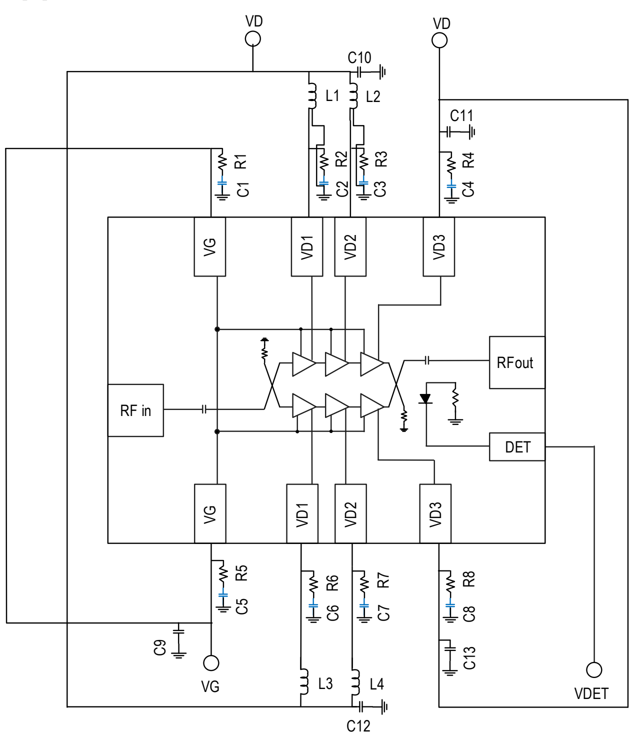
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

Sample Board Layout



Application Schematic



Parts List

Part	Value	Case Style
C1 - C8	0.01 µF	0402
C9 - C13	22 µF	0603
R1 - R8	10 Ω	0402
L1 - L4	Ferrite Bead MURATA BLM18HE601SN1D	0603

Sample Board Thru Loss

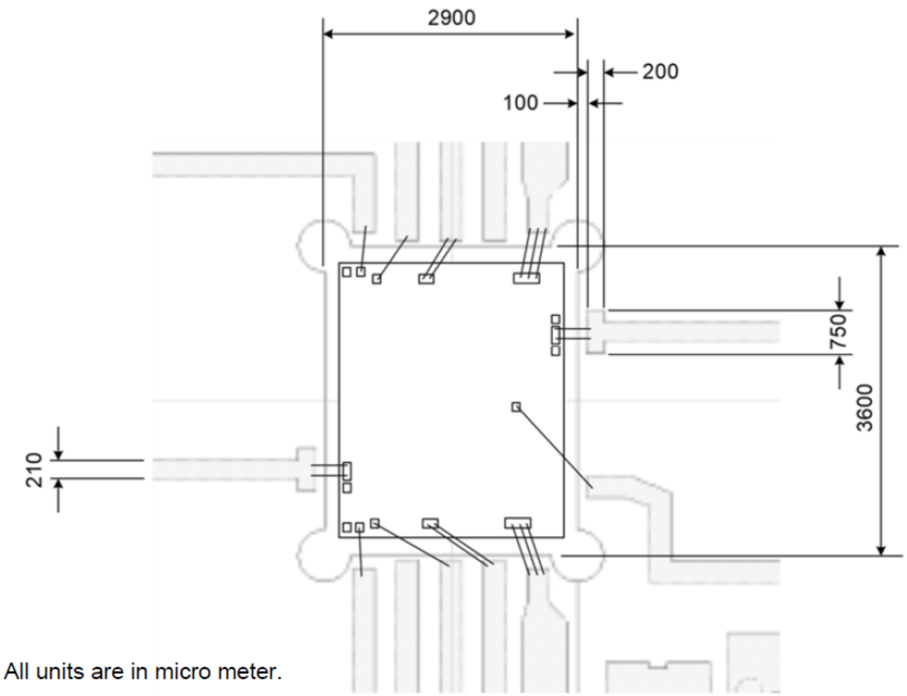
Refer to the plot on page 6 for sample board thru losses.

Sample Board Material Specifications

Top Layer: 1/2 oz Copper Cladding, 0.0175 mm thickness
Dielectric Layer: Rogers RO4350B 0.101 mm thickness
Bottom Layer: 1/2 oz Copper Cladding, 0.0175 mm thickness
Finished overall thickness: 0.136 mm

Recommended Bonding Diagram and PCB Details:

For optimum performance, RF input and output microstrip lines require open stubs on the application board for bonding wire inductance compensation. Optimum bonding wire inductance for the RF I/O connection is 0.2 nH and physical length for the 1 mil diameter gold wire is approximately 350 µm each for the two wire connection.



Biasing conditions

Recommended biasing conditions are V_D = 6 V, I_{DQ} = 1.7 A (controlled with V_G). The drain bias voltage range is 4 to 6 V, and the quiescent drain current biasing range is 1.5 to 2.5 A.

V_G pins 2 and 13 are internally connected; therefore, interconnection is not required. Muting can be accomplished by setting the V_G to the pinched off voltage (V_G = -2 V).

V_D Bias must be applied to V_D1, V_D2 and V_D3 pins from north and south sides. North V_D supplies and south V_D supplies are not connected internally.

Operating the MAAP-011333-DIE

Turn-on

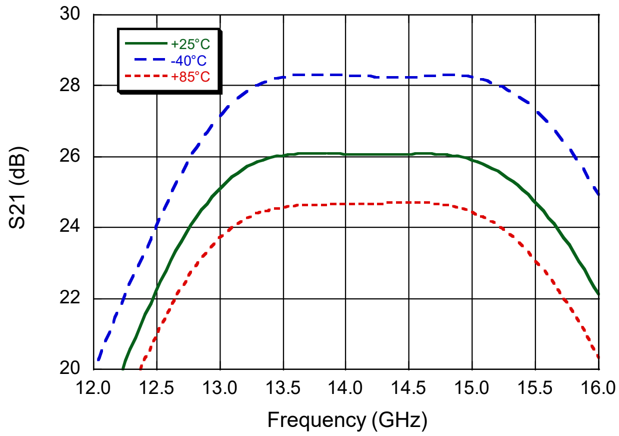
1. Apply V_G (-1.5 V).
2. Apply V_D (6.0 V typical).
3. Set I_{DQ} by adjusting V_G more positive (typically -0.9 to -1.0 V for I_{DQ} = 1.7 A).
4. Apply RF_{IN} signal.

Turn-off

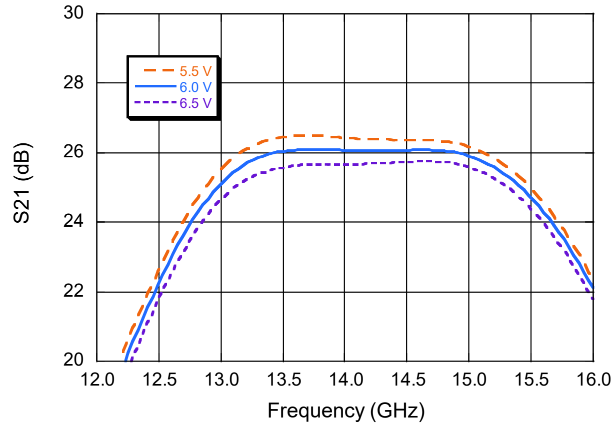
1. Remove RF_{IN} signal.
2. Decrease V_G to -1.5 V.
3. Decrease V_D to 0 V.

Typical Performance Curves: V_D = 6 V, I_{DSQ} = 1700 mA

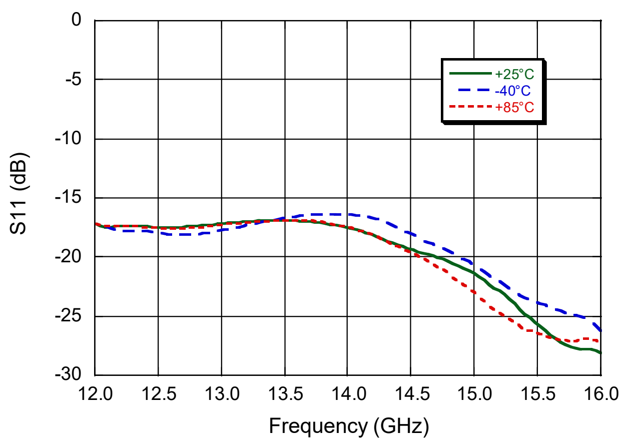
Small Signal Gain vs. Frequency over Temperature



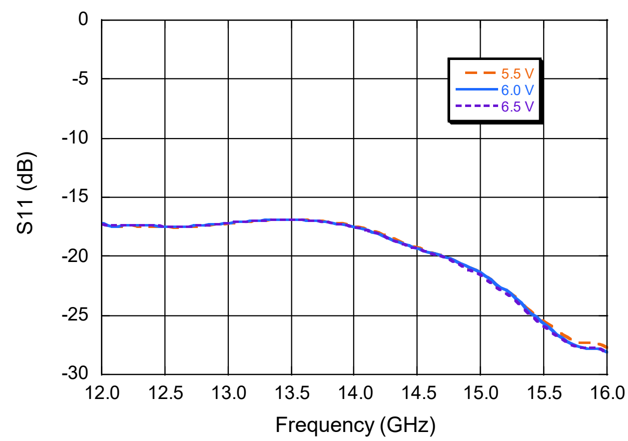
Small Signal Gain vs. Frequency over Bias Voltage



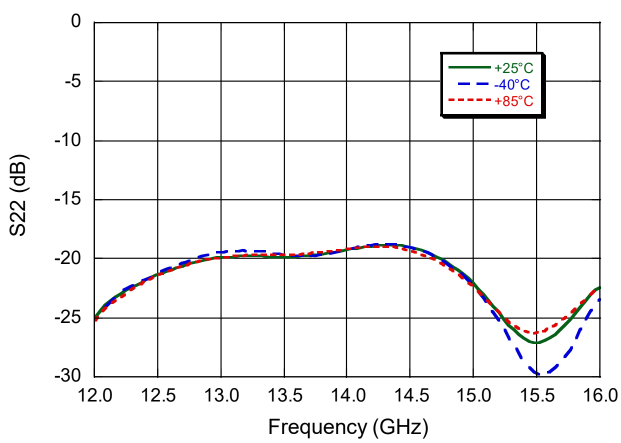
Input Return Loss vs. Frequency over Temperature



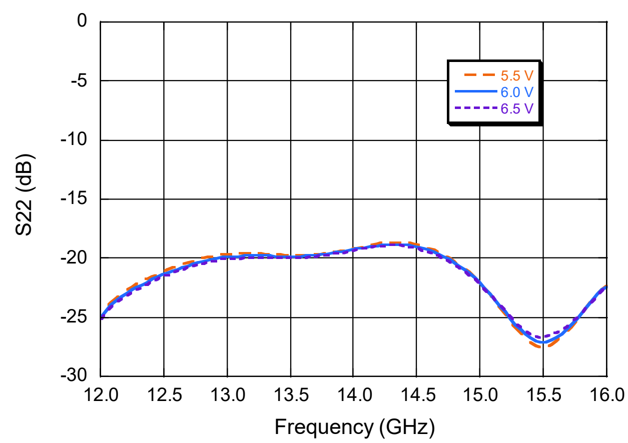
Input Return Loss vs. Frequency over Bias Voltage



Output Return Loss vs. Frequency over Temperature

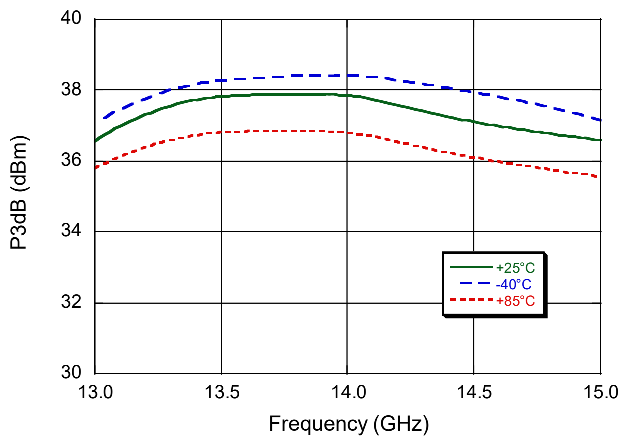


Output Return Loss vs. Frequency over Bias Voltage

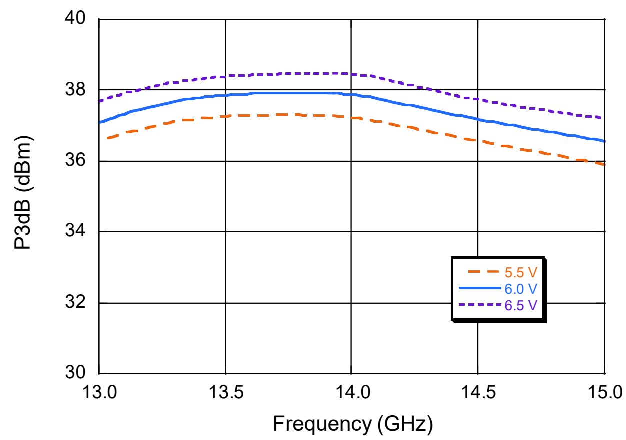


Typical Performance Curves: V_D = 6 V, I_{DSQ} = 1700 mA

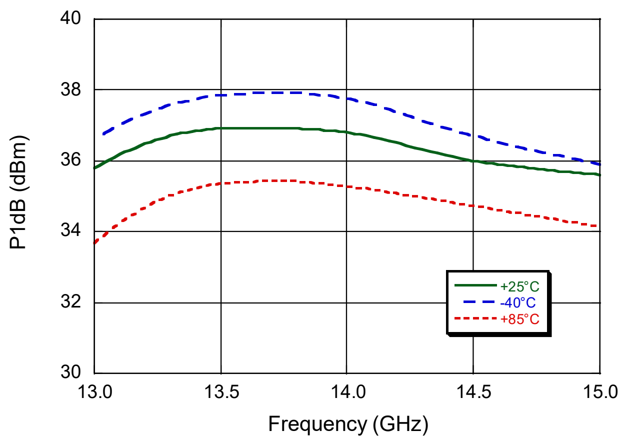
P3dB vs. Frequency over Temperature



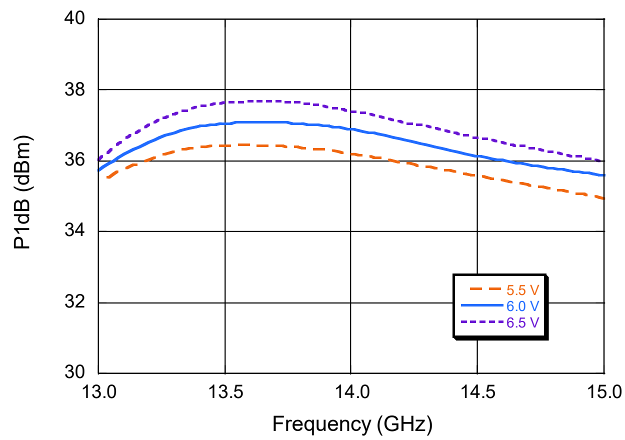
P3dB vs. Frequency over Bias Voltage



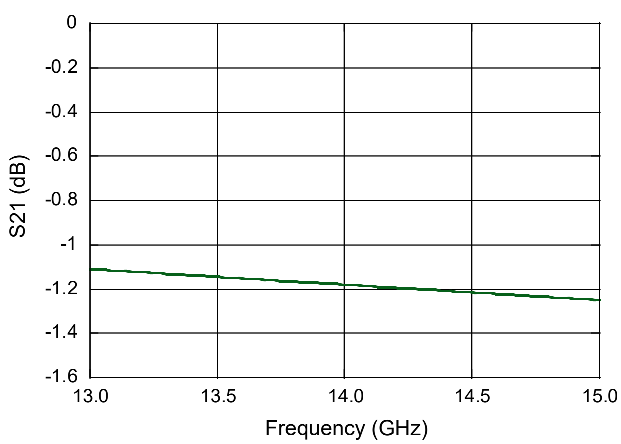
P1dB vs. Frequency over Temperature



P1dB vs. Frequency over Bias Voltage

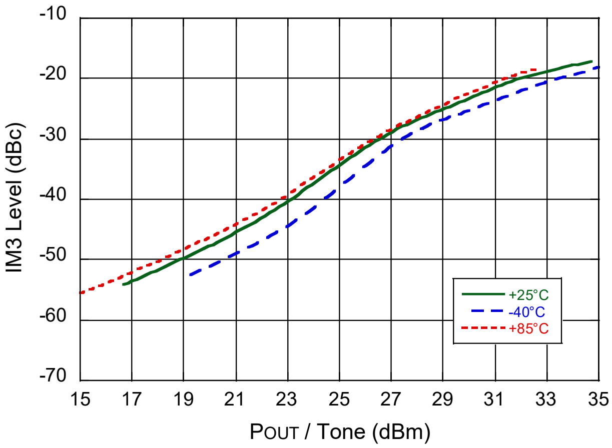


Sample Board Thru Loss
Includes Two 2.4mm Connectors

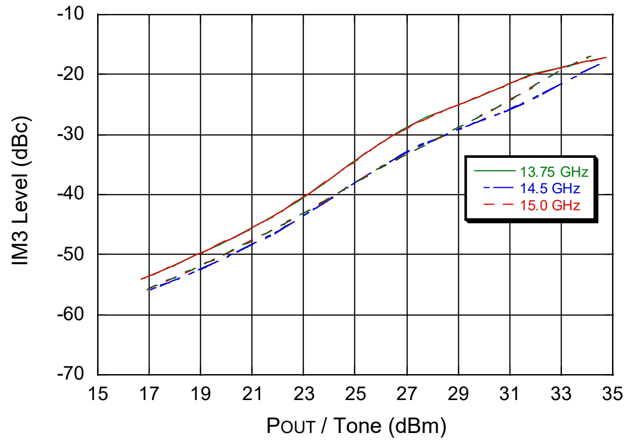


Typical Performance Curves: V_D = 6 V, I_{DSQ} = 1700 mA

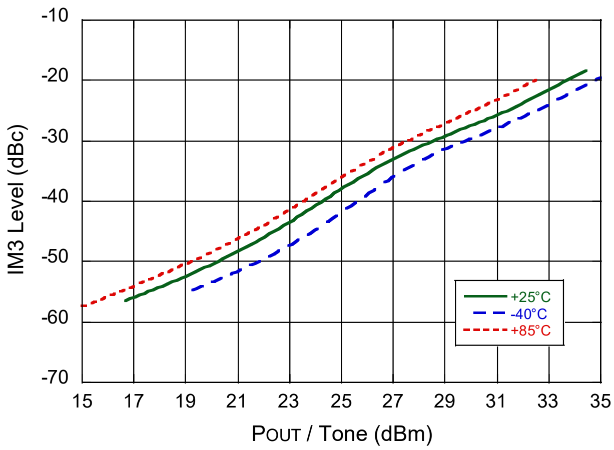
IM3 vs. Output Power by Temperature @ 13.75 GHz



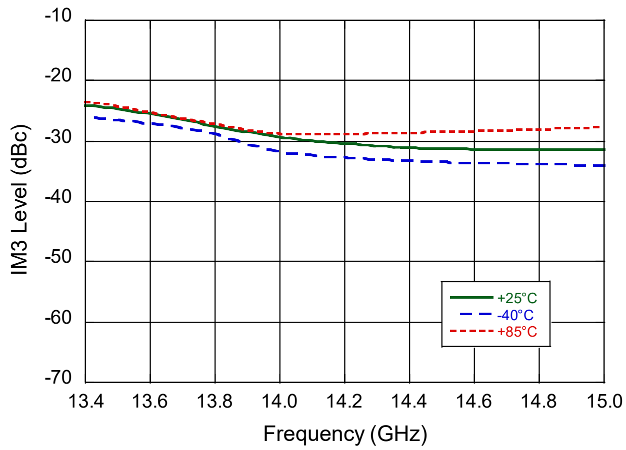
IM3 vs. Output Power by Frequency



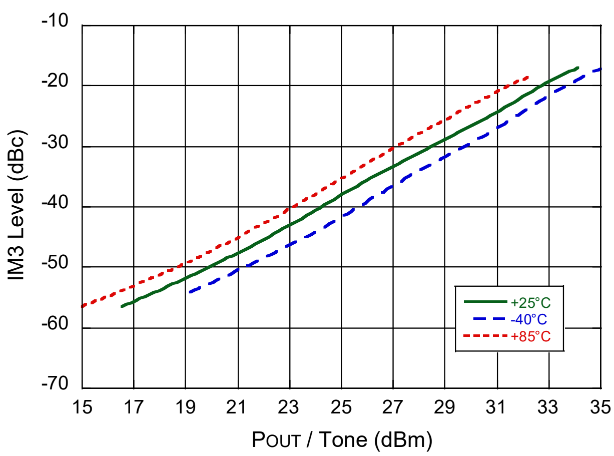
IM3 vs. Output Power by Temperature @ 14.5 GHz



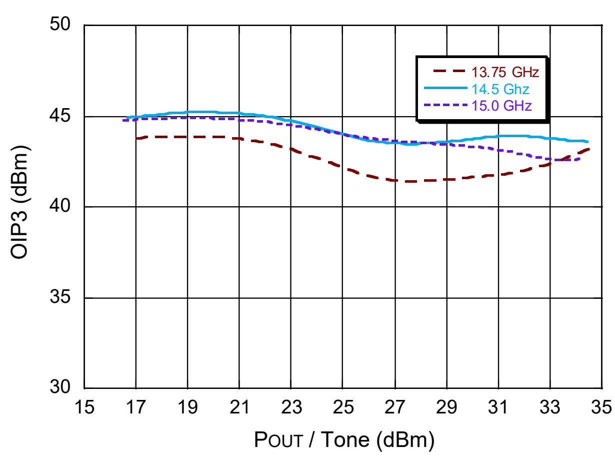
IM3 vs. Frequency @ Output Power = 28 dBm/tone



IM3 vs. Output Power by Temperature @ 15 GHz

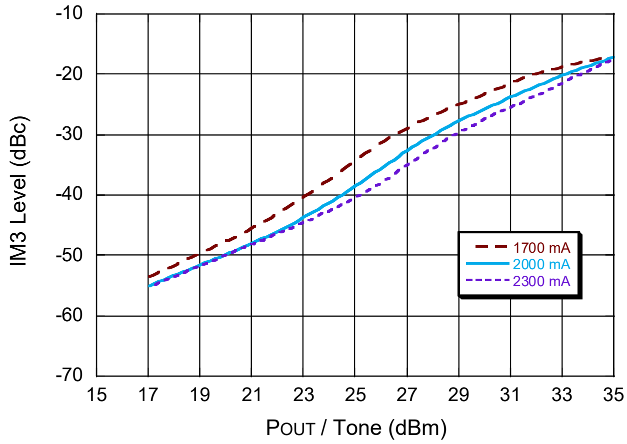


Output IP3 vs. Output Power by Frequency

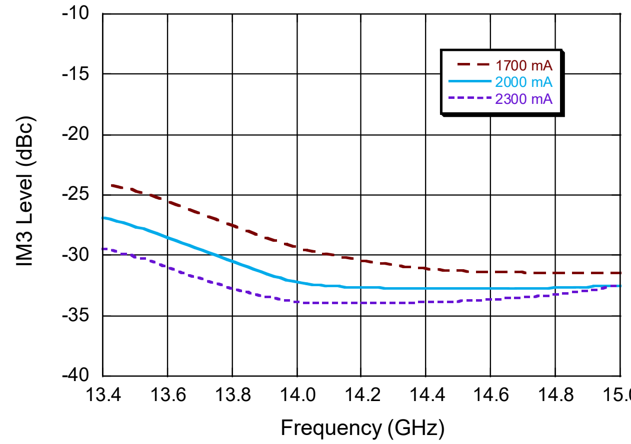


Typical Performance Curves: V_D = 6 V

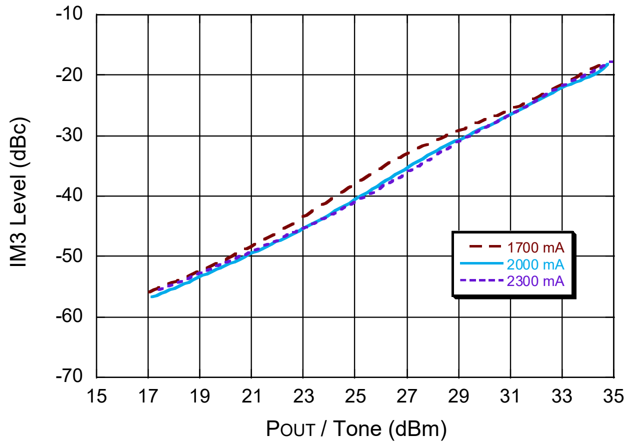
IM3 vs. Output Power by Drain Current @ 13.75 GHz



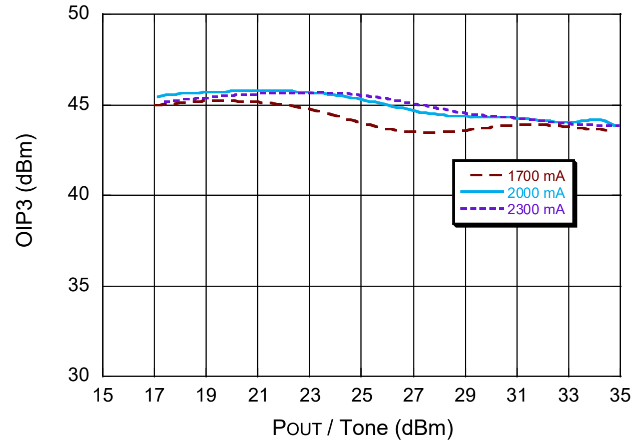
IM3 vs. Frequency by Drain Current @ Pout = 28 dBm/tone



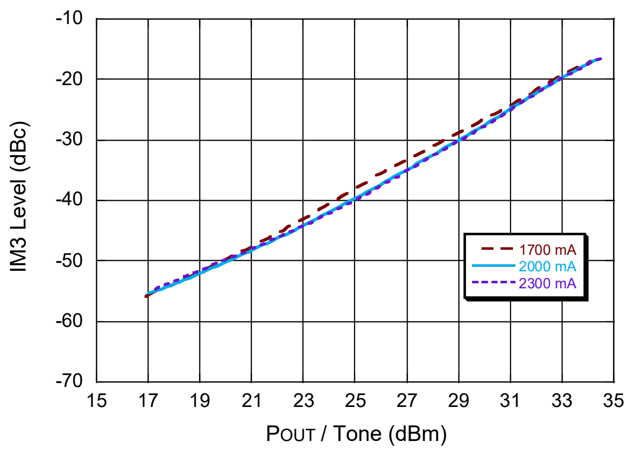
IM3 vs. Output Power by Drain Current @ 14.5 GHz



Output IP3 vs. Output Power by Drain Current @ 14.5 GHz

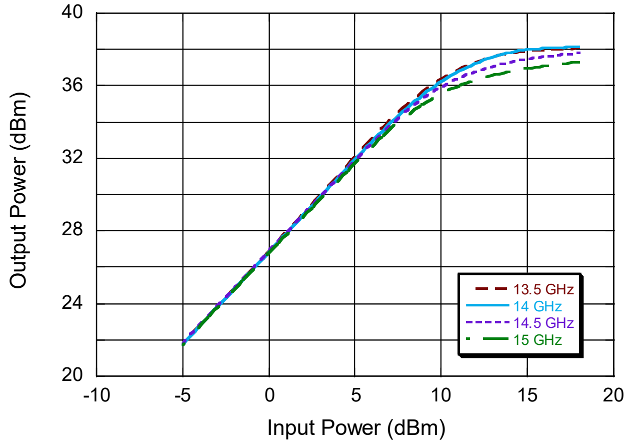


IM3 vs. Output Power by Drain Current @ 15 GHz

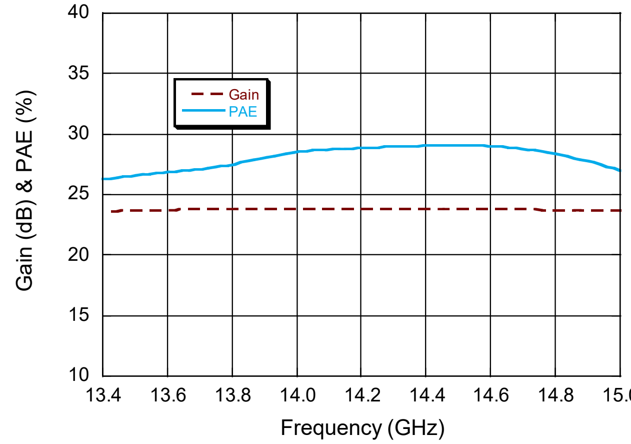


Typical Performance Curves: V_D = 6 V, I_{DSQ} = 1700 mA

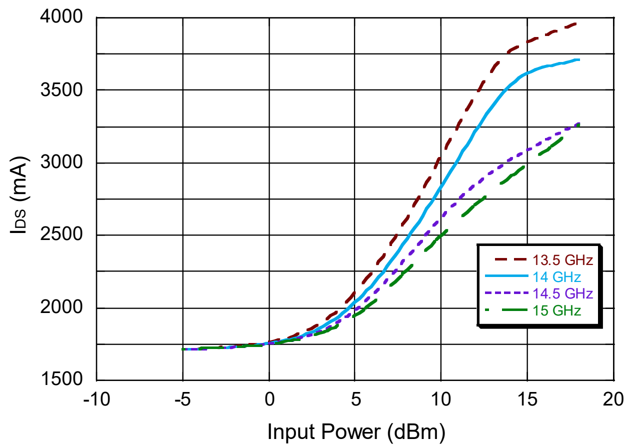
Output Power vs. Input Power



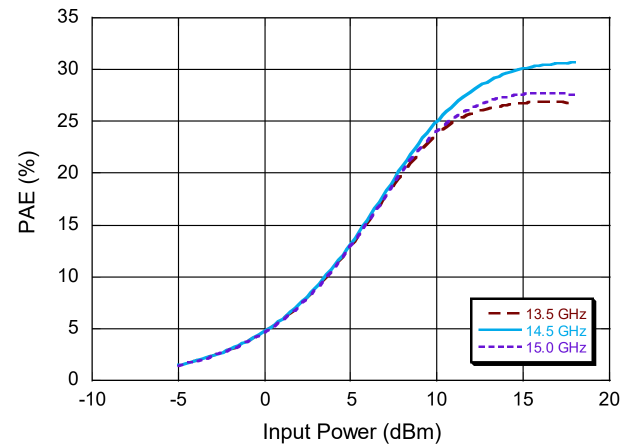
Gain and PAE @ P3dB vs. Frequency



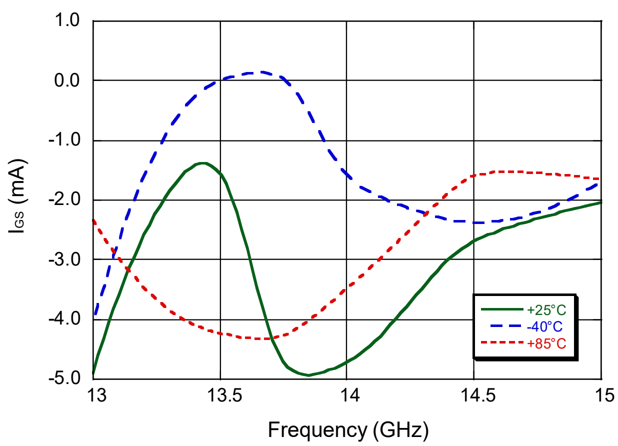
Drain Current vs. Input Power



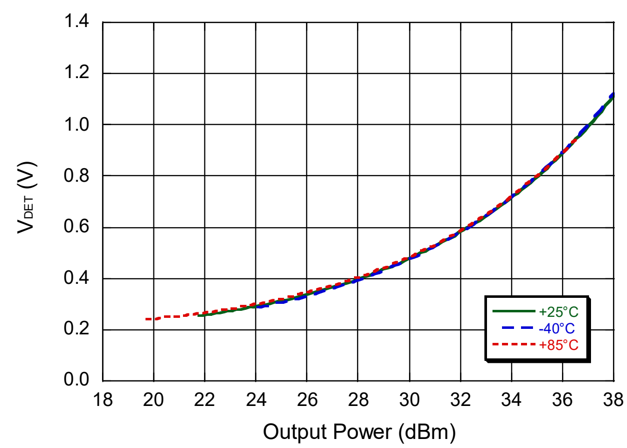
PAE vs. Input Power



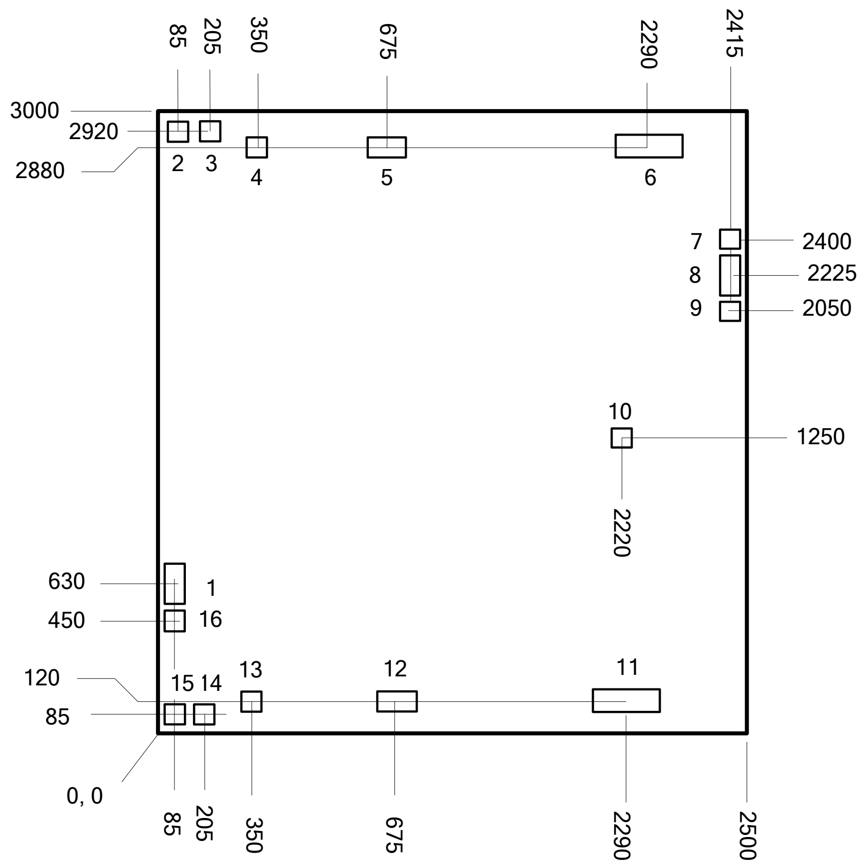
Gate Current vs. Frequency @ P_{SAT}



Detector Voltage vs. Output Power @ 14 GHz



MMIC Die Outline[7,8]



7. All units are in µm, unless otherwise noted, with a tolerance of ±5 µm.
8. Die thickness is 100 ±10 µm.

Bond Pad Detail[9]

Pad	Size (x)	Size (y)
1, 8	100	200
3, 14	90	90
4, 13	100	100
5, 12	160	100
6, 11	240	100
10	75	75

9. Pin 2, 7, 9, 15, and 16 are not in use.