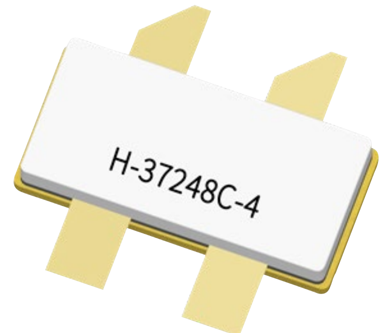
GTRA384802FC

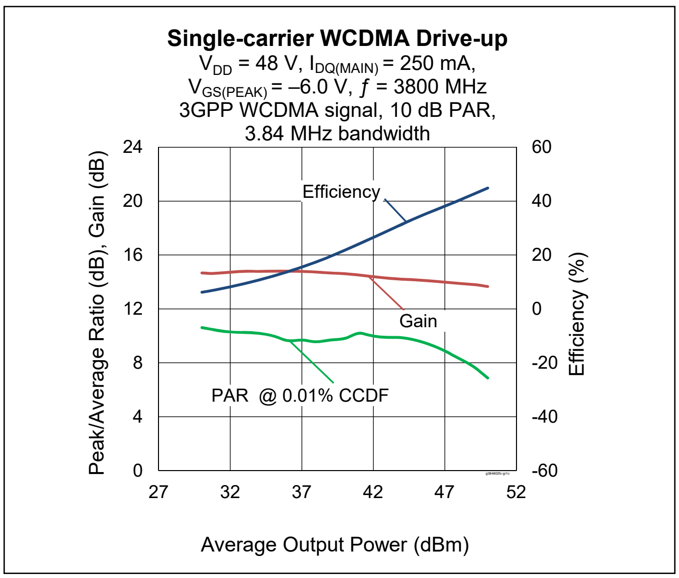
Thermally-Enhanced High Power RF GaN on SiC Amplifier, 400 W, 48 V, 3600 – 3800 MHz



Package Types: H-37248C-4
PN: GTRA384802FC

Description

The GTRA384802FC is a 400-watt (P_{3dB}) GaN on SiC HEMT D-mode amplifier for use in multi-standard cellular power amplifier applications. It features input and output matching, high efficiency, and a thermally-enhanced package with earless flange.



Features

- GaN on SiC HEMT technology
- Asymmetric Doherty design
  - Main: P_{3dB} = 200 W typ
  - Peak: P_{3dB} = 280 W typ
- Typical pulsed CW performance, 3800 MHz, 48 V, combined outputs, Doherty @ P_{3dB}, 10 µs, 10% duty cycle
  - Output power = 400 W
  - Drain efficiency = 62%
  - Gain = 12 dB
- Capable of handling 10:1 VSWR at 48 V, 63 W (WCDMA)output power
- Human Body Model Class 1B (per ANSI/ESDA/JEDEC JS-001)
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in the Doherty test fixture)

V_{DD} = 48 V, I_{DQ} = 250 mA, P_{OUT} = 63 W avg, $V_{GS(PEAK)}$ = –6 V, ƒ = 3800 MHz, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Gain	G_{ps}	12	13	—	dB
Drain Efficiency	η_D	38.5	42	—	%
Adjacent Channel Power Ratio	ACPR	—	–33	–29	dBc
Output PAR @ 0.01% CCDF	OPAR	7.3	7.8	—	dB

Note:
All published data at T_{CASE} = 25°C unless otherwise indicated
ESD: Electrostatic discharge sensitive device—observe handling precautions!

RoHS compliant

DC Characteristics

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source Breakdown Voltage (main)	$V_{BR(DSS)}$	150	—	—	V	V_{GS} = –8 V, I_D = 10 mA
Drain-source Breakdown Voltage (peak)						
Drain-source Leakage Current	I_{DSS}	—	—	5	mA	V_{GS} = -8 V, V_{DS} = 10 V
Gate Threshold Voltage (main)	$V_{GS(th)}$	–3.8	–3.0	–2.3	V	V_{DS} = 10 V, I_D = 25 mA
Gate Threshold Voltage (peak)						V_{DS} = 10 V, I_D = 36 mA

Recommended Operating Voltages

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain Operating Voltage	V_{DD}	0	—	50	V	
Gate Quiescent Voltage	$V_{GS(Q)}$	-3.9	–2.9	-2.0		V_{DS} =48 V, I_D = 250 mA

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	125	V
Gate-source Voltage	V_{GS}	–10 to +2	
Operating Voltage	V_{DD}	55	
Gate Current (main)	I_G	25.2	mA
Gate Current (peak)		36	
Drain Current (main)	I_D	9.5	A
Drain Current (peak)		13.5	
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	

Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range (V_{DD}) specified above.

Thermal Characteristics

Parameter	Symbol	Value	Unit	Conditions
Thermal Resistance (main)	$R_{\theta JC}$	1.6	°C/W	T_{CASE} = 70°C, 95 W DC , 48 V
Thermal Resistance (peak)		1.1		T_{CASE} = 70°C, 141 W DC, 48 V

Ordering Information

Type and Version	Order Code	Package Description	Shipping
GTRA384802FC V1 R0	GTRA384802FC-V1-R0	H-37248C-4, earless flange	Tape & Reel, 50 pcs
GTRA384802FC V1 R2	GTRA384802FC-V1-R2	H-37248C-4, earless flange	Tape & Reel, 250 pcs

Typical Performance (data taken in a the production test fixture)

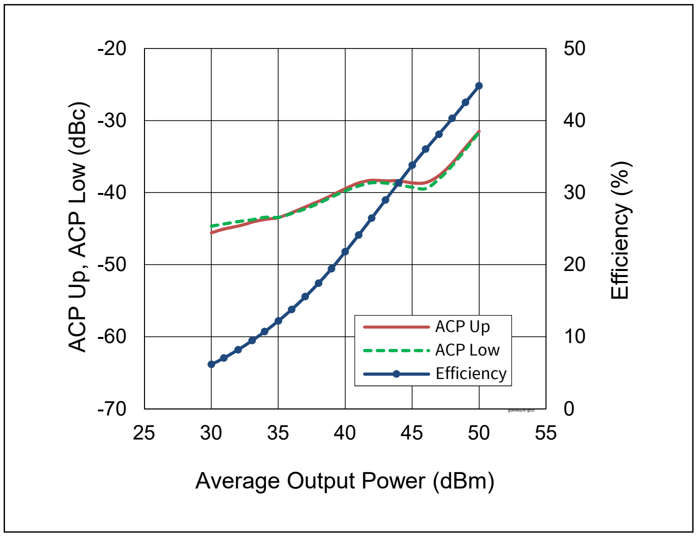


Figure 1. Single-carrier WCDMA Drive-up

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 250 mA,
$V_{GS(PEAK)}$ = –6.0V, f = 3800 MHz
3GPP WCDMA signal, 10 dB PAR,
3.84 MHz bandwidth

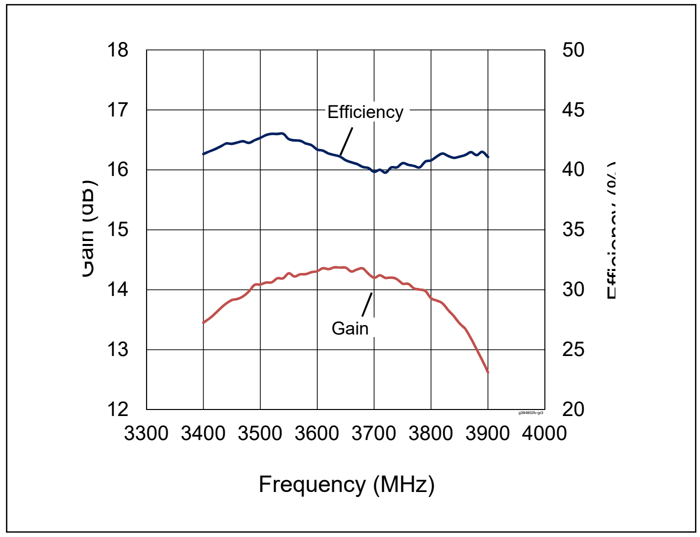


Figure 2. Single-carrier WCDMA Broadband

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 250 mA,
$V_{GS(PEAK)}$ = –6.0V, P_{OUT} = 48 dBm
3GPP WCDMA signal, 10 dB PAR

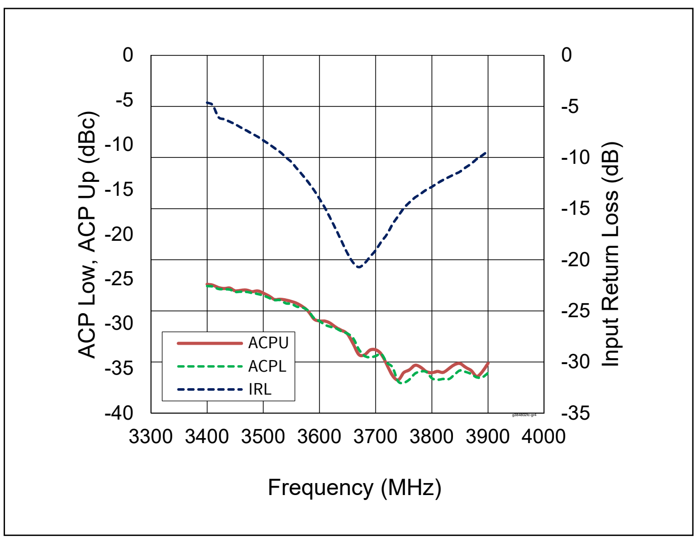


Figure 3. Single-carrier WCDMA Broadband

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 250 mA,
$V_{GS(PEAK)}$ = –6.0 V, P_{OUT} = 48 dBm
3GPP WCDMA signal, 10 dB PAR

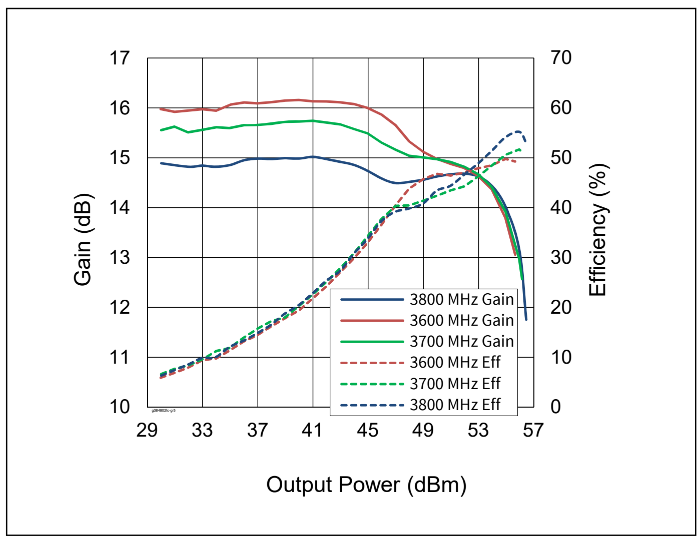


Figure 4. CW Performance

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 250 mA,
$V_{GS(PEAK)}$ = –6.0 V

Typical Performance (cont.)

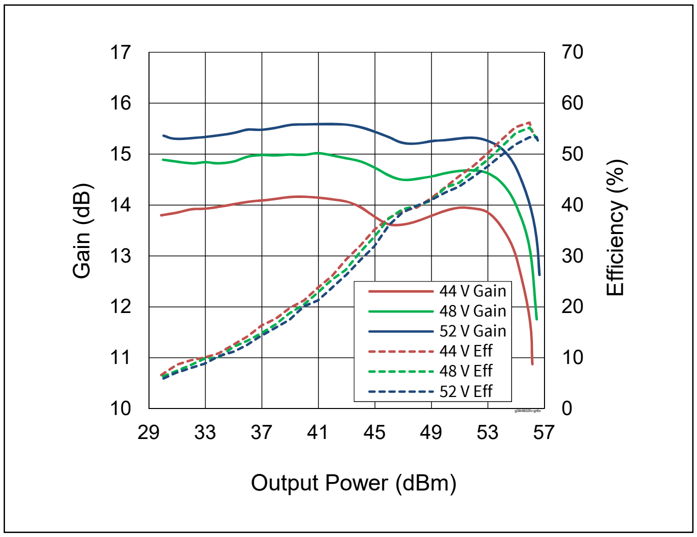


Figure 5. CW Performance at various V_{DD}

$I_{DQ(MAIN)}$ = 250 mA, $V_{GS(PEAK)}$ = –6.0V
f = 3800 MHz

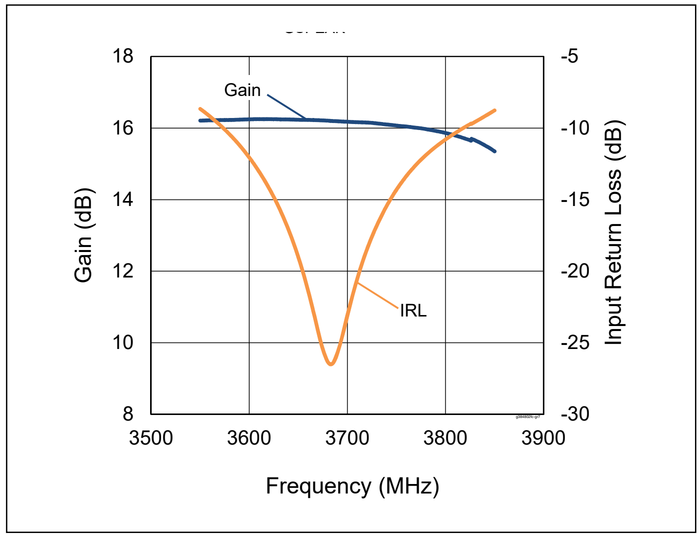


Figure 6. Small Signal CW Gain & Input Return Loss

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 250 mA,
$V_{GS(PEAK)}$ = –6.0 V

Load Pull

Main side load pull performance – pulsed CW signal: 10 µsec, 10% duty cycle, 48 V, I_{DQ} = 250 mA , class AB

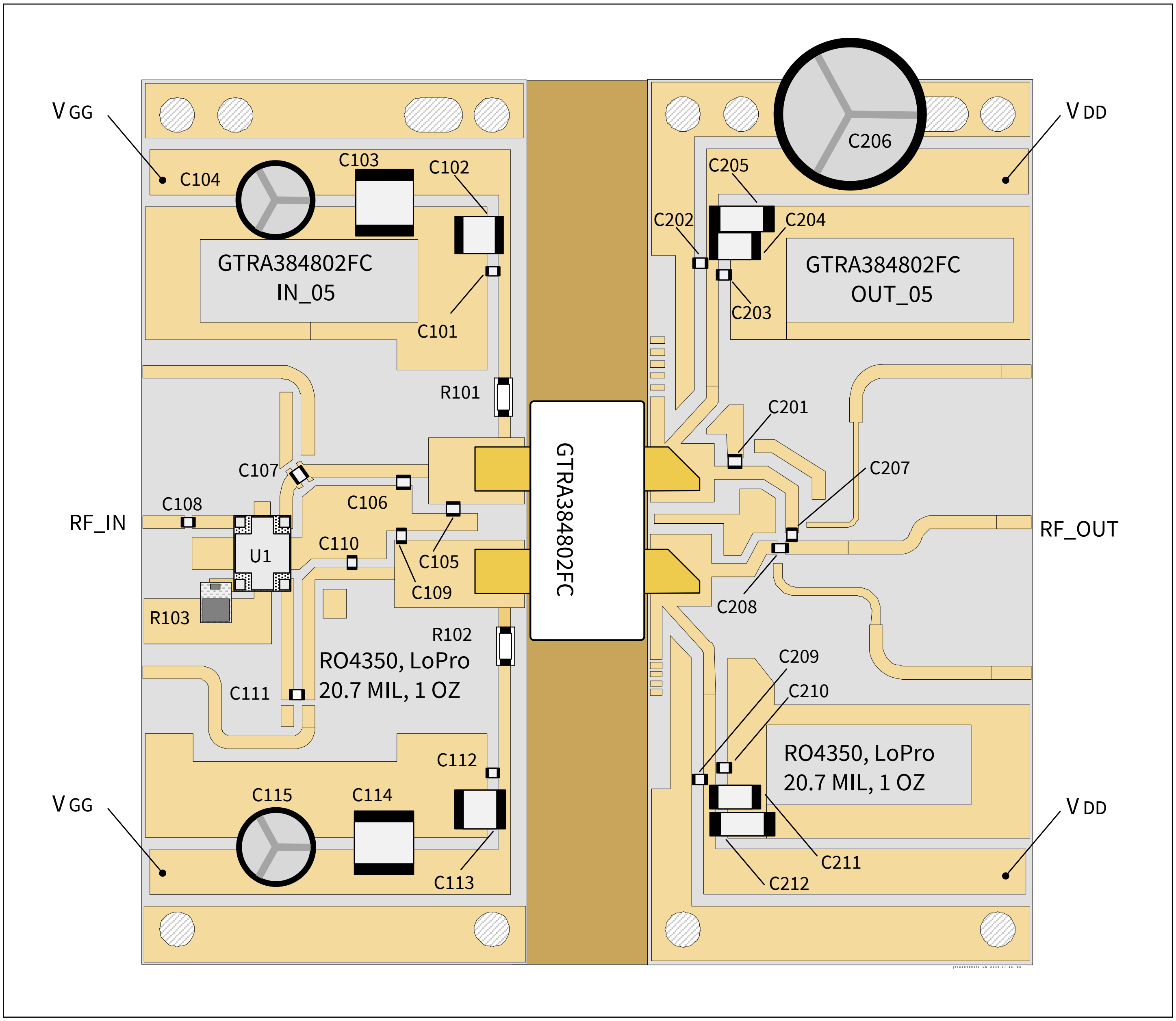
		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Z_s [Ω]	Z_l [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	Efficiency [%]	Z_l[Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	Efficiency [%]
3600	11.2 – j7.4	10.2 + j0	18.1	54.70	295	31.3	11.7 – j7	17.0	48.70	74	57.5
3700	6.2 – j5.7	9.5 + j0.9	17.6	54.60	288	31.3	7.5 – j15.6	16.0	48.10	65	57.5
3800	4.0 – j7.3	8.4 + j2	17.4	54.60	288	31.2	16 – j24	14.6	47.20	52	55.5

Peak side load pull performance – pulsed CW signal: 10 µsec, 10% duty cycle, 48 V, I_{DQ} = 360 mA, class AB

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Z_s [Ω]	Z_l [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	Efficiency [%]	Z_l[Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	Efficiency [%]
3600	15 – j11.4	3 – j8.5	15.4	55.90	389	57.5	1.5 – j7.3	18.5	54.60	288	67.0
3700	10.8 – j8.8	3 – j8.8	14.9	55.60	363	52.2	3 – j7.1	15.7	55.00	316	61.3
3800	6.7 – j8	3 – j8.8	15.2	55.60	363	56.9	1.6 – j7.6	17.0	53.50	224	61.8

Evaluation Board, 3600 – 3800 MHz

Evaluation Board Part Number	LTA/GTRA384802FC-V1
PCB Information	Rogers 4350, LoPro®, 0.526mm [0.0207”] thick, 1 oz. copper, ε_r = 3.55



Reference circuit assembly diagram (not to scale)

Components Information

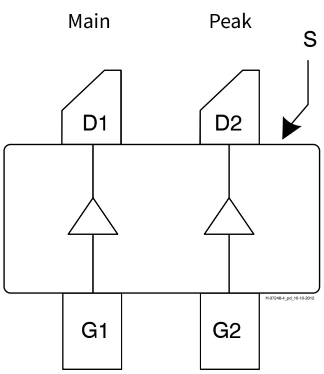
Component	Description	Manufacturer	P/N
Input			
C101, C107, C108, C111, C112	Capacitor, 10 pF	ATC	ATC800A100JT250XT
C102, C113	Capacitor, 1 µF	TDK Corporation	C4532X7R2A105M230KA
C103, C114	Capacitor, 10 µF, 100 V	TDK Corporation	C5750X7S2A106M230KB
C104, C115	Capacitor, 100 µF, 35 V	Panasonic Electronic Components	EEE-FT1V101AP
C105, C110	Capacitor, 1.2 pF	ATC	ATC800A1R2CT250XT
C106	Capacitor, 1.7 pF	ATC	ATC800A1R7CT250XT
C109	Capacitor, 0.5 pF	ATC	ATC800A0R5CT250XT
R101, R102	Resistor, 5.6 ohms	Panasonic Electronic Components	ERJ-8RQJ5R6V
R103	Resistor, 50 ohms	Anaren	C8A50Z4A
U1	Hybrid coupler	Anaren	XC3500P-03S
Output			
C201	Capacitor, 0.2 pF	ATC	ATC800A0R2CT250XT
C202, C209	Capacitor, 1000 pF, 100 V	Murata Electronics North America	GRM188R72A102KA01D
C203, C207, C208, C210	Capacitor, 10 pF	ATC	ATC800A100JT250XT
C204, C211	Capacitor, 1 µF	TDK Corporation	C4532X7R2A105M230KA
C205, C212	Capacitor, 10 µF	TDK Corporation	C5750X7S2A106M230KB
C206	Capacitor, 220 µF	Panasonic Electronic Components	ECA-2AHG221

Bias Sequencing

Bias ON
1. Ensure RF is turned off
2. Apply pinch-off voltage of –5 V to the gate
3. Apply nominal drain voltage
4. Bias gate to desired quiescent drain current
5. Apply RF

Bias OFF
1. Turn RF off
2. Apply pinch-off voltage to the gate
3. Turn-off drain voltage
4. Turn-off gate voltage

Pinout Diagram (top view)



Pin	Description
D1	Drain Device 1 (Main)
D2	Drain Device 2 (Peak)
G1	Gate Device 1 (Main)
G2	Gate Device 2 (Peak)
S	Source (flange)

Lead connections for GTRA384802FC

Package Outline Specifications – Package H-37248C-4

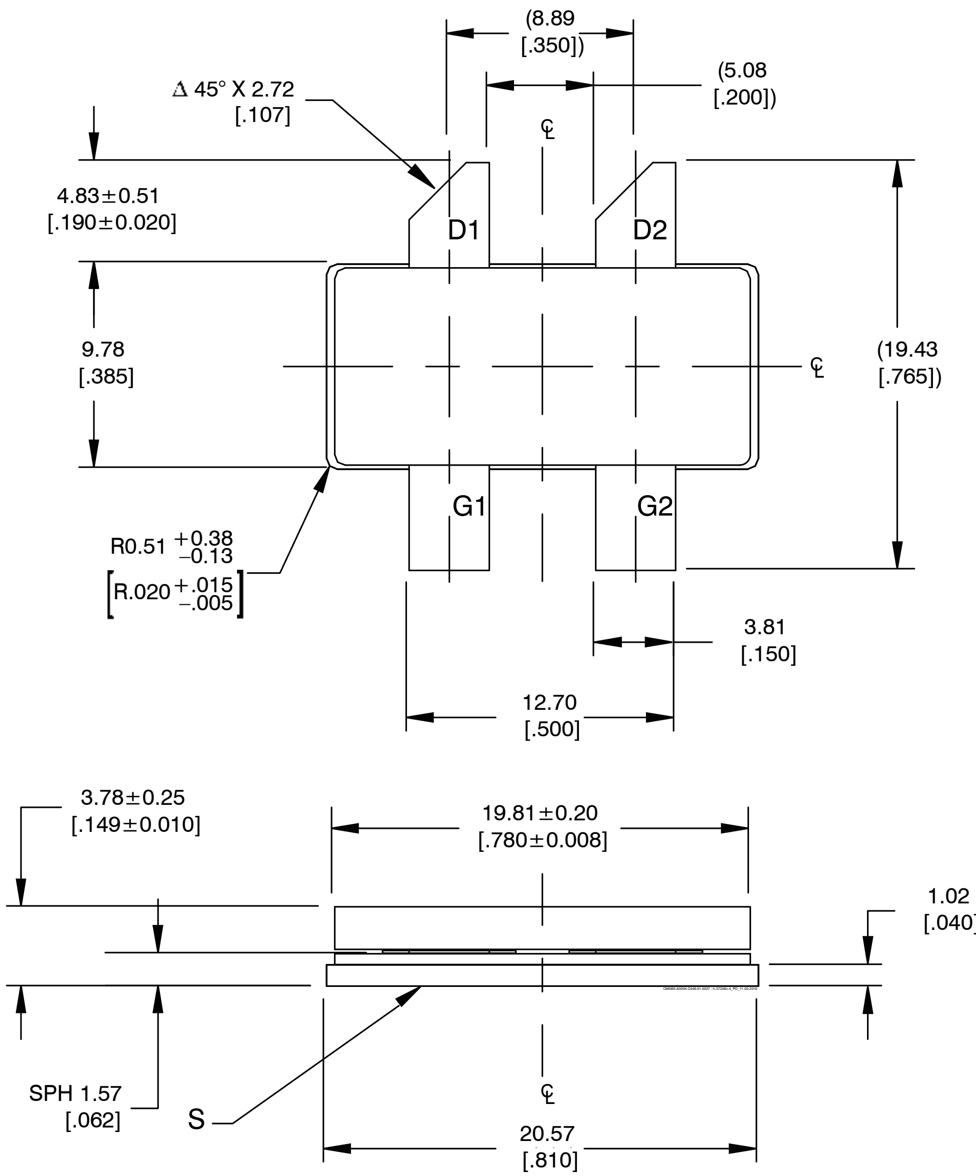


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994
2. Primary dimensions are mm, alternate dimensions are inches
3. All tolerances ± 0.127 [0.005]
4. Pins: D1, D2 – drain, G1, G2 – gate, S – source (flange)
5. Lead thickness: 0.13 ± 0.05 [0.005 ± 0.002]
6. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch]

Notes & Disclaimer