IXYS

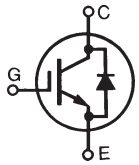
Advance Technical Information

GenX3™ 1200V IGBT w/ Diode

IXGR55N120A3H1

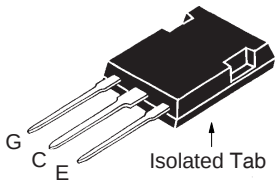
V_{CES} = 1200V
I_{C110} = 30A
$V_{CE(sat)} \leq$ 2.35V

(Electrically Isolated Tab)



Ultra-Low-Vsat PT IGBTs for up to 3kHz Switching

ISOPLUS 247™



G = Gate C = Collector
E = Emitter

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	1200	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	1200	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C (Chip Capability)	70	A
I_{C110}	T_C = 110°C	30	A
I_{F110}	T_C = 110°C	44	A
I_{CM}	T_C = 25°C, 1ms	330	A
SSOA (RBSOA)	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 3Ω Clamped Inductive Load	I_{CM} = 110 @ 0.8 • V_{CES}	A
P_C	T_C = 25°C	200	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062 in.) from Case for 10	260	°C
V_{ISOL}	50/60 Hz, 1 minute	2500	V~
F_C	Mounting Force	20..120/4.5..27	N/lb.
Weight		5	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
$V_{GE(th)}$	I_C = 1mA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V			25	μA
	Note 1, T_J = 125°C			1.5	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V			±100	nA
$V_{CE(sat)}$	I_C = 55A, V_{GE} = 15V, Note 2			2.35	V
	T_J = 125°C		2.20		

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 2500V~ Electrical Isolation
- Anti-Parallel Ultra Fast Diode
- Optimized for Low Conduction Losses

Advantages

- High Power Density
- Low Gate Drive Requirement

Applications

- Power Inverters
- UPS
- Motor Drives
- SMPS
- PFC Circuits
- Battery Chargers
- Welding Machines
- Lamp Ballasts
- Inrush Current Protection Circuits

© 2009 IXYS CORPORATION, All Rights Reserved

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	I_C = 55A, V_{CE} = 10V, Note 2	30	45		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1 MHz		4340		pF
C_{oes}			300		pF
C_{res}			115		pF
$Q_{g(on)}$	I_C = 55A, V_{GE} = 15V, V_{CE} = 0.5 • V_{CES}		185		nC
Q_{ge}			25		nC
Q_{gc}			75		nC
$t_{d(on)}$	**Inductive load, T_J = 25°C**		23		ns
t_{ri}	I_C = 55A, V_{GE} = 15V		42		ns
E_{on}	V_{CE} = 0.8 • V_{CES}, R_G = 3Ω		5.1		mJ
$t_{d(off)}$	Note 3		365		ns
t_{fi}			282		ns
E_{off}			13.3		mJ
$t_{d(on)}$	**Inductive load, T_J = 125°C**		24		ns
t_{ri}	I_C = 55A, V_{GE} = 15V		46		ns
E_{on}	V_{CE} = 0.8 • V_{CES}, R_G = 3Ω		9.5		mJ
$t_{d(off)}$	Note 3		618		ns
t_{fi}			635		ns
E_{off}			29.0		mJ
R_{thJC}				0.62	°C/W
R_{thCK}			0.15		°C/W

Reverse Diode (FRED)

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
V_F	I_F = 60A, V_{GE} = 0V, Note 2		1.85	2.5	V
	T_J = 150°C		1.90		V
t_{rr}	I_F = 60A, V_{GE} = 0V,		200		ns
I_{RM}	$-di_F/dt$ = 350A/μs, V_R = 600V, T_J = 100°C		24.6		A
R_{thJC}				0.42	°C/W

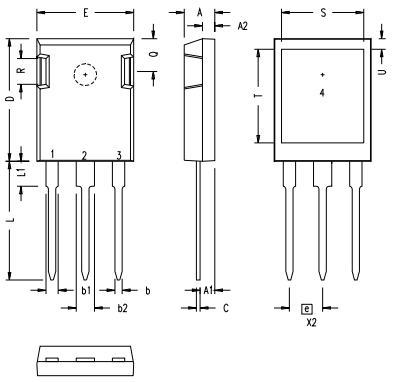
Notes:

1. Part must be heatsunk for high-temp Ices measurement.
2. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.
3. Switching times & energy losses may increase for higher V_{CE}(Clamp), T_J or R_G.

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

ISOPLUS247 (IXGR) Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,850,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405 B2 6,710,463 6,727,585 6,759,692 6,771,478 B2 7,005,734 B2 7,063,975 B2 7,071,537 7,157,338B2

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

IXYS:
IXGR55N120A3H1