

***RoHS Compliant***

## **2GB DDR3 1.35V SO-DIMM**

***Product Specifications***

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***Version 1.1***



***Apacer Technology Inc.***

1F., No.32, Zhongcheng Rd., Tucheng Dist., New Taipei City 236, Taiwan

Tel: +886-2-2267-8000

Fax: +886-2-2267-2261

[www.apacer.com](http://www.apacer.com)

## Table of Contents

|                                                  |    |
|--------------------------------------------------|----|
| General Description .....                        | 2  |
| Ordering Information .....                       | 2  |
| Key Parameters .....                             | 2  |
| Specifications: .....                            | 3  |
| Features: .....                                  | 4  |
| Pin Assignments .....                            | 5  |
| Pin Descriptions .....                           | 7  |
| Functional Block Diagram .....                   | 8  |
| Absolute Maximum Ratings .....                   | 9  |
| DRAM Component Operating Temperature Range ..... | 10 |
| Operating Conditions .....                       | 11 |
| Mechanical Drawing .....                         | 12 |

## General Description

Apacer **78.A2GDA.4010C** is a 256M x 64 DDR3 SDRAM (Synchronous DRAM) SO-DIMM. This high-density memory module consists of 4 pieces 256M x 16 bits with 8 banks DDR3 synchronous DRAMs in BGA packages and a 2K EEPROM. The module is a 204-pins small-outlined, dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR3 SDRAM. The following provides general specifications of this module.

## Ordering Information

| Part Number    | Bandwidth   | Speed Grade | Max Frequency | CAS Latency |
|----------------|-------------|-------------|---------------|-------------|
| 78.A2GDA.4010C | 12.8 GB/sec | 1600 Mbps   | 800 MHz       | CL11        |

| Density | Organization | Component  | Rank |
|---------|--------------|------------|------|
| 2GB     | 256M x 64    | 256M x16*4 | 1    |

## Key Parameters

| MT/s        | DDR3-1066 | DDR3-1333 | DDR3-1600 | Unit |
|-------------|-----------|-----------|-----------|------|
| Grade       | -CL7      | -CL9      | -CL11     |      |
| tCK (min)   | 1.875     | 1.5       | 1.25      | ns   |
| CAS latency | 7         | 9         | 11        | tCK  |
| tRCD (min)  | 13.125    | 13.5      | 13.75     | ns   |
| tRP (min)   | 13.125    | 13.5      | 13.75     | ns   |
| tRAS (min)  | 37.5      | 36        | 35        | ns   |
| tRC (min)   | 50.625    | 49.5      | 48.75     | ns   |
| CL-tRCD-tRP | 7-7-7     | 9-9-9     | 11-11-11  | tCK  |

## Specifications:

- ◆ On-DIMM thermal sensor : No
- ◆ Organization: 256 words x 64 bits, 1 rank
- ◆ Integrating 4 pieces of 4G bits DDR3 SDRAM sealed in FBGA
- ◆ Package: 204-pin socket type small outline dual in-line memory module (SO-DIMM)
- ◆ PCB: height 30.0mm, lead pitch 0.6 mm (pin), lead-free (RoHS compliant)
- ◆ Power supply VDD: 1.35V (+0.1V ~ -0.067V)
- ◆ Serial Presence Detect (SPD)
- ◆ Eight Internal banks for concurrent operation (components)
- ◆ Interface: SSTL\_13
- ◆ Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- ◆ CAS Latency (CL): 6, 7, 8, 9, 10, 11
- ◆ CAS Write Latency (CWL): 5, 6, 7, 8
- ◆ Supports auto pre-charge option for each burst access
- ◆ Supports auto-refresh/self-refresh
- ◆ Refresh cycles:  $7.8 \mu s$  at  $0^{\circ}C \leq TC \leq +85^{\circ}C$

## Features:

- ◆ Double-data-rate architecture: 2 data transfers per clock cycle
- ◆ The high-speed data transfer is realized by the 8-bits prefetch pipelined architecture.
- ◆ Bi-directional differential data strobe (DQS and /DQS) is transmitted / received with data for capturing data at the receiver
- ◆ DQS: edge-aligned with data for read; center-aligned with data for write
- ◆ Differential clock inputs (CK and /CK)
- ◆ DLL aligns DQ and DQS transitions with CK transitions
- ◆ Data mask (DM) for writing data
- ◆ Posted CAS by programmable additive latency for enhanced command and data bus efficiency
- ◆ On-Die-Termination (ODT) for improved signal quality: Synchronous ODT/Dynamic ODT/Asynchronous ODT
- ◆ Multi-Purpose Register (MPR) for temperature read out
- ◆ ZQ calibration for DQ drive and ODT
- ◆ Programmable Partial Array Self-Refresh (PASR)
- ◆ /Reset pin for power-up sequence and reset function
- ◆ SRT range: normal/extended, auto/manual self-refresh
- ◆ Programmable output driver impedance control

## Pin Assignments

| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---------|----------|---------|----------|---------|----------|---------|----------|
| 1       | VREFDQ   | 53      | DQ19     | 105     | VDD      | 157     | DQ42     |
| 3       | VSS      | 55      | VSS      | 107     | A10(AP)  | 159     | DQ43     |
| 5       | DQ0      | 57      | DQ24     | 109     | BA0      | 161     | VSS      |
| 7       | DQ1      | 59      | DQ25     | 111     | VDD      | 163     | DQ48     |
| 9       | VSS      | 61      | VSS      | 113     | /WE      | 165     | DQ49     |
| 11      | DM0      | 63      | DM3      | 115     | /CAS     | 167     | VSS      |
| 13      | VSS      | 65      | VSS      | 117     | VDD      | 169     | /DQS6    |
| 15      | DQ2      | 67      | DQ26     | 119     | A13      | 171     | DQS6     |
| 17      | DQ3      | 69      | DQ27     | 121     | /CS1     | 173     | VSS      |
| 19      | VSS      | 71      | VSS      | 123     | VDD      | 175     | DQ50     |
| 21      | DQ8      | 73      | CKE0     | 125     | NC       | 177     | DQ51     |
| 23      | DQ9      | 75      | VDD      | 127     | VSS      | 179     | VSS      |
| 25      | VSS      | 77      | NC       | 129     | DQ32     | 181     | DQ56     |
| 27      | /DQS1    | 79      | BA2      | 131     | DQ33     | 183     | DQ57     |
| 29      | DQS1     | 81      | VDD      | 133     | VSS      | 185     | VSS      |
| 31      | VSS      | 83      | A12(BC)  | 135     | /DQS4    | 187     | DM7      |
| 33      | DQ10     | 85      | A9       | 137     | DQS4     | 189     | VSS      |
| 35      | DQ11     | 87      | VDD      | 139     | VSS      | 191     | DQ58     |
| 37      | VSS      | 89      | A8       | 141     | DQ34     | 193     | DQ59     |
| 39      | DQ16     | 91      | A5       | 143     | DQ35     | 195     | VSS      |
| 41      | DQ17     | 93      | VDD      | 145     | VSS      | 197     | SA0      |
| 43      | VSS      | 95      | A3       | 147     | DQ40     | 199     | VDDSPD   |
| 45      | /DQS2    | 97      | A1       | 149     | DQ41     | 201     | SA1      |
| 47      | DQS2     | 99      | VDD      | 151     | VSS      | 203     | VTT      |
| 49      | VSS      | 101     | CK0      | 153     | DM5      |         |          |
| 51      | DQ18     | 103     | /CK0     | 155     | VSS      |         |          |

| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---------|----------|---------|----------|---------|----------|---------|----------|
| 2       | VSS      | 54      | VSS      | 106     | VDD      | 158     | DQ46     |
| 4       | DQ4      | 56      | DQ28     | 108     | BA1      | 160     | DQ47     |
| 6       | DQ5      | 58      | DQ29     | 110     | /RAS     | 162     | VSS      |
| 8       | VSS      | 60      | VSS      | 112     | VDD      | 164     | DQ52     |
| 10      | /DQS0    | 62      | /DQS3    | 114     | /CS0     | 166     | DQ53     |
| 12      | DQS0     | 64      | DQS3     | 116     | ODT0     | 168     | VSS      |
| 14      | VSS      | 66      | VSS      | 118     | VDD      | 170     | DM6      |
| 16      | DQ6      | 68      | DQ30     | 120     | ODT1     | 172     | VSS      |
| 18      | DQ7      | 70      | DQ31     | 122     | NC       | 174     | DQ54     |
| 20      | VSS      | 72      | VSS      | 124     | VDD      | 176     | DQ55     |
| 22      | DQ12     | 74      | CKE1     | 126     | VREFCA   | 178     | VSS      |
| 24      | DQ13     | 76      | VDD      | 128     | VSS      | 180     | DQ60     |
| 26      | VSS      | 78      | A15(NC)  | 130     | DQ36     | 182     | DQ61     |
| 28      | DM1      | 80      | A14(NC)  | 132     | DQ37     | 184     | VSS      |
| 30      | /RESET   | 82      | VDD      | 134     | VSS      | 186     | /DQS7    |
| 32      | VSS      | 84      | A11      | 136     | DM4      | 188     | DQS7     |
| 34      | DQ14     | 86      | A7       | 138     | VSS      | 190     | VSS      |
| 36      | DQ15     | 88      | VDD      | 140     | DQ38     | 192     | DQ62     |
| 38      | VSS      | 90      | A6       | 142     | DQ39     | 194     | DQ63     |
| 40      | DQ20     | 92      | A4       | 144     | VSS      | 196     | VSS      |
| 42      | DQ21     | 94      | VDD      | 146     | DQ44     | 198     | /EVENT   |
| 44      | VSS      | 96      | A2       | 148     | DQ45     | 200     | SDA      |
| 46      | DM2      | 98      | A0       | 150     | VSS      | 202     | SCL      |
| 48      | VSS      | 100     | VDD      | 152     | /DQS5    | 204     | VTT      |
| 50      | DQ22     | 102     | CK1      | 154     | DQS5     |         |          |
| 52      | DQ23     | 104     | /CK1     | 156     | VSS      |         |          |

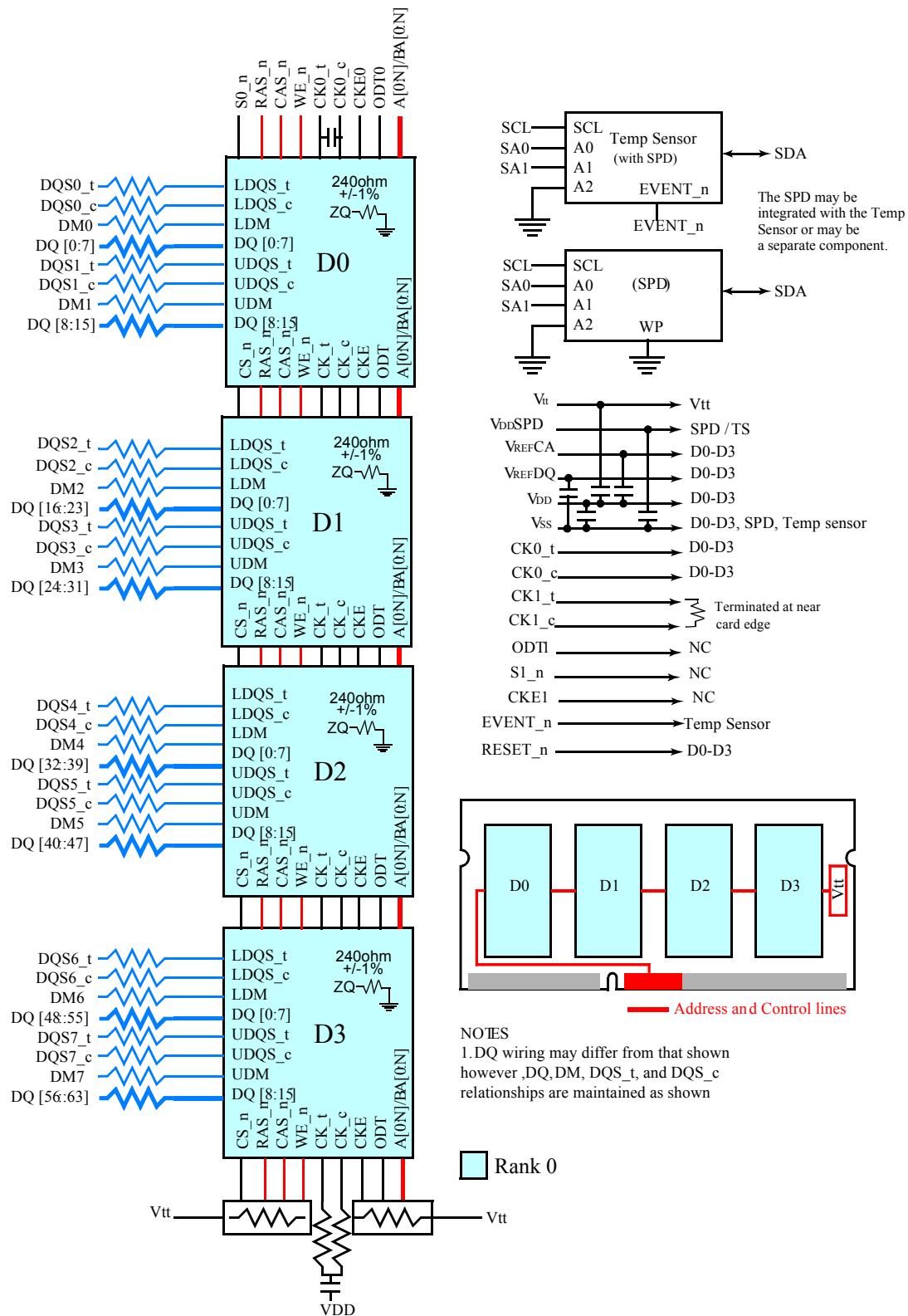
## Pin Descriptions

| Pin Name | Description                                                             |
|----------|-------------------------------------------------------------------------|
| Ax*      | SDRAM address bus                                                       |
| BAx      | SDRAM bank select                                                       |
| DQx      | DIMM memory data bus                                                    |
| /RAS     | SDRAM row address strobe                                                |
| /CAS     | SDRAM column address strobe                                             |
| /WE      | SDRAM write enable                                                      |
| /CSx     | SDRAM Chip select lines                                                 |
| CKEx     | SDRAM clock enable lines                                                |
| CKx      | SDRAM clock input                                                       |
| /CKx     | SDRAM Differential clock input                                          |
| DQSx     | SDRAM data strobes(positive line of differential pair)                  |
| /DQSx    | SDRAM data strobes(negative line of differential pair)                  |
| DMx      | SDRAM input mask                                                        |
| SCL      | Clock input for serial PD                                               |
| SDA      | Data input/output for serial PD                                         |
| SAx      | Serial address input                                                    |
| VDD      | Power for internal circuit                                              |
| VDDSPD   | Serial EEPROM positive power supply                                     |
| VREFDQ   | SDRAM I/O reference supply                                              |
| VREFCA   | SDRAM command/address reference supply                                  |
| VSS      | Power supply return(ground)                                             |
| VTT      | SDRAM I/O termination supply                                            |
| /RESET   | Set DRAM to known state                                                 |
| ODTx     | On-die termination control lines                                        |
| NC       | Spare pins(no connect)                                                  |
| /EVENT   | An output of the thermal sensor to indicate critical module temperature |

\*IC Component Composition:

|         |        |
|---------|--------|
| 128Mx8  | A0~A13 |
| 256Mx8  | A0~A14 |
| 256Mx16 | A0~A14 |
| 512Mx8  | A0~A15 |
| 1024Mx8 | A0~A15 |

# Functional Block Diagram



## NOTES

1. DQ wiring may differ from that shown however ,DQ,DM, DQS\_t, and DQS\_c relationships are maintained as shown

Rank 0

## Absolute Maximum Ratings

| Parameter                           | Symbol                             | Description       | Units |
|-------------------------------------|------------------------------------|-------------------|-------|
| Voltage on VDD pin relative to Vss  | V <sub>DD</sub>                    | - 0.4 V ~ 1.975 V | V     |
| Voltage on VDDQ pin relative to Vss | V <sub>DDQ</sub>                   | - 0.4 V ~ 1.975 V | V     |
| Voltage on any pin relative to Vss  | V <sub>IN</sub> , V <sub>OUT</sub> | - 0.4 V ~ 1.975 V | V     |
| Storage Temperature                 | TSTG                               | -55 to +100       | °C    |

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6 x VDDQ, when VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

# DRAM Component Operating Temperature Range

| Symbol            | Parameter                          | Rating   | Units | Notes |
|-------------------|------------------------------------|----------|-------|-------|
| T <sub>OPER</sub> | Normal Operating Temperature Range | 0 to 85  | °C    | 1,2   |
|                   | Extended Temperature Range         | 85 to 95 | °C    | 1,3   |

## Notes:

- Operating Temperature T<sub>OPER</sub> is the case surface temperature on the center / top side of the DRAM. For measurement conditions please refer to the JEDEC document JESD51-2.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported during operation, the DRAM case temperature must be maintained between 0°C - 85°C under all operating conditions.
- Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
  - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs.
  - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.

## Operating Conditions

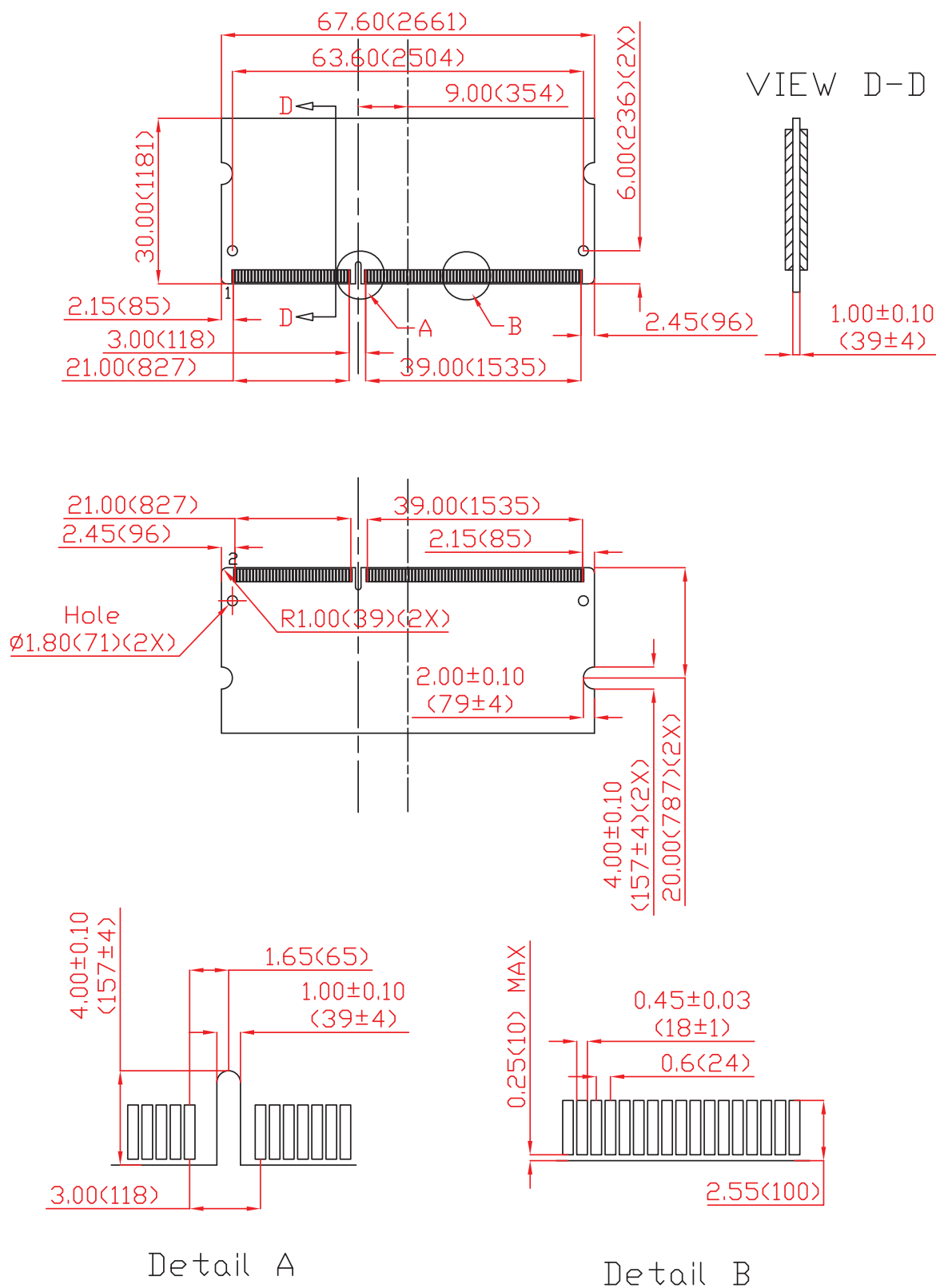
### Recommended DC Operating Conditions - DDR3L (1.35V) operation

| Symbol | Parameter                 | Rating |      |      | Units |
|--------|---------------------------|--------|------|------|-------|
|        |                           | Min.   | Typ. | Max. |       |
| VDD    | Supply Voltage            | 1.283  | 1.35 | 1.45 | V     |
| VDDQ   | Supply Voltage for Output | 1.283  | 1.35 | 1.45 | V     |

#### Notes:

1. If minimum limit is exceeded, input levels shall be governed by DDR3L specifications.
2. Under 1.5V operation, this DDR3L device operates to the DDR3 specifications under the same speed timings as defined for this device.
3. Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3L operation.

# Mechanical Drawing



## Revision History

| Revision | Date       | Description                  | Remark |
|----------|------------|------------------------------|--------|
| 0.9      | 08/28/2012 | Official release             |        |
| 1.0      | 08/29/2012 | release                      |        |
| 1.1      | 07/23/2013 | Changed headquarters address |        |

## Global Presence

### Taiwan (Headquarters)

**Apacer Technology Inc.**

1F., No.32, Zhongcheng Rd., Tucheng Dist.,

New Taipei City 236, Taiwan R.O.C.

Tel: +886-2-2267-8000

Fax: +886-2-2267-2261

[amtsales@apacer.com](mailto:amtsales@apacer.com)

### U.S.A.

**Apacer Memory America, Inc.**

386 Fairview Way, Suite102,

Milpitas, CA 95035

Tel: 1-408-518-8699

Fax: 1-408-935-9611

[sa@apacerus.com](mailto:sa@apacerus.com)

### Japan

**Apacer Technology Corp.**

5F, Matsura Bldg., Shiba, Minato-Ku

Tokyo, 105-0014, Japan

Tel: 81-3-5419-2668

Fax: 81-3-5419-0018

[jpservices@apacer.com](mailto:jpservices@apacer.com)

### Europe

**Apacer Technology B.V.**

Science Park Eindhoven 5051 5692 EB Son,

The Netherlands

Tel: 31-40-267-0000

Fax: 31-40-267-0000#6199

[sales@apacer.nl](mailto:sales@apacer.nl)

### China

**Apacer Electronic (Shanghai) Co., Ltd**

1301, No.251,Xiaomuqiao Road, Shanghai,

200032, China

Tel: 86-21-5529-0222

Fax: 86-21-5206-6939

[sales@apacer.com.cn](mailto:sales@apacer.com.cn)

### India

**Apacer Technologies Pvt Ltd,**

# 535, 1st Floor, 8th cross, JP Nagar 3rd Phase,

Bangalore – 560078, India

Tel: 91-80-4152-9061

[sales\\_india@apacer.com](mailto:sales_india@apacer.com)

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