SiC- JFET

Silicon Carbide- Junction Field Effect Transistor

CoolSiC™

1200 V CoolSiC™ Power Transistor
IJW120R100T1

Final Datasheet

Rev. 2.0, <2013-09-11>

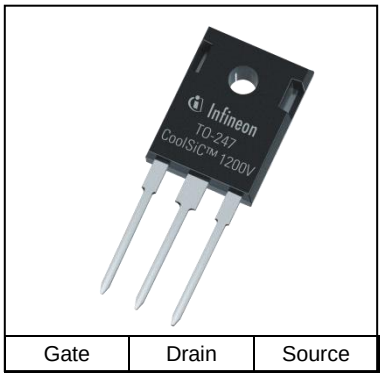
Power Management & Multimarket

1200 V Silicon Carbide JFET

IJW120R100T1

Description

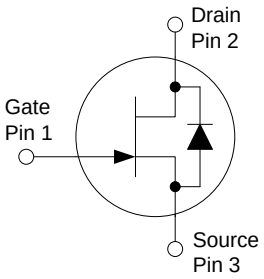
CoolSiC™ is Infineon's new family of active power switches based on silicon carbide. Combining the excellent material properties of silicon carbide with our normally-on JFET concept allows the next steps towards higher performance paired with very high ruggedness. The extremely low switching and conduction losses make applications even more efficient, compact, lighter and cooler.



Gate	Drain	Source

Features

- Ultra fast switching
- Internal fast body diode
- Low intrinsic capacitance
- Low gate charge
- 175 °C maximum operating temperature



Benefits

- Enabling higher system efficiency and/ or higher output power in same housing
- Enabling higher frequency / increased power density solutions
- System cost / space savings due to reduced cooling requirements
- Higher system reliability due to enlarged junction temperatures rates
- Reduced EMI

Applications

- Solar Inverters
- High voltage DC/ DC or AC/ DC conversion
- Bidirectional Inverter
- Compliant for applications according to climate class IEC 60721-3-4 (4K4H)

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	1200	V
$R_{DS(on)\ max}$	100	mΩ
$Q_{G,\ typ}$	72	nC
$I_{D,\ pulse}$	78	A
E_{oss} @ 800 V	28	µJ

Table 2 Pin Definition

Pin 1	Pin 2	Pin 3
Gate	Drain	Source

Type / ordering Code	Package	Marking	Related links
IJW120R100T1 [1)]	PG-TO247-3	120R100T1	www.infineon.com/CoolSiC

1) J-STD20 and JESD22

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1 Application considerations

1.1 Introduction

Wide bandgap semiconductors are very attractive as a basematerial for power devices due to low losses, improved temperature capability and high thermal conductivity. Infineon's silicon carbide schottky diodes have been commercially available on the market for many years. The material and technology knowhow has been used to create new active switches based on silicon carbide providing significant improvement in the value proposition in comparison to known devices such as:

- Resistive forward characteristic in first and third quadrant
- Monolithic integrated body diode, in switching performance very close to SiC schottky barrier diodes
- Very fast and controllable switching transients
- Very low capacitances and gate charge

These benefits result in higher system efficiency, allow higher switching frequencies, increased power density and reduced cooling efforts. Due to the normally-on JFET concept any reliability-relevant issues from gate oxides on SiC are completely avoided. To allow the use of this normally-on concept in voltage-source-inverter configurations we propose the following driver circuit.

1.2 Driver circuit

Being a normally-on device, the JFET is in its on-state at zero gate voltage and will go into the off-state at negative gate voltage. The normally off behavior can be easily realized by implementing a cascode configuration with a low voltage MOSFET as shown in Figure 1 *(state of the art cascode*). At e.g. startup, the LV MOSFET is in the off-state pushing the source of the JFET to positive potential relative to its gate and keeping the JFET hence in the off-state.

In this conventional cascode, the LV MOSFET will be switched on and off together with the JFET in each switching cycle. This approach has two major drawbacks: firstly, at turn-on additional switching losses will occur as the output capacitance of the LV MOSFET needs to be charged from the positive rail voltage, secondly the combination allows no direct control of the JFET due to the absence of a (JFET) - Drain- to- (LV MOS) - Gate capacitance. These drawbacks can be avoided with the proposed "direct drive" approach. Here, the JFET is directly switched on and off by applying a negative gate voltage and 0V respectively, whereas the series connected LV MOSFET is always in its on- state. The LV MOSFET is turned off only during start- up and e.g. emergency cases such as loss of auxiliary power supply. This solution represents the best match between performance and safety requirements. The driving scheme with a dedicated driver is shown in Fig. 2 *(direct drive technology with 1EDI30J12Cx).*

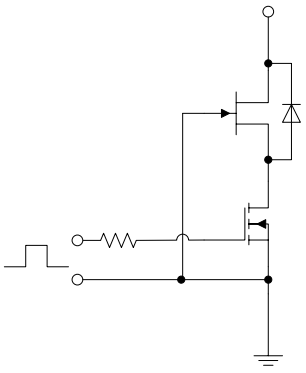


Figure 1: state of the art cascode

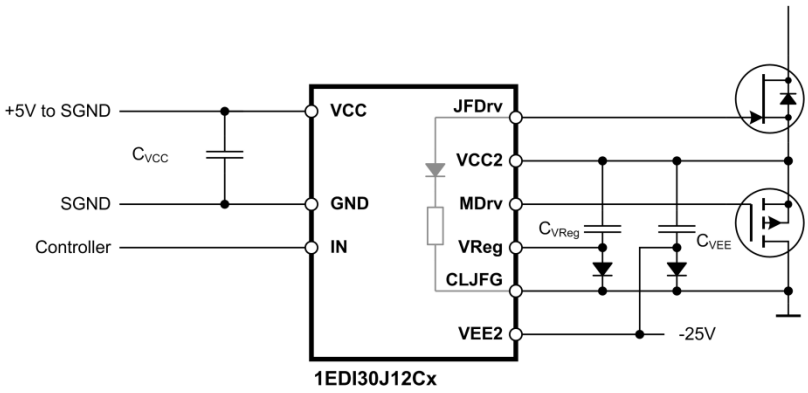


Figure 2: direct drive technology with 1EDI30J12Cx

1.3 Device characteristics

1.3.1 Gate voltage window

The gate electrode of the JFET shows, in contrary to isolated MOSFET concepts, a bipolar pn-junction like characteristic: it get's forward biased at around +2.5 V, hence a bipolar current will flow into the gate once the gate- to- source voltage exceeds 2.5 V. This is uncritical and may be used to turn-on the device faster than with the recommended 0 V turn-on. At 25 °C the threshold voltage of the channel can vary between -12 V and -15 V (*Figure 3: $V_{GS(th)}=f(T_j)$ parameter: I_{GSS})*. The products will be delivered within three groups (bin1, bin2, bin3) of 1 V range each. For paralleling, it is only allowed to parallel devices from the same bin. The use of devices from different bins for paralleling leads to different thermal device behavior. At a voltage of around -23 V the gate- to-source junction enters reverse breakdown, which leads to a temperature dependend bipolar current flow across the junction. In pure voltage driven turn-on and turn-off the lower gate voltage should stay within the window between the pinch-off (threshold) and the punch-through (increased leakage) voltage. For fast and safe turn-off it is strongly recommended to move the lower gate voltage level as close as possible to the punch-through threshold.

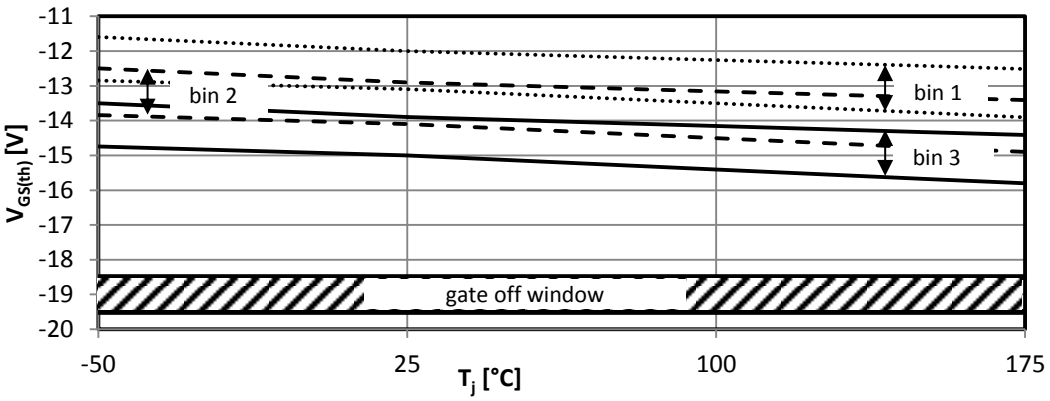


Figure 3: $V_{GS(th)}=f(T_j)$ parameter: I_{DSS}=10 µA

1.3.2 Controllability

The JFET can be well controlled through its miller plateau with an external gate resistor (*Figure 4: $dV_{off}/dt= f(I_{DS})$, $dV_{on}/dt= f(I_{DS})$, $dI_{off}/dt= f(I_{DS})$, $dI_{on}/dt= f(I_{DS})$ parameter: T_j=25 °C, $R_{G,\ external}$)*. Especially dI/ dt is saturating at high current levels. This helps to avoid voltage overshoots in peak current conditions. It is strongly recommended to use very low turn-off gate resistors (down to zero Ohm external gate resistor) to achive maximum performance from the device as well as to avoid any parasitic dV/dt or dI/dt coupled turn-on effects. As shown in the maximum rating division of the datasheet the external gate loop resistance should be lower than 5.1 Ω.

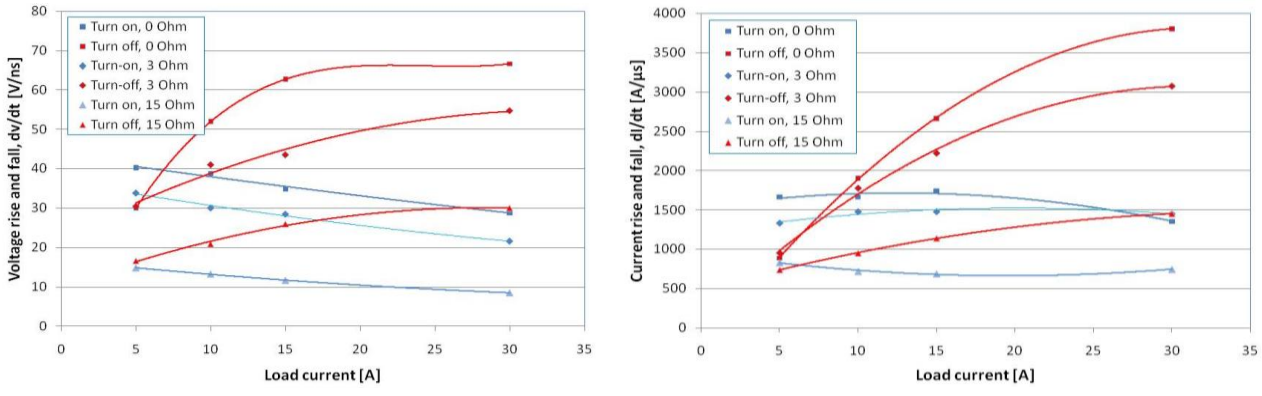


Figure 4: $dV_{off}/dt= f(I_{DS})$, $dV_{on}/dt= f(I_{DS})$, $dI_{off}/dt= f(I_{DS})$, $dI_{on}/dt= f(I_{DS})$ parameter: T_j=25 °C, $R_{G,\ external}$

1.3.3 Reverse biased behavior

The monolithically integrated body diode shows a switching performance close to that of an external SiC schottky barrier diodes, renowned for their zero reverse recovery characteristic. Figure 5 *(reverse recovery characteristic I_{SD}= 2 A left and I_{SD}= 10 A; T_j= 150 °C; V_{bulk}=400 V; $R_{G,\ external}$ = (T1) 3.3 Ω, (T2) 10 Ω)* shows the reverse recovery characteristic of the monolithic integrated body diode of the JFET. The reverse recovery charge is load current independent. To avoid any additional losses during hard commutation of the body diode, it is recommended to couple the gate of the switch (acting as diode) with a very low external gate resistor to the gate driver.

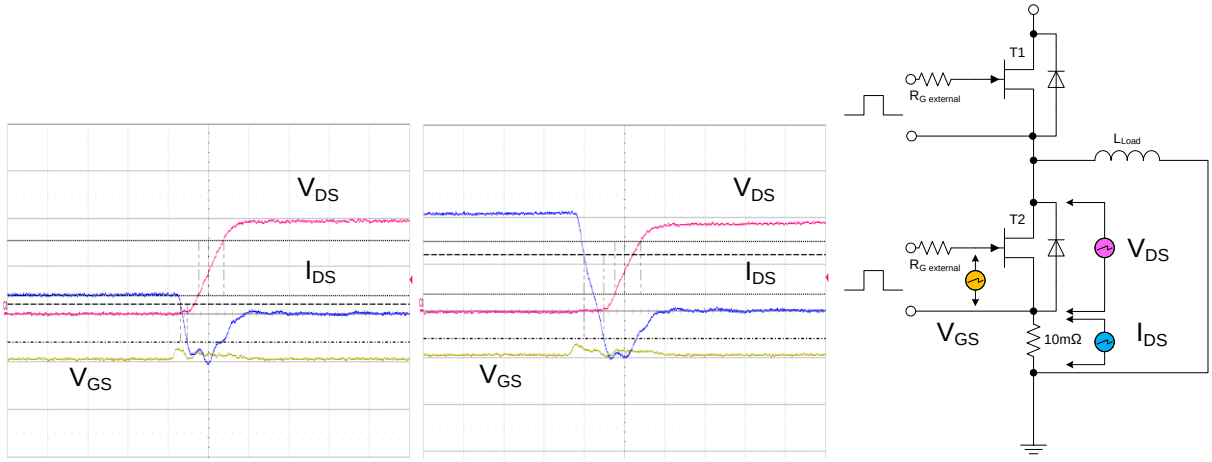


Figure 5:

reverse recovery characteristic I_{SD}= 2 A left and I_{SD}= 10 A; T_j= 150 °C; V_{bulk}=400 V; $R_{G,\ external}$ = (T1) 3.3 Ω (T2) 10 Ω

Due to the material properties of SiC the forward voltage drop V_f of the internal body diode is significantly higher compared to a SiC schottky barrier diode. Therefore, active turn-on of the channel of the JFET during reverse operation (synchronous rectification) is the preferred way of operation.

1.3.4 Short circuit ruggedness

Due to excellent material properties and a very high temperature level for intrinsic carrier generation the device shows extremely good short circuit ruggedness.

1.3.5 Switching and conduction losses

The switching energies are typically one order of magnitude lower than the losses of IGBTs. It is noteworthy to consider that the JFET, as pure majority carrier device, has no forward knee voltage and can be used on its ohmic characteristic both in forward and reverse direction.

Nevertheless, the JFET shows a strong dependency of the switching energies as function of the used gate resistor. A low resistive value of the gate resistor is recommended to operate the JFET at optimal conditions. The conduction losses in comparison to Super Junction MOSFET's are less temperature dependent. A factor of only 1.6 between 25 °C and 100 °C is measurable.

1.4 Environmental Conditions

The parts are proofed according to IEC 60721-3-4 (4K4H). (Low air temperature -20 °C; High air temperature +55 °C; Low relative humitidy 4 %; High relative humitidy 100 %; Low absolute humitidy 0.9 g/ m³; High absolute humitidy 36 g/ m³…)

2 Maximum ratings

Table 3 Maximum ratings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Continuous current, drain source [1]	I_{DS}	–	–	26	A	V_{GS} = 0 V; T_C = 25 °C; R_{thJC} = $R_{thJC, max}$
		–	–	18 [5]		V_{GS} = 0 V; T_C = 100 °C; R_{thJC} = $R_{thJC, max}$
		–	–	10 [5]		V_{GS} = 0 V; T_C = 150 °C; R_{thJC} = $R_{thJC, max}$
Pulsed current, drain source [1]	$I_{DS, pulse}$	–	–	78		V_{GS} = 0 V; T_C = 25 °C; R_{thJC} = $R_{thJC, max}$
		–	–	68 [5]		V_{GS} = 0 V; T_C = 100 °C; R_{thJC} = $R_{thJC, max}$
		–	–	60 [5]		V_{GS} = 0 V; T_C = 150 °C; R_{thJC} = $R_{thJC, max}$
Gate source voltage [2]	V_{GS}	-19.5	–	2	V	
Power dissipation	P_{tot}	–	–	190	W	T_C = 25 °C
dV/ dt ruggedness, drain source	dV_{DS}/dt	–	–	80	V/ ns	$I_{DS} \le I_{DS, pulse}$
Pulsed current, source drain [1]	$I_{SD, pulsed}$	–	–	78	A	V_{GS} = -19.5 V; T_j = 25 °C; R_{thJC} = $R_{thJC, max}$
		–	–	60 [5]		V_{GS} = -19.5 V; T_j = 150 °C; R_{thJC} = $R_{thJC, max}$
dV/ dt ruggedness, source drain	dV_{SD}/dt	–	–	80	V/ ns	$I_{SD} \le I_{DS, pulse}$
Gate loop resistance, turn off [3]	$R_{G, off}$	–	–	5.1	Ω	
Operating and storage temp. [4]	T_j;T_{stg}	-55	–	175	°C	
Mounting torque		–	–	60	Ncm	M 2.5 screws

1) Limited by $T_{j, max}$

2) The device is proofed against V_{GS} peaks. That allows to drive the parts shortly outside of the given maximum ratings ($V_{GS, max}$= 20 V, $V_{GS, min}$= -50 V @ $t_{p, max}$= 20 ns). This will result in a temporary gate leakage peak only.

3) See application information

4) Prolonged storage at high temperatures reduces the lifetime of the product. Tested according to EIA/JESD22-A103D

5) Limits derived from product characterization, parameter not measured during production

3 Thermal characteristics

Table 4 Thermal characteristics TO-247-3

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	–	–	0.78	K/W	
Thermal resistance, junction-ambient	R_{thJA}	–	–	62		leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	–	–	260	°C	1.6 mm (0.063 in.) from case for 10 s

4 Electrical characteristics

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Breakdown voltage, drain source	$V_{(BR)DSS}$	1200	–	–	V	V_{GS}= -19.5 V; I_{DS}= 1 mA; T_C= -50 °C
Gate threshold voltage [2]	$V_{GS(th)}$	-13.1 bin1	–	-12.0 bin1		I_{DS}= 10 µA; V_{DS}= 40 V; T_j= 25 °C
		-14.1 bin2	–	-12.9 bin2		
		-15.0 bin3	–	-13.9 bin3		
		-13.5 bin1	–	-12.3 bin1		I_{DS}= 10 µA; V_{DS}= 40V; T_j= 100 °C; [1]
		-14.5 bin2	–	-13.2 bin2		
		-15.4 bin3	–	-14.2 bin3		
		-13.8 bin1	–	-12.4 bin1		I_{DS}= 10 µA; V_{DS}= 40 V; T_j= 150 °C; [1]
		-14.8 bin2	–	-13.3 bin2		
		-15.7 bin3	–	-14.3 bin3		
Drain- source leakage current	I_{DSS}	–	1.5	30	µA	V_{DS}= 1200 V; V_{GS}= -19.5 V; T_C= 25 °C
		–	3	60 [1]		V_{DS}= 1200 V; V_{GS}= -19.5 V; T_C= 100 °C
		–	6	120 [1]		V_{DS}= 1200 V; V_{GS}= -19.5 V; T_j= 150 °C
Gate- source leakage current	I_{GSS}	–	–	90		V_{DS}= 0 V; V_{GS}=-19.5 V; T_C= 25 °C
		–	–	360 [1]		V_{DS}= 0 V; V_{GS}= -19.5 V; T_C= 100 °C
		–	–	720 [1]		V_{DS}= 0 V; V_{GS}= -19.5 V; T_C= 150 °C
Drain- source on- state resistance	$R_{DS(on)}$	–	0.080	0.100	Ω	V_{GS}= 0 V; I_D=9 A; T_C= 25 °C
		–	0.130	–		V_{GS}= 0 V; I_D=9 A; T_C= 100 °C
		–	0.175	–		V_{GS}= 0 V; I_D=9 A; T_C= 150 °C
Gate resistance	R_G	–	1.4	–		f= 1 MHz, open drain; T_C = 25 °C

1) Limits derived from product characterization, parameter not measured during production
2) For paralleling see application note

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	–	1550	–	pF	V_{GS}= -19.5 V; V_{DS}= 0 V; f= 1 MHz
		–	1200	–		V_{GS}= -19.5 V; V_{DS}= 800 V; f= 1 MHz
Output capacitance	C_{oss}	–	1070	–		V_{GS}= -19.5 V; V_{DS}= 0 V; f= 1 MHz
		–	80	–		V_{GS}= -19.5 V; V_{DS}= 800 V; f= 1 MHz
Effective output capacitance, energy related[1)]	$C_{o(er)}$	–	89	–		V_{GS}= -19.5 V; V_{DS}= 0 V/ 800 V; T_C=25 °C
Effective output capacitance, time related[2)]	$C_{o(tr)}$	–	112	–		V_{GS}= -19.5 V; V_{DS}= 0 V/ 800 V; T_C=25 °C
Turn- on delay time	$t_{d(on)}$	–	49	–	ns	V_{DS}= 800 V; V_{GS}= -19.5 V/ 0 V; I_D= 20 A; T_C= 25 °C; $R_{G,tot}$= 2 Ω
Turn- off delay time	$t_{d(off)}$	–	30	–		
Rise time	t_r	–	26	–		
Fall time	t_f	–	19	–		

1) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 V to 800 V

2) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to 800 V

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge, gate to source	Q_{GS}	–	16	–	nC	V_{DS}= 800 V to 0 V; I_{DS}= 18 A; V_{GS}= -19.5 V to 0 V
Gate charge, gate to drain	Q_{GD}	–	32	–		
Gate charge, total	Q_G	–	72	–		
Gate plateau voltage	$V_{plateau}$	–	-8	–	V	

Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	–	7.2	–	V	I_{SD} = 18 A; V_{GS}= -19.5 V; T_C = 25 °C
		–	7.5	–		I_{SD} = 18 A; V_{GS}= -19.5 V; T_C = 100 °C
		–	7.6	–		I_{SD} = 18 A; V_{GS}= -19.5 V; T_C = 150 °C
Reverse recovery time	t_{rr}	–	15.6	–	ns	I_{SD} = 18 A; V_{DS} = 800 V; R_G= 0 Ω; T_j = 25 °C
Reverse recovery charge	Q_{rr}	–	118	–	nC	
Peak reverse recovery current	I_{rrm}	–	11	–	A	
Current slope forward	dI_F/dt	–	3	–	A/ns	
Current slope reverse	dI_{rr}/dt	–	1.3	–		

5 Electrical characteristics diagrams

Table 9

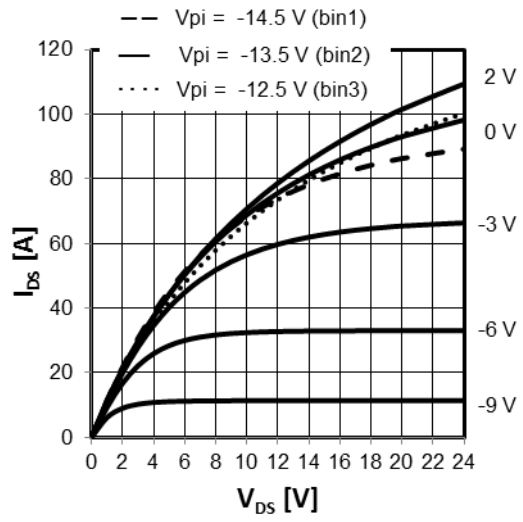
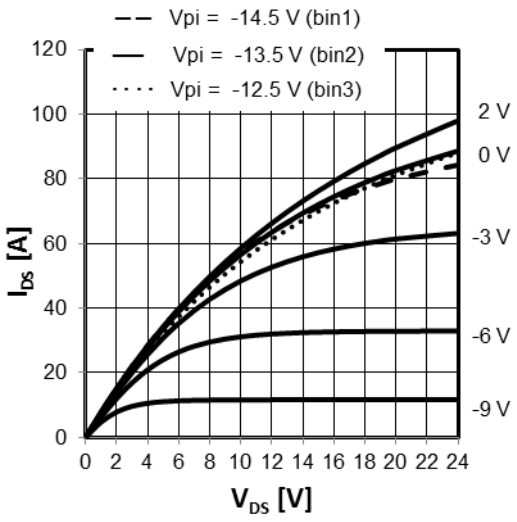
Typical output characteristic	Typical output characteristic
	
$I_{DS}= f(V_{DS})$; $T_j= 25$ °C; parameter: V_{GS}; $V_{pi\ 25\ °C}$	$I_{DS}= f(V_{DS})$; $T_j= 100$ °C; parameter: V_{GS}; $V_{pi\ 25\ °C}$

Table 10

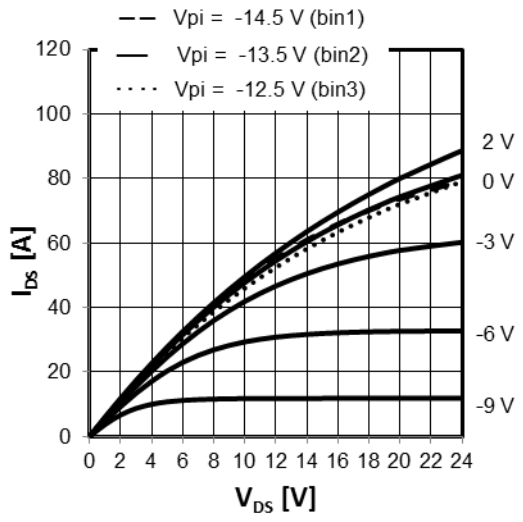
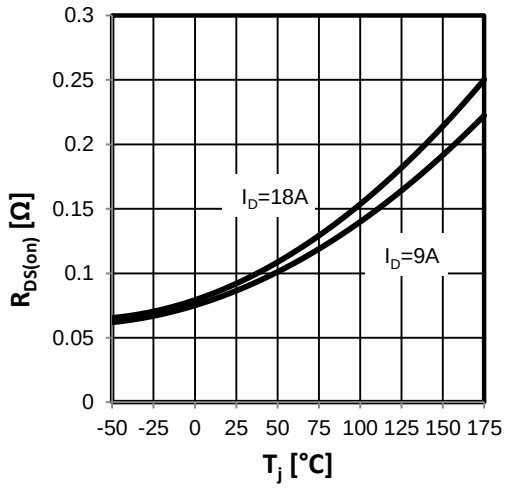
Typical output characteristic	Typical drain- source on- state resistance
	
$I_{DS}= f(V_{DS})$; $T_j= 150$ °C; parameter: V_{GS}; $V_{pi\ 25\ °C}$	$R_{DS(on)}= f(T_j)$; $V_{GS}= 0$ V; $T_j= 25$ °C; parameter: I_{DS}

Table 11

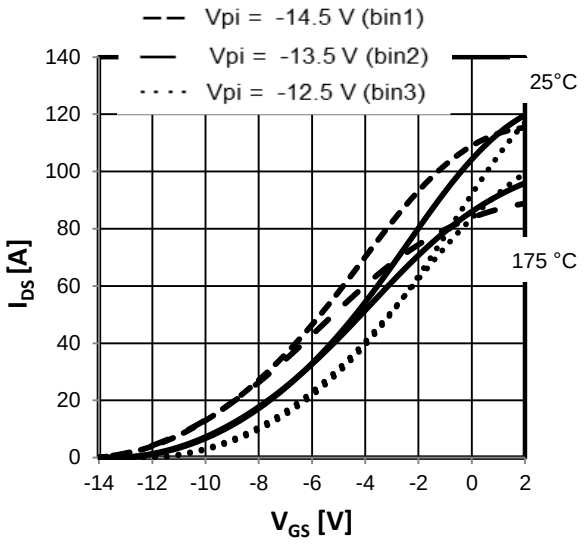
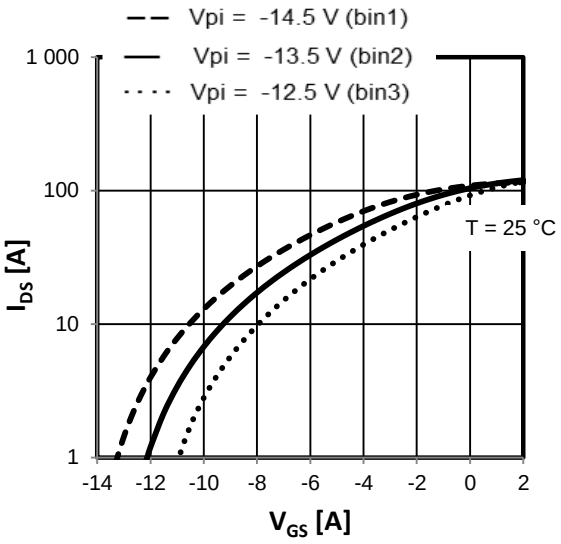
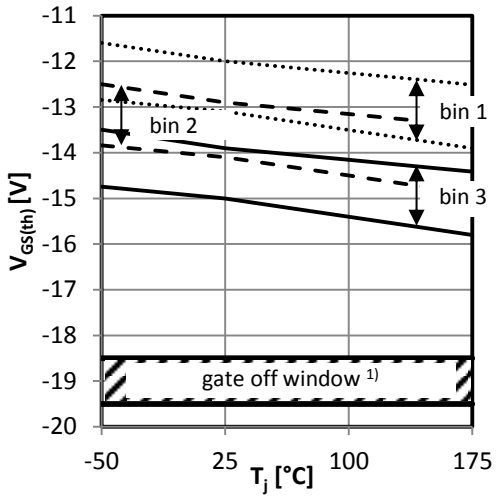
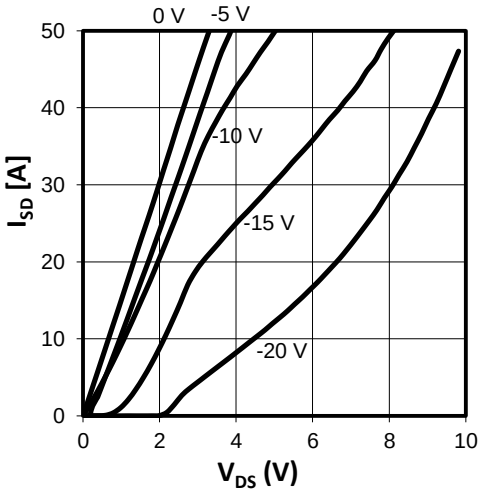
Typical transfer characteristic- linear scale	Typical transfer characteristic- logarithmic scale
	
I_{DS}= ƒ(V_{GS}); V_{DS}= 30 V; parameter: T_j; $V_{pi\ 25\ °C}$	I_{DS}= ƒ(V_{GS}); V_{DS}= 30 V; parameter: T_j; $V_{pi\ 25\ °C}$

Table 12

Gate voltage window	Body diode characteristics
	
$V_{GS(th)}$ = ƒ(T_j), V_{DS}=40 V; parameter: I_{DSS}=10 µA	I_{SD}= ƒ(V_{DS}); T_j= 25 °C parameter: V_{GS}

1) lower gate voltage leads to increased leakage current

Table 13

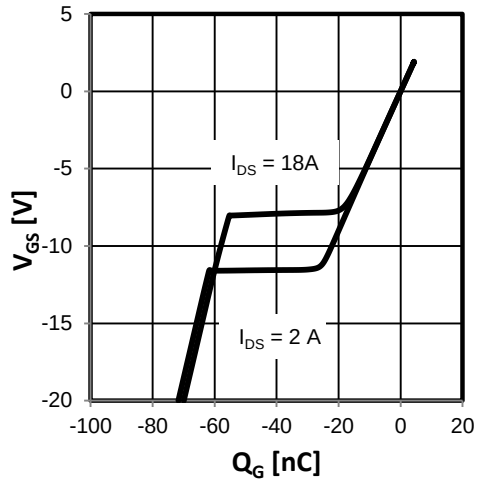
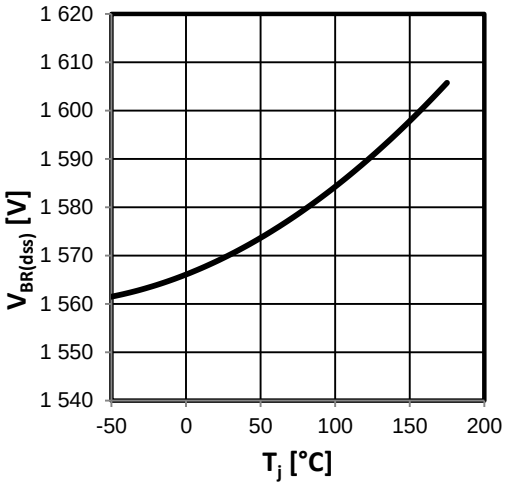
Typical gate charge	Typical breakdown voltage
	
V_{GS}= ƒ(Q_G); V_{DS}= 800 V; parameter: I_{DS}	*$V_{BR(dss)}$= ƒ(T_j); I_{DS}= 1 mA*

Table 14

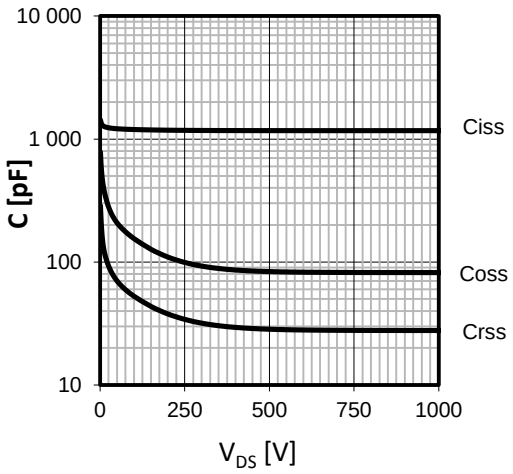
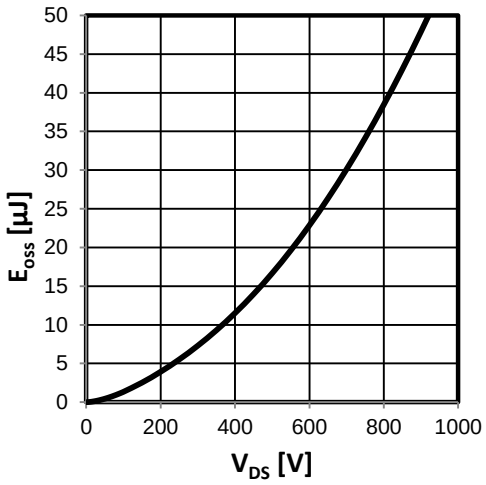
Typical capacitances	Typical stored energy in C_{oss}
	
C_{iss}= ƒ(V_{DS}); V_{GS}= -19.5 V; f= 1 MHz *C_{oss}= ƒ(V_{DS}); V_{GS}= -19.5 V; f= 1 MHz* *C_{rss}= ƒ(V_{DS}); V_{GS}= -19.5 V; f= 1 MHz*	*E_{oss}= ƒ(V_{DS})*

Table 15

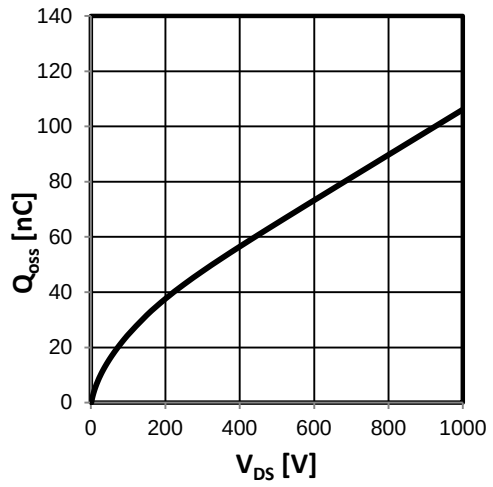
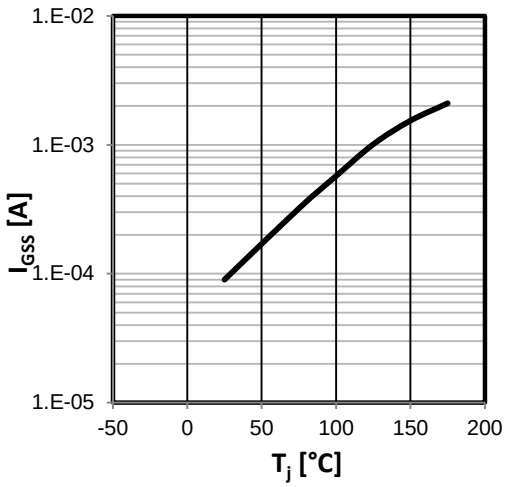
Typical stored charge in C_{oss}	Maximum gate leakage current I_{GSS}
	
$Q_{oss} = f(V_{DS})$	$I_{Gss} = f(T_j)$; parameter V_{GS} = -19.5 V

Table 16

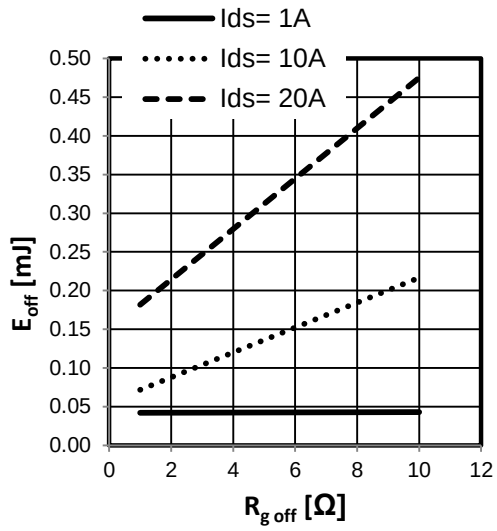
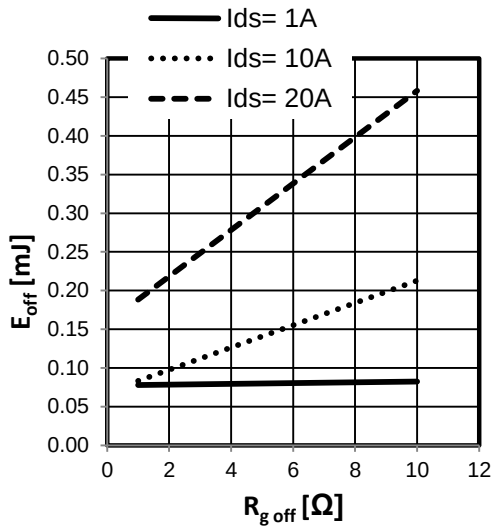
Typical switching losses- JFET vs. IDH15S120	Typical switching losses- JFET vs. JFET
	
$E_{off} = f(R_G)$; V_{bulk} = 800 V; T_j = 25 °C; V_{pi} = -13.5 V; parameter: I_{DS}	$E_{off} = f(R_G)$; V_{bulk} = 800 V; T_j = 25 °C; V_{pi} = -13.5 V; parameter: I_{DS}

Table 17

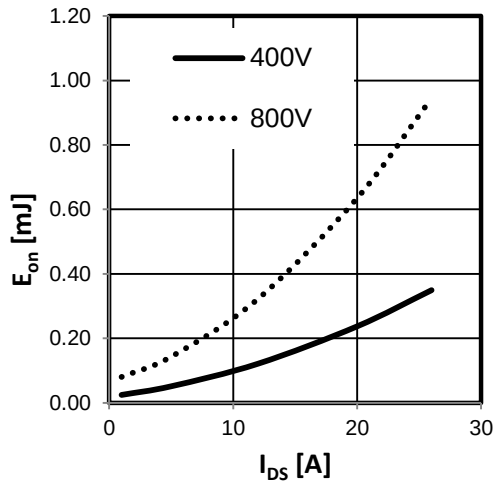
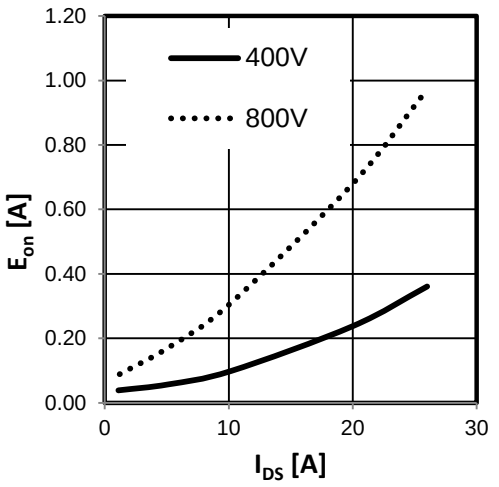
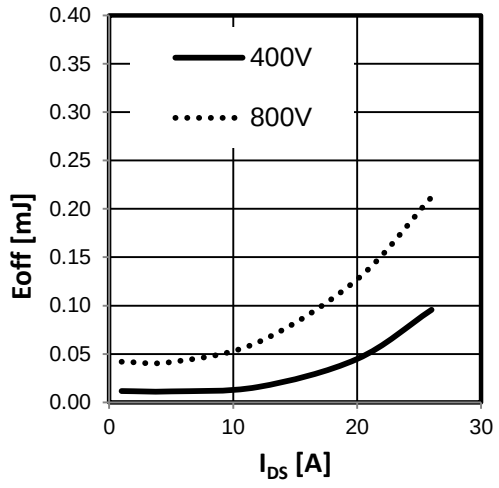
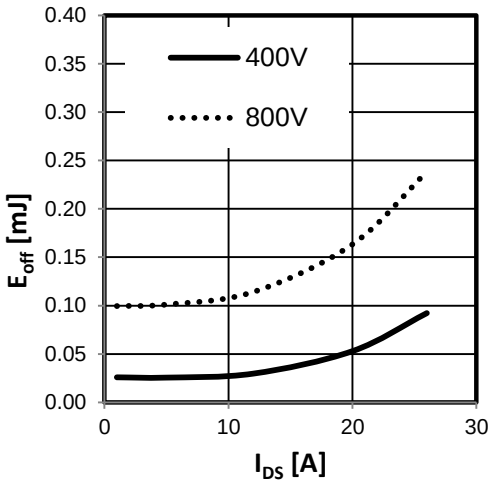
Typical switching losses- JFET vs. IDH15S120 [1]	Typical switching losses- JFET vs. JFET[1]
	
E_{on}= ƒ(I_{DS}); V_{bulk}= 800 V; T_j = 25 °C; $R_{G\,on}$= 3.3 Ω; V_{pi} = -13.5 V; parameter: V_{bulk}	*E_{on}= ƒ(I_{DS}); V_{bulk}= 800 V; T_j = 25 °C; $R_{G\,on}$= 3.3 Ω; V_{pi} = -13.5 V; parameter: V_{bulk}*

Table 18

Typical switching losses- JFET vs. IDH15S120 [1]	Typical switching losses- JFET vs. JFET [1]
	
E_{off}= ƒ(I_{DS}); V_{bulk}= 800 V; T_j = 25 °C; $R_{G\,off}$= 3.3 Ω; V_{pi} = -13.5 V; parameter: V_{bulk}	*E_{off}= ƒ(I_{DS}); V_{bulk}= 800 V; T_j = 25 °C; $R_{G\,off}$= 3.3 Ω; V_{pi} = -13.5 V; parameter: V_{bulk}*

1) Measured with Push Pull stage close to the gate; Rg =0 Ω

Table 19

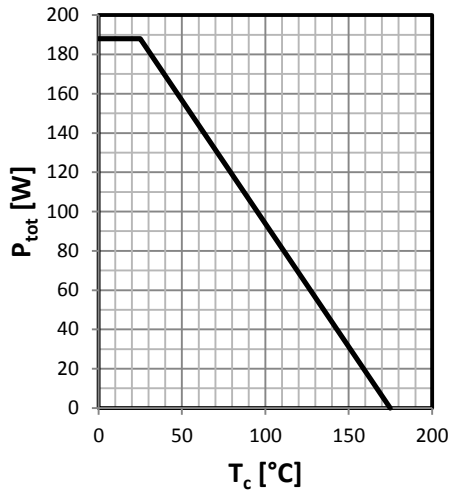
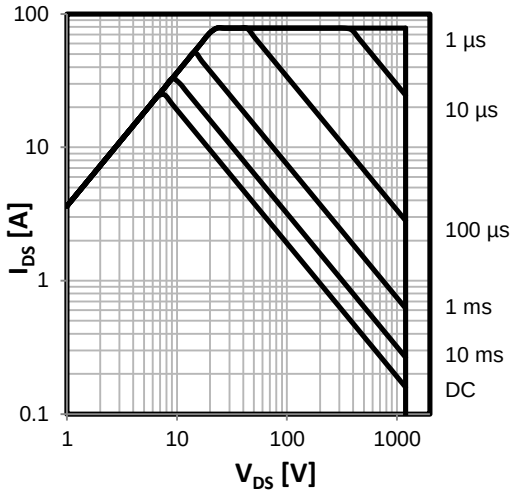
Power dissipation	Safe operating area
	
$P_{tot}= f(T_C)$	$I_{DS}= f(V_{DS})$; $T_c= 25$ °C; D= 0 parameter: t_p

Table 20

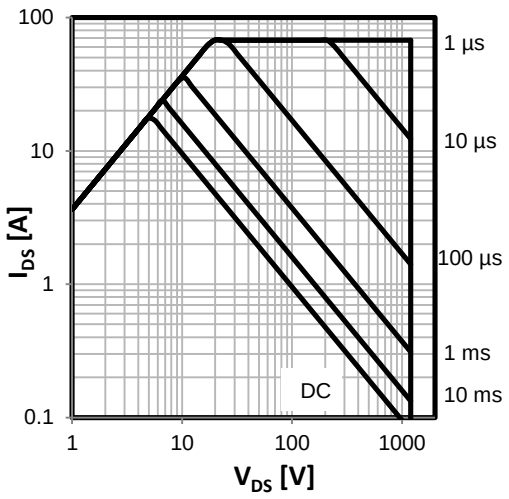
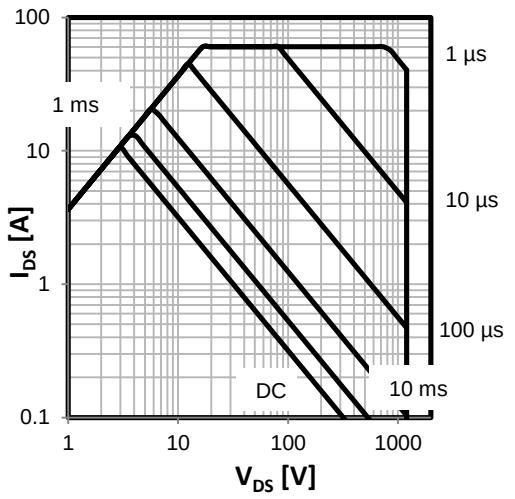
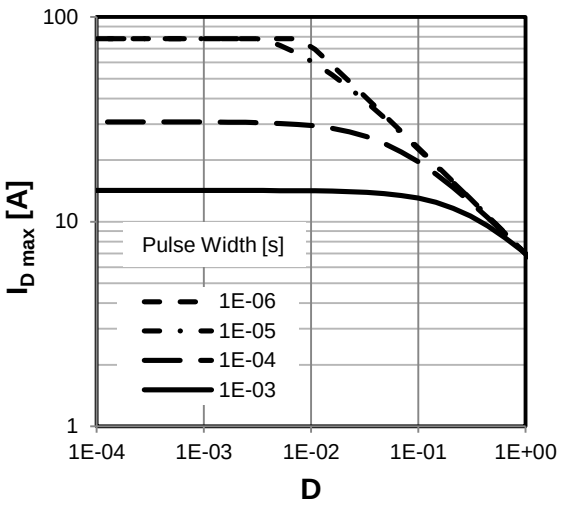
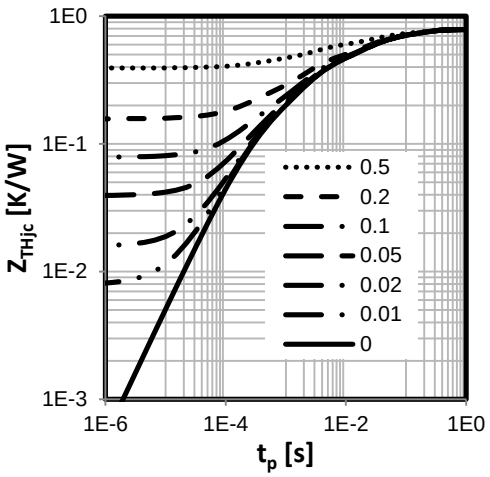
Safe operating area	Safe operating area
	
$I_{DS}= f(V_{DS})$; $T_c= 100$ °C; D= 0 parameter: t_p	$I_{DS}= f(V_{DS})$; $T_c= 150$ °C; D= 0 parameter: t_p

Table 21

Safe operating area diode	Maximum transient thermal impedance
	
$I_{SD\,max}$= ƒ(D= t_p/ T); T_c= 25 °C; parameter: t_p	*Z_{THjc}= ƒ(t_p); parameter: D= t_p/ T*

6 Test circuits

Table 22

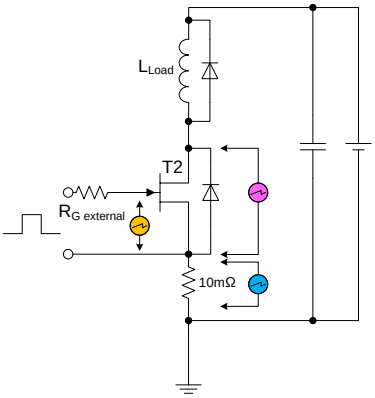
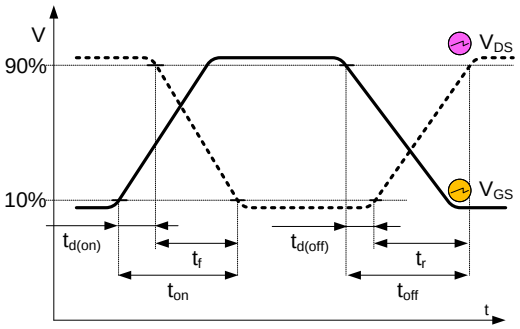
Switching times test circuit for inductive load	Switching time waveform
	

Table 23

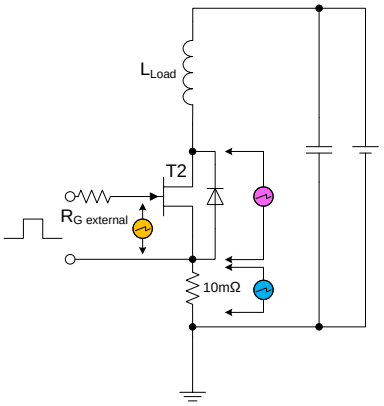
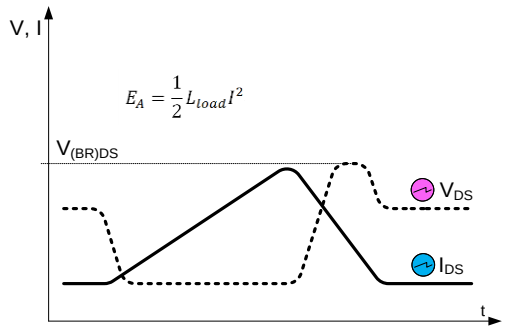
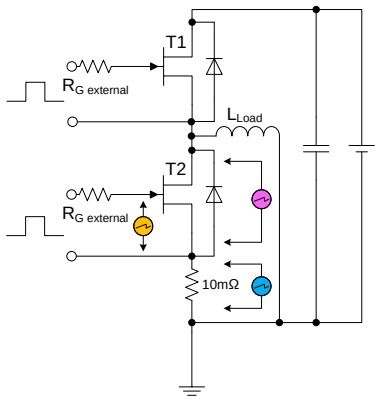
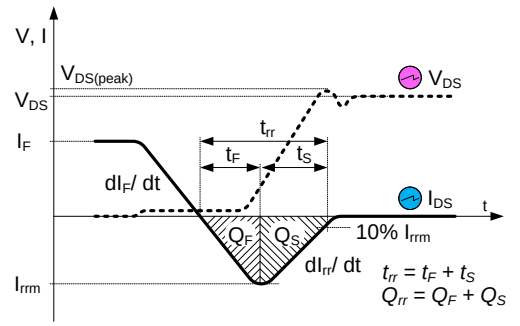
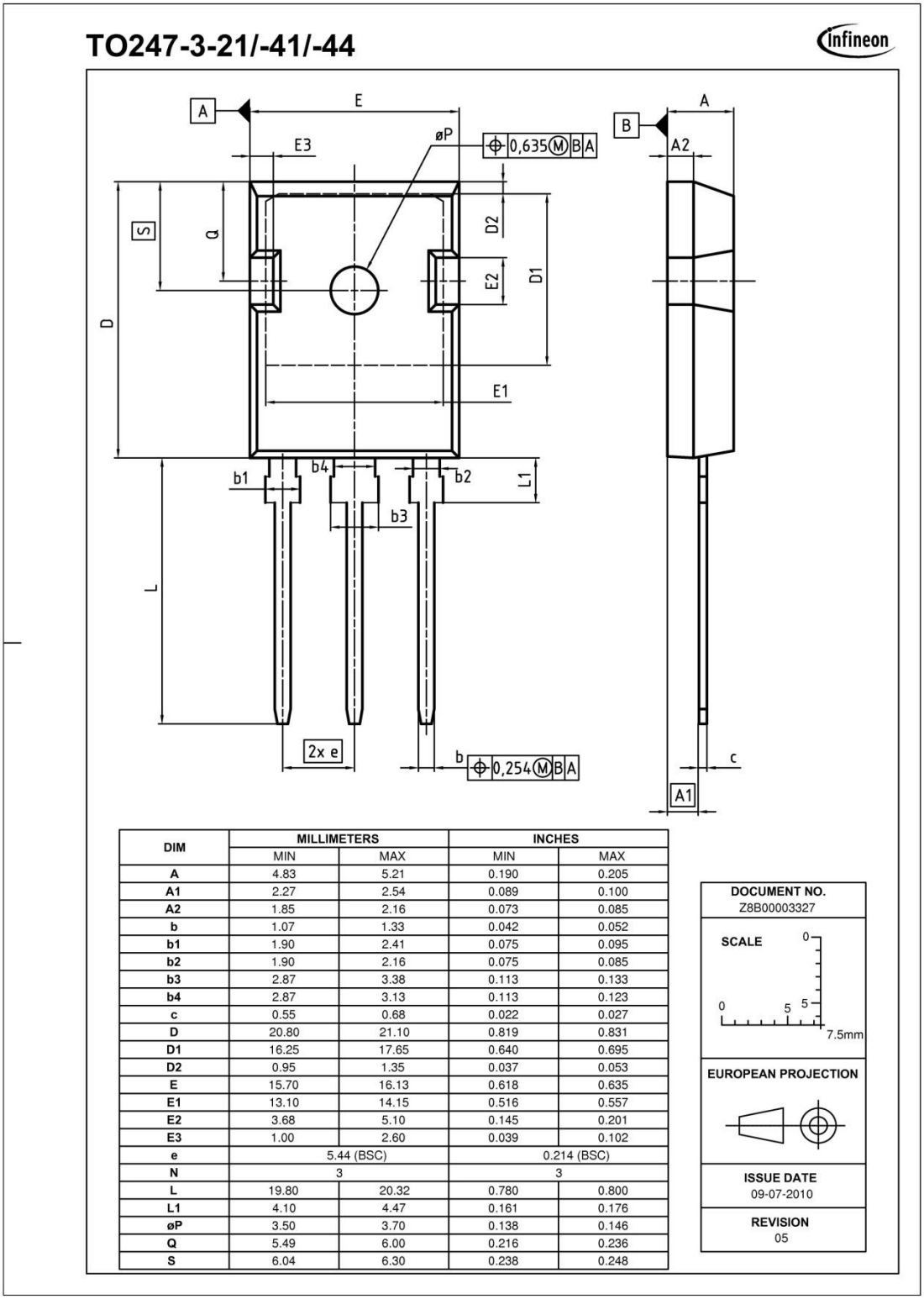
Unclamped inductive load test circuit	Unclamped inductive waveform
	

Table 24

Test circuit for diode characteristics	Diode recovery waveform
	

7 Package outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.83	5.21	0.190	0.205
A1	2.27	2.54	0.089	0.100
A2	1.85	2.16	0.073	0.085
b	1.07	1.33	0.042	0.052
b1	1.90	2.41	0.075	0.095
b2	1.90	2.16	0.075	0.085
b3	2.87	3.38	0.113	0.133
b4	2.87	3.13	0.113	0.123
c	0.55	0.68	0.022	0.027
D	20.80	21.10	0.819	0.831
D1	16.25	17.65	0.640	0.695
D2	0.95	1.35	0.037	0.053
E	15.70	16.13	0.618	0.635
E1	13.10	14.15	0.516	0.557
E2	3.68	5.10	0.145	0.201
E3	1.00	2.60	0.039	0.102
e	5.44 (BSC)		0.214 (BSC)	
N	3		3	
L	19.80	20.32	0.780	0.800
L1	4.10	4.47	0.161	0.176
øP	3.50	3.70	0.138	0.146
Q	5.49	6.00	0.216	0.236
S	6.04	6.30	0.238	0.248

DOCUMENT NO.
Z8B00003327

SCALE
0 5 5 7.5mm

EUROPEAN PROJECTION

ISSUE DATE
09-07-2010

REVISION
05

Figure 1 Outlines PG-TO247-3, dimensions in mm/inches

8 Revision History

IJW120R100T1, 1200 V CoolSiC™ Power Transistor

Revision History: Rev. 2.0, <2013-09-11>

Previous Revision:

Revision	Subjects (major changes since last version)
0.9	Target datasheet
1.0	Preliminary Datasheet
2.0	Final Datasheet

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