



# XDP<sup>™</sup> XDP700-002 evaluation PCBA user guide

## About this document

#### Scope and purpose

This document describes how to set up the XDP<sup>™</sup> XDP700-002 Evaluation Board and configure the internal registers to evaluate the performance of the XDP700-002 hot-swap controller for negative rail.

#### **Intended audience**

This document is intended for test engineers who want to evaluate the performance of the XDP700-002 hot-swap controller.



**Important notice** 

## **Important notice**

"Evaluation Boards and Reference Boards" shall mean products embedded on a printed circuit board (PCB) for demonstration and/or evaluation purposes, which include, without limitation, demonstration, reference and evaluation boards, kits and design (collectively referred to as "Reference Board").

Environmental conditions have been considered in the design of the Evaluation Boards and Reference Boards provided by Infineon Technologies. The design of the Evaluation Boards and Reference Boards has been tested by Infineon Technologies only as described in this document. The design is not qualified in terms of safety requirements, manufacturing, and operation over the entire operating temperature range or lifetime.

The Evaluation Boards and Reference Boards provided by Infineon Technologies are subject to functional testing only under typical load conditions. Evaluation Boards and Reference Boards are not subject to the same procedures as regular products regarding returned material analysis (RMA), process change notification (PCN) and product discontinuation (PD).

Evaluation Boards and Reference Boards are not commercialized products, and are solely intended for evaluation and testing purposes. In particular, they shall not be used for reliability testing or production. The Evaluation Boards and Reference Boards may therefore not comply with CE or similar standards (including but not limited to the EMC Directive 2004/EC/108 and the EMC Act) and may not fulfill other requirements of the country in which they are operated by the customer. The customer shall ensure that all Evaluation Boards and Reference Boards will be handled in a way which is compliant with the relevant requirements and standards of the country in which they are operated.

The Evaluation Boards and Reference Boards as well as the information provided in this document are addressed only to qualified and skilled technical staff, for laboratory usage, and shall be used and managed according to the terms and conditions set forth in this document and in other related documentation supplied with the respective Evaluation Board or Reference Board.

It is the responsibility of the customer's technical departments to evaluate the suitability of the Evaluation Boards and Reference Boards for the intended application, and to evaluate the completeness and correctness of the information provided in this document with respect to such application.

The customer is obliged to ensure that the use of the Evaluation Boards and Reference Boards does not cause any harm to persons or third party property.

The Evaluation Boards and Reference Boards and any information in this document is provided "as is" and Infineon Technologies disclaims any warranties, express or implied, including but not limited to warranties of non-infringement of third party rights and implied warranties of fitness for any purpose, or for merchantability.

Infineon Technologies shall not be responsible for any damages resulting from the use of the Evaluation Boards and Reference Boards and/or from any information provided in this document. The customer is obliged to defend, indemnify and hold Infineon Technologies harmless from and against any claims or damages arising out of or resulting from any use thereof.

Infineon Technologies reserves the right to modify this document and/or any information provided herein at any time without further notice.



## Safety precautions

## Safety precautions

*Note:* Please note the following warnings regarding the hazards associated with development systems.

Table 1	Safety precautions
	Warning: The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death.
	<b>Caution:</b> The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.
	<b>Caution:</b> The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing, or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.
	<b>Caution:</b> The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.



## Table of contents

## **Table of contents**

About	t this document	. 1
Impo	rtant notice	. 2
Safet	y precautions	. 3
Table	of contents	. 4
1	Introduction	. 5
2	Hardware and software requirements	. 6
3	XDP700-002 evaluation platform	. 8
3.1	Flectrical specifications	. 8
3.2	Block diagram	8
3.3	XDP700-002 Evaluation Board schematics	9
3.4	XDP700-002 Evaluation Board layout	11
3.5	XDP700-002 Evaluation Board bill of materials	14
3.6	XDP700-002 Evaluation Board default settings	18
3.7	Current sensing resistor (R <sub>sns</sub> )	19
3.8	FET board	19
3.9	Different FET footprint options on the FET board	19
3.10	USB007A dongle schematics	21
4	Programming, setup, and turn-on instructions	22
4.1	XDP <sup>™</sup> Designer communication setup	23
4.1.1	Dongle connection in XDP <sup>™</sup> Designer	23
4.1.2	Detecting XDP700-002	24
4.1.3	Reading and writing registers	26
4.1.4	Programming the FET	27
4.1.5	Programming R <sub>sns</sub>	28
4.1.6	Selecting the watchdog timer	29
4.1.7	Programming the current sense range (CS_RNG) and start-up current limit (IST)	29
4.1.8	Programming VIN_UV_FAULT_LIMIT	30
4.1.9	Programming VIN_OV_FAULT_LIMIT	31
4.1.10	Programming VOUT_UV_FAULT_LIMIT	32
4.2	Programming XDP700-002 in different modes	32
4.2.1	Fully Digital Mode (FDM)	32
4.2.1.1	1 Digital Comparator Mode (DCM)	33
4.2.1.2	2 Analog Comparator Mode (ACM)	33
4.2.2	Analog Assisted Digital Mode (AADM)	34
5	Loading the configuration file	35
6	Hands-on	37
6.1	Turn ON FET test	37
6.2	Boost mode test	39
6.3	I urn-UN in output short test	40
7	Programming SOA, OTP, and MTP	41
1.1	Program OTP or MTP sections	41
Refer	ences	43
Revis	ion history	44
Discla	nimer	45



Introduction

## 1 Introduction

Infineon's XDP<sup>™</sup> XDP7x0-002 family of devices (XDP700-002, XDP710-002) are highly integrated wide-input voltage system monitoring and inrush current protection devices. These are digitally configurable and use a power management bus (PMBus) communication interface to access their register map to configure their features.

The USB007A series dongle is a PC-USB COM port-to-PMBus bridge dongle that allows access to XDP700-002 registers from the software configurator.

This document describes how to set up the evaluation board and configure the internal registers to evaluate the performance of XDP700-002 in limiting the inrush current during startup by using regulation on the programmed FET safe operating area (SOA). This document also highlights the fault detection control.



#### Hardware and software requirements

## 2 Hardware and software requirements

The following hardware and software are required for the setup:

- XDP700-002 Evaluation Board
   Order code: EVAL\_XDP700
- XDP<sup>™</sup> Designer USB dongle USB007 or higher
   Order code: USB007A1
- XDP<sup>™</sup> Designer GUI
  - Download from Infineon Development Center



Figure 1 XDP700-002 Evaluation Board



Figure 2 USB007A1 dongle



#### Hardware and software requirements





**XDP<sup>™</sup> Designer** 



## 3 XDP700-002 evaluation platform

The following sections describe the XDP700-002 Evaluation Board highlighting the electrical specifications, block diagram, schematics, layout, bill of materials (BOM), and different configuration settings that could be used on this evaluation board.

## **3.1 Electrical specifications**

- Input and output voltage range: -12 V DC to -80 V DC
- Input current range: Up to 40 A
- Note:

The input current range depends on the number of paralleled MOSFET adapter boards. The MOSFET adapter boards can be removed and added to the evaluation board based on the required current level. The board can handle up to 75 A of current with three MOSFET adapter boards without the need of forced air cooling.

## 3.2 Block diagram

The XDP700-002 evaluation platform consists of the following:

- **XDP700-002 Evaluation Board**: Negative input hot-swap controller and eFuse circuitry designed to run a single-channel controller including its corresponding FET. Additionally, communication, control, and protection circuitry are included.
- **USB007A1 dongle**: Acts as the interface between the PC and XDP700-002. XDP<sup>™</sup> Designer uses PMBus communication to send commands to XDP700-002. The USB007A1 dongle translates these commands from USB to PMBus, enabling XDP700-002.
- **XDP<sup>™</sup> Designer**: Configuration and general control software tool for XDP700-002 PMBus communication.



Figure 4 XDP700-002 evaluation platform







Figure 5

Main IC and bias



Figure 6 Communication and isolation

















## 3.4 XDP700-002 Evaluation Board layout



Figure 10 Top layer layout of main PCB





Figure 11 Mid 1 layer layout of main PCB



Figure 12 Mid 2 layer layout of main PCB





Figure 13 Bottom layer layout of main PCB



Figure 14 Top, Mid 1, Mid 2, and bottom layer layouts of MOSFET PCB



## 3.5 XDP700-002 Evaluation Board bill of materials

Table 2Bill of materials (BOM) for the main PCBA

ltem	Qty	Reference designator	Value	Footprint	Manufacturer	Part number			
1	1	BRD1	PC Board (FAB)	-	-	P100156 D			
2	7	C1, C2, C3, C4, C9, C21, C22	0.1 uF	C0603	AVX	06031C104K4 Z2A			
3	2	C5, C11	1 uF	C0805	ТDК	C2012X7R1H1 05K125AB			
4	3	C6, C12, C23	1 uF	C0603	ТDК	C1608X7R1E1 05K080AB			
5	1	C10	1000 pF	C0603	ТДК	C1608C0G2A1 02J080AA			
6	2	C13, C14	0.1 uF	C1206	ТДК	C3216C0G2A1 04J160AE			
7	2	C15, C19	10 uF	C0805	Samsung	CL21B106KO QNNNE			
8	1	C16	1000 pF	C0805	ТДК	C2012C0G2A1 02J060AA			
9	1	C17	0.047 uF	C0603	ТДК	C1608X7R1H4 73K080AA			
10	2	C18, C20	0.022 uF C0603		TDK	C1608X7R1H2 23K080AA			
11	2	C24, C25	100 uF	Cap12p5x25m m	Panasonic	EEU-EE2C101			
12	1	D1	Yellowish Green	LED-SMD- SMLP13BC8T	ROHM Semiconductors	SML- P11MTT86R			
13	2	D2, D7	Red	LED-SMD- SMLP13BC8T	ROHM Semiconductors	SML- P11UTT86R			
14	1	D3	Orange	LED-SMD- SMLP13BC8T	ROHM Semiconductors	SML- P11DTT86R			
15	1	D4	B3100-13-F	DIOM7959X250 N	Diodes Incorporated	B3100-13-F			
16	1	D5	5.0SMDJ64A	DIOM7959X262 N	Bourns	5.0SMDJ64A			
17	1	D6	STPS5L60SFY	V10PL45-M3	STMicroelectron ics	STPS5L60SFY			
18	3	D8, D9,D11	.5A	SOD523	NXP	BAS516,135			
19	1	D10	.2A	SOD323	On	BAS20HT1G			
20	4	J1, J2, J3, J4	PEM NUT 8-32	Screw and nut for JACK1	Penn Eng	P-KF2-832-ET			
21	2	J5,J6	7466105R	CON-MOSFET	Würth Elektronik	7466105R			



ltem	Qty	Reference designator	Value	Footprint	Manufacturer	Part number		
22	3	Q1, Q2, Q3	BSR315P	SOT23	Infineon Technologies	BSR315P		
23	1	Q4	2N7002E	sot23	On	2N7002ET1G		
24	1	Q5	MMBT3904	Sot23	Nexperia	MMBT3904,2 15		
25	1	Q7	IPB017N10N5	PG-TO263-7	Infineon Technologies	IPB017N10N5 ATMA1		
26	4	R1, R2, R5, R6	1.5K	R0603	Panasonic	ERJ- 3EKF1501V		
27	4	R3, R4, R9, R10	1	R0603	Panasonic	ERJ- 3GEYJ1ROV		
28	12	R7, R8, R11, R12, R13, R16, R19, R20, R30, R31, R33, R48	4.7k	R0603	Yageo	RC0603FR- 074K7L		
29	4	R14, R17, R21, R23	12k	R0603	Vishay	CRCW060312 KOFKEAC		
30	6	R15, R18, R22, R24, R52, R53	20К	R0603	Panasonic	ERJ- 3EKF2002V		
31	1	R25	4.53K	R0603	Panasonic	ERJ- 3EKF4531V		
32	1	R26	7.5K	R0603	Panasonic	ERJ- 3EKF7501V		
33	1	R27	11K	R0603	Panasonic	ERJ- 3EKF1102V		
34	1	R28	15K	R0603	Panasonic	ERJ- 3EKF1502V		
35	1	R29	19.6k	R0603	Vishay	CRCW060319 K6FKEA		
36	1	R32	24.9k	R0603	Vishay	CRCW060324 K9FKEA		
37	1	R34	147k	R0805	Vishay	CRCW080514 7KFKEA		
38	1	R36	1.96K	R0603	Panasonic	ERJ- 3EKF1961V		
39	7	R37, R41, R43, R44, R46, R49, R57	0	R0603	Panasonic	ERJ- 3GEY0R00V		
40	1	R38	2.7k	R0805	Vishay	CRCW08052K 70FKEA		
41	1	R39	100	R1206	Panasonic	ERJ- 8ENF1000V		
42	1	R50	124k	R0603	Vishay	CRCW060312 4KFKEA		
43	1	R51	221K	R0603	Panasonic	ERJ- 3EKF2213V		



Item	Qty	ty Reference designator Value		Footprint	Manufacturer	Part number		
44	1	R54	8.87k	R0603	Vishay	CRCW06038K 87FKEA		
45	1	R55	14k	R0603	Panasonic	ERJ- 3EFK1402V		
46	1	R56	2.74K	R0603	Panasonic	ERJ- 3EKF2741V		
47	2	R58, R59	20	R1206	Panasonic	ERJ- 8GEYJ200V		
48	1	R60	1	R0805	Panasonic	ERJ- 6RQF1R0V		
49	1	Rsns1	1mR	5930	Bourns	CSS2H- 5930K-1L00F		
50	1	Rsns2	1mR	3920	Bourns	Not Used		
51	1	Rsns3	0.5uR	2512	Bourns	Not Used		
52	1	T1	220uH	LPD5030V	Coilcraft	LPD5030V- 224MRC		
53	1	U1	ISO1641B	SO8	ТІ	ISO1641BDR		
54	1	U2	2DIB1410F	SO8	Infineon	2DIB1410FXU MA1		
55	1	U3	LM5018SD/NO PB	WSON-8	Texas Instruments	LM5018SD/N OPB		
56	2	U4, U5	3.3 V	SOT23-5	STMicroelectron ics	LDK320AM33 R		
57	1	U7	XDP700-002	IFX-PG-VQFN- 29-1	Infineon Technologies	XDP700-002		
58	1	X1	CON4-H	CON2_HZ_BCS- 102-X-S-HE	Samtec	BCS-102-F-S- HE		
59	8	X2, X5, X7, X12, X33, X41, X48, X49	CON2	CON-M-THT- M20-9770246_2	Harwin	M20-9770246		
60	1	X6	CON4	CONN4PIN100	Würth Elektronik	61300411121		
61	29	X9, X16, X17, X19, X20, X22, X23, X24, X25, X26, X27, X28, X29, X30, X31, X32, X34, X35, X36, X37, X38, X39, X40, X42, X43, X44, X45, X46, X47	TP SMD	CON-SMD-TP- 5015	Keystone Electronics	5015		
62	2	X15, X18	CON12	CON-M-THT- TSW-106-07-L-D	Samtec	TSW-106-07- L-D		
63	1	X21	CON14	CON-M-THT- HTSW-107-07-L- D	Samtec	HTSW-107- 07-L-D		



Item	Qty	Reference designator	Value	Footprint	Manufacturer	Part number	
64	4	S1a, S2a, S3a, S4a	Screw PHMS 4-40 x 1/4	-	Keystone	9900	
65	4	S1, S2, S3, S4	Standoff 4- 40x1/2	mtg_hole_125	Keystone	2203	
66	2	C7, C8	N/U	C0603	ТДК	Not used	
67	2	C24a, C25a	N/U	CAP18X46mm	Nichicon	Not used	
68	1	D12	N/U	DO-219AC	Vishay	Not used	
69	1	Q6	N/U	PG-HSOF-8-1	Infineon Technologies	Not used	
70	1	Q8	N/U	PG-HSOG-8-1	Infineon Technologies	Not used	
71	1	Q9	N/U	PG-HDSOP-16	Infineon Technologies	Not used	
72	1	Q10	N/U	PG-TDSON-8_1	Infineon Technologies	Not used	
73	4	R35, R45, R47, R62	N/U	R0603	Yageo	Not used	
74	1	R61	N/U	R0805	Panasonic	Not used	

#### Table 3 BOM for MOSFET PCBA

ltem	Qty	Reference designator	Value	Footprint	Manufacturer	Part number
1	1	BRD1	PC Board (FAB)	-	-	P100173 A
2	2	J1, J2	SO-SMD-M5- FEMALE	CON-MOSFET	Würth Elektronik	7466105R
3	1	J700	CON4-H	CON2_HZ_BCS- 102-X-S-HE	Samtec	BCS-102-F-S- HE
4	1	P700	CON2	CON2_RA_TSW- 102-08-F-S-RA	Samtec	TSW-102-08- F-S-RA
5	1	Q7	IPB017N10N5	PG-TO263-7	Infineon Technologies	IPB017N10N 5ATMA1
6	1	R2	10	R0603	Panasonic	ERJ- 3EKF10R0V
7	1	C1	N/U	C0603	TDK	Not used
8	1	D1	N/U	SOD523	On	Not used
9	1	D2	N/U	SMC-diode	Littelfuse	Not used
10	1	J7	N/U	CON2_SMD_AVX- 20-9159	KYOCERA AVX	Not used
11	1	J710	N/U	CON2_HZ_BCS- 102-X-S-HE	Samtec	Not used
12	1	P7	N/U	CON2_SMD_AVX- 10-9159	KYOCERA AVX	Not used



ltem	Qty	Reference designator	Value	Footprint	Manufacturer	Part number
13	1	P710	N/U	CON2_RA_TSW- 102-08-F-S-RA	Samtec	Not used
14	1	Q6	N/U	PG-HSOF-8-1	Infineon Technologies	Not used
15	1	Q8	N/U	PG-HSOG-8-1	Infineon Technologies	Not used
16	1	Q9	N/U	PG-HDSOP-16	Infineon Technologies	Not used
17	1	Q10	N/U	PG-TDSON-8_1	Infineon Technologies	Not used
18	1	R1	N/U	R0603	Panasonic	Not used
19	1	R3	N/U	R0603	Panasonic	Not used

## 3.6 XDP700-002 Evaluation Board default settings

See the jumpers on the board as shown in Table 4.

TUDIC	Sumper settings	
Reference designator	Default configuration	Usage
X48	Open	Shorted 1 to 2: Connects UV/EN to VREG
		<b>Open</b> : UV/EN can be driven by dongle
X15	Between Pin 5 and 6 and in between Pins 11 and 12	ADDRx pins configuration to 0x10. Move the jumper to change the PMBus address.
X18	Open	MODEx pins configuration. Leave them open for fully digital mode (FDM)
X21	Open	IST pin configuration
X33	Open	Shorted: Connects UV/EN to voltage divider
		<b>Open</b> : UV/EN can be driven by Vreg or dongle
X6	Open	Shorted: Bypass isolation between UV/EN and UV/EN_MCU
X5	Open	Shorted: Bypass isolation between FAULT and FAULT_MCU
X12	Open	<b>Shorted</b> : Connects RTN_Neg and GND together and bypass isolation
X2	Open	<b>Shorted</b> : Connects GPO2 to GND (used to test CGDN application)
X49	Open	<b>Shorted</b> : Connects GPO3 to GND (used to test PMBUS Disable application)
X41	Open	Shorted: Connects OV to voltage divider
		<b>Open</b> : This header can be left open for DCM

#### Table 4 Jumper settings



Table 5	<b>Resistors and capacitors</b>	
Reference designator	Default configuration	Notes
R44	Check depending on FET	-
C7, C8	DNF	$C_{gd}$ and $C_{gs}$ of FET
R37, R41	Check depending on sense resistor	Can be populated: 10 $\Omega$
C9	Max 100 nF	R <sub>sns</sub> filter
R62	DNF	Used to modify the gain of $R_{sns}$ for accurate telemetry
C10	1 nF	Temperature sensor filter
R43	0 Ω	Populate: If EN is driven by dongle
		DNF: If EN is driven by header X48
R45	DNF	Populate: If EN is driven by header X48
		<b>DNF</b> : If EN is driven by dongle
Rin	100 Ω	Or lower depending on test slew rate requirements

## 3.7 Current sensing resistor (R<sub>sns</sub>)

The following three footprints are provided to support different resistor sizes, with the default onboard resistor of  $1 \text{ m}\Omega$ . These footprints are optimized for resistor packages:

- R<sub>sns1</sub>: 5930, 5931
- R<sub>sns2</sub>: 3920, 3921, 2818
- R<sub>sns3</sub>: 2512

## 3.8 FET board

The XDP700-002 Evaluation Board comes with an option to parallel up to three FET boards to increase the current-carrying capability for testing heavy loads. This allows the board to drive multiple parallel N-channel MOSEFTs. Necessary heatsinking is provided via a copper bus bar; forced cooling is required if operating at currents greater than 50 A.

## 3.9 Different FET footprint options on the FET board

The FET footprint supports D<sup>2</sup>PAK, TOLL, and TDSON packages in the following positions:



Figure 15 D2PAK7 position (top side)





Figure 16 TOLL position (top side)



#### Figure 17 PG-TDSON-8-1 position (top side)











## 3.10 USB007A dongle schematics







## 4 Programming, setup, and turn-on instructions

Set up the system as follows:

- 1. Connect the USB007 dongle to the XDP700-002 Evaluation Board connector X6 as shown in Figure 21.
- 2. Connect the USB007 dongle to the PC USB port.
- 3. Ensure that the jumpers are connected properly.
- 4. Connect 48 V from RTN/+ (J1 connector) to Negative/- (J2) on the left of the board.

XDP700-002 powers up as soon as RTN/+ is equal to or greater than 9 V. At this point, communication and programming is possible, but the FET will be OFF. To turn ON the FET, a minimum of 14 V is required. After turn on, at least the following registers must be programmed to turn ON the device.

- FET select
- R<sub>sns</sub>

The UV/EN signal (signal used to enable or disable the hot-swap controller) can be controlled in one of the following ways:

- Controlled by a dongle; it will hold the signal down until it is toggled manually inside the GUI as shown in Figure 40.
- Controlled by the UV/EN1 signal, which is controlled by the X48 header. It must be held LOW until the necessary registers are written.



Figure 21

XDP700-002 Evaluation Board and dongle setup

#### **XDP<sup>™</sup> Designer communication setup** 4.1

Install XDP<sup>™</sup> Designer from the Infineon Development Center.

#### Dongle connection in XDP<sup>™</sup> Designer 4.1.1

- 1. Open XDP<sup>™</sup> Designer.
- 2. Wait for a few moments and check the bottom status bar for the dongle connection. When the dongle is detected, the highlighted area shown in Figure 22 turns green and displays USB007.
- 3. Ensure that the enable signal is LOW (EN L); if not, click on it to toggle to EN L from EN H.



Figure 22 USB007A1 detection on XDP<sup>™</sup> Designer

ineon



## 4.1.2 Detecting XDP700-002

1. Click the button highlighted in Figure 23 and then wait for a few seconds to detect the device. If the device is not detected on its own, click on **Scan For Devices**, as shown in Figure 24.



#### Figure 23 XDP700-002 detection



Figure 24Scan For Devices to find XDP700-002

XDP700V002 is detected, with **Telemetry** displayed on the left as shown in Figure 25.







2. Click the **PMB** button to view PMBus registers and their stored values. See Figure 26.

Sea Sea	irch	Q				TLVF <u>G</u>	PMB	FW 🔍	GC	E CF	G 🤨	φ ·	
Active Controller	:	Search	All Fault MF	R Status	Telem Vout						Live Rea	d (On) 🗨	
DP700V0	02: 0x10	Code	Command	Lo	A doc								
🔴 Loop /	: Vout = 47.26V   lout = 0A	0.076		Hex	Value								
Telemetry	: P	0x01	OPERATION	0x80									
	• •	0x03	CLEAR_FAULTS										
Vin	47.991 V	0x19	CAPABILITY	0xD0									
lout	0 A	0x42	VOUT_OV_WARN_LIMIT	0x0FFF	88.0077 V								
Temp (Ext)	-275.4 °C	0x43	VOUT_UV_WARN_LIMIT	0x0000	0 V								
Temp (Int)	36.74 °C	0x44	VOUT_UV_FAULT_LIMIT	0x0000	0 V								
Pín	0 W	0x4A	IOUT OC WARN LIMIT	0x0FFF	53.5683 A								
		OvdE		0×0EEE	512 0962 °C								
		UA4F	OT_PAGE_EIMIT	UXUPPP	512.0502 C								
		0x51	OT_WARN_LIMIT	0x0FFF	512.0962 °C								
		0x55	VIN_OV_FAULT_LIMIT	0x0FFF	88.0077 V								
		0x57	VIN_OV_WARN_LIMIT	0x0FFF	88.0077 V								
		0x58	VIN_UV_WARN_LIMIT	0x0000	0 V								
		0x59	VIN_UV_FAULT_LIMIT	0x0000	0 V								
		0x6B	PIN_OP_WARN_LIMIT	OxFFFF	4716.0035 W								
		0x78	STATUS_BYTE	0x40	2								
		0x79	STATUS_WORD	0x0840									
		0x7A	STATUS_VOUT	0x00									
- 10 <b>- 6</b> 1	ar View Da -	0x7B	STATUS_IOUT	0x00									

Figure 26 XDP<sup>™</sup> Designer displaying PMBus registers of connected XDP700-002



## 4.1.3 Reading and writing registers

- 1. To edit a register individually, click on the corresponding PMBus register.
- 2. Make the necessary changes, and then click **Write**. See Figure 27.

Infineon - XDP <sup>™</sup> Designer (Dev	/_Build-2825)					- • ×
Infineon	ch	Q				TLVF 🏝 📃 PMB 🕼 FW 🔧 🖺 GC 🖶 CFG 🛎 🌣 📲 🚱
Active Controller	:	Search	All Fault MFF	R Status T	elem Vout	VIN_OV_FAULT_LIMIT Live Read (0n)
A (XDP700V00	2: 0x10	Code	Command	Hex	Value	Selected Loop
🔅 🔴 Loop A :	Vout = 47.28V   Iout = 0A	0x01	OPERATION	0x80		Loop A
Telemetry	: 2	0x03	CLEAR_FAULTS			Command Value (Decimal)
Vin	48.012 V	0×19	CAPABILITY	0xD0		69.9978508489
Vout	47.281 V	0x42	VOUT_OV_WARN_LIMIT	0x0F73	84.9989 V	
Temp (Ext)	-275.4 °C	0x43	VOUT_UV_WARN_LIMIT	0x0000	0 V	
Temp (Int)	37.17 °C	0x44	VOUT_UV_FAULT_LIMIT	0x06E8	37.997 V	
Pin	0 W	0x4A	IOUT_OC_WARN_LIMIT	0x0FFF	35.3566 A	
		0x4F	OT_FAULT_LIMIT	0x0FFF	512.0962 °C	
		0x51	OT_WARN_LIMIT	0x0FFF	512.0962 °C	
		0x55	VIN_OV_FAULT_LIMIT	0x0CB9	69.9979 V	Pand
		0x57	VIN_OV_WARN_LIMIT	0x0FFF	88.0077 V	
		0x58	VIN_UV_WARN_LIMIT	0x0000	0 V	Description The VIN_OV_FAULT_LIMIT command sets the value of the input voltage measured at the VDD_RTNS pin that causes an input overvoltage fault.
		0x59	VIN_UV_FAULT_LIMIT	0x0000	0 V	OV fault can be programmed from 0 to 22, 0 to 44 or 0 to 88V (absolute value) depending on VTLM RNG settings.
		0x6B	PIN_OP_WARN_LIMIT	0xFFFF	3112.7102 W	
		0x78	STATUS_BYTE	0x40		
		0x79	STATUS_WORD	0x0840		
		0x7A	STATUS_VOUT	0x00		
Foulte 🔊		0x7B	STATUS_IOUT	0x00		
USB007 v66.0 EN L	Device Checksum 0x95FD		ATITUA 010117			

Figure 27 Editing VIN\_OV\_FAULT\_LIMIT

Most of the registers are updated automatically.

#### 3. To read the latest register values, click **Read**. See Figure 28.

Infineor	n - XDP™ Designer	(Dev_Build-2825)					- ø ×
İnfir	s s	earch	Q				TLVF 🙅 📃 🎫 😰 FW 🔧 🖺 GC 🖨 CFG 🗰 🌣 📲 🚱
E	Active Controlle	er i	Search	All Fault MF	R Status T	Felem Vout	VIN_OV_FAULT_LIMIT Live Read (On) 🛑 🗙
ŧ	<b>()</b> XDP700	V002: 0x10	Code	Command	Hex	value	Selected Loop
۲	🔴 Loop	o A : Vout = 47.28V   Iout = 0A	0x01	OPERATION	0x80		Loop A
	Telemetry	: 2	0x03	CLEAR_FAULTS			Command Value (Decimal)
	Vin	48.012 V	0x19	CAPABILITY	0xD0		69.9978508489 — 🛨 V
	Vout	47.281 V	0x42	VOUT_OV_WARN_LIMIT	0x0F73	84.9989 V	
	Temp (Ext)	0 A -275.4 ℃	0x43	VOUT_UV_WARN_LIMIT	0x0000	0 V	
	Temp (Int)	37.17 °C	0x44	VOUT_UV_FAULT_LIMIT	0x06E8	37.997 V	
	Pin	0 W	0x4A	IOUT_OC_WARN_LIMIT	0x0FFF	35.3566 A	
			0x4F	OT_FAULT_LIMIT	0x0FFF	512.0962 °C	
			0x51	OT_WARN_LIMIT	0x0FFF	512.0962 °C	
			0x55	VIN_OV_FAULT_LIMIT	0x0CB9	69.9979 V	Read Write
			0x57	VIN_OV_WARN_LIMIT	0x0FFF	88.0077 V	
			0x58	VIN_UV_WARN_LIMIT	0x0000	0 V	Description The VIN_OV_FAULT_LIMIT command sets the value of the input voltage measured at the VDD_RTNS pin that causes an input overvoltage fault.
			0x59	VIN_UV_FAULT_LIMIT	0x0000	0 V	OV fault can be programmed from 0 to 22, 0 to 44 or 0 to 88V (absolute value) depending on VTLM RNG settings.
			0x6B	PIN_OP_WARN_LIMIT	0xFFFF	3112.7102 W	
			0x78	STATUS_BYTE	0x40		
			0x79	STATUS_WORD	0x0840		
			0x7A	STATUS_VOUT	0x00		
	Faulte 👩		0x7B	STATUS_IOUT	0x00		
	USB007 v66.0 EI	N L Device Checksum 0x95FD	0.70		0.00		



User manual



## 4.1.4 Programming the FET

Note:

This section is applicable only if fully digital mode (FDM) is used. If using analog-assisted digital mode (AADM), the FET will be pre-programmed. These modes are discussed in detail in Section 4.2. You can skip this step in that case.

If FDM is used, the FET must be programmed in the FET\_SELECT bits of the MODE register (0xD1) according to the one populated on the board. The board has the **IPB017N10N5** FET populated.

- 1. Select the IPB017N10N5 FET.
- 2. Modify the FET\_SELECT bit to 0xB, and then click **Write**. See Figure 29.

neon - XDP <sup>™</sup> Designer (De fineon	rv_Build-2825) rch	Q					TLVR 4	\$ D	рмв 🖉	FW	٩	GC	₿	CFG	<b>₫</b> 1	¢ •(	I (
Active Controller		Search	All Fault MF	R Status 1	felem Vout	MODE								L	ive Read (	0n) 📢	
	02: 0×10	Code	Command	Hex	Value	Selected Loop											
😑 Loop A	: Vout = 47.26V   Iout = 0A	0x97	READ_PIN	0x0000	0 W	Loop A											
Telemetry	: 2	0×98	PMBUS_REVISION	0x33		Command Value											
Vin	48.012 V	0x99	MFR_ID	0x004649		FET_SELECT 0xB	-+										
Vout	47.26 V	0x9A	MFR_MODEL	0x0000000		MODE 0x1	-+										
Iout	0 A	0x9B	MFR REVISION	0x0001													
Temp (Ext)	36.74 °C	0xD0	PMBUS CEG	0×10													
Pin	0 W	0vD1	MODE	0x4B													
		0xD3	REG_CFG	0x0803													
		0xD4	V_SNS_CFG	0x0028	4												
		0xD5	I_SNS_CFG	0xB418	-										-		
		0xD6	I_SNS_OFFSET_COMP	0x0000											Read		Write
		0xD7	TSNS_LVL_CTRL	0x07BF		Description			P 1 1				lease ale				
		0xD8	WATCHDOG_TMR	0x67	3	Digital mode. Either ana compared digitally with	og comparators at the U he VIN_UV_FAULT_LIMI	JV/EN, OV and F T, VIN_OV_FAU	B pins are us LT_LIMIT and	ed to trigg	ger the UV,	OV and OU MIT values	V faults; o to trigger	r ADC com the faults.	versions re	sults will	be
		0xD9	V_TMR	0x0FFF		MODE	Description										
		0xDA	PIN_POLARITY	0x01	-	0x0 0x1	Analog Comparators M Digital Comparators M	Iode (ACM) Iode (DCM)									
		0xDB	GPO_CFG	0x0000		FET_SELECT	Description	A1 - DC Line		FET_SELE	CT	Des	cription	SATMAT	10ms line		
		0xDC	IOUT_UC_WARN_LIMIT	0x0000		0x01 (00 0001 bin)	BSC035N10NS5ATMA BSC040N10NS5ATMA	A1 - DC Line		0x21 (10 0	001 bin)	BSC	035N10N	SSATMA1	10ms line		
		0xDD	ONCHIP TSD FAULT LIMIT	0x03		0x03 (00 0010 bin)	IPTG011N08NM5 - DO	C Line		0x23 (10 0	011 bin)	IPT	G011N08M	IM5 - 10ms	s line		
Faults 2	Clear All 🛛 🖉 🔻			31100		0x04 (00 0100 bin)	IPTC012N08NM5 - DC	Line		UX24 (10 0	TOO DIN)	IPT	CO12N08N	M5 - 10m	sune l'	_	

Figure 29 FET selection in FDM



## 4.1.5 Programming R<sub>sns</sub>

The sense resistor value must be programmed in the  $R_{sns}$  bits of the REG\_CFG register according to the one populated on the board. The board has  $R_{sns}$  of **1 m** $\Omega$  populated.

- 1. Select the 1 m  $\Omega$  resistor.
- 2. Modify the R<sub>sns</sub> bit to 0xD, and then click **Write**. See Figure 30.

		-												• (Đ
Ineon	Search	Q							TLVR ANA I	РМВ 😰	i FW 🔧 📗	GC E	🕉 CFG 🤨	\$
Active Cor	ntroller	Search	All Fault MF	R Status T	elem Vout	REG_C	G						Live Read	(On) 🛑
<b>(</b> ) x0	DP700V002: 0x10	Code	Command	Hex	Value 4	Select	d Loop							
i 🔴	Loop A : Vout = 47.28V   Iout = 0A	0x97	READ_PIN	0x0000	0 W	● Lo	op A							
Telemetry	/ 10	2 <sub>0x98</sub>	PMBUS_REVISION	0x33		Comm	and Value							
Vin	47.969 V	0x99	MFR_ID	0x004649		RSNS		0xD	<u>-</u> +					
Vout	47.281 V 0 A	0x9A	MFR_MODEL	0x0000000		RMS_E	N MODE EN	0x0						
Temp (Ext	t) -275.4 ℃	0x9B	MFR_REVISION	0x0001		BOOS	MODE_EN	0x0						
Temp (Int	) 37.17 °C	0xD0	PMBUS_CFG	0×10		BOOS	MODE_DC	0x2 (						
Pin	0 W	0xD1	MODE	0x4B										
		0xD3	REG_CFG	0x080D	-									
		0xD4	V_SNS_CFG	0x0028										
		0xD5	I_SNS_CFG	0xB458									Read	Write
		0xD6	I_SNS_OFFSET_COMP	0x0000				<b>b</b>		-				
		0xD7	TSNS_LVL_CTRL	0x07BF		0x00 (0	0 0000 bin)	0.2 mΩ	0x10 (01 0000 bin)	1.25 mΩ	0x20 (10 0000 bin)	2.8 mΩ	0x30 (11 0000 bin)	d f mΩ
		0xD8	WATCHDOG_TMR	0x67		0x01 (0 0x02 (0	0 0001 bin) 0 0010 bin)	0.25 mΩ 0.3 mΩ	0x12 (01 0001 bin)	1.3 mΩ 1.4 mΩ	0x22 (10 0001 bin) 0x22 (10 0010 bin)	3.1 mΩ	0x31 (11 0001 bin) 0x32 (11 0010 bin)	4.7 mΩ
		0xD9	V_TMR	0x0FFF		0x03 (0 0x04 (0	0 0100 bin)	0.55 mΩ 0.4 mΩ	0x15 (01 0011 bin) 0x14 (01 0100 bin)	1.5 mΩ 1.6 mΩ	0x24 (10 0100 bin)	3.3 mΩ	0x34 (11 0100 bin)	4.9 mΩ
		0xDA	PIN_POLARITY	0x01		0x05 (0 0x06 (0	0 0110 bin)	0.5 mΩ	0x16 (01 0101 bin)	1.8 mΩ	0x26 (10 0101 bin) 0x26 (10 0110 bin)	3.5 mΩ	0x36 (11 0101 bin)	5.5 mΩ
			GPO CEG	0x0000		0x08 (0	0 1000 bin)	0.67 mΩ	0x18 (01 1000 bin)	2 mΩ	0x28 (10 1000 bin)	3.7 mΩ	0x38 (11 1000 bin)	6.5 mΩ
		0xDB				0,003 (0	0 4004 DIII)	011 1102	0×14 (01 1010 bin)	2.2 mD	0x2A (10 1001 bin)	3.9 mΩ	0x3A (11 1010 bin)	7.5 m0
		0xDB 0xDC	IOUT_UC_WARN_LIMIT	0x0000		0x0A (0	0 1010 bin)	0.75 mΩ 0.8 mΩ	0x18 (01 1010 bin)	2.3 m0	0x2B (10 1011 bin)	4 m0	0x3B (11 1011 bin)	8m0
		0xDB 0xDC 0xDD	IOUT_UC_WARN_LIMIT	0x0000 0x03		0x0A (0 0x0B (0 0x0C (0 0x0C (0	0 1010 bin) 0 1011 bin) 0 1100 bin)	0.75 mΩ 0.8 mΩ 0.9 mΩ	0x1R (01 1010 bin) 0x1B (01 1011 bin) 0x1C (01 1100 bin) 0x1D (01 1101 bin)	2.3 mΩ 2.4 mΩ 2.5 mΩ	0x2B (10 1011 bin) 0x2C (10 1100 bin) 0x2D (10 1101 bin)	4 mΩ 4.1 mΩ 4.2 mΩ	0x3B (11 1011 bin) 0x3C (11 1100 bin) 0x3D (11 1101 bin)	8 mΩ 8.5 mΩ 9 mΩ

Figure 30 R<sub>sns</sub> selection



## 4.1.6 Selecting the watchdog timer

Set the watchdog timer higher than the turn-on time to ensure that the watchdog timer does not expire before the turn-on. At the same time, ensure that the watchdog timer is not set much longer than the turn-on time to prevent damage to the FET in the event of a short-circuit during turn-on. The watchdog timer is modified to 200 ms, as shown in Figure 31.

	rch	Q				4	🖗 РМВ 🕼 FW 🔧	🖺 cc 🚓 🏟 📲	
Active Controller	:	Search	All Fault MFR SI	tatus Telem Vout	WATCHDOG_TMR			Live Read (On)	1
C XDP700V00	02: 0x10	Code	Command	Loop A	* Selected Loop				
loop A	: Vout = 0.04V   lout = 0A	0xD7	TSNS_LVL_CTRL	0x07BF	Loop A				
Telemetry	: 🗹	0xD8	WATCHDOG_TMR	0x66	Command Value				
Vin	48.098 V	0xD9	V_TMR	0x0FB6	0x66				
Vout	0.043 V	0xDA	PIN_POLARITY	0x01	WATCHDOG 0x6	-+			
Temp (Ext)	31.33 °C	0xDB	GPO_CFG	0x0000	EN_DG 0x6	-+			
Temp (Int)	35 °C	0xDC	IOUT_UC_WARN_LIMIT	0x0000					
Pin	0 W	0xDD	ONCHIP_TSD_FAULT_LIMIT	0x03					
		0xDE	ENABLE_FAULTS	0x7EFF					
		0xDF	MASK_FAULTS	0x7EFF					
		0xDF 0xE0	MASK_FAULTS STATUS_FAULTS	0x7EFF 0x0000	_			Read	rite
		0xDF 0xE0 0xE1	MASK_FAULTS STATUS_FAULTS ENABLE_WARNS	0x7EFF 0x0000 0x0FDC	2:0/WATCHDOG the FET.	סיט צובט און עטער אווויג (און און אין אין און און און אין אין אין אין אין אין אין אין אין אי	rnownong and have can accempt to po	Read Wr	rite
		0xDF 0xE0 0xE1 0xE2	MASK_FAULTS STATUS_FAULTS ENABLE_WARNS MASK_WARNS	0x7EFF 0x0000 0x0FDC 0x0FDC	2:0 WATCHDOG the FET.	סט אוני אויז איז איז איז איז איז איז איז איז איז א	nnow rong Swelene can accomp corpo	Read Wr	rite
		0xDF 0xE0 0xE1 0xE2	MASK_FAULTS STATUS_FAULTS ENABLE_WARNS MASK_WARNS	0x7EFF 0x0000 0x0FDC 0x0FDC	2:0/WATCHDOG the FET.	Decription	rnovriong Swolew Carratemperorpo	Read Wr wer up the output wondoor tany enname Description One	rite
		0xDF 0xE0 0xE1 0xE2 0xE3	MASK_FAULTS STATUS_FAULTS ENABLE_WARNS MASK_WARNS STATUS_WARNS	0x7EFF 0x0000 0x0FDC 0x0FDC 0x0FDC	2:0[WATCHDOG the FEI. WATCHDOG watchdow (1990) 000 (1990) bin) 001 (1990) bin)	Description Sms 10ms	THY YOUR GAT ASSEMPTS OF PO     [EN_DG     (0x0 (0000 bin)     (0x1 (0x1 (0x1 (0x1 (0x1 (0x1 (0x1 (	Read Wr wer op the output without tany emission Description Oms Ams	rite
		0x0F 0xE0 0xE1 0xE2 0xE3	MASK_FAULTS STATUS_FAULTS ENABLE_WARNS MASK_WARNS STATUS_WARNS	0x7EFF 0x0000 0x0FDC 0x0FDC 0x00FDC	2:0[WATCHDOG [wertschap] the FET. WATCHDOG 0x0 (0000 bin) 0x1 (000 bin) 0x2 (000 bin)	Pescription Sms 10ms 20ms	EN. DG         Can assempt to po           EN. DG         Ox0 (0000 bin)           Ox1 (0001 bin)         Ox2 (0001 bin)           Ox2 (0001 bin)         Ox2 (0001 bin)	Read Wr wer up ore output version rung remain Description Oms Arns Brns	rite
		0xDF 0xE0 0xE1 0xE2 0xE3 0xE4	MASK_FAULTS STATUS_FAULTS ENABLE_WARNS MASK_WARNS STATUS_WARNS PWRGD_DG_TMR	0x7EFF 0x0000 0x0FDC 0x0FDC 0x0000 0xF5	2:0(WATCHDOG the FET. WATCHDOG bin (the FET. WATCHDOG bin) 0:4 (0000 bin) 0:4 (0000 bin) 0:4 (0010 bin) 0:5 (0010 bin) 0:5 (0010 bin)	Description Sms 10ms 20ms 50ms	EN.DG         Carr assempced point           0x0 (0000 bin)         0x1 (0000 bin)           0x2 (0000 bin)         0x2 (0000 bin)           0x2 (0010 bin)         0x2 (0010 bin)	Read Wr Description Ons Ans Brns Brns Brns	rite
		0xDF 0xE0 0xE1 0xE2 0xE3 0xE4 0xE5	MASK_FAULTS STATUS_FAULTS ENABLE_WARNS MASK_WARNS STATUS_WARNS PWRGD_DG_TMR	0x7EFF 0x0000 0x0FDC 0x0FDC 0x0FDC 0x0FDC 0x0FDC 0x0FS	2:0[WATCHDOG         WATCHDOG           watchdoc         dweren           0:0(000 bin)         000 bin)           0:1(000 bin)         001 bin)           0:2(0010 bin)         001 bin)           0:4(0010 bin)         000 bin)	Description Sms 10ms 20ms 56ms 75ms	EN_DG         Carrasempero po           EN_DG         0x0 (0000 bin)           0x1 (0001 bin)         0x2 (0010 bin)           0x3 (0011 bin)         0x3 (0011 bin)           0x3 (0011 bin)         0x4 (0100 bin)	Read Wr Description Ons Ams Bms 16ms 32ms	rite
		0xDF 0xE0 0xE1 0xE2 0xE3 0xE4 0xE5	MASK_FAULTS STATUS_FAULTS ENABLE_WARNS MASK_WARNS STATUS_WARNS PWRGD_DG_TMR SOA_TMR	0x7EFF 0x0000 0x0FDC 0x0FDC 0x0FDC 0xFS 0x55 0x0000	2:0[WATCHDOG         Imm Sol to the FET.           WATCHDOG         0:000 bin           0:0000 bin         0:0000 bin           0:010000 bin         0:000 bin           0:02000 bin         0:000 bin	Description Sms 10ms 20ms 56ms 75ms 100ms	En, DG         Can assempt to po           EN, DG         Opc (0000 bin)           Opt (0001 bin)         Opt (0001 bin)	Read Wr wer up vie output worken nan Ons Arns Brns Ifons Ifons S2ms 64ms	rite
		0xDF 0xE0 0xE1 0xE2 0xE3 0xE4 0xE5 0xE6	MASK_FAULTS STATUS_FAULTS ENABLE_WARNS MASK_WARNS STATUS_WARNS PWRGD_DG_TMR SQA_TMR TURN_QEC_CTR	0x7EFF 0x0000 0x0FDC 0x0FDC 0x0FDC 0x0FDC 0x0500 0xFS 0x0002 0x0002	2:0[WATCHDOG         WartCHD           WATCHDOG         the FET.           WATCHDOG         0.0 (0000 bin)           0.4 (0000 bin)         0.0 (0000 bin)           0.4 (0010 bin)         0.4 (0100 bin)           0.4 (0100 bin)         0.4 (0100 bin)           0.4 (0100 bin)         0.5 (010 bin)	Description Sms 10ms 20ms 50ms 75ms 100ms 200ms	EN_DG         Carr assempt to po           Co/ (0000 bin)         Oct (0000 bin)           Oct (0000 bin)         Oct (0001 bin)           Oct (0010 bin)         Oct (0101 bin)           Oct (0100 bin)         Oct (0101 bin)           Oct (0101 bin)         Oct (0101 bin)	Read Wr bescription Ons Arns Brns Järns Järns Sörns Järns Järns Järns	rite
		0xDF 0xE0 0xE1 0xE2 0xE3 0xE4 0xE5 0xE6	MASK_FAULTS STATUS_FAULTS ENABLE_WARNS MASK_WARNS STATUS_WARNS STATUS_WARNS PWRGD_DG_TMR SOA_TMR TURN_OFF_CTRL	0x7EFF 0x0000 0x0FDC 0x0FDC 0x0FDC 0x0000 0xF5 0x0002 0x0002	2:0[WATCHDOG [Wardena the FET. WATCHDOG 0x0 (0000 bin) 0x1 (0001 bin) 0x2 (0010 bin) 0x3 (0011 bin) 0x5 (1001 bin) 0x6 (1010 bin) 0x6 (1010 bin) 0x6 (1010 bin) 0x6 (1010 bin) 0x6 (1010 bin) 0x6 (1010 bin)	Description Sms 10ms 20ms 50ms 75ms 100ms 200ms 200ms 500ms 500ms	EN_DG           0x0 (0000 bin)           0x1 (0001 bin)           0x2 (0010 bin)           0x2 (0010 bin)           0x2 (0010 bin)           0x6 (0010 bin)           0x6 (0100 bin)           0x6 (0100 bin)           0x6 (010 bin)           0x6 (010 bin)           0x6 (0110 bin)           0x7 (0111 bin)           0x7 (0111 bin)	Read         Wr           Description         Ons           Oms         Ams           Bms         Idms           32ms         64ms           128ms         256ms           256ms         256ms	rite
		0xDF 0xE0 0xE1 0xE2 0xE3 0xE4 0xE5 0xE5 0xE6 0xE7	MASK_FAULTS STATUS_FAULTS ENABLE_WARNS MASK_WARNS STATUS_WARNS PWRGD_DG_TMR SOA_TMR TURN_OFF_CTRL RETRY	0x7EFF 0x0000 0x0FDC 0x0FDC 0x0000 0xF5 0x0002 0x002 0x002 0x002	2:0(WATCHDOG the FET. WATCHDOG the FET. WATCHDOG 0:0000 bin) 0:1(0000 bin) 0:2(0000 bin) 0:3(001 bin) 0:4(000 bin) 0:4(000 bin) 0:5(0010 bin) 0:5(0010 bin) 0:5(0010 bin) 0:5(000 bin) 0:	Description Sms I0ms 20ms 20ms 75ms 100ms 200ms 200ms 500ms	EN_D6         Contrastemptor pro           EN_D6         Ox0 (0000 bin)         Ox1 (0000 bin)         Ox2 (0000 bin)         Ox2 (0010 bin)         Ox4 (1000 bin)         Ox6 (1010 bin)         Ox	Read Wr Description Oms Ams Ams Bms Bms Jams Gens Jams Sens Softma 256ms 256ms 250ms	rite
		0xDF 0xE0 0xE1 0xE2 0xE3 0xE4 0xE5 0xE6 0xE6	MASK_FAULTS STATUS_FAULTS ENABLE_WARNS MASK_WARNS STATUS_WARNS STATUS_WARNS PWRGD_DG_TMR SOA_TMR TURN_OFF_CTRL RETRY	0x7EFF 0x0000 0x0FDC 0x0FDC 0x0FDC 0x0000 0xFS 0x0002 0x0002 0x082F	2:0[WATCHDOG         Wordering the FET.           WATCHDOG         0:0000 bin)           0:0000 bin)         0:0000 bin)           0:01000 bin)         0:0100 bin)           0:4 (0100 bin)         0:04 (0100 bin)           0:6 (010 bin)         0:6 (010 bin)	Description Sms L0ms Sms Sms Sms 20ms Sms 20ms Sms 200ms S00ms S00ms T5ms 100ms 100ms S00ms 75ms 1000ms S00ms S00m	EN_DG         Gasterie Carr assempt to pro           EN_DG         Ox0 (0000 bin)           Ox1 (0000 bin)         Ox1 (0001 bin)           Ox2 (0010 bin)         Ox4 (0100 bin)           Ox3 (0010 bin)         Ox5 (1011 bin)           Ox6 (1010 bin)         Ox6 (1010 bin)           Ox7 (0111 bin)         Ox6 (1000 bin)           Ox7 (0111 bin)         Ox6 (1000 bin)           Ox6 (1000 bin)         Ox6 (1000 bin)           Ox6 (1000 bin)         Ox6 (1000 bin)	Read         Wr           Description         Oms           Ams         Bms           Bms         Sms           J8ms         J3ms           J4ms         J3ms           J2ms         J3ms	rite
		0x0F 0xE0 0xE1 0xE2 0xE2 0xE3 0xE4 0xE5 0xE5 0xE6 0xE7 0xE8	MASK_FAULTS STATUS_FAULTS ENABLE_WARNS MASK_WARNS STATUS_WARNS PWRGD_DG_TMR SQA_TMR TURN_OFF_CTRL RETRY TELEMETRY_EN	0x7EFF 0x0000 0x0FDC 0x0FDC 0x0FDC 0xF5 0x0000 0xF5 0x0002 0x002 0x3E3F 0x7FFF	2:0(WATCHDOG         Unit Size           WATCHDOG         Unit Size           0:0(0000 bin)         0:0(0000 bin)           0:0(0000 bin)         0:0(010 bin)           0:0(0100 bin)         0:0(0100 bin)	Description Sms 10ms 20ms 20ms 75ms 100ms 200ms 500ms 750ms 750ms 1000ms 2000ms 2000ms	EN_DG         Conversion         Conversion </td <td>Read         Wr           Description         Oms           Ams         Brins           Ifoms         Jams           Sms         Ifoms           Jams         Sense           Softmax         Sense           Softmax         Sense           Softmax         Sense           Softmax         Sense           Softmax         Softmax           Softmax         Softmax</td> <td>rite</td>	Read         Wr           Description         Oms           Ams         Brins           Ifoms         Jams           Sms         Ifoms           Jams         Sense           Softmax         Sense           Softmax         Sense           Softmax         Sense           Softmax         Sense           Softmax         Softmax           Softmax         Softmax	rite

Figure 31 Watchdog timer selection

# 4.1.7 Programming the current sense range (CS\_RNG) and start-up current limit (IST)

*Note:* If using AADM, skip this step because the resistor on the IST pin selects the start-up current limit and current sense range.

In FDM, program the desired current sense range and start-up current limit in the I\_SNS\_CFG register (0xD5), as shown in Figure 32.

Note: Do not set the current sense range as 100 mV with  $1 \text{ m}\Omega$  sense resistor. The SOA regulation loop does not work when (current sense range (mV)/ R (mohm)) > 83.33 A.



	arch	Q						TLVF 🎝		FW 🔧 📗	CC 🛱	CFG 🟮	\$ ·[]
Active Controller	:	Search	All Fault M	FR Status T	elem Vout	I_SNS_CFG						Live Read	(On)
TXDP700V0	002: 0×10	Code	Command	Hex	Value Juli Juli Juli	Selected Loop							
🔴 Loop /	A : Vout = 47.3V   Iout = 0A	0x97	READ_PIN	0x0000	0 W	Loop A							
Telemetry	: 2	0x98	PMBUS_REVISION	0x33		Command Value							
Vin	48.012 V	0x99	MFR_ID	0x004649		START_ILIM	0x5	-+					
Vout	47.303 V	0x9A	MFR_MODEL	0x0000000		SOC_FAULT_LIMIT	0x3	-+					
Temp (Ext)	0 A -275.4 °C	0x9B	MFR_REVISION	0x0001		CS_RNG	0x1						
Temp (Int)	36.74 °C	0xD0	PMBUS_CFG	0x10		C2_RNG_TRIM	0.04						
Pin	0 W	0xD1	MODE	0x4B									
		0xD3	REG_CFG	0x080D	8								
		0xD4	V_SNS_CFG	0x0028	2								
		0xD5	L_SNS_CFG	0xB45D	- 1							Read	
		0xD6	I_SNS_OFFSET_COMP	0x0000		0x0 (000 bin)				100% of OC			
						0x1 (001 bin)				75% of OC			
		0.07	TOALC INC. CTDI			[[]] [[]] []_] []_] []_] []_] [				50% of OC			
		0xD7	TSNS_LVL_CTRL	0x07BF		0x2 (010 bin)				25% of OC			
		0xD7 0xD8	TSNS_LVL_CTRL WATCHDOG_TMR	0x67		0x3 (011 bin) 0x4 (100 bin)				25% of OC 15% of OC			
		0xD7 0xD8	TSNS_LVL_CTRL WATCHDOG_TMR	0x67		0x2 (010 bin) 0x3 (011 bin) 0x4 (100 bin) 0x5 (101 bin)				25% of OC 15% of OC 12.5% of OC			
		0xD7 0xD8 0xD9	TSNS_LVL_CTRL WATCHDOG_TMR V_TMR	0x07BF 0x67 0x0FFF	-	0x2 (010 bin) 0x3 (011 bin) 0x4 (100 bin) 0x5 (101 bin) 0x6 (110 bin)				25% of OC 15% of OC 12.5% of OC 9% of OC			
		0xD7 0xD8 0xD9	TSNS_LVL_CTRL WATCHDOG_TMR V_TMR	0x078F 0x67 0x0FFF		0x3 (011 bin) 0x4 (100 bin) 0x5 (101 bin) 0x6 (110 bin) 0x7 (111 bin)				25% of OC 15% of OC 12.5% of OC 9% of OC 5% of OC			
		0xD7 0xD8 0xD9 0xDA	TSNS_LVL_CTRL WATCHDOG_TMR V_TMR PIN_POLARITY	0x078F 0x67 0x0FFF 0x01	-	0x3 (010 bin) 0x3 (011 bin) 0x4 (100 bin) 0x6 (110 bin) 0x6 (110 bin) 0x7 (111 bin) SOC FAULT LIMIT			CS_RNG 2'b0x	25% of OC 15% of OC 12.5% of OC 9% of OC 5% of OC	CS_RNG 2 <sup>+1</sup>	blx	
		0xD7 0xD8 0xD9 0xDA	TSNS_LVL_CTRL WATCHDOG_TMR V_TMR PIN_POLARITY	0x078F 0x67 0x0FFF 0x01	-	0x3 (010 bin) 0x3 (011 bin) 0x5 (100 bin) 0x5 (101 bin) 0x6 (110 bin) 0x7 (111 bin) SOC_FAULT_LIMIT 0x0 (000 bin)			C\$_RNG 2'b0x 12.5mV	25% of OC 15% of OC 12.5% of OC 9% of OC 5% of OC	CS_RNG 2'1 25mV	blx	
		0xD7 0xD8 0xD9 0xDA 0xDB	TSNS_LVL_CTRL WATCHDOG_TMR V_TMR PIN_POLARITY GPO_CFG	0x078F 0x67 0x0FFF 0x01 0x000	-	0x2 (010 bin) 0x3 (011 bin) 0x4 (100 bin) 0x5 (101 bin) 0x6 (110 bin) 0x7 (111 bin) SOC_FAULT_LIMIT 0x0 (000 bin) 0x1 (001 bin)			CS_RNG 2'b0x 12.5mV 18.75mV	25% of OC 15% of OC 12.5% of OC 9% of OC 5% of OC	CS_RNG 2' 25mV 37.5mV	blx	
		0xD7 0xD8 0xD9 0xDA 0xDB 0xDB	TSNS_LVL_CTRL WATCHDOG_TMR V_TMR PIN_POLARITY GPO_CFG IOUT_UC_WARN_LIMIT	0x078F 0x67 0x0FFF 0x01 0x0000 0x0000		0x2 (010 bin) 0x3 (011 bin) 0x4 (100 bin) 0x5 (101 bin) 0x6 (110 bin) 0x7 (111 bin) <b>SOC_FAULT_LIMIT</b> 0x0 (000 bin) 0x1 (001 bin) 0x2 (010 bin)			CS_RNG 2'b0x 12.5mV 18.75mV 25mV	25% of OC 15% of OC 12.5% of OC 9% of OC 5% of OC	C5_RNG 2'1 25mV 37.5mV 50mV	blx	
		0xD7 0xD8 0xD9 0xDA 0xDB 0xDB	TSNS_LVL_CTRL WATCHDOG_TMR V_TMR PIN_POLARITY GPO_CFG IOUT_UC_WARN_LIMIT	0x078F 0x67 0x0FFF 0x01 0x0000 0x0000		bx2 (010 bin)           bx3 (011 bin)           bx4 (100 bin)           bx6 (101 bin)           bx7 (111 bin)           bx7 (111 bin)           bx0 (000 bin)           bx1 (001 bin)           bx2 (010 bin)           bx2 (010 bin)           bx2 (010 bin)           bx2 (010 bin)           bx3 (011 bin)			CS_RNG 2'b0x 12.5mV 18.75mV 25mV 37.5mV	25% of OC 15% of OC 12.5% of OC 9% of OC 5% of OC	CS_RNG 2'1 25mV 37.5mV 50mV 75mV	blx	

Figure 32 Current sense range and start-up current limit setting

## 4.1.8 **Programming VIN\_UV\_FAULT\_LIMIT**

If using AADM or ACM, skip this step because the input undervoltage (UV) fault limit is set by external resistors on the UV pin.

If using DCM, program the desired UV fault limit in the VIN\_UV\_FAULT\_LIMIT register (0x59). If the UV fault is not used, the register can be programmed to 0 V, or the fault can be disabled.

infi	neon Searc	_Build-2825) :h	Q				TLVF 🕼 🗖 🎫 🕲 FW 🔦 🖹 GC 🚓 CFG 🐞 💠 🖞 😧
=<	Active Controller	:	Search	All Fault MFI	R Status T	elem Vout	VIN_UV_FAULT_LIMIT Live Read (On) 🛑 🗙
ñ		2: 0x10	Code	Command	Hex	Value	Selected Loop
<u>)</u>	Talamatry	: 7	0x01	OPERATION	0x80	· ·	Command Malace (Decime B
٥	Min	48.012.V	0x03		0,00	•	37.9969911885
	Vout	47.281 V	0x42	VOUT_OV_WARN_LIMIT	0x0F73	84.9989 V	
	lout Temp (Ext)	0 A -275.4 °C	0x43	VOUT_UV_WARN_LIMIT	0x0000	0 V	
	Temp (Int)	37.17 °C	0x44	VOUT_UV_FAULT_LIMIT	0x06E8	37.997 V	
	Pin	0 W	0x4A	IOUT_OC_WARN_LIMIT	0x0FFF	35.3566 A	
			0x4F	OT_FAULT_LIMIT	0x0FFF	512.0962 °C	
			0x51	OT_WARN_LIMIT	0x0FFF	512.0962 °C	
			0x55	VIN_OV_FAULT_LIMIT	0x0CB9	69.9979 V	Read Write
			0x57	VIN_OV_WARN_LIMIT	0x0FFF	88.0077 V	
			0x58	VIN_UV_WARN_LIMIT	0x0000	0 V	Description This command sets the value of the input voltage measured at the VDD_RTNS pin that causes an input undervoltage fault.
			0x59	VIN_UV_FAULT_LIMIT	0x06E8	37.997 V	UV lault can be programmed from 0 to 22, 0 to 44 or 0 to 88V (absolute value) depending on VTLM RNG settings.
			0x6B	PIN_OP_WARN_LIMIT	0xFFFF	3112.7102 W	
			0x78	STATUS_BYTE	0x40		
			0x79	STATUS_WORD	0x0840		
			0x7A	STATUS_VOUT	0x00		
	Faults 🙆	Clear All	0x7B	STATUS_IOUT	0×00		

Figure 33 Program VIN\_UV\_FAULT\_LIMIT



## 4.1.9 **Programming VIN\_OV\_FAULT\_LIMIT**

Note:

If using AADM or ACM, skip this step because the input overvoltage (OV) fault limit is set by external resistors on the OV pin.

If using DCM, program the desired OV fault limit in the VIN\_OV\_FAULT\_LIMIT register (0x55). If the OV fault is not used, the register can be programmed to 88 V, or the fault can be disabled.

Infineon - XDP™ Desi	igner (Dev_Build+2825)					- 0 >>
infineon	Search	Q				TLVF 🕸 📃 PMB 🕼 FW 🔦 🖺 GC 🚓 CFG 🛎 🌣 💶 🔮
Active Cont	roller :	Search	All Fault MFR	Status T	ielem Vout	VIN_OV_FAULT_LIMIT Live Read (On) 🗰 🛛 🗙
n 😑 🚺	700V002: 0x10	Code	Command	Hex	on A Yalue	selected Loop
ji 🦾 🔶 I	Loop A : Vout = 47.28V   Iout = 0A	0x01	OPERATION	0x80		Loop A
Telemetry	: 🛛	0x03	CLEAR_FAULTS	-		Command Value (Decimal)
Vin	48.012 V	0x19	CAPABILITY	0xD0		69.9978508489 — 🕂 v
Vout	47.281 V	0x42	VOUT_OV_WARN_LIMIT	0x0F73	84.9989 V	
lout	0 A	0x43	VOUT_UV_WARN_LIMIT	0x0000	0 V	
Temp (Int)	37.17 °C	0x44	VOUT_UV_FAULT_LIMIT	0x06E8	37.997 V	
Pin	0 W	0x4A	IOUT_OC_WARN_LIMIT	0x0FFF	35.3566 A	
		0x4F	OT_FAULT_LIMIT	0x0FFF	512.0962 °C	
		0x51	OT WARN LIMIT	0x0FFF	512.0962 °C	
		0x55	VIN OV FAULT LIMIT	0x0CB9	69.9979 V	
		0x57	VIN OV WARN LIMIT	0x0FFF	88.0077 V	Read Write
		0v58	VIN UV WARN LIMIT	0×0000	0.1	Description
		0,50	VIN IN FAULT LIMIT	0~0000	01	The VIN_OV_FAULT_LIMIT command sets the value of the input voltage measured at the VDD_RTNS pin that causes an input overvoltage fault. OV fault can be programmed from 0 to 22, 0 to 44 or 0 to 88V (absolute value) depending on VTLM RNG settings.
		0.05		0.0000	2112 7102 W	
		079	CTATUS DVTE	0xFFFF	5212./102 W	
		0x78	STATUS_BYTE	0x40		
		0x79	STATUS_WORD	0x0840		
		0x7A	STATUS_VOUT	0x00		
Faults [ 2]	Clear All 🔽 👻	0x7B	STATUS_IOUT	0x00	· ·	
USB007 v66.0	EN L Device Checksum 0x95FD	0.70	ATITUA UIBLIT	0.00		

Figure 34 Program VIN\_OV\_FAULT\_LIMIT



## 4.1.10 **Programming VOUT\_UV\_FAULT\_LIMIT**

To program the desired UV fault limit, set the VOUT\_UV\_FAULT\_LIMIT register (0x44). If the UV fault is not used, the fault can be disabled.

Note:

If enabled, VOUT\_UV\_FAULT should not be set to 0 V because hot swap will turn off after turning on, detecting it as a VOUT\_UV fault.

ineon - XDP™ Designer (De <b>nfineon</b> Sear	ev_Build-2825)	Q				т.LVF 🖑 📃 РИВ 🐵 FW 🔧 🖹 GC 🚓 СFG 🛎 🌣 📲
Active Controller	:	Search	All Fault MFR	Status	Telem Vout	VOUT_UV_FAULT_LIMIT Lives Read (On)
CODE CODE A	02: 0x10 : Vout = 48.14V   Iout = 0A	Code 0x01	Command	Hex 0x80	Value	Selected Loop © Loop A
Telemetry	: 2	0x03	CLEAR_FAULTS			Command Value (Decimal)
Vin	48.098 V	0x19	CAPABILITY	0xD0		35.9982806791 — + V
Vout	48.141 V	0x42	VOUT_OV_WARN_LIMIT	0x0BD0	64.9903 V	
lout Temp (Ext)	0 A	0x43	VOUT_UV_WARN_LIMIT	0x06E8	37.997 V	
Temp (Int)	37.61 °C	0x44	VOUT_UV_FAULT_LIMIT	0x068B	35.9983 V	
Pin	0 W	0x4A	IOUT_OC_WARN_LIMIT	0x090C	19.9965 A	
		0x4F	OT_FAULT_LIMIT	0x07A0	99.9808 °C	
		0x51	OT_WARN_LIMIT	0x076C	89.9808 °C	
		0x55	VIN_OV_FAULT_LIMIT	0x0B45	62.003 V	
		0x57	VIN_OV_WARN_LIMIT	0x0AE8	60.0043 V	Read Write
		0x58	VIN_UV_WARN_LIMIT	0x0717	39.0071 V	Description The WHIT LINE TANKS I HAIT assessed rate the value of the output unlines measured at the WHIT pin that success as submit under allows foult
		0x59	VIN_UV_FAULT_LIMIT	0x06E8	37.997 V	OUV fault can be programmed from 0 to 22, 0 to 44 or 0 to 88V (absolute value) depending on VTLM RNG settings.
		0x6B	PIN_OP_WARN_LIMIT	0x62B1	1200.0095 W	
		0x78	STATUS_BYTE	0x40		
		0x79	STATUS_WORD	0x0840	-	
		0x7A	STATUS_VOUT	0x20	-	
		0x7B	STATUS_IOUT	0x00		
Faults 2	Clear All		ARTELA DIRUT			

Figure 35 Program VOUT\_UV\_FAULT\_LIMIT

## 4.2 Programming XDP700-002 in different modes

XDP700-002 can be operated in two different modes: FDM and AADM. FDM has two selections: DCM and ACM. AADM or FDM can be selected based on the resistor connected on the Mode 0 and Mode 1 pins on the evaluation board. Based on the mode selected, you need to configure different PMBus registers.

## 4.2.1 Fully Digital Mode (FDM)

FDM lets you select the FET, start-up current limit, and current sense range via PMBus registers. In digital comparator mode (DCM), the fault sensing on input and output voltages is done via digital comparators and is based on the telemetry of the device. This approach reduces the analog circuitry required while in analog comparator mode (ACM). This method uses external voltage dividers on the UV and OV pins. The voltage on the divider is compared with the internal threshold to detect faults. Voltage warnings are set internally via PMBus. You need to program the following registers through PMBus in FDM for both DCM and ACM:

- FET\_SELECT: See Section 4.1.4
- R<sub>sns</sub>: See Section 4.1.5
- Watchdog (optional): See Section 4.1.6
- Current sense range (CS\_RNG) and start-up current limit (IST): See Section 4.1.7

User manual



- Enable telemetry
- Enable warnings (if needed)
- Setting warnings (if needed)

## 4.2.1.1 Digital Comparator Mode (DCM)

If the device is programmed using DCM, select DCM in the register 0xD1 and modify bit '7' to '1'. You need to modify the following register to detect the necessary faults if the corresponding fault bits are enabled in the PMBus register (0xDE).

- VOUT\_UV\_FAULT\_LIMIT (0x44): See Section 4.1.10
- VIN\_OV\_FAULT\_LIMIT (0x55): See Section 4.1.9
- VIN\_UV\_FAULT\_LIMIT (0x59): See Section 4.1.8

To turn ON the FET, toggle the enable signal to **HIGH** (EN H) on the GUI, as shown in Figure 36.



Figure 36 Enabling FET by toggling enable signal high

## 4.2.1.2 Analog Comparator Mode (ACM)

If the device is programmed using ACM, select the ACM in the 0xD1 register, and modify bit '7' to '0'. In this mode, all the voltage faults are sensed using external resistors. Therefore, you need to place the following jumpers on the evaluation board to detect faults if the corresponding fault bits are enabled in the PMBus register (0xDE):

- VIN\_OV\_FAULT\_LIMIT (OV pin): Jumper is required on connector X41; the input OV fault limit can be set by modifying R34, R36, and R38.
- VIN\_UV\_FAULT\_LIMIT (UV pin): Jumper is required on connector X33. If UV\_FAULT is disabled, ensure that the UV pin gets the necessary enable signal voltage to turn ON the FET.



## 4.2.2 Analog Assisted Digital Mode (AADM)

AADM lets you select the FET, start-up current (IST) limit, and current sense range (CS\_RNG) via external resistors connected on pins Mode 0, Mode 1, and IST. For the evaluation board, the settings are done as shown in Table 6.

#### Table 6AADM selection resistors

Connector	Jumper position (resistor)	Function
X18 (mode pins)	Between 3 and 4 (Mode 0: Open)	Selects the FET
	Between 9 and 10 (Mode 1: 20 kΩ (2.0 V))	IPB017N10N5ATMA1
X21 (IST pins)	Between 5 and 6 recommended (IST: 11 kΩ (1.1 V))	25 mV current sense range is selected and IST as 12.5 percent of overcurrent (OC) level is selected.

Place the following jumpers on the evaluation board to detect faults if the corresponding fault bits are enabled in the PMBus register (0xDE):

- VIN\_OV\_FAULT\_LIMIT (OV pin): Jumper is required on connector X41; the input OV fault limit can be set by modifying R34, R36 and R38.
- VIN\_UV\_FAULT\_LIMIT (UV pin): Jumper is required on connector X33. If UV\_FAULT is disabled, ensure that the UV pin gets the necessary enable signal voltage to turn on the FET.

Modify the necessary PMBus registers for proper operation:

- R<sub>sns</sub>: See Section 4.1.5
- Watchdog: See Section 4.1.6
- Enable telemetry
- Enable warnings (if needed)
- Setting warnings (if needed)



#### Loading the configuration file

## 5 Loading the configuration file

You can load the configuration file into the device, which eliminates the need to manually modify the required registers. The configuration file can be loaded into the device as follows:

- 1. Click Load Config, as shown in Figure 37.
- 2. Click **Browse** and select the *.txt* file, as shown in Figure 38.
- 3. Click **Load** to load the configuration onto the device, as shown in Figure 39.



Figure 37 Select Load Config option

Load Config File	×
Select a Configuration File	
	Browse
	Close

Figure 38 Browse to select the necessary configuration file



#### Loading the configuration file

Load Config	File				×
Select a Co	onfiguration File	e			
XDP700V00	2_EvalBoard-0x0	000291F.txt		Bro	wse
Type: Checksum: Created By: Select Targ	Design 0x29BACD0 choim <b>get Devices:</b>	File Versio GUI Versio Created D	n: 1.1 n: Dev_Build te: 2024-02-0	1-3086 2T23:15	:47
Conf	ig File Device	<b>→</b>	Connected [	Device	
XDP7	00V002:0x10		XDP700V002:	0x10	~
			Clo	ose	Load

Figure 39 Load to load the selected configuration file

An example configuration file in .txt format is available in the XDP700-002 Evaluation Board page [2] as *XDP700V002\_EvalBoard-0x0000291F.txt*. This configuration file is compatible with the evaluation board in the default configuration.

## 6 Hands-on

Ensure the following:

- Proper input voltage (48 V) is available on the input of the evaluation board.
- The example configuration is loaded onto the device.
- The device is not yet enabled.

## 6.1 Turn ON FET test

The FET is turned ON by toggling the enable signal to HIGH (EN H) as shown in Figure 40.

*Note:* Ensure that the load is not ON when enabling the FET because it could cause the watchdog timer fault; in such a case, the FET will not turn ON.



Figure 40 Enabling FET by toggling enable signal to high

Figure 41 shows the turn-on waveforms. Note that the start-up current follows the programmed SOA of the FET as shown in Figure 41 closely, and ensures that the FET SOA is not violated during turn-on operation, thereby providing a safe and fast turn-on. Additionally, the maximum startup current observed is 1.626 A at an IST setting of 12.5%. Figure 42 highlights the regulation current at various VDS levels based on the SOA of IPB017N10N5.

İnfineon





Figure 41 Startup current waveform at 48 V input



Figure 42

Startup current regulation at various VDS levels



## 6.2 Boost mode test

For FETs with weaker SOA, with current capability of less than 0.25 A at higher voltages, it is recommended to turn ON the FET in boost mode. In the following example, boost mode is enabled, and the parameters are set as follows:

- Type of boost mode: Automatic boost mode
- SOA line: 1 ms
- Duty cycle: 20%

If the SOA is below 0.5 A, boost mode is activated; the controller sends gate pulses allowing the drain current for only 1 ms with its limit restricted to 8x the programmed SOA level. When the regulation current reaches 0.5 A, boost mode turns off, and the FET is regulated with regular SOA. Figure 43 shows the startup behavior with automatic boost mode and at  $V_{DS}$  = 25 V where  $I_{SOA}$  = 0.5 A, the controller resumes with regular current regulation.



Figure 43 Automatic boost mode operation

Attention: Set the duty cycle according to  $C_{gs}$  to provide sufficient time for the gate to discharge to avoid double pulses and violation of SOA on 1 ms line.



## 6.3 Turn-ON in output short test

The output of the evaluation board is shorted together, and the watchdog timer is reduced down to 200 ms from 500 ms. Hot swap is enabled by toggling the enable signal to **HIGH** (EN H). Figure 44 shows that the current has been regulated down to the minimum level of 0.25 A; after the watchdog timer expires, the gate is turned OFF and a watchdog timer fault is issued.



Figure 44 Turn on in output short



#### Programming SOA, OTP, and MTP

## 7 **Programming SOA, OTP, and MTP**

Do the following to program the required settings in internal commands or OTP at power-up. See the XDP700-002 datasheet [1] for details.

- 1. Apply a voltage at the VDD\_RTN and VDD\_RTNS pins:
  - At least 9 V to program commands (evaluation board bias is activated at 9 V)
  - At least 20 V to program OTP or MTP
- 2. Keep the UV/EN pin at chip GND potential.
- 3. Wait for the device to enter STANDBY state. Communication via PMBus is possible now.
- 4. Program the commands, OTP, or MTP.
- *Note:* To ensure successful programming, keep the internal temperature of the device below 125°C at all times.

## 7.1 **Program OTP or MTP sections**

- 1. Program the commands in volatile memory as required.
- 2. Click the button highlighted in red as shown in Figure 45.



Figure 45 Programming tab

3. Set the program from **Registers**, select the memory section that needs to be programmed, and click **Program to OTP**, as shown in Figure 46.



#### Programming SOA, OTP, and MTP



#### Figure 46 OTP and MTP programming

The command configuration will be automatically copied to the selected memory section.



#### References

#### References

- [1] Infineon Technologies AG: XDP700-002 hot-swap controller datasheet; Available online
- [2] Infineon Technologies AG: XDP700-002 Evaluation Board webpage; Available online



## **Revision history**

## **Revision history**

Document revision	Date	Description of changes
V 1.0	2024-04-12	Initial release

#### Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2024-04-12 Published by

Infineon Technologies AG 81726 Munich, Germany

© 2024 Infineon Technologies AG. All Rights Reserved.

Do you have a question about this document? Email: erratum@infineon.com

Document reference UM012553

#### Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

# **Mouser Electronics**

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Infineon:

EVALXDP700TOBO1