

## MOSFET

### StrongIRFET™ 2 Power-Transistor, 30 V

#### Features

- Optimized for wide range of applications
- N-channel, logic level
- 100% avalanche tested
- 175°C rated
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

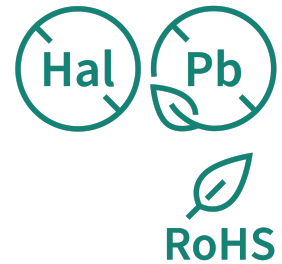
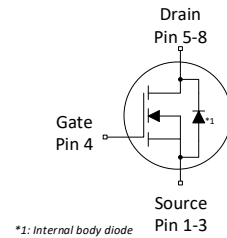
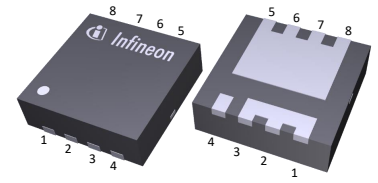
#### Product validation

Qualified according to JEDEC Standard

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	30	V
$R_{DS(on),max}$	5.6	mΩ
$I_D$	72	A
$Q_{oss}$	12	nC
$Q_G (0V..4.5V)$	7.4	nC

PG-TSDSON-8 FL



Type/Ordering Code	Package	Marking	Related Links
ISZ056N03LF2S	PG-TSDSON-8	056N03F	-



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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	72 51 16	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ , $R_{THJA}=60\text{ °C/W}^2)$
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	288	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse <sup>4)</sup>	$E_{AS}$	-	-	54 109	mJ	$I_D=20\text{ A}$ , $R_{GS}=25\text{ }\Omega$ $I_D=10\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	52 3.0	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{THJA}=50\text{ °C/W}^2)$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	175	°C	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	2.9	°C/W	-
Thermal resistance, junction - case, top	$R_{thJC}$	-	-	20	°C/W	-
Device on PCB, 6 cm <sup>2</sup> cooling area <sup>5)</sup>	$R_{thJA}$	-	-	60	°C/W	-

<sup>5)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.35	1.85	2.35	V	$V_{DS}=V_{GS}$ , $I_D=30\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=30\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=30\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	4.8 6.2	5.6 10	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=20\text{ A}$ $V_{GS}=4.5\text{ V}$ , $I_D=10\text{ A}$
Gate resistance	$R_G$	-	3.2	-	$\Omega$	-
Transconductance <sup>6)</sup>	$g_{fs}$	28	-	-	S	$ V_{DS} \geq 2 I_D $ , $R_{DS(on)max}$ , $I_D=20\text{ A}$

<sup>6)</sup> Defined by design. Not subject to production test.

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	1012	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=15\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	207	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=15\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	63	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=15\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	9.9	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=20\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	4.5	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=20\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	6.3	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=20\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	5.3	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=20\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$

**Table 6 Gate charge characteristics <sup>7)</sup>**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	3.4	-	nC	$V_{DD}=15\text{ V}$ , $I_D=20\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	1.9	-	nC	$V_{DD}=15\text{ V}$ , $I_D=20\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge	$Q_{gd}$	-	2.3	-	nC	$V_{DD}=15\text{ V}$ , $I_D=20\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	$Q_{sw}$	-	3.9	-	nC	$V_{DD}=15\text{ V}$ , $I_D=20\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total <sup>8)</sup>	$Q_g$	-	7.4	11	nC	$V_{DD}=15\text{ V}$ , $I_D=20\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$

**Table 6 Gate charge characteristics** <sup>7)</sup>

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate plateau voltage	$V_{\text{plateau}}$	-	3.3	-	V	$V_{\text{DD}}=15\text{ V}$ , $I_{\text{D}}=20\text{ A}$ , $V_{\text{GS}}=0\text{ to }4.5\text{ V}$
Gate charge total <sup>8)</sup>	$Q_{\text{g}}$	-	15	20	nC	$V_{\text{DD}}=15\text{ V}$ , $I_{\text{D}}=20\text{ A}$ , $V_{\text{GS}}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{\text{g(sync)}}$	-	6.3	-	nC	$V_{\text{DS}}=0.1\text{ V}$ , $V_{\text{GS}}=0\text{ to }4.5\text{ V}$
Output charge	$Q_{\text{oss}}$	-	12	-	nC	$V_{\text{DS}}=15\text{ V}$ , $V_{\text{GS}}=0\text{ V}$

<sup>7)</sup> See "Gate charge waveforms" for parameter definition

<sup>8)</sup> Defined by design. Not subject to production test.

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_{\text{S}}$	-	-	47	A	$T_{\text{c}}=25\text{ °C}$
Diode pulse current	$I_{\text{S,pulse}}$	-	-	288	A	$T_{\text{c}}=25\text{ °C}$
Diode forward voltage	$V_{\text{SD}}$	-	0.82	1.0	V	$V_{\text{GS}}=0\text{ V}$ , $I_{\text{F}}=20\text{ A}$ , $T_{\text{j}}=25\text{ °C}$
Reverse recovery time	$t_{\text{rr}}$	-	10	-	ns	$V_{\text{R}}=15\text{ V}$ , $I_{\text{F}}=20\text{ A}$ , $di_{\text{F}}/dt=500\text{ A}/\mu\text{s}$
Reverse recovery charge	$Q_{\text{rr}}$	-	15	-	nC	$V_{\text{R}}=15\text{ V}$ , $I_{\text{F}}=20\text{ A}$ , $di_{\text{F}}/dt=500\text{ A}/\mu\text{s}$

## 4 Electrical characteristics diagrams

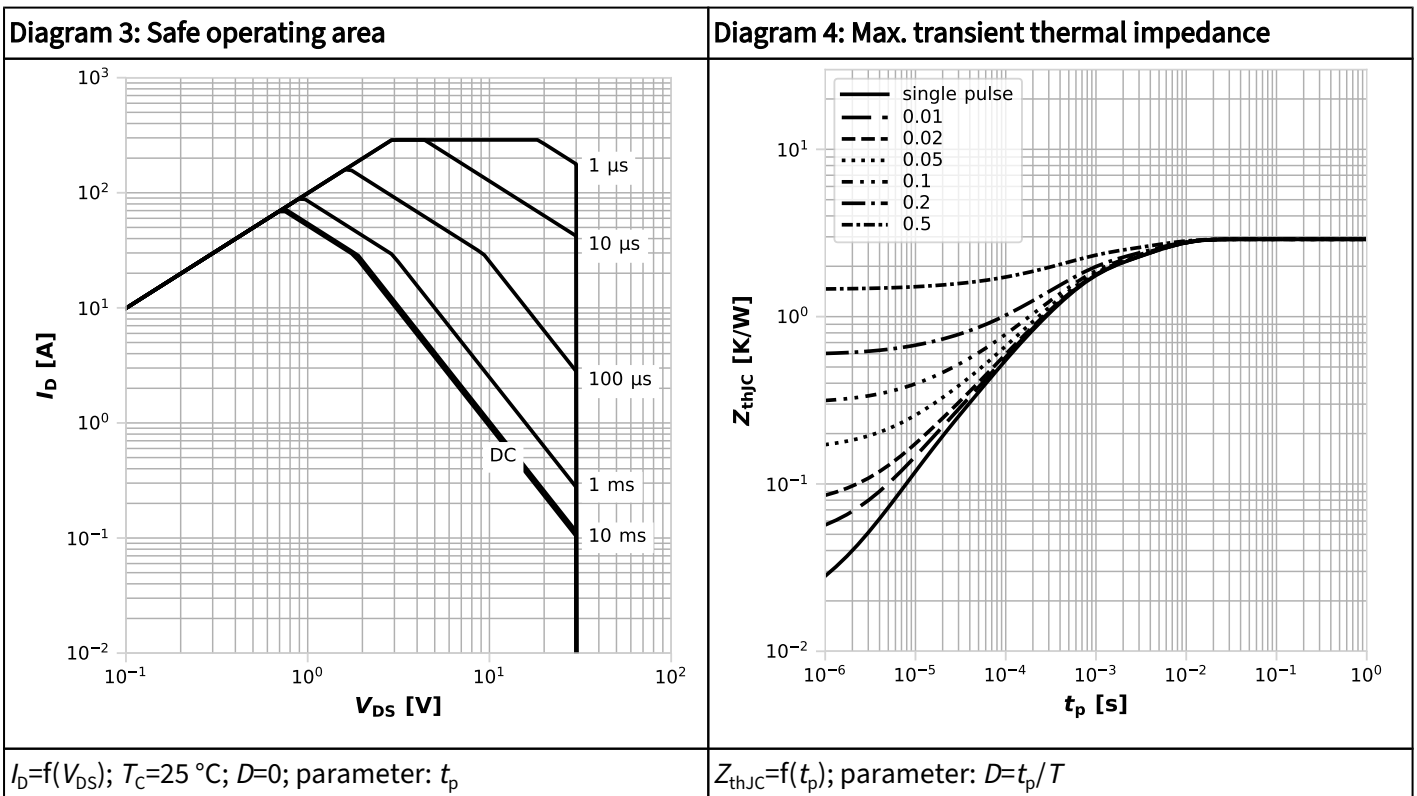
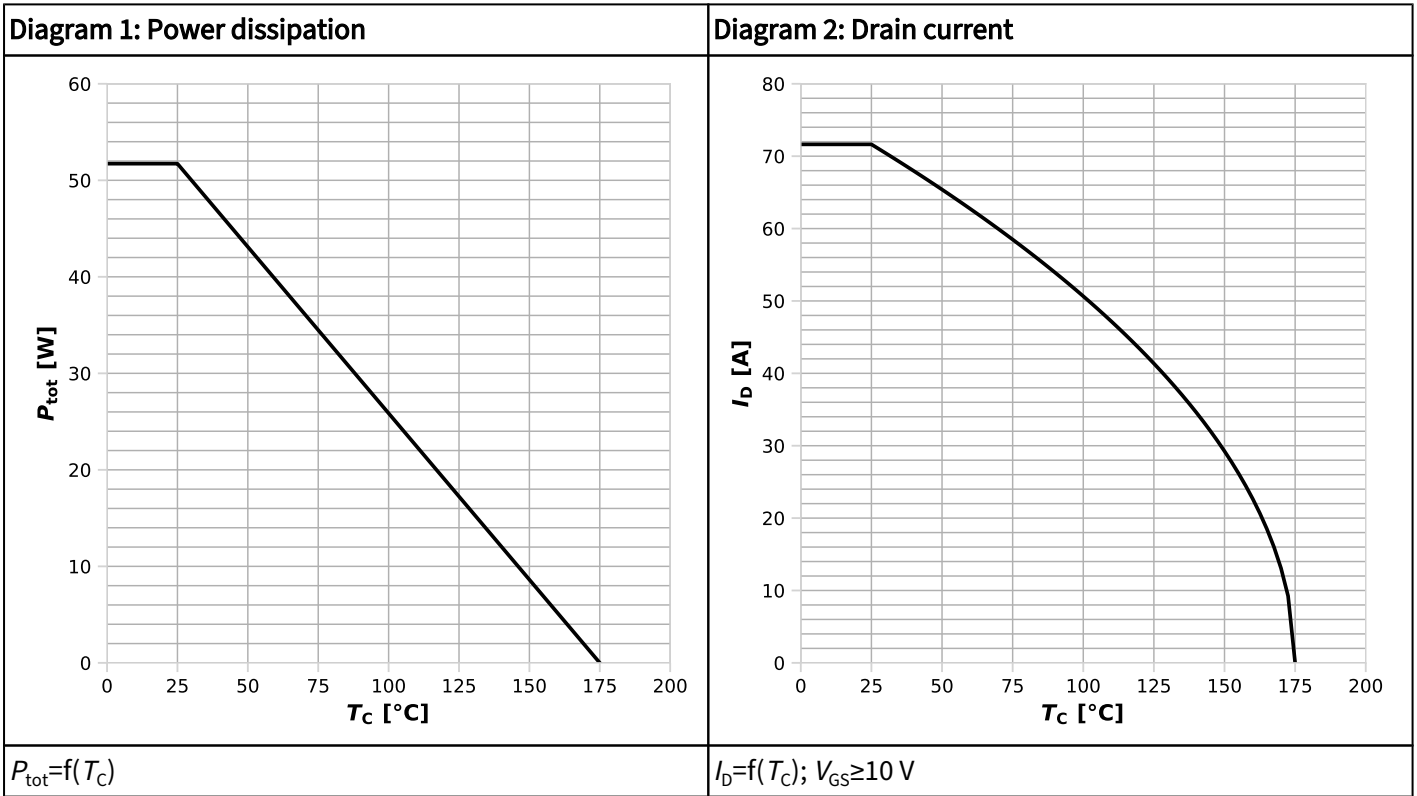


Diagram 5: Typ. output characteristics

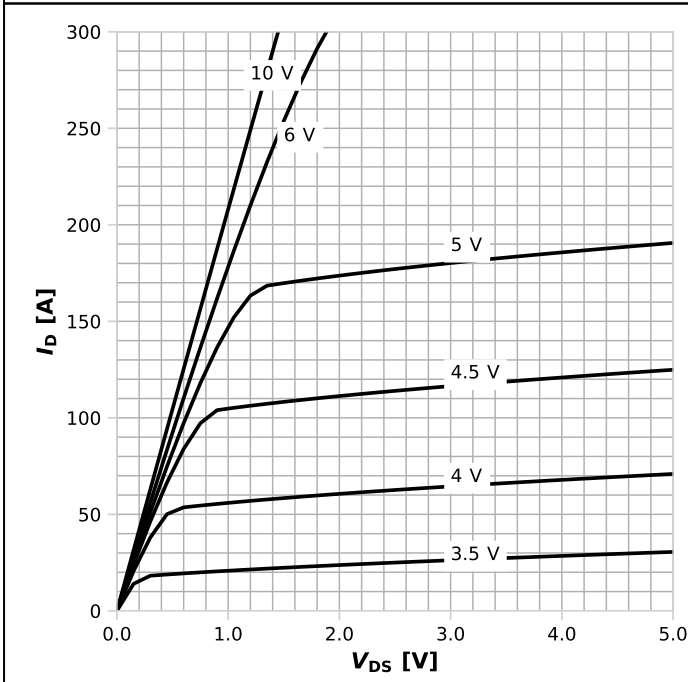

 $I_D = f(V_{DS}), T_j = 25\text{ °C}; \text{parameter: } V_{GS}$ 

Diagram 6: Typ. drain-source on resistance

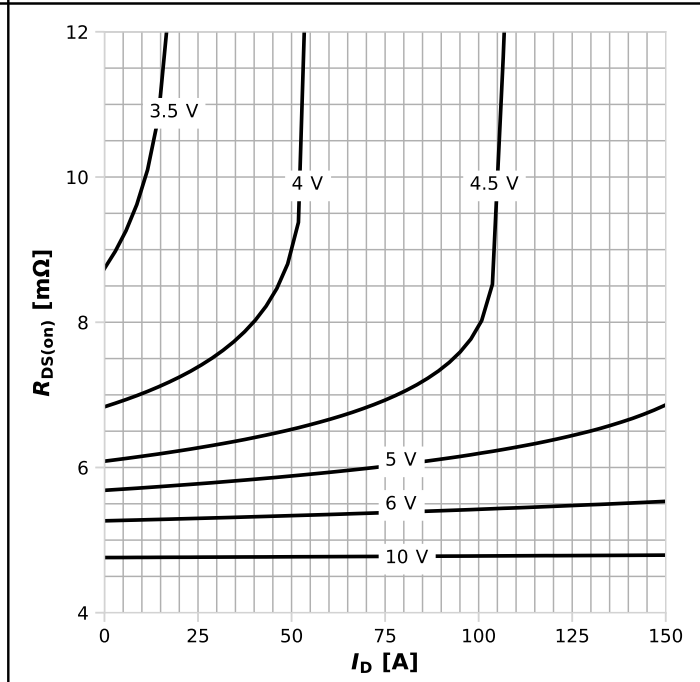

 $R_{DS(on)} = f(I_D), T_j = 25\text{ °C}; \text{parameter: } V_{GS}$ 

Diagram 7: Typ. transfer characteristics

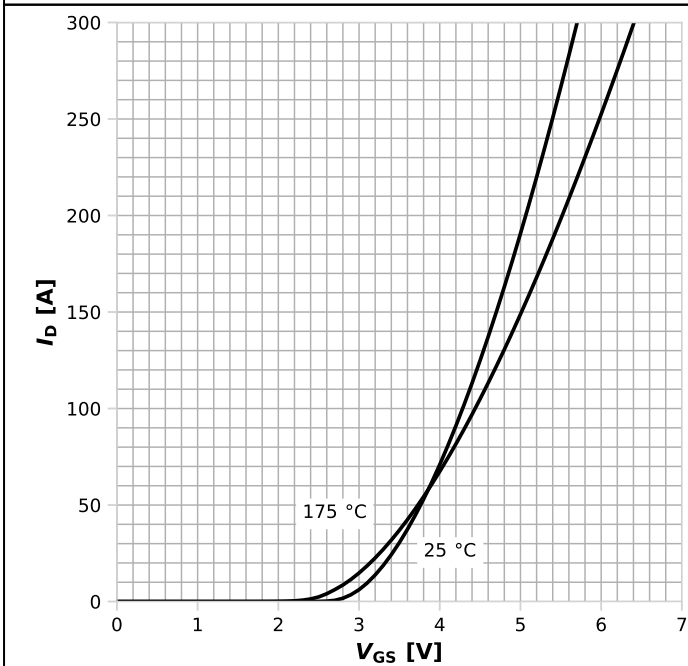

 $I_D = f(V_{GS}), |V_{DS}| > 2|I_D|R_{DS(on)max}; \text{parameter: } T_j$ 

Diagram 8: Typ. drain-source on resistance

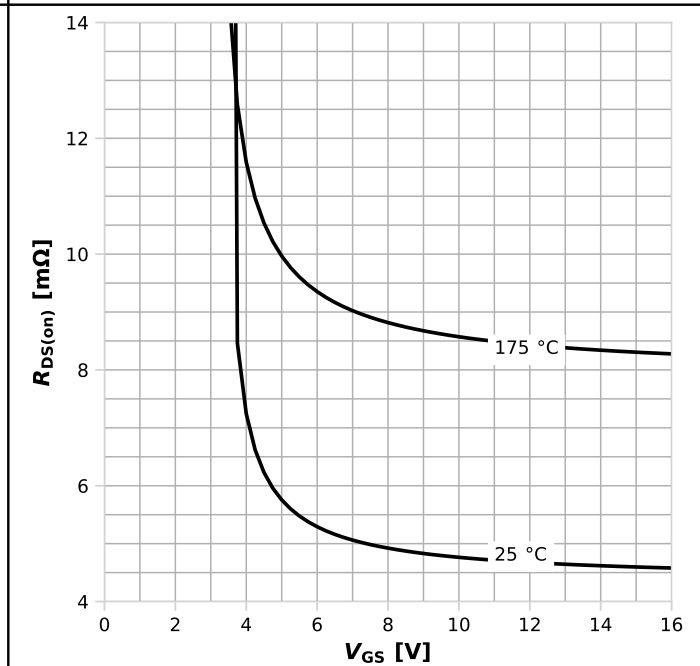
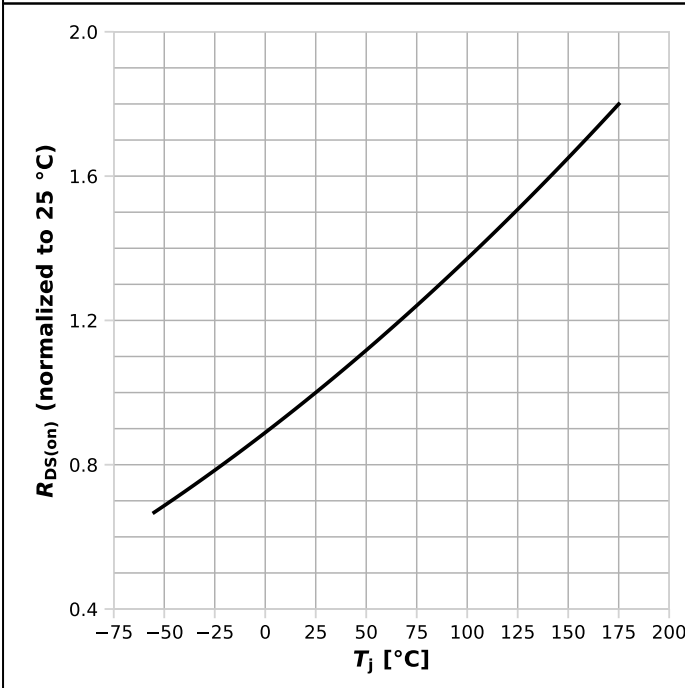

 $R_{DS(on)} = f(V_{GS}), I_D = 20\text{ A}; \text{parameter: } T_j$

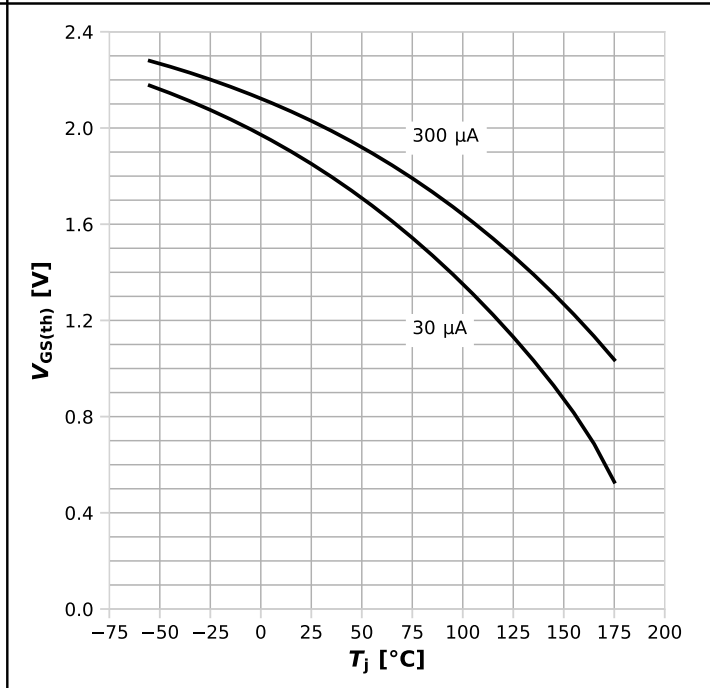


Diagram 9: Normalized drain-source on resistance



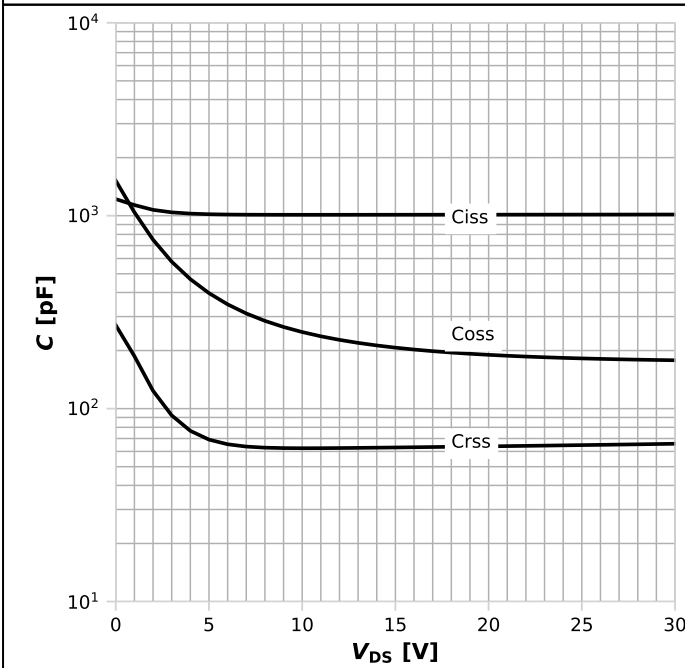
$R_{DS(on)}=f(T_j), I_D=20\text{ A}, V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



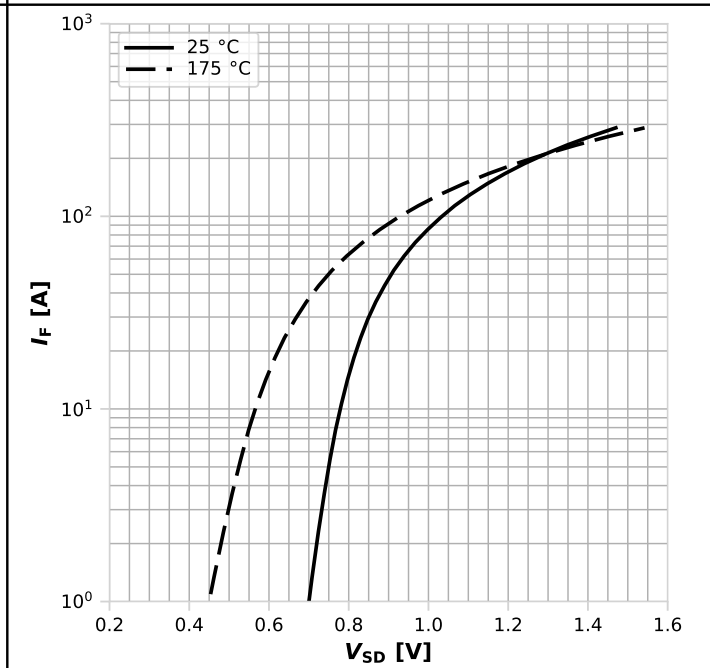
$V_{GS(th)}=f(T_j), V_{GS}=V_{DS}; \text{parameter: } I_D$

Diagram 11: Typ. capacitances



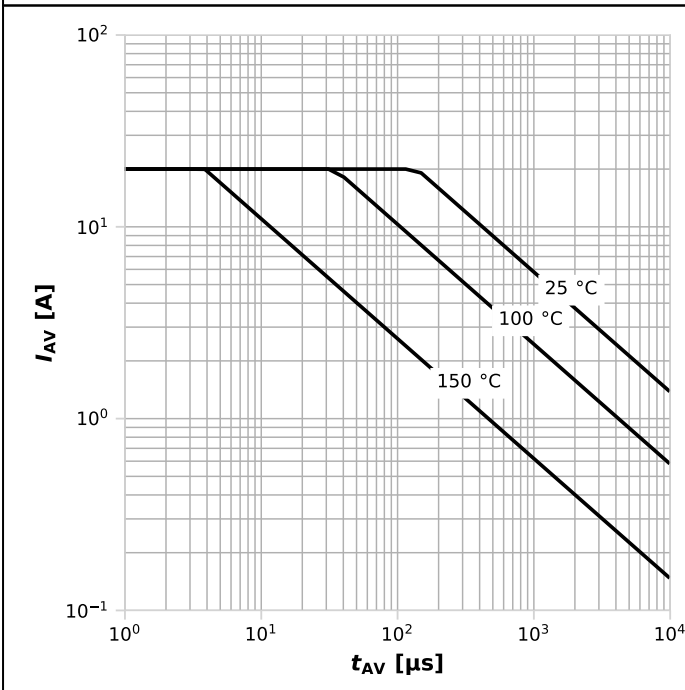
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



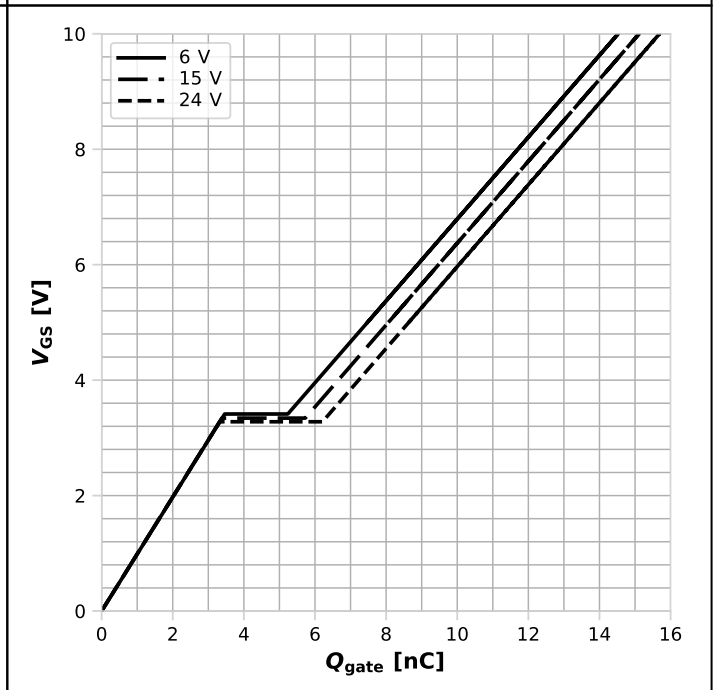
$I_F=f(V_{SD}); \text{parameter: } T_j$

Diagram 13: Avalanche characteristics



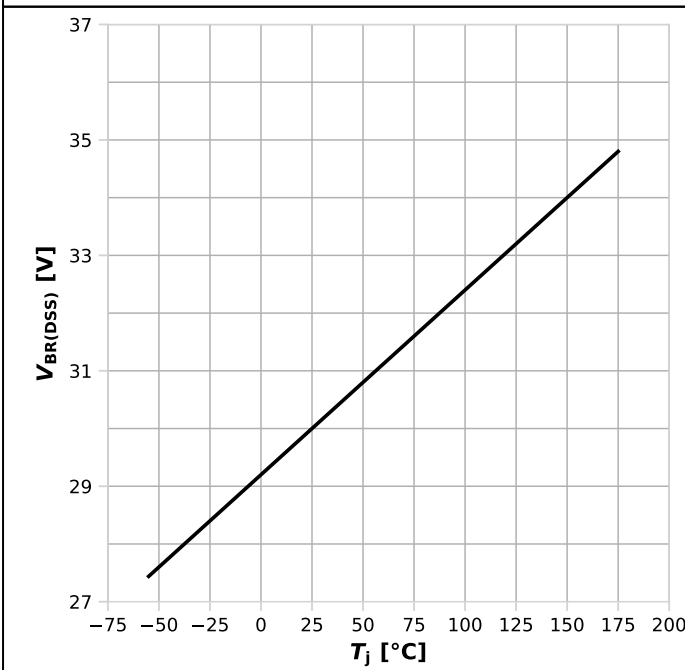
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j,start}$

Diagram 14: Typ. gate charge



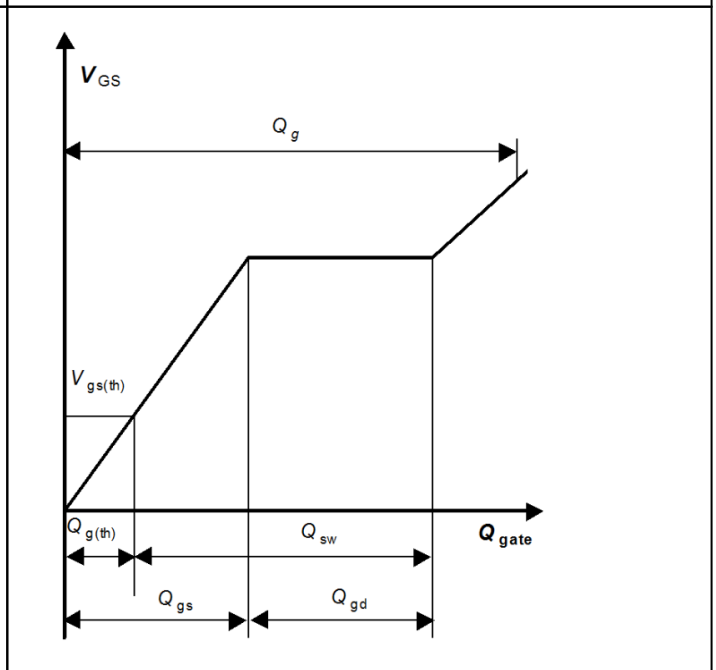
$V_{GS}=f(Q_{gate}), I_D=20$  A pulsed,  $T_j=25$  °C; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage



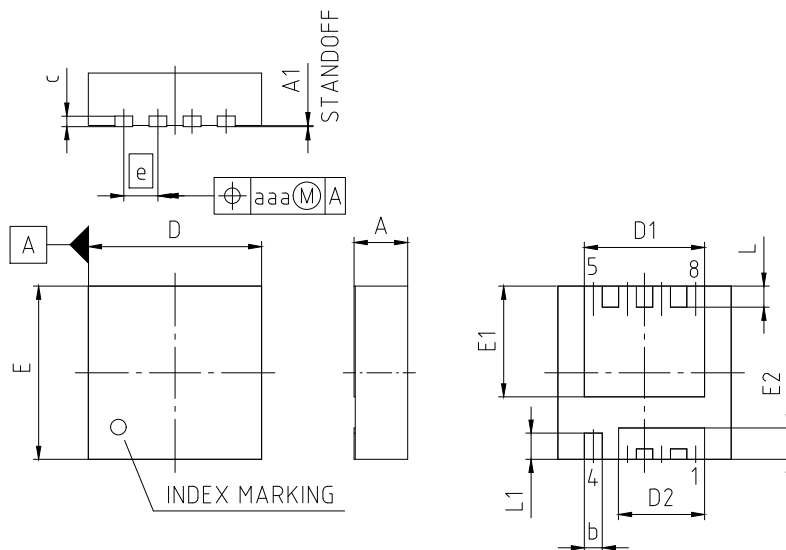
$V_{BR(DSS)}=f(T_j); I_D=1$  mA

Gate charge waveforms



-

## 5 Package Outlines



PACKAGE - GROUP NUMBER: <b>PG-TSDSON-8-U03</b>		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
<b>A</b>	0.90	1.10
<b>A1</b>	0	0.05
<b>b</b>	0.24	0.44
<b>c</b>	0.10	0.30
<b>D</b>	3.20	3.40
<b>D1</b>	2.19	2.39
<b>D2</b>	1.54	1.74
<b>E</b>	3.20	3.40
<b>E1</b>	2.01	2.21
<b>E2</b>	0.50	0.70
<b>e</b>	0.65	
<b>L</b>	0.30	0.50
<b>L1</b>	0.40	0.60
<b>aaa</b>	0.06	
<b>N</b>	8	

NOTE:  
 DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

**Figure 1 Outline PG-TSDSON-8, dimensions in mm**

## Revision History

ISZ056N03LF2S

### Revision 2024-10-12, Rev. 1.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2024-10-12	Release of final

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