

MOSFET

OptiMOS™ 3 Power-Transistor, 40 V

Features

- Dual N-channel, logic level
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified according to JEDEC Standard

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on),max}$	17	mΩ
I_D	9.6	A
Q_{oss}	7.8	nC
Q_G	6.0	nC

Type/Ordering Code	Package	Marking	Related Links
ISA170170N04LMDS	PG-DSO-8	1717N04L	-

PG-DSO-8

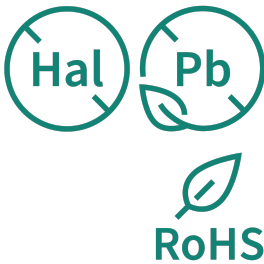
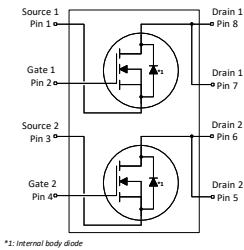
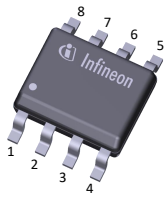




Table of Contents

Description 1

Maximum ratings 3

Thermal characteristics 4

Electrical characteristics 5

Electrical characteristics diagrams 7

Package Outlines 11

Revision History 12

Trademarks 12

Disclaimer 12

1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	9.6 6.1 5.2 7.2	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=4.5\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=90\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	38	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	36	mJ	$I_D=9.6\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	2.5 1.4	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=90\text{ °C/W}$ ²⁾
Operating and storage temperature	T_j , T_{stg}	-55	-	150	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - solder point	R_{thJC}	-	-	50	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}	-	-	90	°C/W	-
Thermal resistance, junction - ambient, minimum footprint	R_{thJA}	-	-	150	°C/W	-

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.1	-	2.7	V	$V_{DS}=V_{GS}$, $I_D=1000\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	13 18	17 23.6	m Ω	$V_{GS}=10\text{ V}$, $I_D=9.6\text{ A}$ $V_{GS}=4.5\text{ V}$, $I_D=8.5\text{ A}$
Gate resistance	R_G	-	1.1	-	Ω	-
Transconductance ⁶⁾	g_{fs}	12	25	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=9.6\text{ A}$

⁶⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance ⁷⁾	C_{iss}	-	880	1100	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Output capacitance ⁷⁾	C_{oss}	-	220	290	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ⁷⁾	C_{rss}	-	15	26	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	6.7	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=9.6\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	5.0	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=9.6\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	4.6	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=9.6\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	4.0	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=9.6\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

⁷⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics ⁸⁾

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	2.7	-	nC	$V_{DD}=20\text{ V}$, $I_D=9.6\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	1.5	-	nC	$V_{DD}=20\text{ V}$, $I_D=9.6\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge	Q_{gd}	-	1.6	-	nC	$V_{DD}=20\text{ V}$, $I_D=9.6\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	Q_{sw}	-	2.8	-	nC	$V_{DD}=20\text{ V}$, $I_D=9.6\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ⁹⁾	Q_g	-	6.0	9.0	nC	$V_{DD}=20\text{ V}$, $I_D=9.6\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	3.1	-	V	$V_{DD}=20\text{ V}$, $I_D=9.6\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ⁹⁾	Q_g	-	13	19.5	nC	$V_{DD}=20\text{ V}$, $I_D=9.6\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	7.8	-	nC	$V_{DS}=20\text{ V}$, $V_{GS}=0\text{ V}$

⁸⁾ See "Gate charge waveforms" for parameter definition

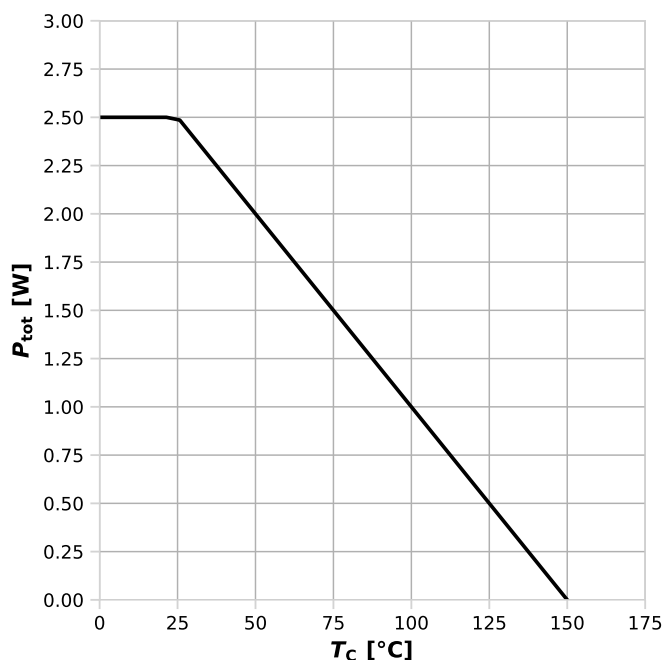
⁹⁾ Defined by design. Not subject to production test.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	3.1	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	38	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.86	1.0	V	$V_{GS}=0\text{ V}$, $I_F=9.6\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	13	-	ns	$V_R=20\text{ V}$, $I_F=9.6\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	4.3	-	nC	$V_R=20\text{ V}$, $I_F=9.6\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$

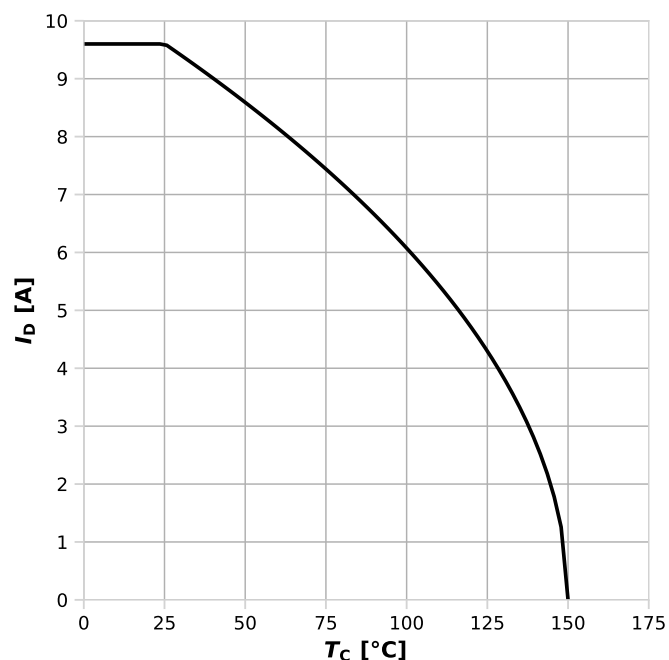
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



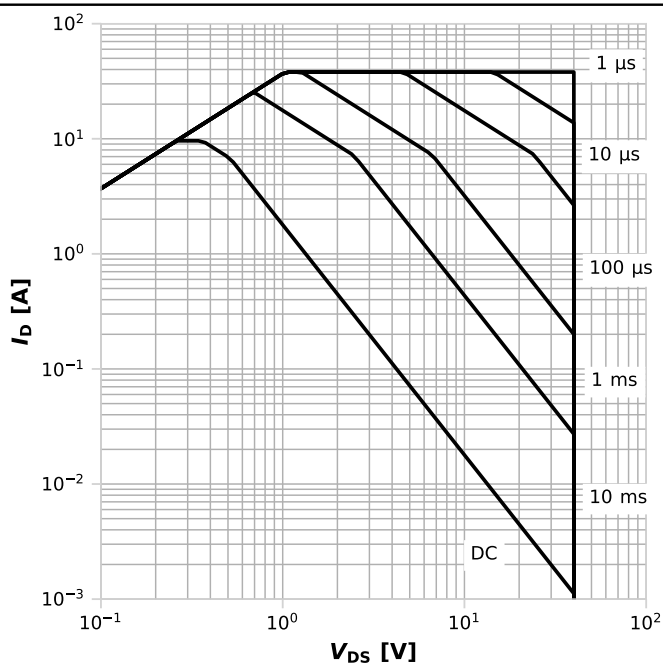
$$P_{tot}=f(T_c)$$

Diagram 2: Drain current



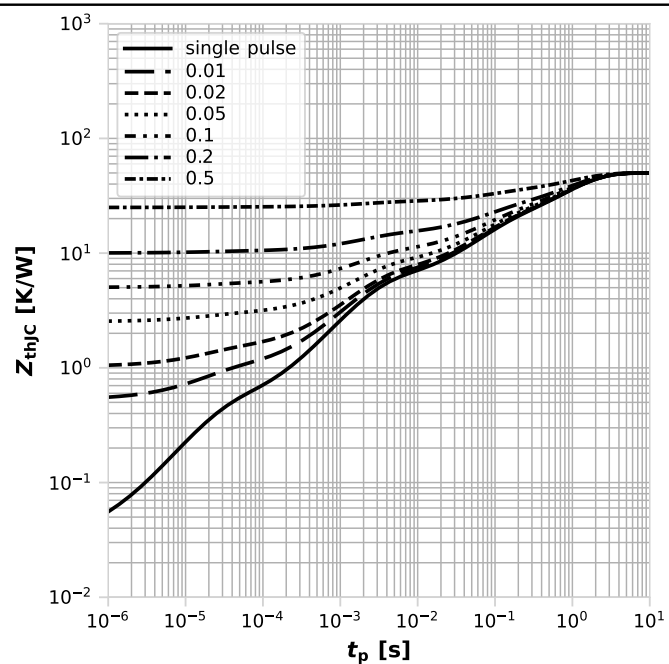
$$I_D=f(T_c); V_{GS}\geq 10\text{ V}$$

Diagram 3: Safe operating area



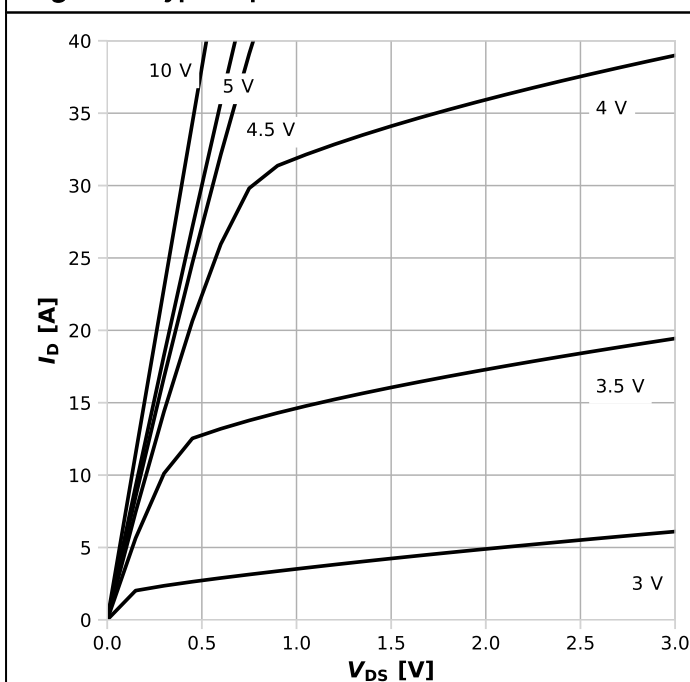
$$I_D=f(V_{DS}); T_c=25\text{ °C}; D=0; \text{parameter: } t_p$$

Diagram 4: Max. transient thermal impedance



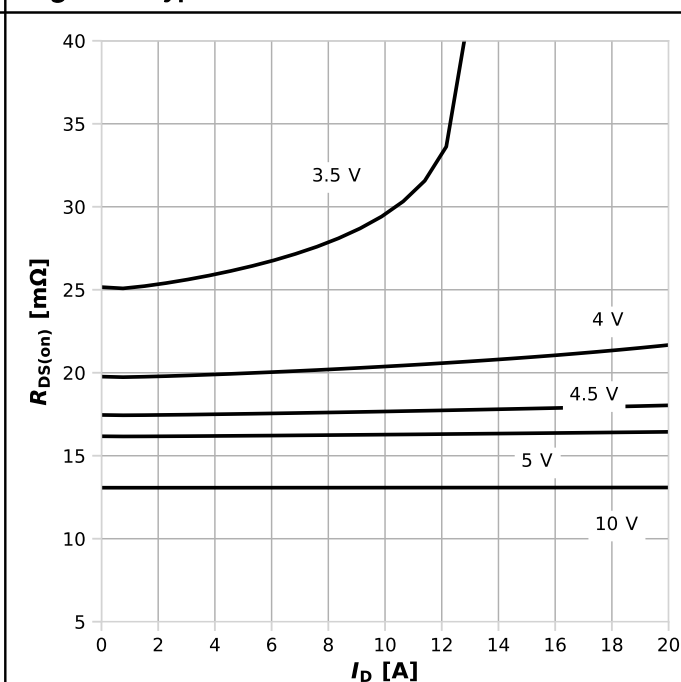
$$Z_{thJC}=f(t_p); \text{parameter: } D=t_p/T$$

Diagram 5: Typ. output characteristics



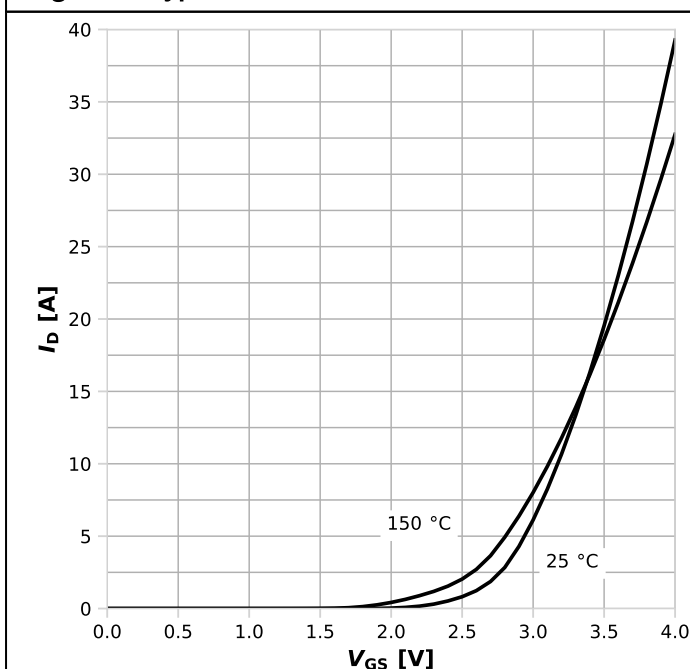
$I_D = f(V_{DS}), T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. drain-source on resistance



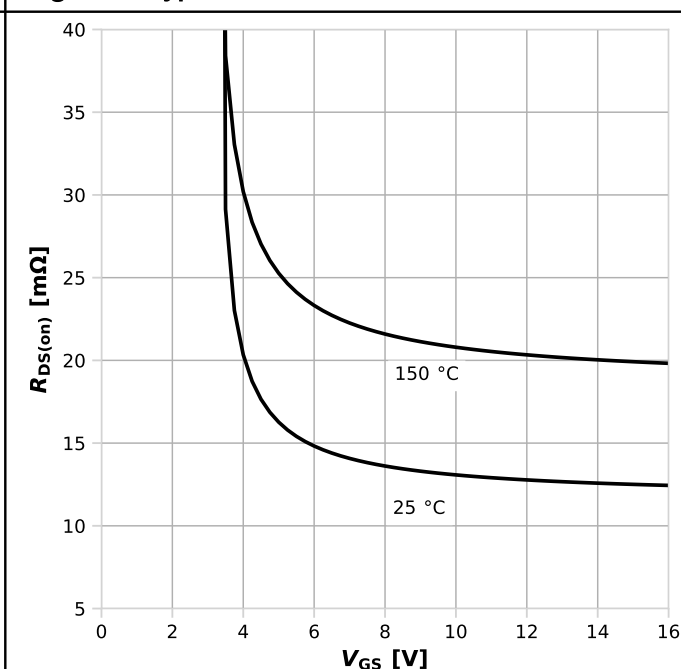
$R_{DS(on)} = f(I_D), T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. transfer characteristics



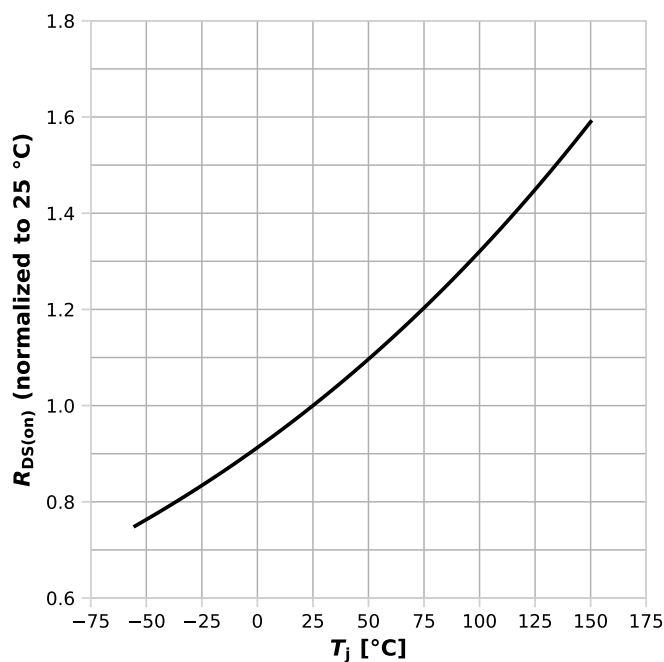
$I_D = f(V_{GS}), |V_{DS}| > 2|I_D|R_{DS(on)\max}; \text{parameter: } T_j$

Diagram 8: Typ. drain-source on resistance



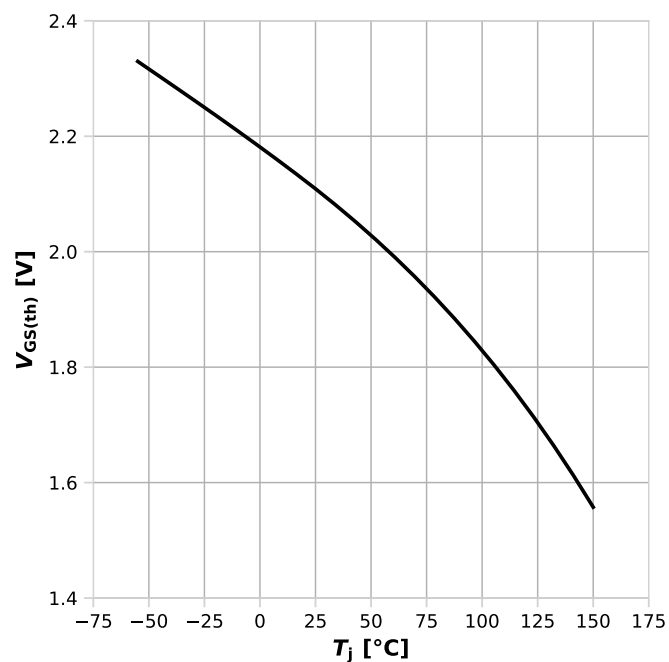
$R_{DS(on)} = f(V_{GS}), I_D = 9.6 \text{ A}; \text{parameter: } T_j$

Diagram 9: Normalized drain-source on resistance



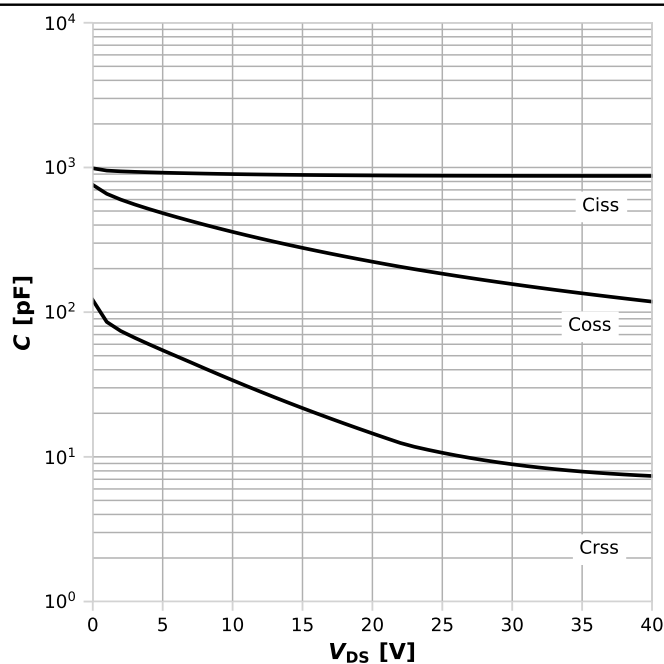
$R_{DS(on)} = f(T_j)$, $I_D = 9.6$ A, $V_{GS} = 10$ V

Diagram 10: Typ. gate threshold voltage



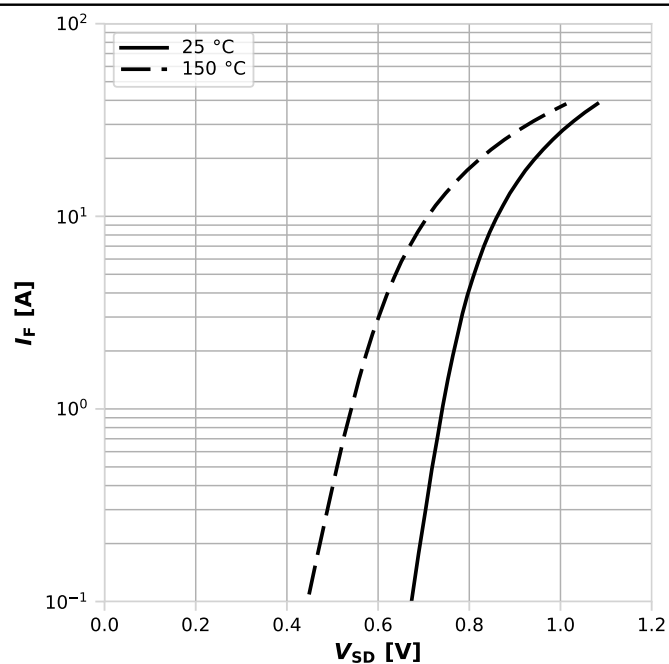
$V_{GS(th)} = f(T_j)$, $V_{GS} = V_{DS}$; parameter: $I_D = 1000 \mu A$

Diagram 11: Typ. capacitances



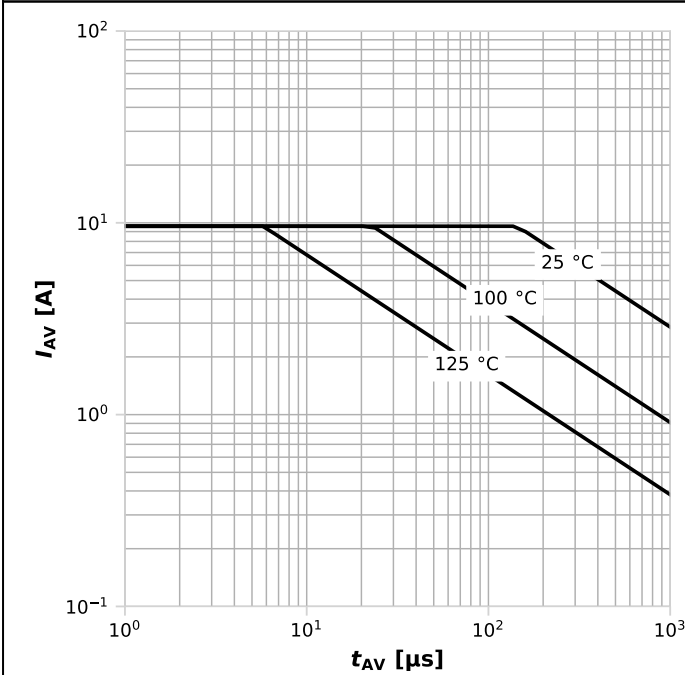
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

Diagram 12: Forward characteristics of reverse diode



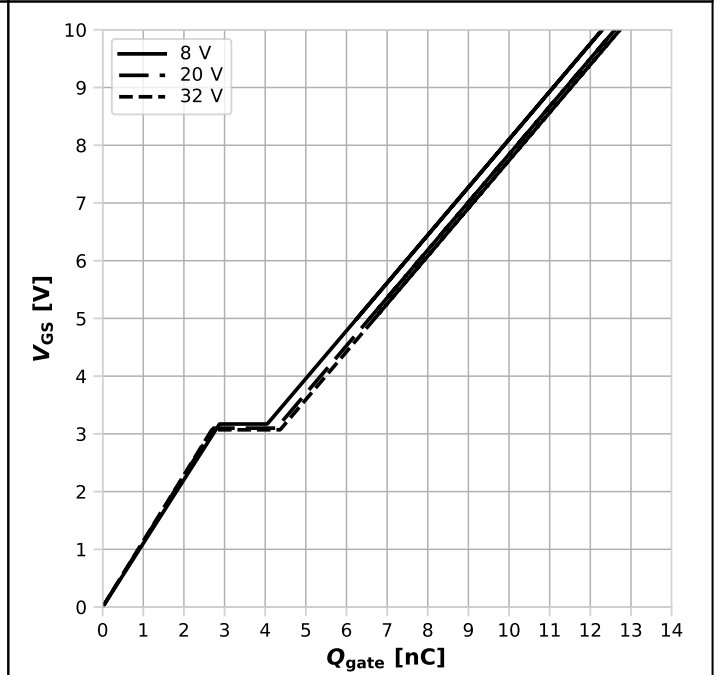
$I_F = f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



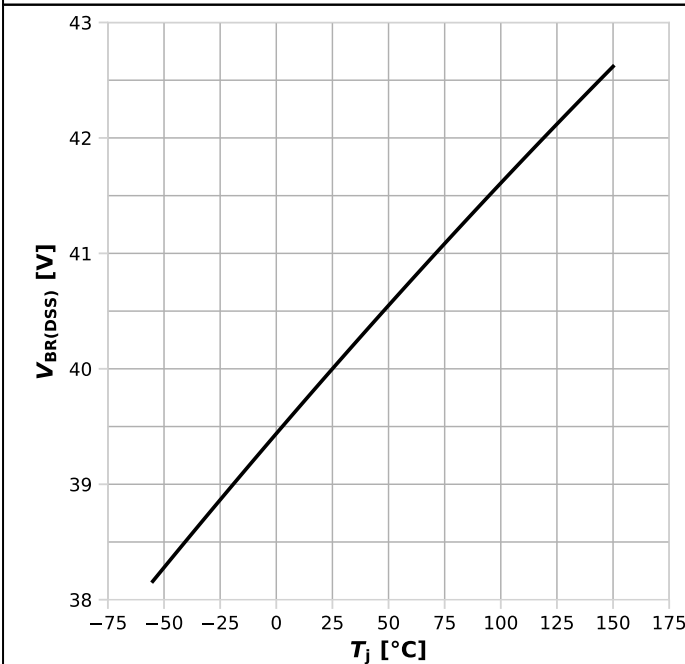
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



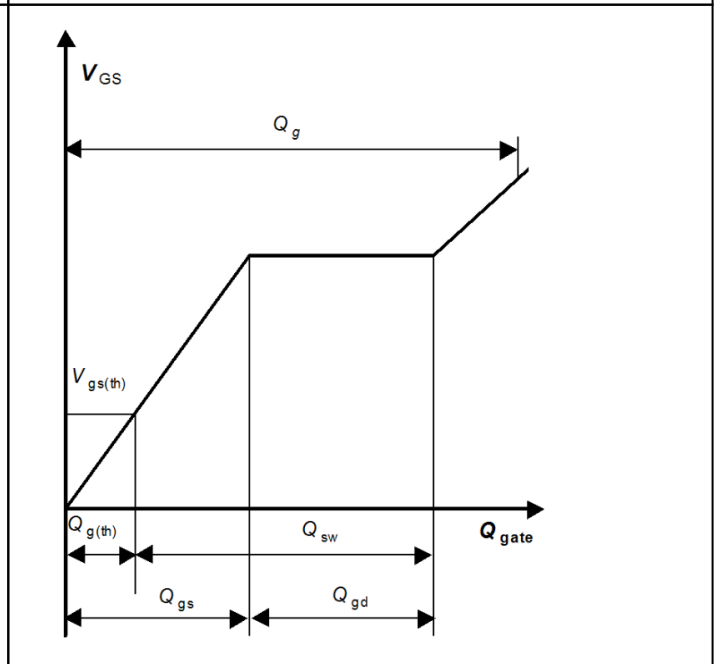
$V_{GS}=f(Q_{gate})$, $I_D=9.6\text{ A}$ pulsed, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



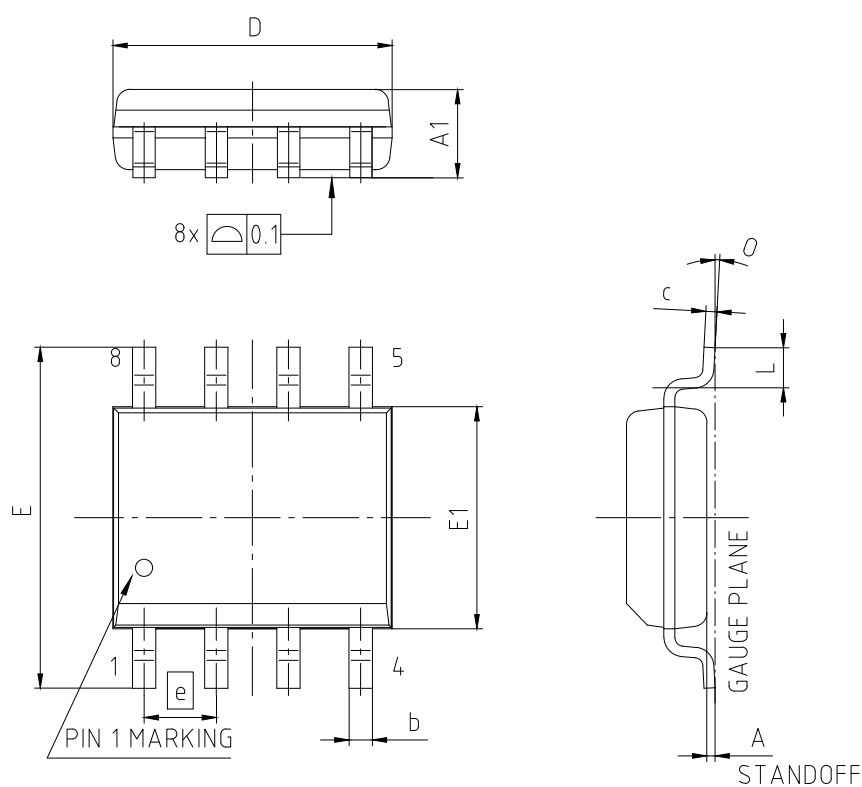
$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Gate charge waveforms



-

5 Package Outlines



PACKAGE - GROUP NUMBER: PG-DSO-8-U02		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.18	0.25
A1	1.35	1.75
b	0.38	0.51
c	0.254	
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
e	1.27	
L	0.48	0.91
O	4°	
N	8	

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-DSO-8, dimensions in mm

Revision History

ISA170170N04LMDS

Revision 2024-10-02, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2024-10-02	Release of final datasheet

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