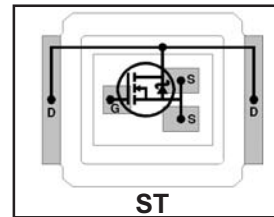


IRF6623PbF IRF6623TRPbF

DirectFET™ Power MOSFET ⑩

- RoHS Compliant ⑨
- Lead-Free (Qualified up to 260°C Reflow)
- Application Specific MOSFETs
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- High Cdv/dt Immunity
- Low Profile (<0.7mm)
- Dual Sided Cooling Compatible ⑨
- Compatible with existing Surface Mount Techniques ⑨

| V _{DSS} | R _{DS(on)} max | Qg(typ.) |
|------------------|--------------------------------|----------|
| 20V | 5.7mΩ @ V _{GS} = 10V | 11nC |
| | 9.7mΩ @ V _{GS} = 4.5V | |



Applicable DirectFET Outline and Substrate Outline (see p.8,9 for details)

| | | | | | | | | | | |
|----|----|-----------|--|----|----|----|--|--|--|--|
| SQ | SX | ST | | MQ | MX | MT | | | | |
|----|----|-----------|--|----|----|----|--|--|--|--|

Description

The IRF6623PbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of a MICRO-8 and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

The IRF6623PbF balances both low resistance and low charge along with ultra low package inductance to reduce both conduction and switching losses. The reduced total losses make this product ideal for high efficiency DC-DC converters that power the latest generation of processors operating at higher frequencies. The IRF6623PbF has been optimized for parameters that are critical in synchronous buck operating from 12 volt bus converters including Rds(on) and gate charge to minimize losses in the control FET socket.

Absolute Maximum Ratings

| | Parameter | Max. | Units |
|--|---|--------------|-------|
| V _{DS} | Drain-to-Source Voltage | 20 | V |
| V _{GS} | Gate-to-Source Voltage | ±20 | |
| I _D @ T _C = 25°C | Continuous Drain Current, V _{GS} @ 10V ⑦ | 55 | A |
| I _D @ T _A = 25°C | Continuous Drain Current, V _{GS} @ 10V ④ | 16 | |
| I _D @ T _A = 70°C | Continuous Drain Current, V _{GS} @ 10V ④ | 13 | |
| I _{DM} | Pulsed Drain Current ① | 120 | |
| P _D @ T _C = 25°C | Power Dissipation ⑦ | 42 | W |
| P _D @ T _A = 25°C | Power Dissipation ④ | 1.4 | |
| P _D @ T _A = 70°C | Power Dissipation ④ | 2.1 | |
| E _{AS} | Single Pulse Avalanche Energy ② | 43 | mJ |
| I _{AR} | Avalanche Current ① | 40 | A |
| | Linear Derating Factor | 0.017 | W/°C |
| T _J | Operating Junction and | -40 to + 150 | °C |
| T _{STG} | Storage Temperature Range | | |

Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|---------------------|-------------------------|------|------|-------|
| R _{θJA} | Junction-to-Ambient ④⑧ | — | 58 | °C/W |
| R _{θJA} | Junction-to-Ambient ⑤⑧ | 12.5 | — | |
| R _{θJA} | Junction-to-Ambient ⑥⑧ | 20 | — | |
| R _{θJC} | Junction-to-Case ⑦⑧ | — | 3.0 | |
| R _{θJ-PCB} | Junction-to-PCB Mounted | 1.0 | — | |

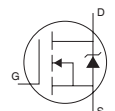
Notes ① through ⑩ are on page 2

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|--------------------------------|--------------------------------------|------|------|------|-------|--|
| BV_{DSS} | Drain-to-Source Breakdown Voltage | 20 | — | — | V | $V_{GS} = 0V, I_D = 250\mu A$ |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 15 | — | mV/°C | Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | 4.4 | 5.7 | mΩ | $V_{GS} = 10V, I_D = 15A$ ③ |
| | | — | 7.5 | 9.7 | | $V_{GS} = 4.5V, I_D = 12A$ ③ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.4 | — | 2.2 | V | $V_{DS} = V_{GS}, I_D = 250\mu A$ |
| $\Delta V_{GS(th)}/\Delta T_J$ | Gate Threshold Voltage Coefficient | — | -5.4 | — | mV/°C | |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | 1.0 | μA | $V_{DS} = 16V, V_{GS} = 0V$ |
| | | — | — | 150 | | $V_{DS} = 16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS} = 20V$ |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS} = -20V$ |
| g_{fs} | Forward Transconductance | 34 | — | — | S | $V_{DS} = 10V, I_D = 12A$ |
| Q_g | Total Gate Charge | — | 11 | 17 | nC | $V_{DS} = 10V$ $V_{GS} = 4.5V$ $I_D = 12A$ See Fig. 16 |
| Q_{gs1} | Pre-Vth Gate-to-Source Charge | — | 3.3 | — | | |
| Q_{gs2} | Post-Vth Gate-to-Source Charge | — | 1.2 | — | | |
| Q_{gd} | Gate-to-Drain Charge | — | 4.0 | — | | |
| Q_{godr} | Gate Charge Overdrive | — | 2.5 | — | | |
| Q_{sw} | Switch Charge ($Q_{gs2} + Q_{gd}$) | — | 5.2 | — | | |
| Q_{oss} | Output Charge | — | 8.9 | — | nC | $V_{DS} = 10V, V_{GS} = 0V$ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 9.7 | — | ns | $V_{DD} = 16V, V_{GS} = 4.5V$ ③ $I_D = 12A$ Clamped Inductive Load |
| t_r | Rise Time | — | 40 | — | | |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 12 | — | | |
| t_f | Fall Time | — | 4.5 | — | | |
| C_{iss} | Input Capacitance | — | 1360 | — | pF | $V_{GS} = 0V$ $V_{DS} = 10V$ $f = 1.0\text{MHz}$ |
| C_{oss} | Output Capacitance | — | 630 | — | | |
| C_{rss} | Reverse Transfer Capacitance | — | 240 | — | | |

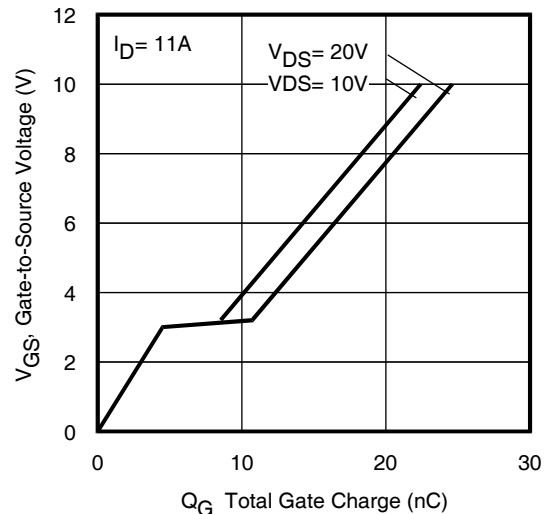
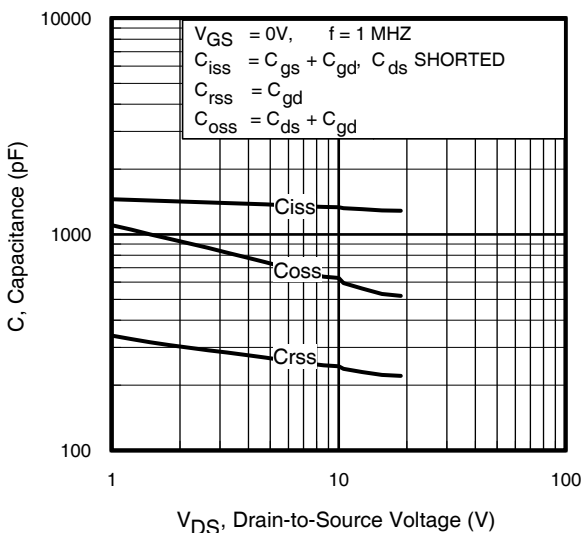
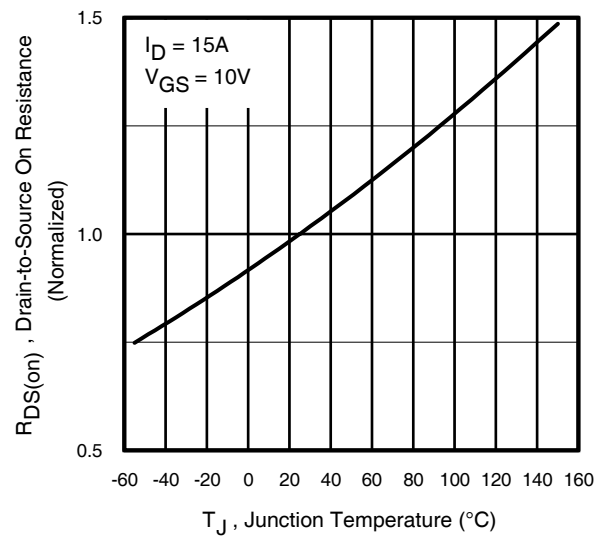
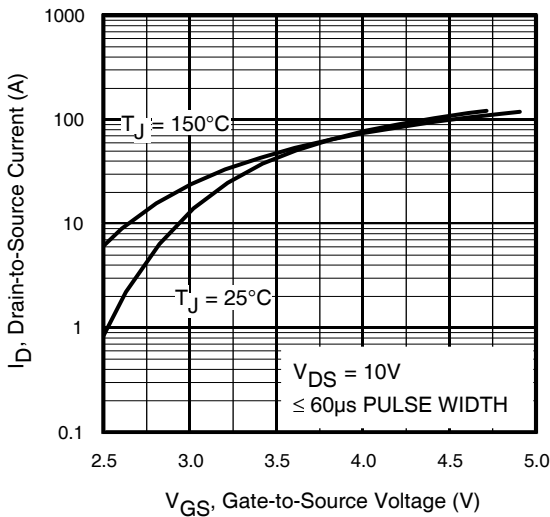
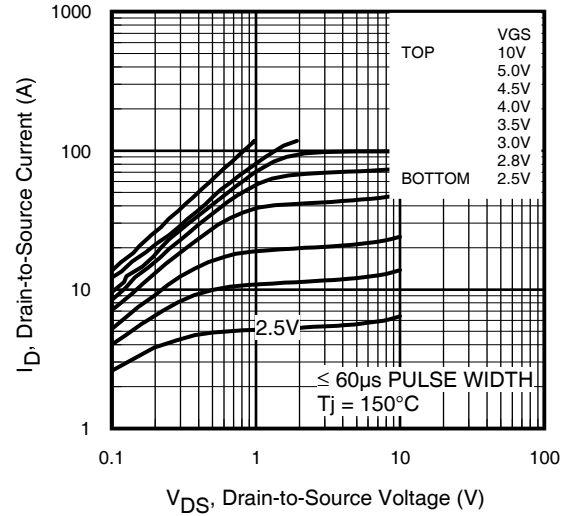
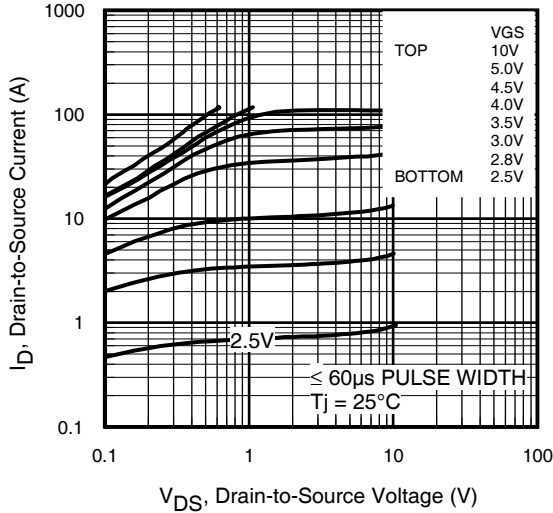
Diode Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------|---|------|------|------|-------|---|
| I_S | Continuous Source Current (Body Diode) | — | — | 53 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| I_{SM} | Pulsed Source Current (Body Diode) ① | — | — | 120 | | |
| V_{SD} | Diode Forward Voltage | — | 0.81 | 1.0 | V | $T_J = 25^\circ\text{C}, I_S = 12A, V_{GS} = 0V$ ③ |
| t_{rr} | Reverse Recovery Time | — | 20 | 30 | ns | $T_J = 25^\circ\text{C}, I_F = 12A$ |
| Q_{rr} | Reverse Recovery Charge | — | 12 | 18 | nC | $di/dt = 100A/\mu s$ ③ |



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}, L = 0.61\text{mH}, R_G = 25\Omega, I_{AS} = 12A$.
- ③ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ④ Surface mounted on 1 in. square Cu board.
- ⑤ Used double sided cooling, mounting pad.
- ⑥ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ⑦ T_C measured with thermal couple mounted to top (Drain) of part.
- ⑧ R_θ is measured at T_J of approximately 90°C .
- ⑨ Click on this section to link to the appropriate technical paper.
- ⑩ Click on this section to link to the DirectFET Website.



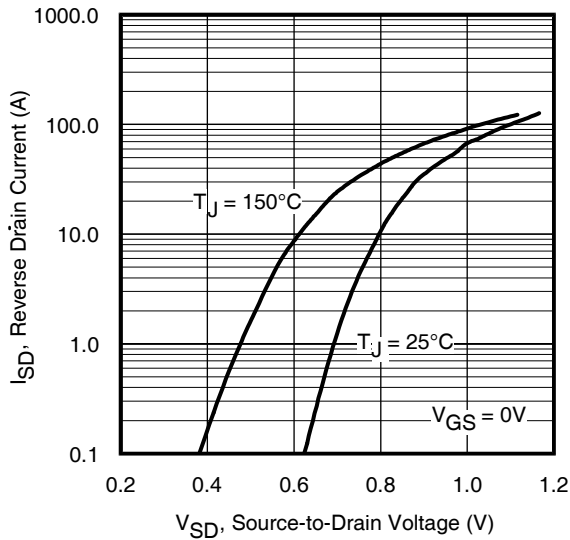


Fig 7. Typical Source-Drain Diode Forward Voltage

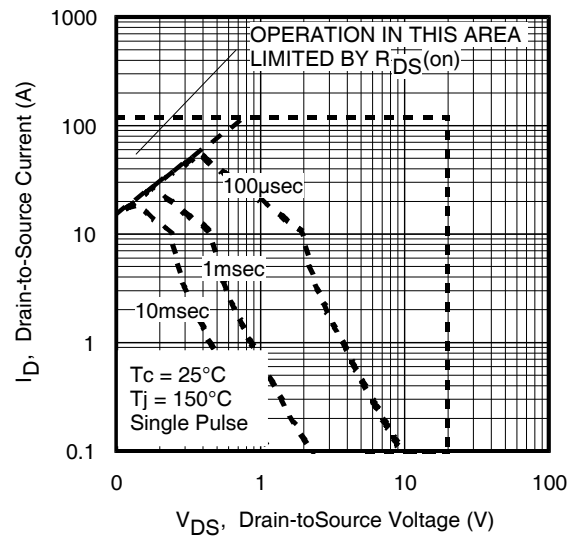


Fig 8. Maximum Safe Operating Area

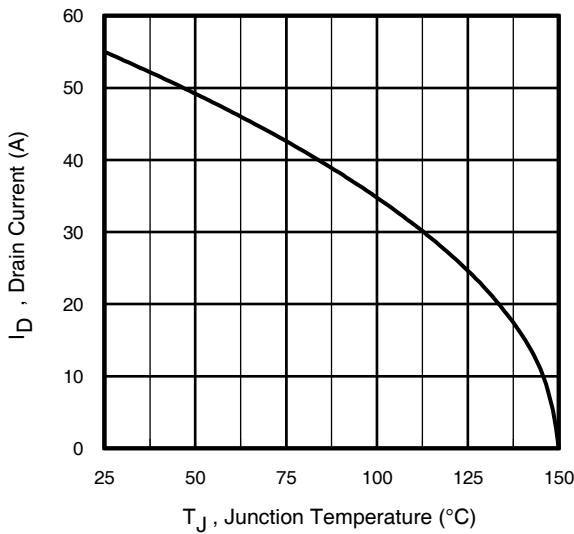


Fig 9. Maximum Drain Current vs. Case Temperature

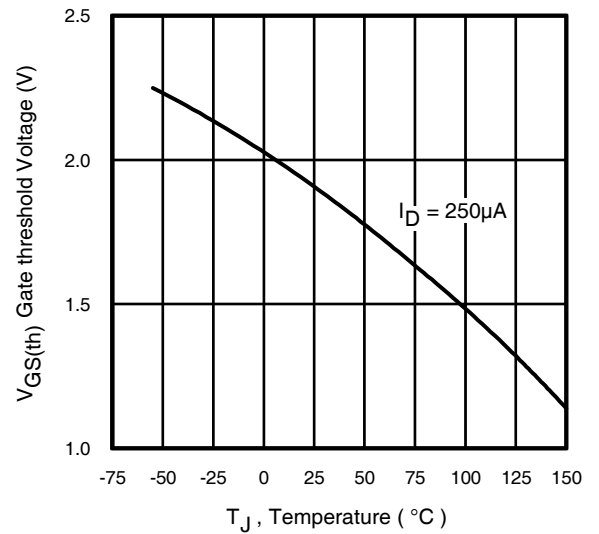


Fig 10. Threshold Voltage vs. Temperature

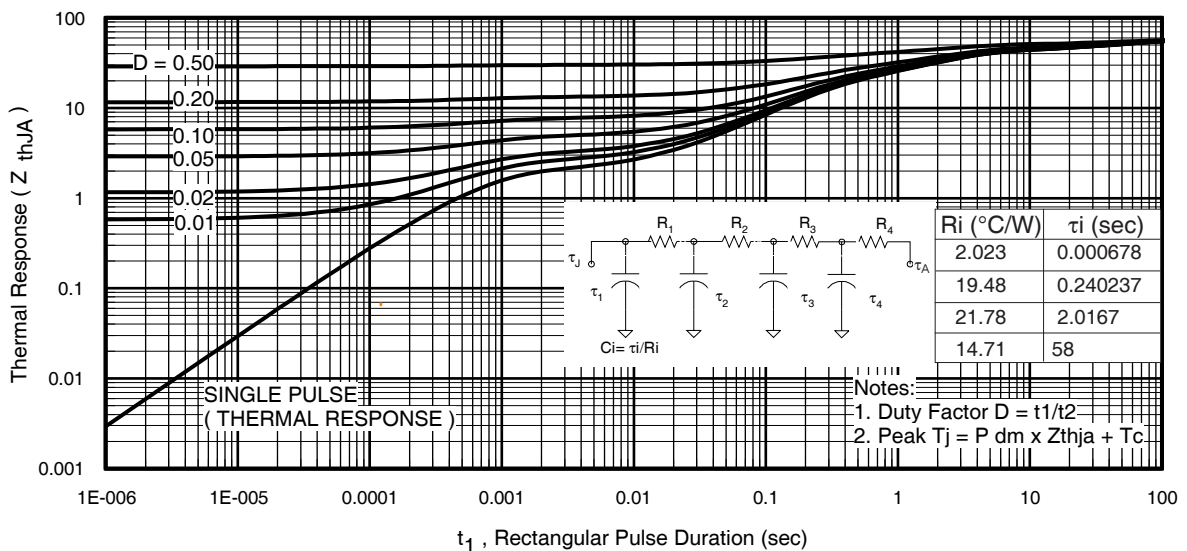


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

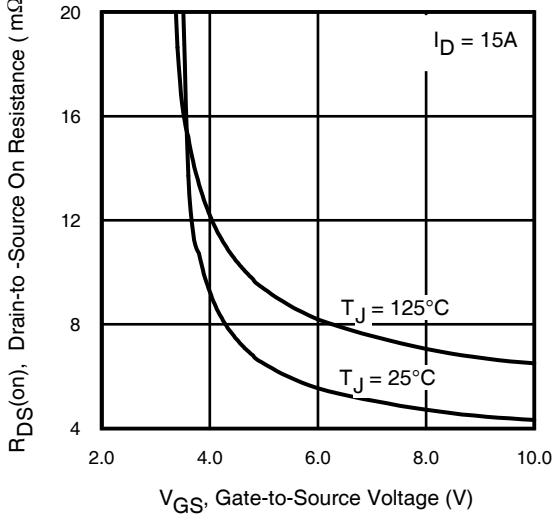


Fig 12. On-Resistance Vs. Gate Voltage

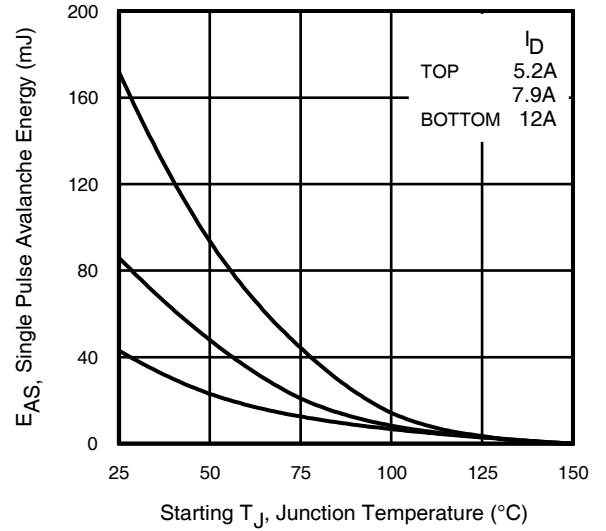


Fig 13. Maximum Avalanche Energy Vs. Drain Current

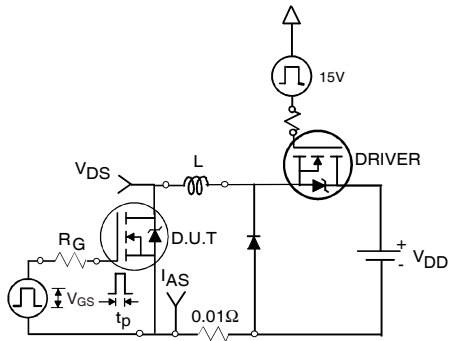


Fig 14a. Unclamped Inductive Test Circuit

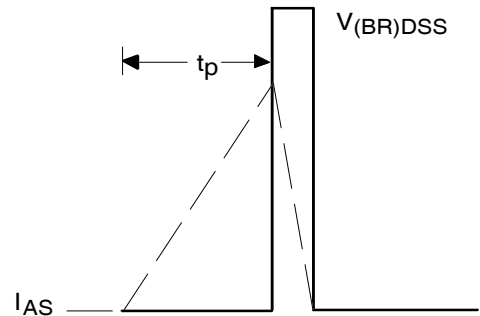


Fig 14b. Unclamped Inductive Waveforms

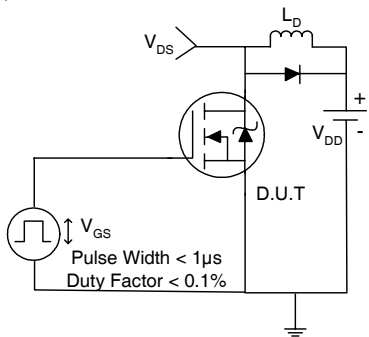


Fig 15a. Switching Time Test Circuit

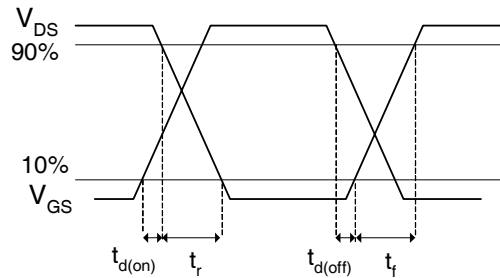


Fig 15b. Switching Time Waveforms

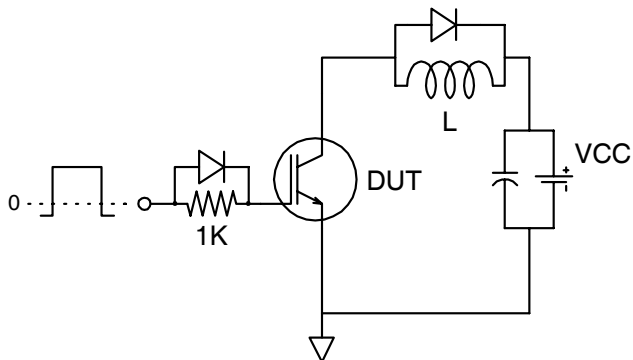


Fig 16a. Gate Charge Test Circuit

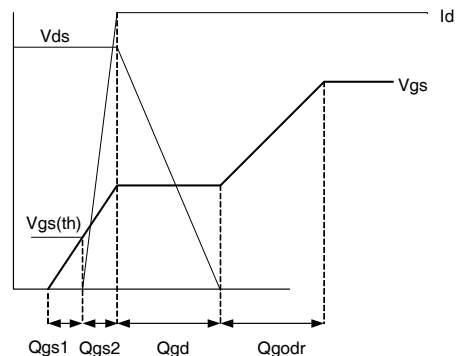


Fig 16b. Gate Charge Waveform

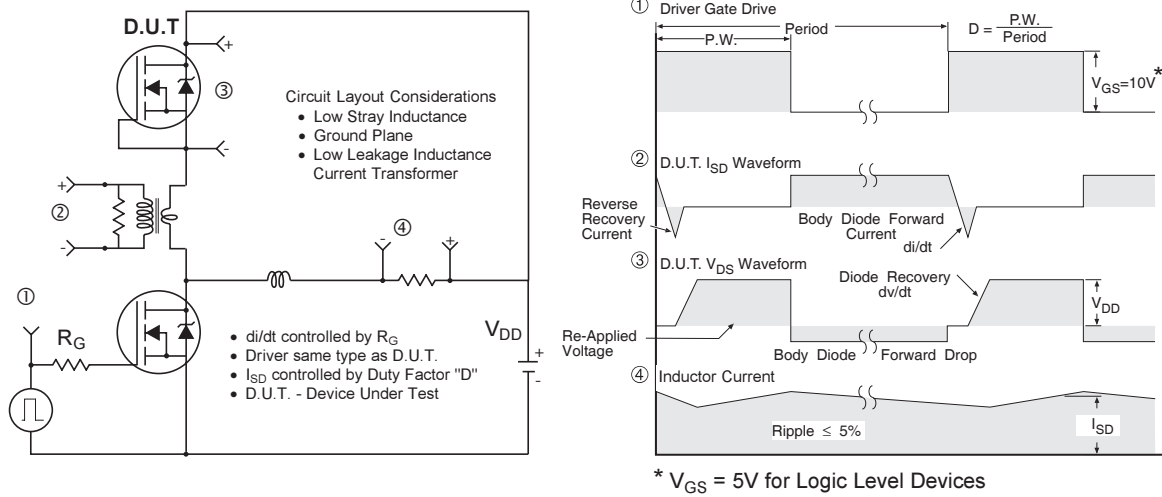
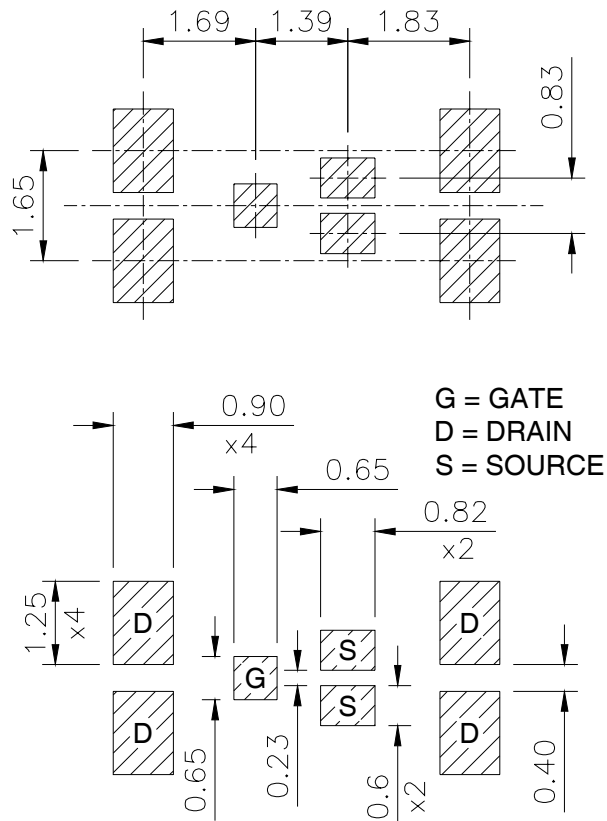


Fig 17. Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs

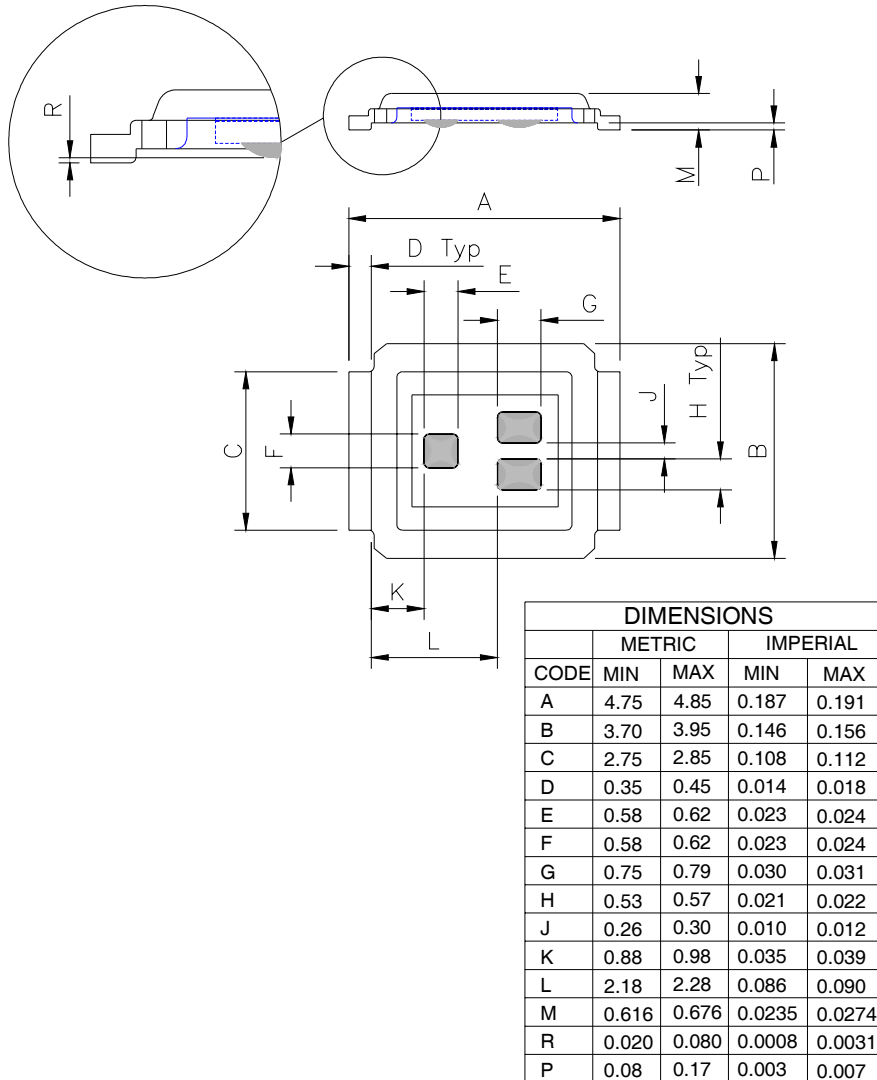
DirectFET™ Substrate and PCB Layout, ST Outline (Small Size Can, T-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.

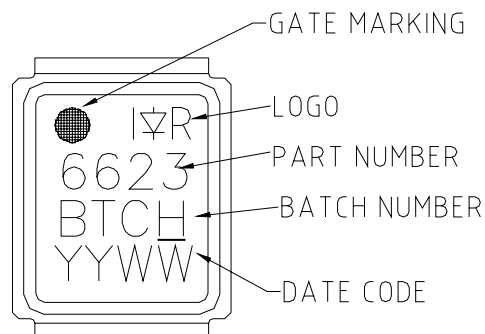


DirectFET™ Outline Dimension, ST Outline (Small Size Can, T-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



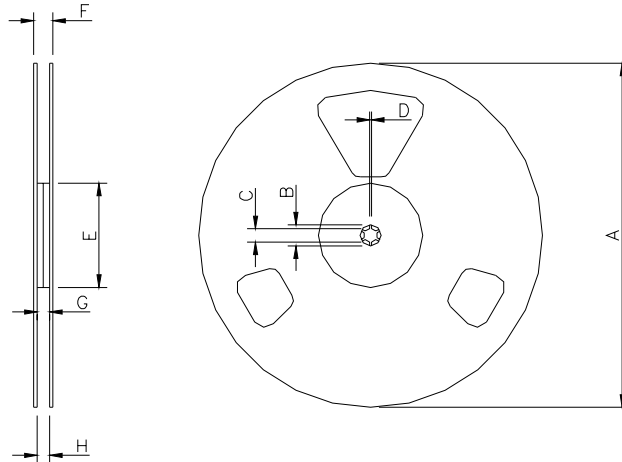
DirectFET™ Part Marking



Note: Line above the last character of the date-code indicates "Lead-Free".

IRF6623PbF

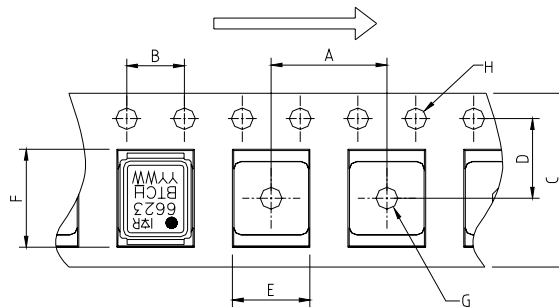
DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm
Std reel quantity is 4800 parts. (ordered as IRF6623TRPBF). For 1000 parts on 7" reel, order IRF6623TR1PBF

| REEL DIMENSIONS | | | | | | | | |
|-----------------|----------------------------|------|----------|-------|-----------------------|-------|----------|------|
| CODE | STANDARD OPTION (QTY 4800) | | | | TR1 OPTION (QTY 1000) | | | |
| | METRIC | | IMPERIAL | | METRIC | | IMPERIAL | |
| | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
| A | 330.0 | N.C | 12.992 | N.C | 177.77 | N.C | 6.9 | N.C |
| B | 20.2 | N.C | 0.795 | N.C | 19.06 | N.C | 0.75 | N.C |
| C | 12.8 | 13.2 | 0.504 | 0.520 | 13.5 | 12.8 | 0.53 | 0.50 |
| D | 1.5 | N.C | 0.059 | N.C | 1.5 | N.C | 0.059 | N.C |
| E | 100.0 | N.C | 3.937 | N.C | 58.72 | N.C | 2.31 | N.C |
| F | N.C | 18.4 | N.C | 0.724 | N.C | 13.50 | N.C | 0.53 |
| G | 12.4 | 14.4 | 0.488 | 0.567 | 11.9 | 12.01 | 0.47 | N.C |
| H | 11.9 | 15.4 | 0.469 | 0.606 | 11.9 | 12.01 | 0.47 | N.C |

Loaded Tape Feed Direction



| CODE | DIMENSIONS | | | |
|------|------------|-------|----------|-------|
| | METRIC | | IMPERIAL | |
| | MIN | MAX | MIN | MAX |
| A | 7.90 | 8.10 | 0.311 | 0.319 |
| B | 3.90 | 4.10 | 0.154 | 0.161 |
| C | 11.90 | 12.30 | 0.469 | 0.484 |
| D | 5.45 | 5.55 | 0.215 | 0.219 |
| E | 4.00 | 4.20 | 0.158 | 0.165 |
| F | 5.00 | 5.20 | 0.197 | 0.205 |
| G | 1.50 | N.C | 0.059 | N.C |
| H | 1.50 | 1.60 | 0.059 | 0.063 |

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>

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