

## MOSFET

### OptiMOS™ 6 Power-Transistor, 150 V

#### Features

- N-channel, normal level
- Very low on-resistance  $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

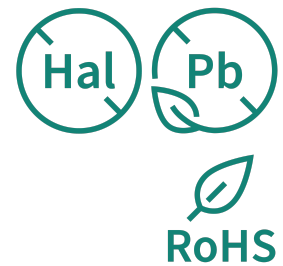
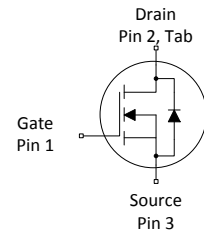
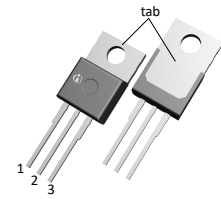
#### Product validation

Fully qualified according to JEDEC for Industrial Applications

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	150	V
$R_{DS(on),max}$	2.9	m $\Omega$
$I_D$	197	A
$Q_{oss}$	310	nC
$Q_G$	105	nC
$Q_{rr}$ (500A/ $\mu$ s)	220	nC

PG-TO220-3



Type/Ordering Code	Package	Marking	Related Links
IPP029N15NM6	PG-TO220-3	029N15N6	-



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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	197 151 151 24	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$ $V_{GS}=10\text{ V}, T_C=100\text{ °C}$ $V_{GS}=8\text{ V}, T_C=100\text{ °C}$ $V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=40\text{ °C/W}$ <sup>2)</sup>
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	788	A	$T_C=25\text{ °C}$
Avalanche current, single pulse <sup>4)</sup>	$I_{AS}$	-	-	100	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	1047	mJ	$I_D=58\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	395 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}, R_{thJA}=40\text{ °C/W}$ <sup>2)</sup>
Operating and storage temperature	$T_j, T_{stg}$	-55	-	175	°C	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	0.38	°C/W	-
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>5)</sup>	$R_{thJA}$	-	-	40	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	$R_{thJA}$	-	-	62	°C/W	-

<sup>5)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	3.0	3.5	4.0	V	$V_{DS}=V_{GS}, I_D=276\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=120\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$ $V_{DS}=120\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$
Drain-source on-state resistance <sup>6)</sup>	$R_{DS(on)}$	-	2.4 2.5 2.8	2.8 2.9 3.3	m $\Omega$	$V_{GS}=15\text{ V}, I_D=100\text{ A}$ $V_{GS}=10\text{ V}, I_D=100\text{ A}$ $V_{GS}=8\text{ V}, I_D=50\text{ A}$
Gate resistance	$R_G$	-	1.04	1.56	$\Omega$	-
Transconductance	$g_{fs}$	88	180	-	S	$ V_{DS}  \geq 2 I_D  R_{DS(on)max}, I_D=100\text{ A}$

<sup>6)</sup>  $R_{DS(on)}$  is specified at a distance of 1.8 mm distance to the package body; mounting at a larger distance increases the overall package resistance of approximately 0.04 mOhm/mm per leg.

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance <sup>7)</sup>	$C_{iss}$	-	7600	9900	pF	$V_{GS}=0\text{ V}, V_{DS}=75\text{ V}, f=1\text{ MHz}$
Output capacitance <sup>7)</sup>	$C_{oss}$	-	2300	3000	pF	$V_{GS}=0\text{ V}, V_{DS}=75\text{ V}, f=1\text{ MHz}$
Reverse transfer capacitance <sup>7)</sup>	$C_{rss}$	-	25	38	pF	$V_{GS}=0\text{ V}, V_{DS}=75\text{ V}, f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	22	-	ns	$V_{DD}=75\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A}, R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	26	-	ns	$V_{DD}=75\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A}, R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	39	-	ns	$V_{DD}=75\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A}, R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	24	-	ns	$V_{DD}=75\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A}, R_{G,ext}=1.6\text{ }\Omega$

<sup>7)</sup> Defined by design. Not subject to production test.

**Table 6 Gate charge characteristics** <sup>8)</sup>

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge <sup>9)</sup>	$Q_{gs}$	-	41	55	nC	$V_{DD}=75\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	26	-	nC	$V_{DD}=75\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge <sup>9)</sup>	$Q_{gd}$	-	23	35	nC	$V_{DD}=75\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	37	-	nC	$V_{DD}=75\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>9)</sup>	$Q_g$	-	105	137	nC	$V_{DD}=75\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DD}=75\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	89	-	nC	$V_{DS}=0.1\text{ V}, V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>9)</sup>	$Q_{oss}$	-	310	403	nC	$V_{DS}=75\text{ V}, V_{GS}=0\text{ V}$

<sup>8)</sup> See "Gate charge waveforms" for parameter definition

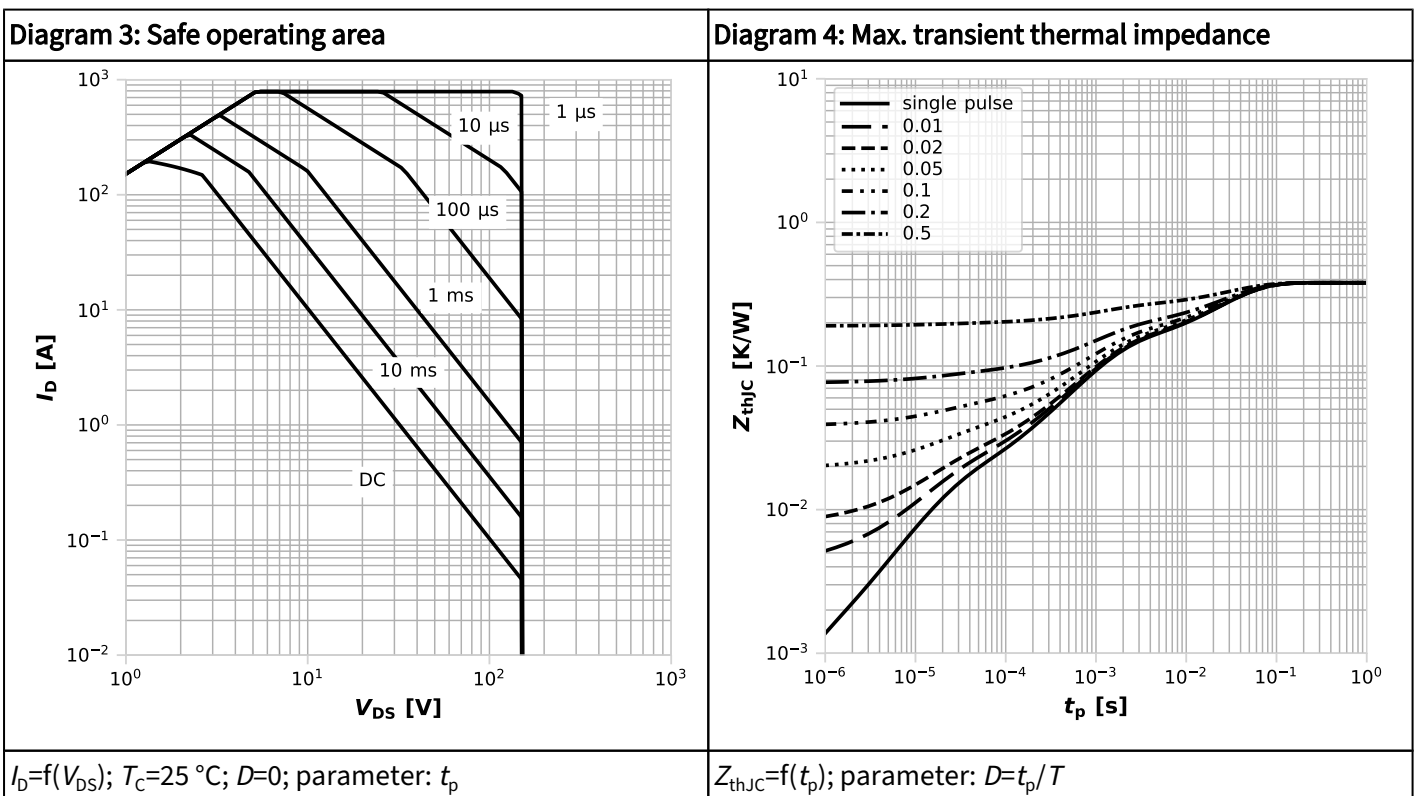
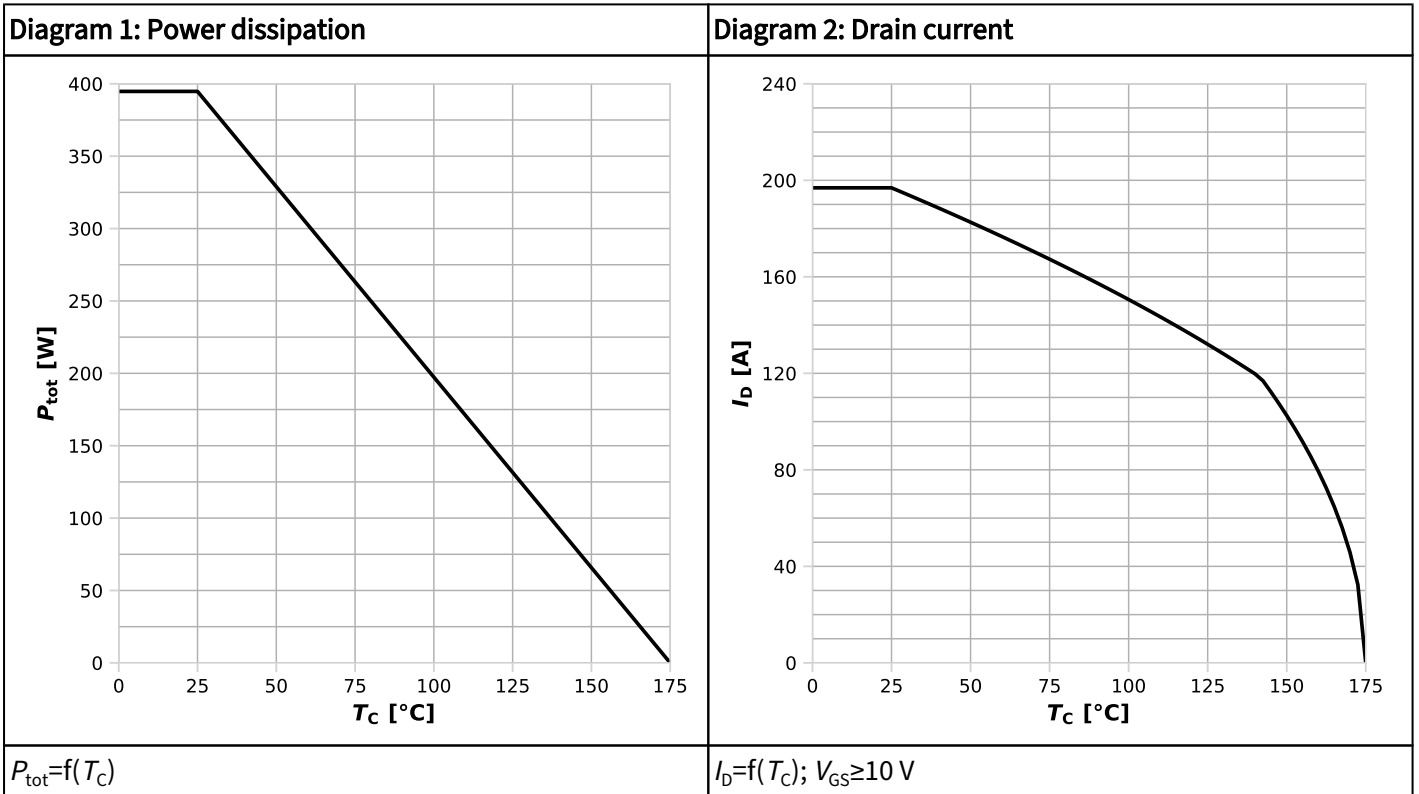
<sup>9)</sup> Defined by design. Not subject to production test.

**Table 7 Reverse diode**

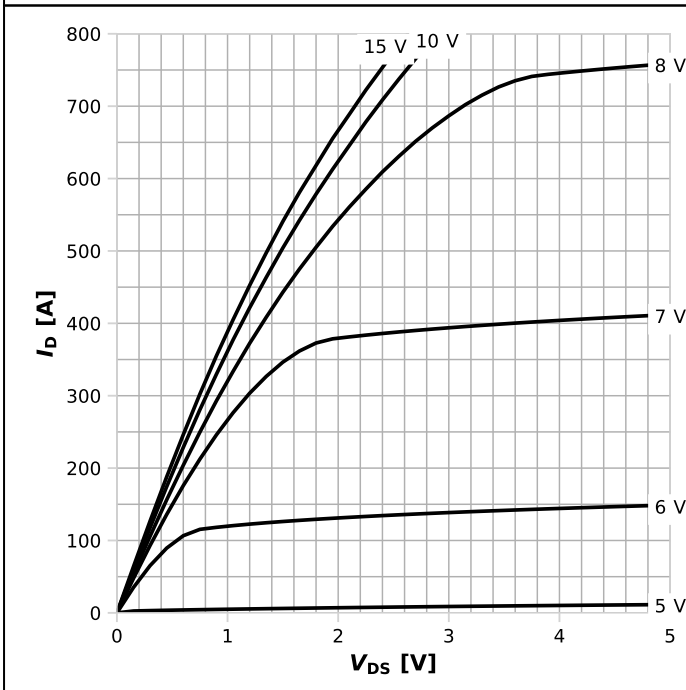
Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	182	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	788	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.89	1.0	V	$V_{GS}=0\text{ V}, I_F=100\text{ A}, T_j=25\text{ °C}$
Reverse recovery time <sup>10)</sup>	$t_{rr}$	-	44	88	ns	$V_R=75\text{ V}, I_F=50\text{ A}, di_F/dt=500\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>10)</sup>	$Q_{rr}$	-	220	440	nC	$V_R=75\text{ V}, I_F=50\text{ A}, di_F/dt=500\text{ A}/\mu\text{s}$
Reverse recovery time <sup>10)</sup>	$t_{rr}$	-	40	80	ns	$V_R=75\text{ V}, I_F=50\text{ A}, di_F/dt=1000\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>10)</sup>	$Q_{rr}$	-	410	820	nC	$V_R=75\text{ V}, I_F=50\text{ A}, di_F/dt=1000\text{ A}/\mu\text{s}$

<sup>10)</sup> Defined by design. Not subject to production test.

## 4 Electrical characteristics diagrams

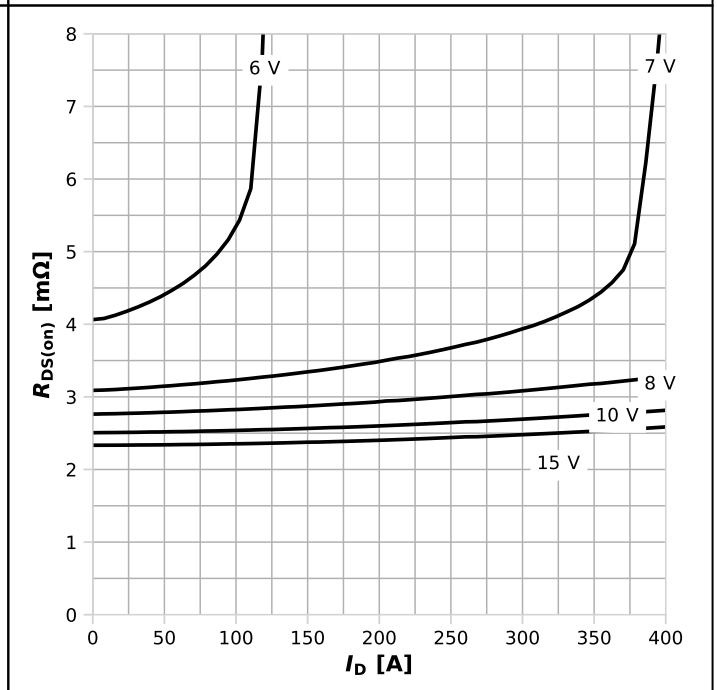


**Diagram 5: Typ. output characteristics**



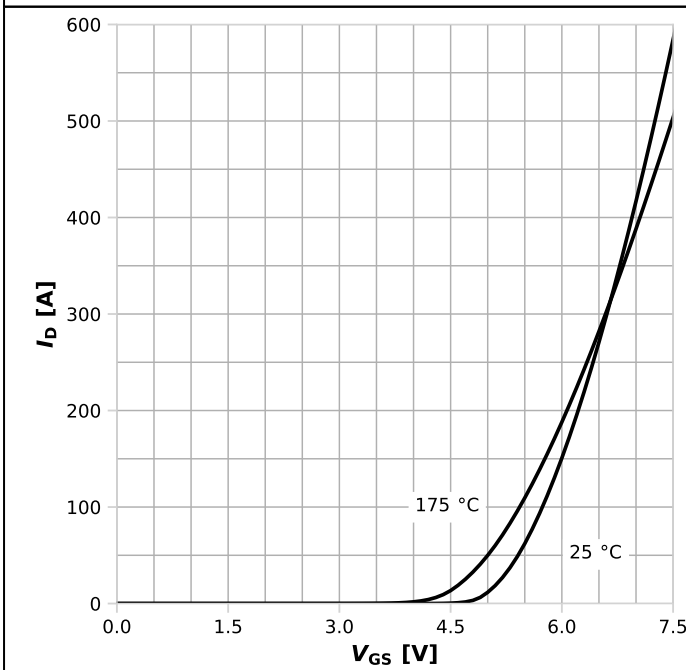
$I_D = f(V_{DS}), T_j = 25\text{ °C};$  parameter:  $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



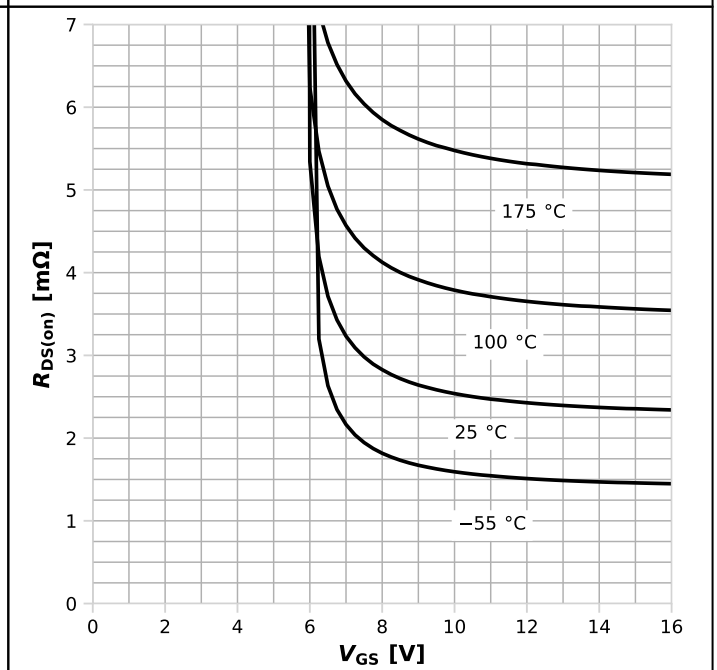
$R_{DS(on)} = f(I_D), T_j = 25\text{ °C};$  parameter:  $V_{GS}$

**Diagram 7: Typ. transfer characteristics**



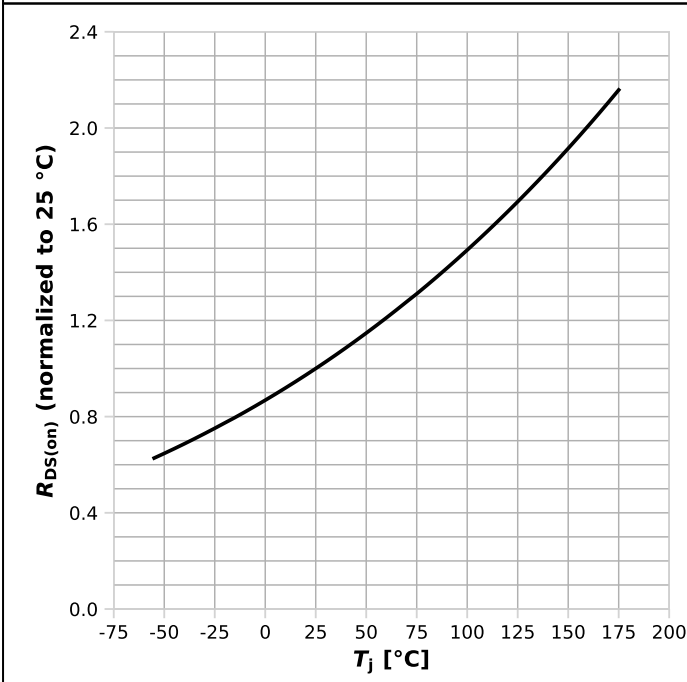
$I_D = f(V_{GS}), |V_{DS}| > 2|I_D|R_{DS(on)max};$  parameter:  $T_j$

**Diagram 8: Typ. drain-source on resistance**



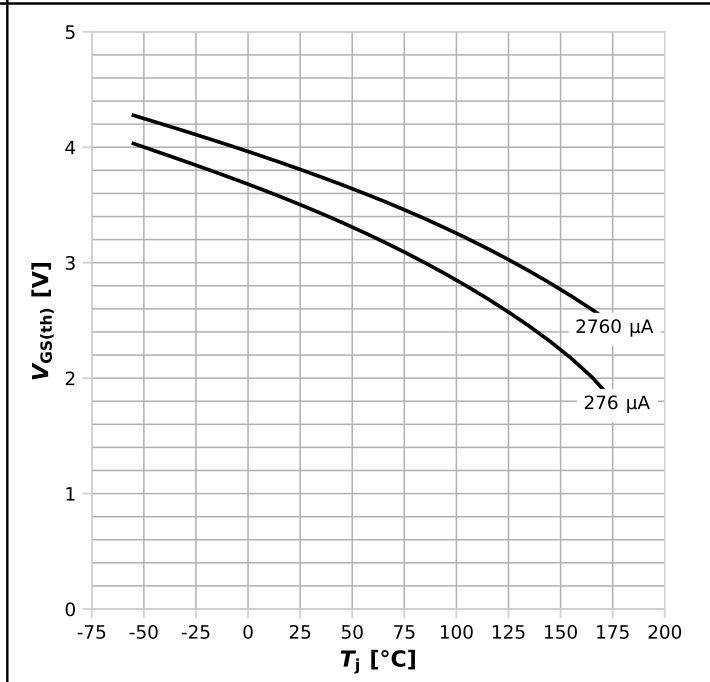
$R_{DS(on)} = f(V_{GS}), I_D = 100\text{ A};$  parameter:  $T_j$

Diagram 9: Normalized drain-source on resistance



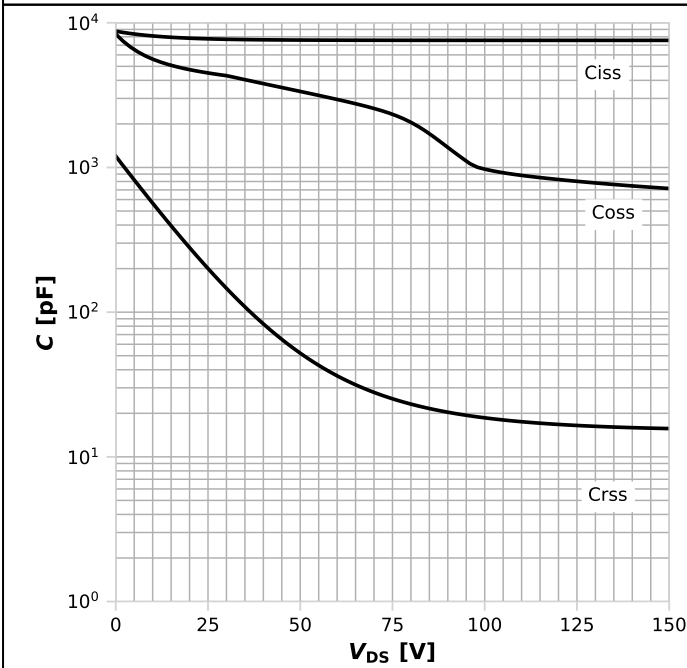
$R_{DS(on)}=f(T_j), I_D=100\text{ A}, V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



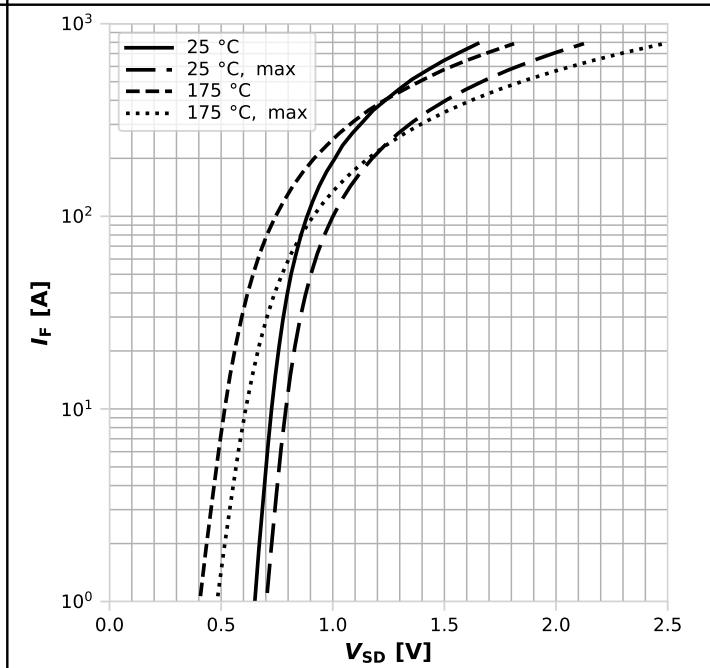
$V_{GS(th)}=f(T_j), V_{GS}=V_{DS}; \text{parameter: } I_D$

Diagram 11: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

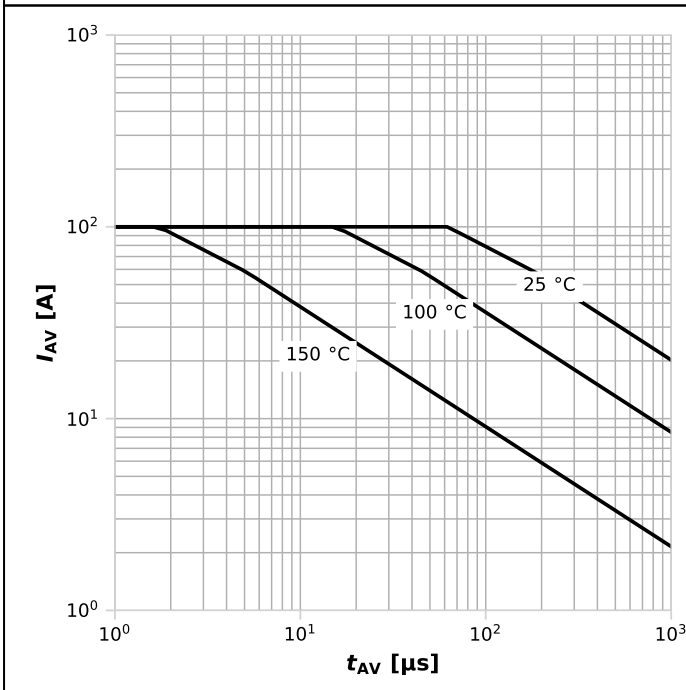
Diagram 12: Forward characteristics of reverse diode



$I_F=f(V_{SD}); \text{parameter: } T_j$

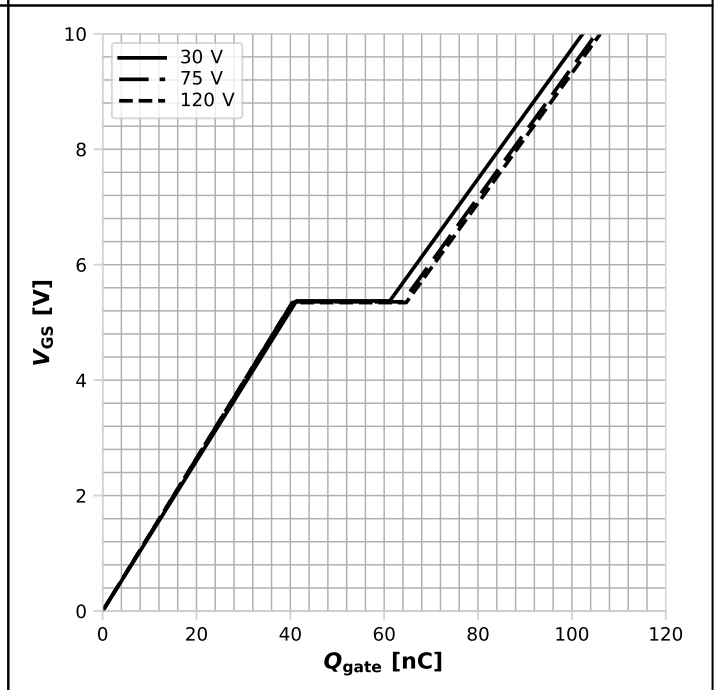


**Diagram 13: Avalanche characteristics**



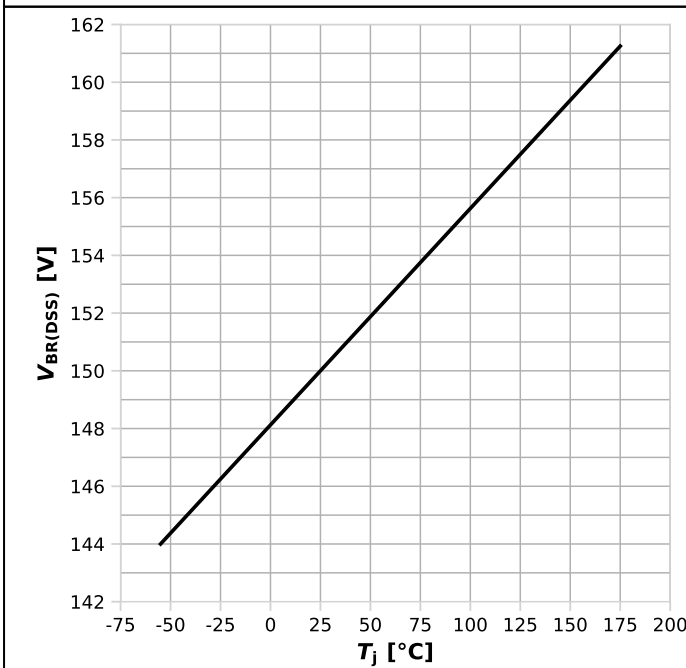
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j,start}$

**Diagram 14: Typ. gate charge**



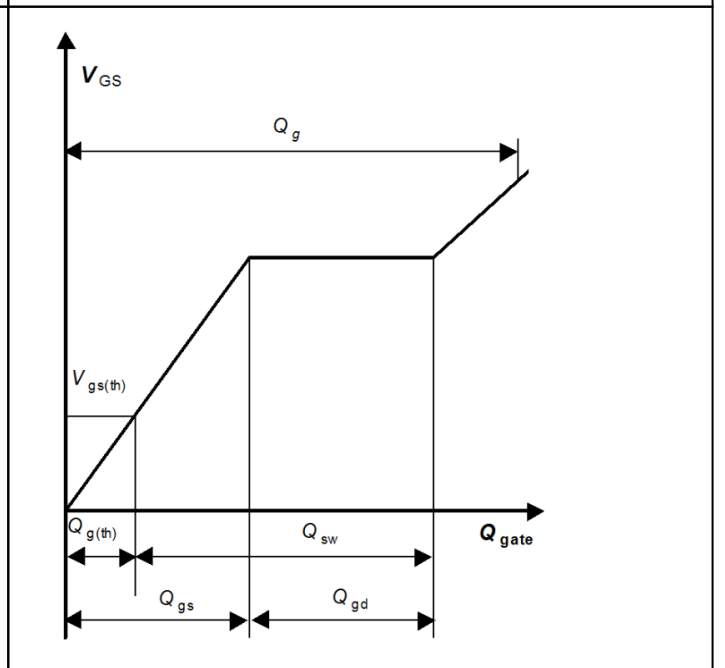
$V_{GS}=f(Q_{gate}), I_D=50 \text{ A pulsed}, T_j=25 \text{ °C}$ ; parameter:  $V_{DD}$

**Diagram 15: Min. drain-source breakdown voltage**



$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Gate charge waveforms**



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## 5 Package Outlines

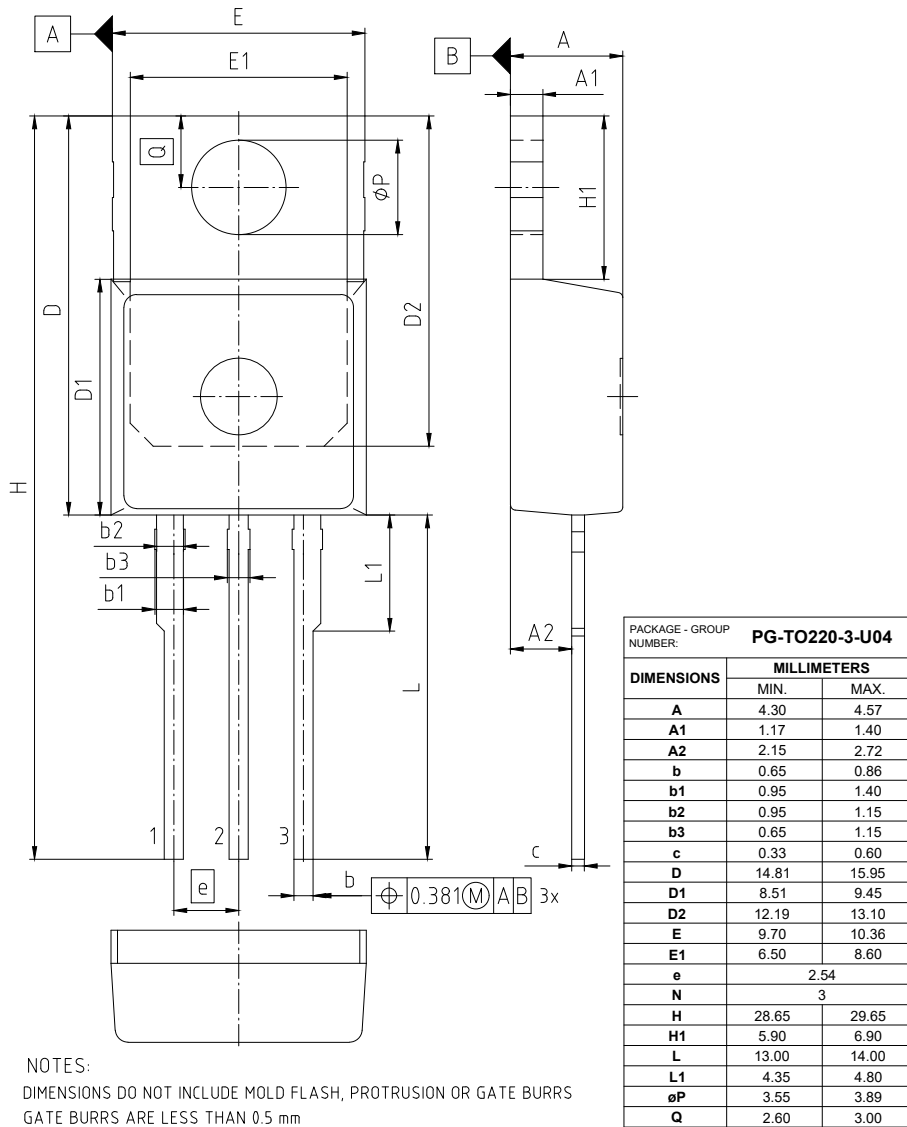


Figure 1 Outline PG-TO220-3, dimensions in mm

## Revision History

IPP029N15NM6

### Revision 2024-04-22, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2024-03-15	Release of preliminary version
2.0	2024-04-22	Release of final

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