

# MOSFET

## 650V CoolMOS™ CFD7A SJ Power Device

650V CoolMOS™ CFD7A is Infineon's latest generation of market leading automotive qualified high voltage CoolMOS™ MOSFETs. In addition to the well-known attributes of high quality and reliability required by the automotive industry, the new CoolMOS™ CFD7A series provides for an integrated fast body diode and can be used for PFC and resonant switching topologies like the ZVS phase-shift full-bridge and LLC.

### Features

- Latest 650V automotive qualified technology with integrated fast body diode on the market featuring ultra low  $Q_{rr}$
- Lowest FOM  $R_{DS(on)} * Q_g$  and  $R_{DS(on)} * E_{oss}$
- 100% avalanche tested
- Best-in-class  $R_{DS(on)}$  in SMD and THD packages

### Benefits

- Optimized for higher battery voltages up to 475 V thanks to further improved robustness
- Lower switching losses enabling higher switching frequencies
- High quality and reliability
- Increased efficiency in light load and full load conditions

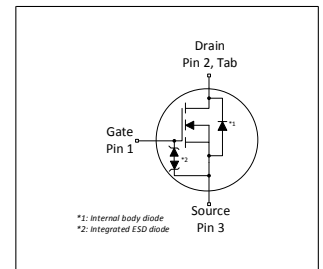
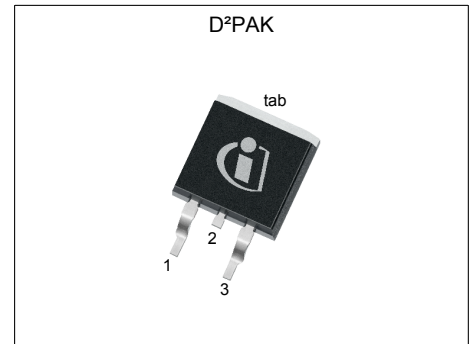
### Potential applications

- Suitable for PFC and DC-DC stages for:
  - Unidirectional and bidirectional DC-DC converters,
  - On-Board battery Chargers

### Product validation

Qualified according to AEC Q101

*Please note: For production part approval process (PPAP) release we propose to share application related information during an early design phase to avoid delays in PPAP release. Please contact Infineon sales office.*



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	650	V
$R_{DS(on),max}$	115	mΩ
$Q_{g,typ}$	41	nC
$I_{D,pulse}$	82	A
$E_{oss} @ 400V$	5.6	μJ
Body diode $di_F/dt$	1300	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPB65R115CFD7A	PG-TO263-3	65A115F7	see Appendix A

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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	21 13	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	82	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	97	mJ	$I_D=4.7\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche current, single pulse	$I_{AS}$	-	-	4.7	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS,pulse}$	-30	-	30	V	$f_{repetition} \leq 100\text{kHz}$ , $t_{pulse} \leq 2\text{ns}$
Power dissipation	$P_{tot}$	-	-	114	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	$T_j$	-40	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	-	Ncm	-
Continuous diode forward current	$I_S$	-	-	21	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	82	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	70	V/ns	$V_{DS}=0\dots400\text{V}$ , $I_{SD} \leq 9.7\text{A}$ , $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	$di_f/dt$	-	-	1300	A/ $\mu\text{s}$	$V_{DS}=0\dots400\text{V}$ , $I_{SD} \leq 9.7\text{A}$ , $T_j=25^\circ\text{C}$ see table 8

<sup>1)</sup> Limited by  $T_{j,max}$ .

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_\theta$

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	1.10	°C/W	-
Soldering temperature, reflow soldering allowed	$T_{sold}$	-	-	260	°C	reflow MSL1

### 3 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage <sup>1)</sup>	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage <sup>2)</sup>	$V_{(GS)th}$	3.5	4	4.5	V	$V_{DS}=V_{GS}, I_D=0.49mA$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu\text{A}$	$V_{DS}=650V, V_{GS}=0V, T_j=25^\circ\text{C}$ $V_{DS}=650V, V_{GS}=0V, T_j=150^\circ\text{C}$
Gate-source leakage current incl. protection diode	$I_{GSS}$	-	-	1	$\mu\text{A}$	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.103	0.115	$\Omega$	$V_{GS}=10V, I_D=9.7A, T_j=25^\circ\text{C}$ $V_{GS}=10V, I_D=9.7A, T_j=150^\circ\text{C}$
Gate resistance	$R_G$	-	6.0	-	$\Omega$	$f=250kHz$ , open drain

**Table 5 Dynamic characteristics**

External parasitic elements (PCB layout) influence switching behavior significantly.

Stray inductances and coupling capacitances must be minimized.

For layout recommendations please use provided application notes or contact Infineon sales office.

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	1950	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Output capacitance	$C_{oss}$	-	29	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Effective output capacitance, energy related <sup>3)</sup>	$C_{o(er)}$	-	70	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related <sup>4)</sup>	$C_{o(tr)}$	-	741	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	17	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=9.7A, R_G=1.8\Omega$ ; see table 9
Rise time	$t_r$	-	9	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=9.7A, R_G=1.8\Omega$ ; see table 9
Turn-off delay time	$t_{d(off)}$	-	71	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=9.7A, R_G=1.8\Omega$ ; see table 9
Fall time	$t_f$	-	5	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=9.7A, R_G=1.8\Omega$ ; see table 9

<sup>1)</sup> For applications with applied blocking voltage > 475 V, we recommend to evaluate the impact of the cosmic radiation effect in early design phase. For assessment, please contact local Infineon sales office.

<sup>2)</sup> We do not recommend using the CoolMOS mentioned in this datasheet to operate in "linear mode". For assessment of potential "linear mode", please contact Infineon sales office.

<sup>3)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>4)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

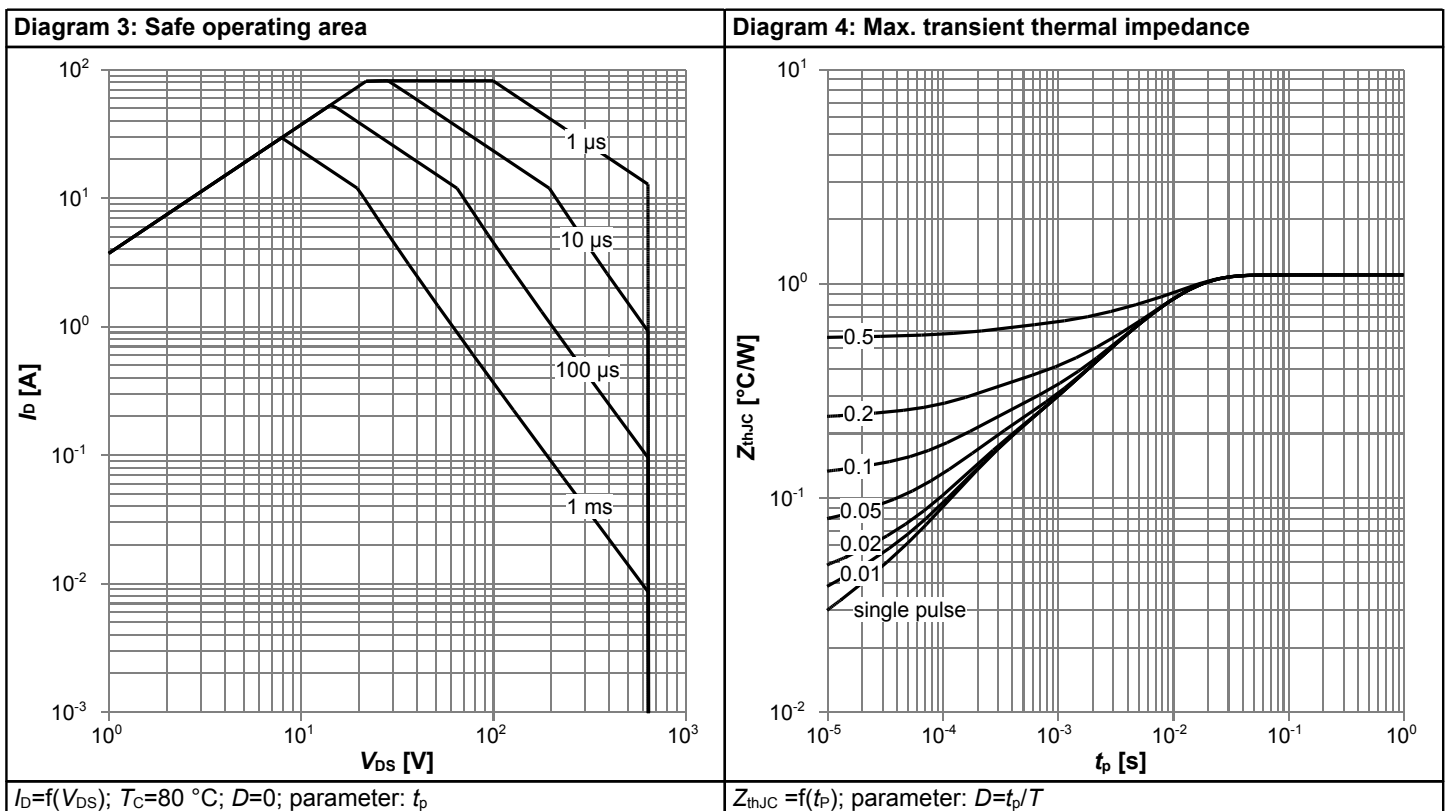
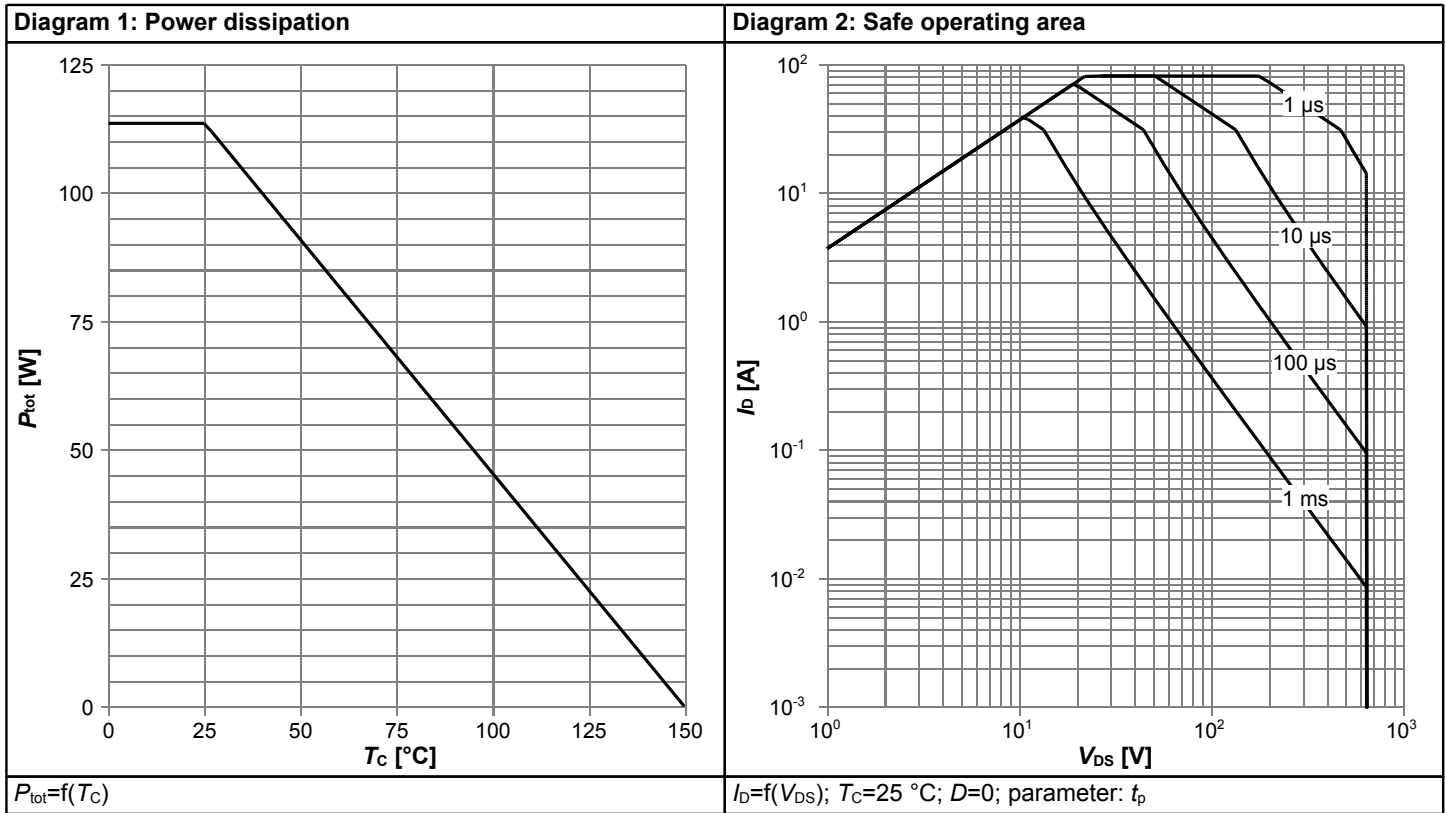
**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	11	-	nC	$V_{DD}=400V, I_D=9.7A, V_{GS}=0$ to 10V
Gate to drain charge	$Q_{gd}$	-	13	-	nC	$V_{DD}=400V, I_D=9.7A, V_{GS}=0$ to 10V
Gate charge total	$Q_g$	-	41	-	nC	$V_{DD}=400V, I_D=9.7A, V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	5.6	-	V	$V_{DD}=400V, I_D=9.7A, V_{GS}=0$ to 10V

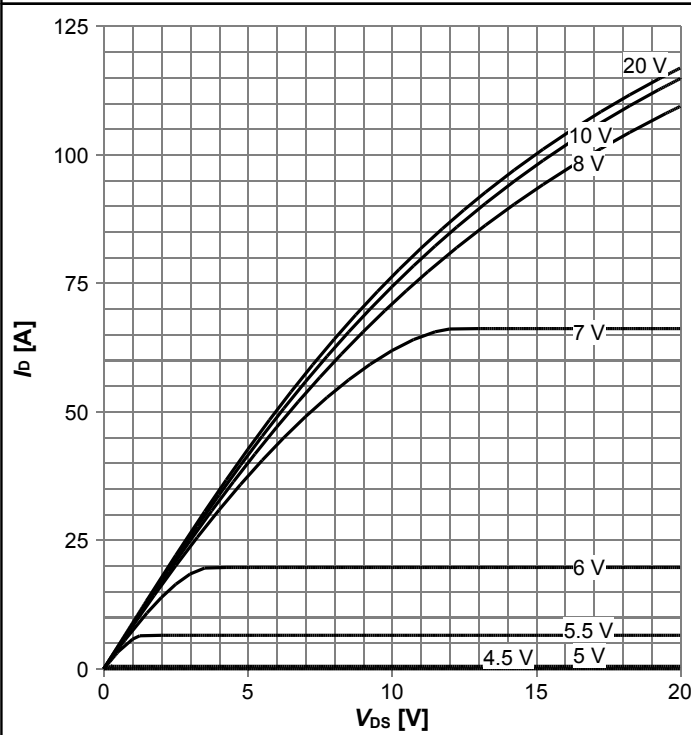
**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	1.1	-	V	$V_{GS}=0V, I_F=9.7A, T_j=25^\circ C$
Reverse recovery time	$t_{rr}$	-	110	-	ns	$V_R=400V, I_F=9.7A, di_F/dt=100A/\mu s$ ; see table 8
Reverse recovery charge	$Q_{rr}$	-	0.56	-	$\mu C$	$V_R=400V, I_F=9.7A, di_F/dt=100A/\mu s$ ; see table 8
Peak reverse recovery current	$I_{rrm}$	-	8.7	-	A	$V_R=400V, I_F=9.7A, di_F/dt=100A/\mu s$ ; see table 8

### 4 Electrical characteristics diagrams

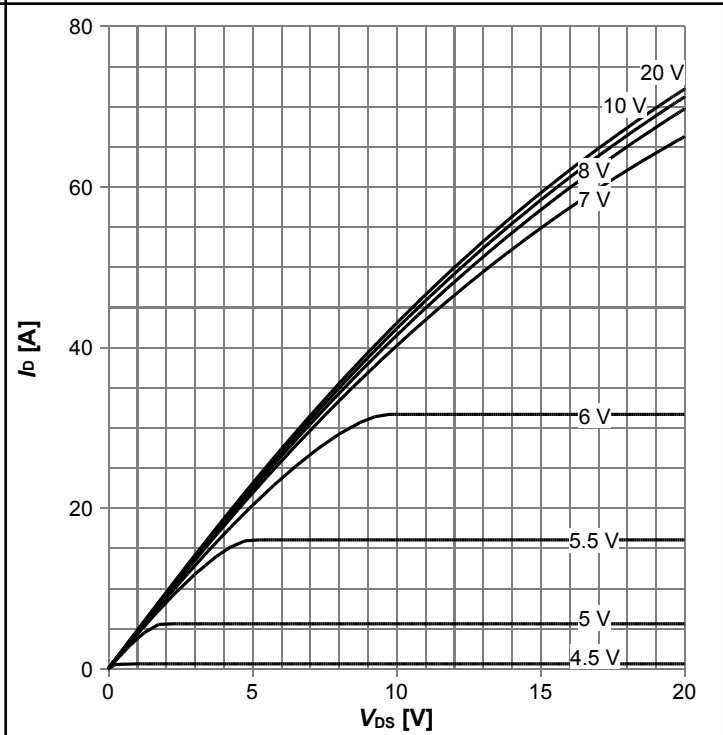


**Diagram 5: Typ. output characteristics**



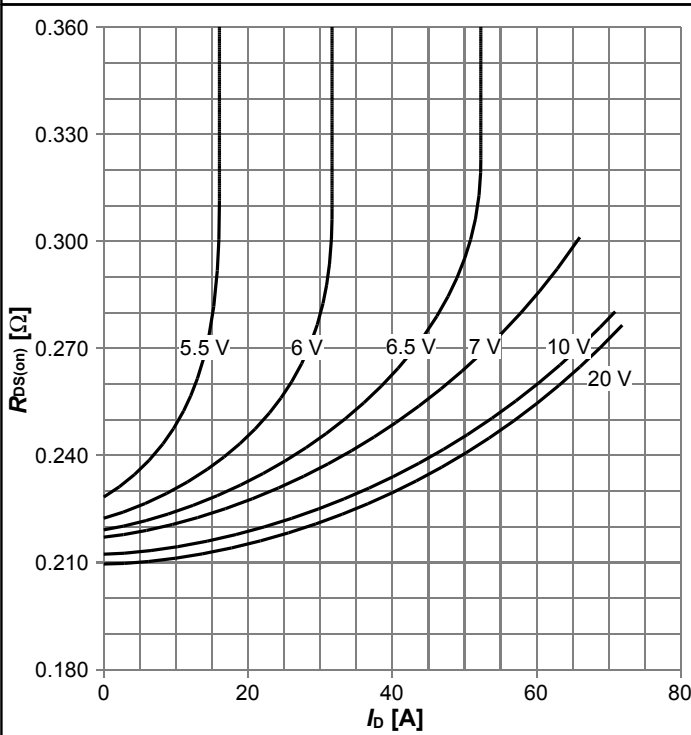
$I_D = f(V_{DS})$ ;  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

**Diagram 6: Typ. output characteristics**



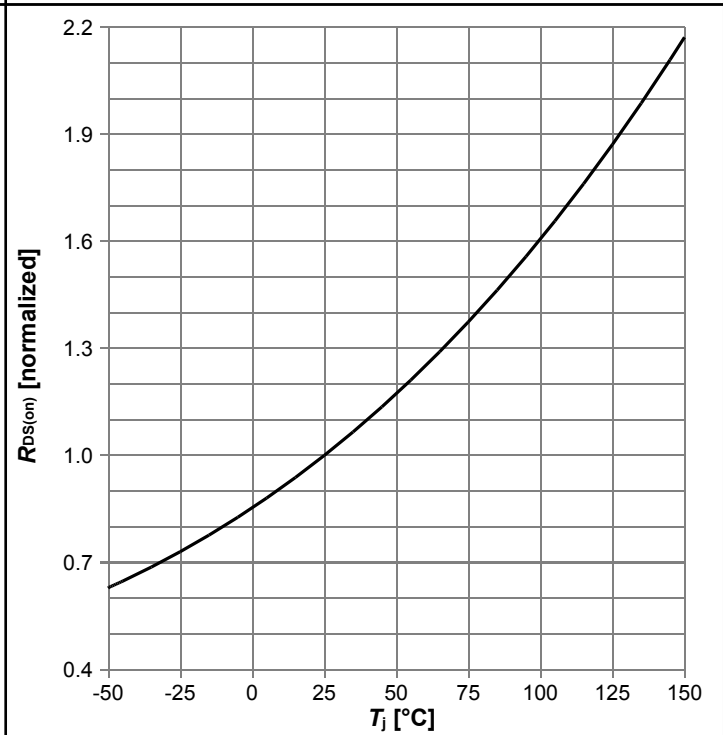
$I_D = f(V_{DS})$ ;  $T_j = 125^\circ\text{C}$ ; parameter:  $V_{GS}$

**Diagram 7: Typ. drain-source on-state resistance**



$R_{DS(on)} = f(I_D)$ ;  $T_j = 125^\circ\text{C}$ ; parameter:  $V_{GS}$

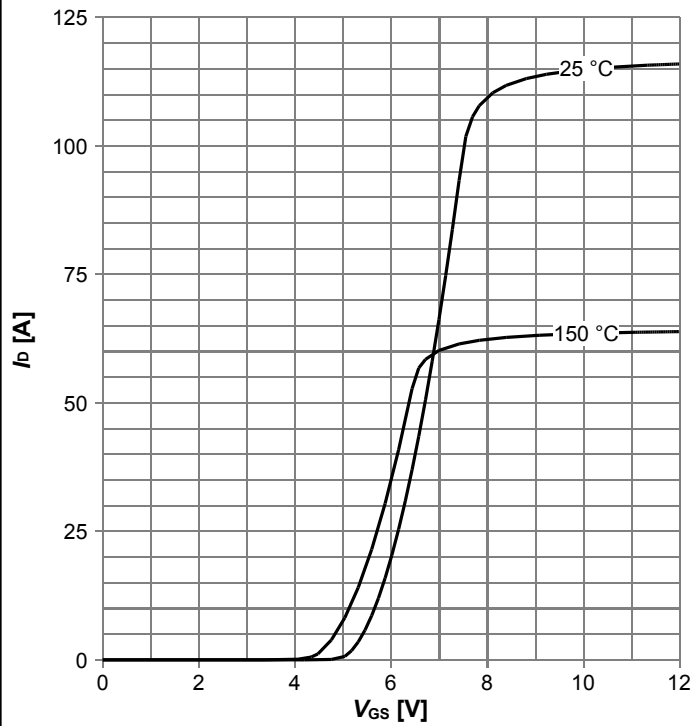
**Diagram 8: Drain-source on-state resistance**



$R_{DS(on)} = f(T_j)$ ;  $I_D = 9.7\text{ A}$ ;  $V_{GS} = 10\text{ V}$

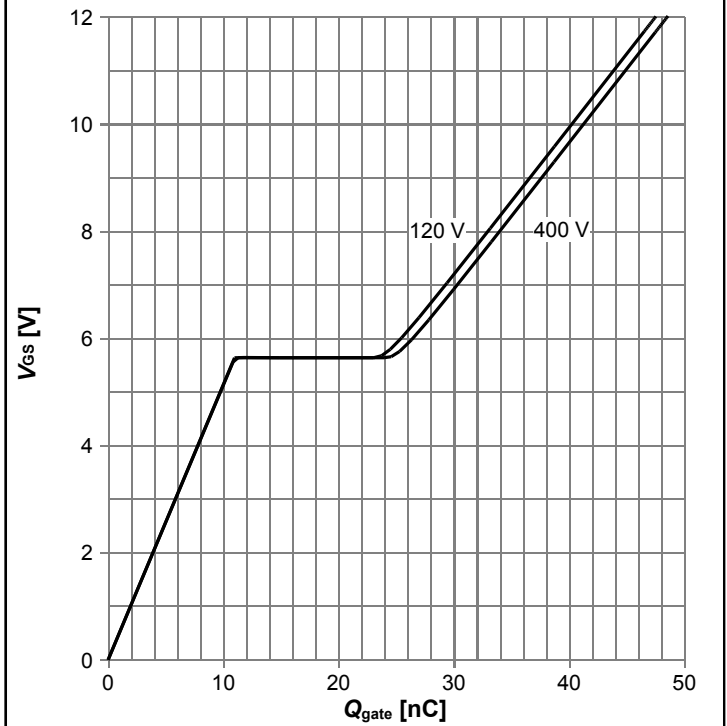


Diagram 9: Typ. transfer characteristics



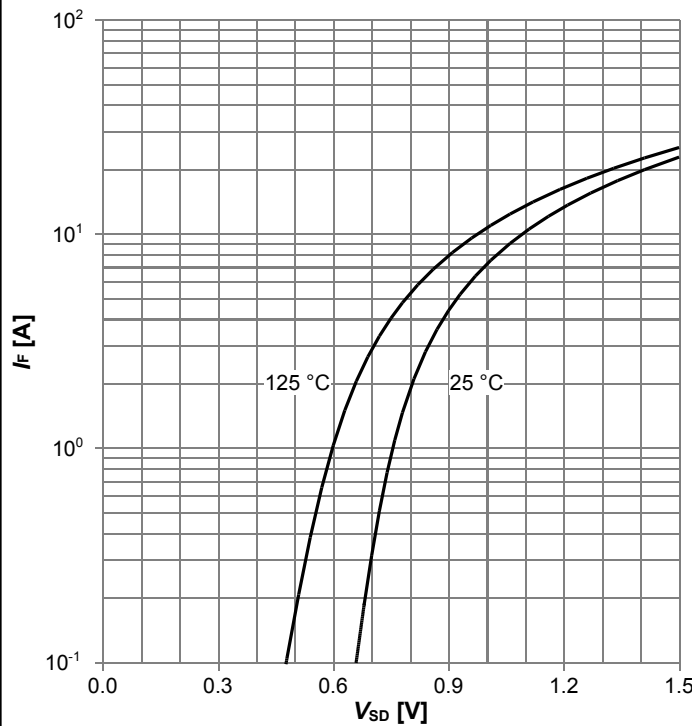
$I_D=f(V_{GS}); V_{DS}=20V$ ; parameter:  $T_j$

Diagram 10: Typ. gate charge



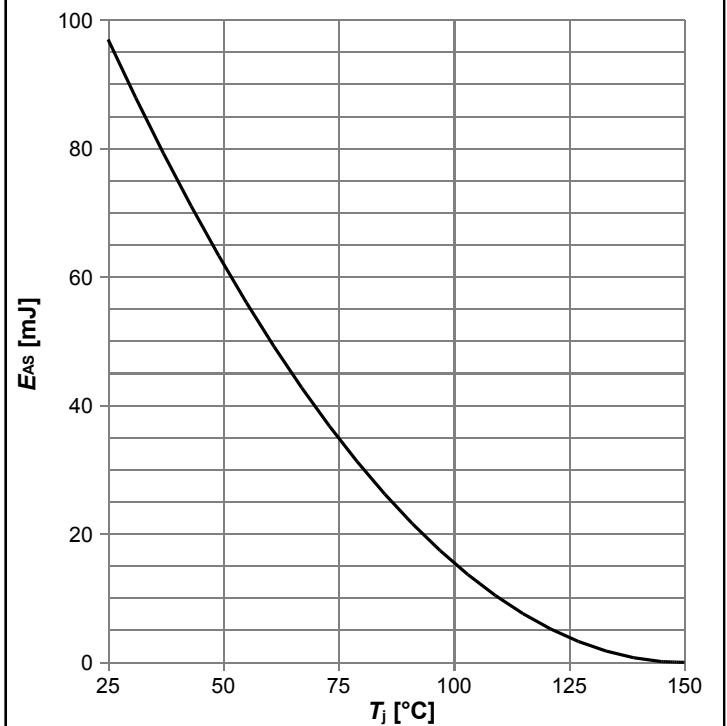
$V_{GS}=f(Q_{gate}); I_D=9.7$  A pulsed; parameter:  $V_{DD}$

Diagram 11: Forward characteristics of reverse diode



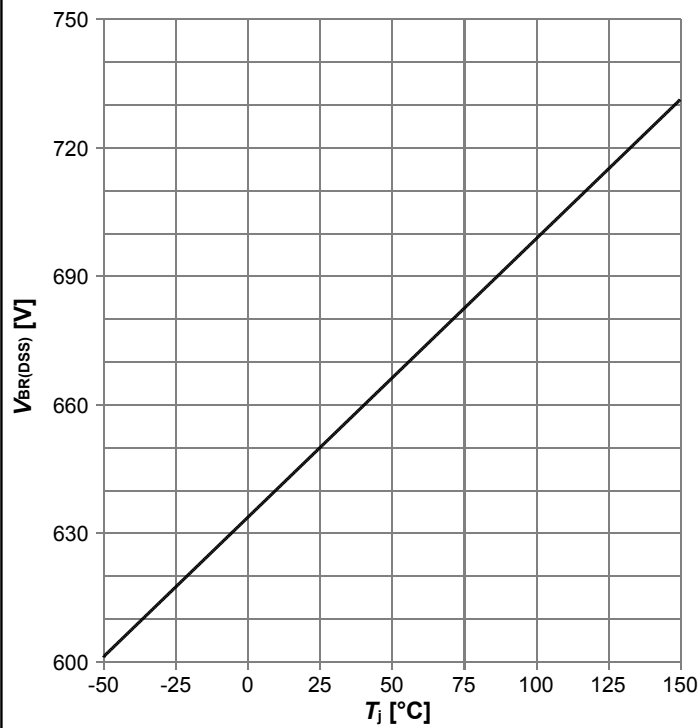
$I_F=f(V_{SD})$ ; parameter:  $T_j$

Diagram 12: Avalanche energy



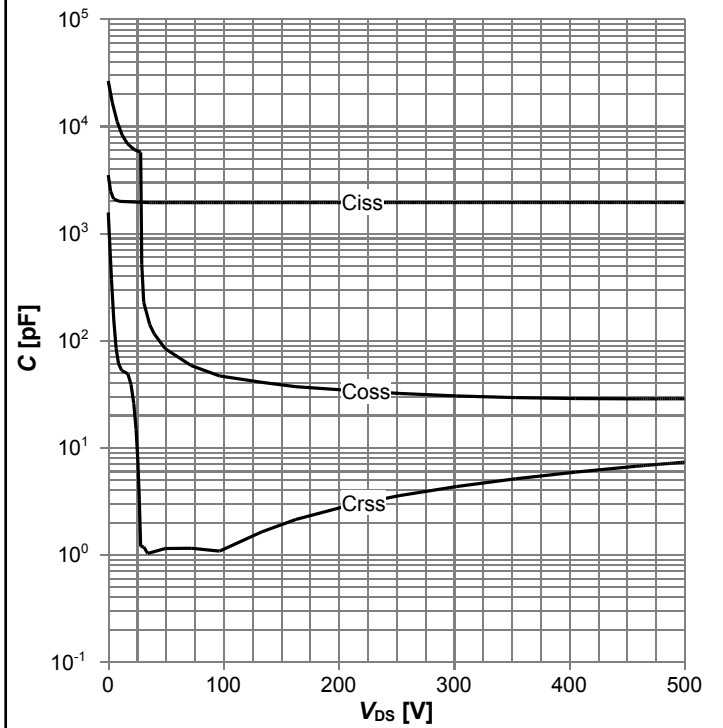
$E_{AS}=f(T_j); I_D=4.7$  A;  $V_{DD}=50$  V

**Diagram 13: Drain-source breakdown voltage**



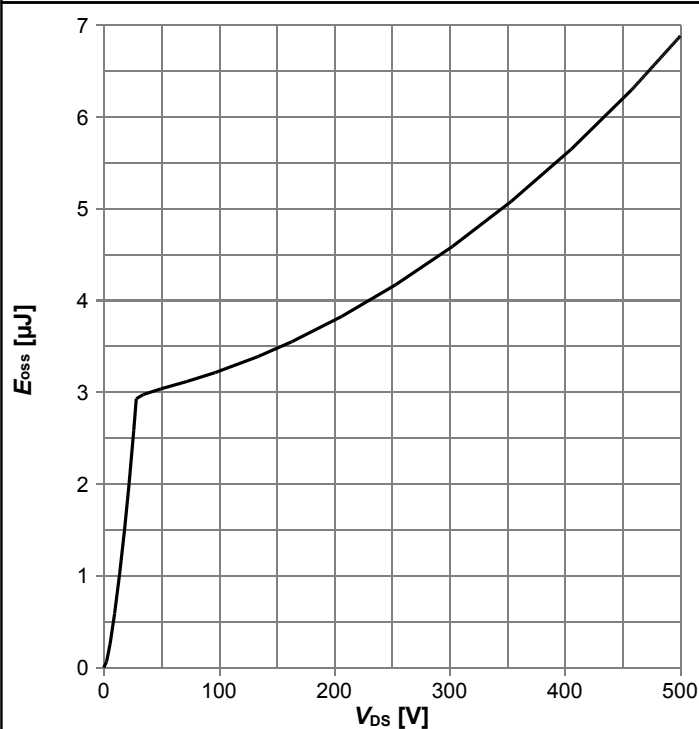
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Diagram 14: Typ. capacitances**



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=250 \text{ kHz}$

**Diagram 15: Typ. Coss stored energy**



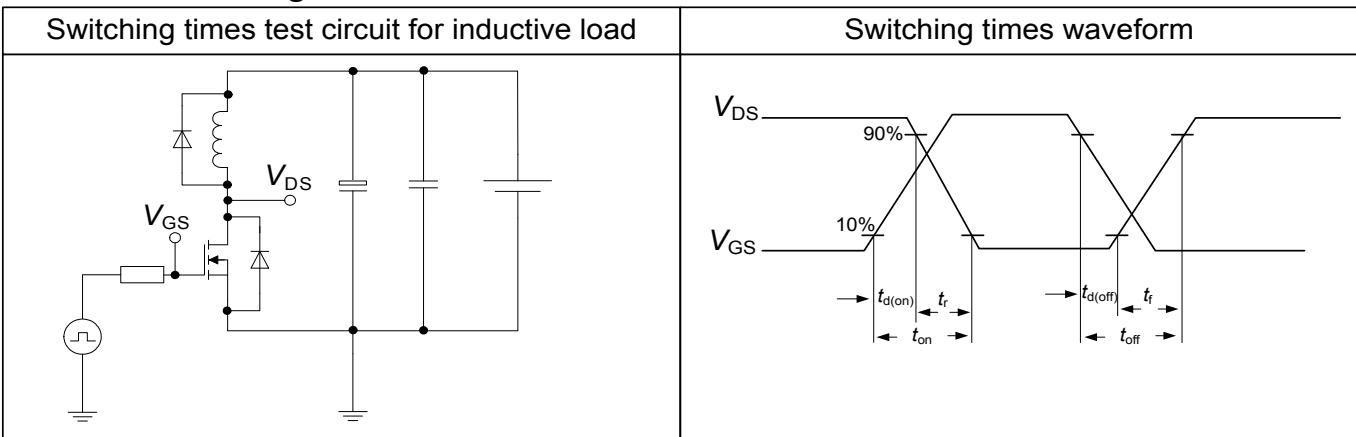
$E_{oss}=f(V_{DS})$

## 5 Test Circuits

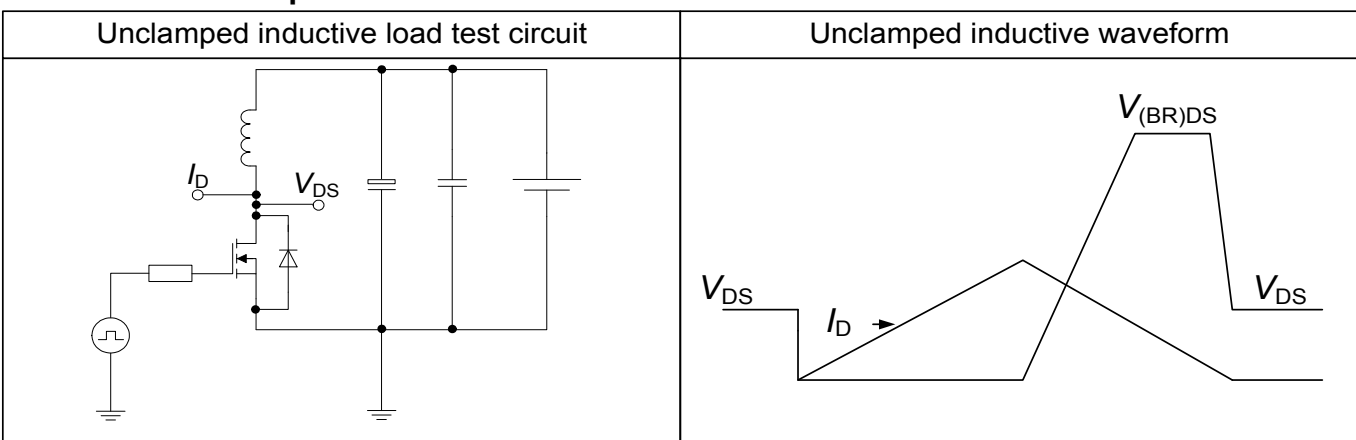
**Table 8 Diode characteristics**



**Table 9 Switching times**



**Table 10 Unclamped inductive load**



## 6 Package Outlines

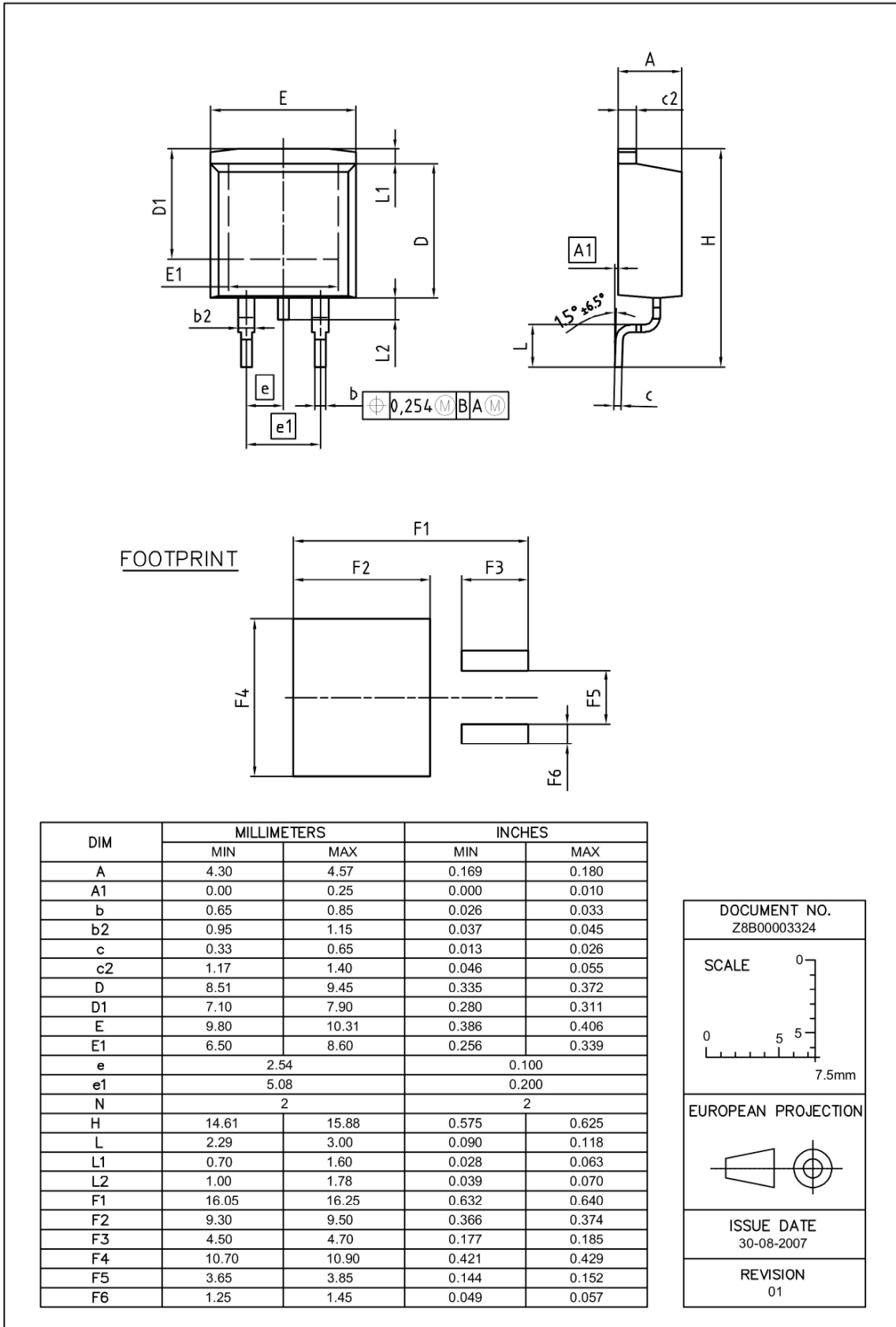


Figure 1 Outline PG-TO263-3, dimensions in mm/inches

## 7 Appendix A

### Table 11 Related Links

- IFX CoolMOS CFD7A Webpage: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS CFD7A application note: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS CFD7A simulation model: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

## Revision History

IPB65R115CFD7A

**Revision: 2020-03-31, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
0.9	2018-05-04	Release of target version
1.0	2018-08-14	Release of preliminary version
1.1	2018-10-15	Update of parameter "Id" and update of avalanche current and related test conditions.
2.0	2018-12-17	Release of final version
2.1	2020-03-31	Updated marketing text, minimum storage temperature, drain-source breakdown voltage footnote and disclaimer page.

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