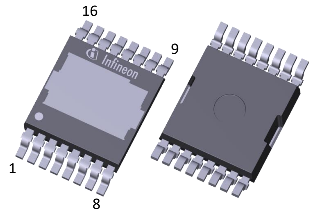
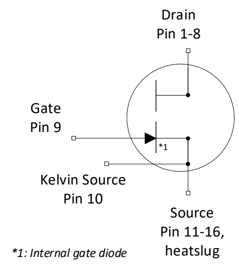
CoolGaN™ Gen2

650 V CoolGaN™ enhancement-mode Power Transistor

Infineon's CoolGaN™ is a highly efficient GaN (gallium nitride) transistor technology for power conversion in the voltage range up to 650 V. With extensive experience on the semiconductor market, Infineon's GaN technology brought the e-mode concept to maturity with end-to-end production in high volumes. The pioneering quality ensures the highest standards and offers the most reliable and performing solution among all GaN HEMTs on the market.

TOLT





Features

- Enhancement mode transistor - Normally OFF switch
- Ultra fast switching
- No reverse-recovery charge
- Capable of reverse conduction
- Low gate charge, low output charge
- Superior commutation ruggedness
- ESD (HBM/CDM) JEDEC standards

Benefits

- Improves system efficiency
- Improves power density
- Enables highest operating frequency
- System cost reduction savings
- Reduces EMI

Potential applications

Industrial, telecom, datacenter SMPS, charger and adapter based on half-bridge topologies (half-bridge topologies for hard and soft switching such as Totem pole PFC, high frequency LLC).

Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: Target Datasheet to change without further notice

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS,max}$	650	V
$R_{DS(on),max}$	140	mΩ
$Q_{g,typ}$	3.4	nC
$I_{D,pulse}$	30	A
Q_{oss} @ 400 V	18	nC
Q_{rr}	0	nC

Type/Ordering Code	Package	Marking	Related Links
IGLT65R110D2	PG-HDSOP-16	65R110D2	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25 °C, unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80 % of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain source voltage, continuous	$V_{DS,max}$	-	-	650	V	V_{GS} = 0 V, derating recomendation acc. JEDEC JEP198
Leakage current at drain source transient voltage	$I_{DS,trans}$	-	-	6.2	mA	V_{GS} = 0 V, $V_{DS,trans}$ = 900 V
Drain source voltage transient	$V_{DS,trans}$	-	-	900	V	<1 % duty cycle, <1 µs, 1 M pulses
Drain source voltage, pulsed	$V_{DS,pulse}$ $V_{DS,pulsed}$	-	-	750 650	V	T_j = 25 °C; V_{GS} ≤ 0 V; cumulated stress time ≤ 1 h T_j = 125 °C; V_{GS} ≤ 0 V; cumulated stress time ≤ 1 h
Switching surge voltage, pulsed	$V_{DS,surge}$	-	-	750	V	DC bus voltage = 700 V; turn off $V_{DS,pulse}$ = 750 V; turn on $I_{D,pulse}$ =13 A; T_j = 105 °C; f ≤ 100 kHz, t ≤100 sec. (10 million pulses)
Continuous current, drain source [1]	I_D	-	-	15	A	T_C=25 °C; T_j = $T_{j,max}$
Pulsed current, drain source	$I_{D,pulse}$	-30 -17	-	30 17	A	T_j=25 °C; I_G=13 mA; See Diagram 3, 5 T_j=125 °C; I_G=13 mA; See Diagram 4, 6
Gate current, continuous [2]	$I_{G,avg}$	-	-	10	mA	T_j=-55 °C to T_j=150 °C; See Table 9
Gate current, pulsed [2]	$I_{G,pulsed}$	-1	-	1	A	T_j=-55 °C to T_j=150 °C; t_{PULSE}= 50 ns, f = 100 kHz; See Table 9
Gate source voltage, continuous [2]	V_{GS}	-10	-	-	V	T_j=-55 °C to T_j=150 °C; See Diagram 12
Gate source voltage, pulsed [2]	$V_{GS,pulse}$	-25	-	-	V	T_j=-55 °C to T_j=150 °C; t_{PULSE}= 50 ns, f = 100 kHz; open drain
Power dissipation	P_{tot}	-	-	54	W	T_C=25 °C
Operating junction temperature	T_j	-55	-	150	°C	-
Storage temperature	T_{stg}	-55	-	150	°C	Max shelf life depends on storage conditions
Drain-source voltage slew-rate	dv/dt	-	-	200	V/ns	-

[1] Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.75

[2] We recommend using an advanced driving technique to optimize the device performance. Please see gate drive application note for more details.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2.3	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	68	°C/W	Device on PCB, minimum footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	92	°C/W	Device on 40 mm*40 mm*1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thickness) copper area. PCB is vertical without air stream cooling.
Reflow soldering temperature	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at T_j=25 °C, unless specified otherwise

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	0.9 -	1.2 1	1.6 -	V	I_{DS}=1.3 mA; V_{DS}=10 V; T_j=25 °C I_{DS}=1.3 mA; V_{DS}=10 V; T_j=150 °C
Gate-Source reverse clamping voltage	$V_{GS,\ clamp}$	-	-	-8	V	I_{GS}=-1 mA
Drain-Source leakage current	I_{DSS}	-	0.5 10	51 -	µA	V_{DS}=650 V, V_{GS}=0 V, T_j=25 °C V_{DS}=650 V, V_{GS}=0 V, T_j=150 °C
Drain-Source on-state resistance	$R_{DS(on)}$	-	0.110 0.240	0.140 -	Ω	I_G=13 mA; I_D=4 A; T_j=25 °C I_G=13 mA; I_D=4 A; T_j=150 °C
Gate resistance	$R_{G,int}$	-	tbd	-	Ω	LCR impedance measurement; f=f_{res}, open drain;

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	170	-	pF	V_{GS}=0 V; V_{DS}=400 V, f=1 MHz
Output capacitance	C_{oss}	-	27	-	pF	V_{GS}=0 V, V_{DS}=400 V, f=1 MHz
Reverse Transfer capacitance	C_{rss}	-	0.32	-	pF	V_{GS}=0 V, V_{DS}=400 V, f=1 MHz
Effective output capacitance, energy related [3)]	$C_{o(er)}$	-	tbd	-	pF	V_{DS}=0 to 400 V
Effective output capacitance, time related [4)]	$C_{o(tr)}$	-	tbd	-	pF	V_{GS}=0 V; V_{DS}=0 to 400 V; I_D=const
Output charge	Q_{oss}	-	18	-	nC	V_{DS}=0 to 400 V
Turn-on delay time	$t_{d(on)}$	-	tbd	-	ns	I_D= 4 A; R_{ON}=10 Ohm; R_{OFF}=10 Ohm; R_{SS}=680 Ohm; C_C=1.5 nF; V_{DRV}=12 V; see Table 8
Turn-off delay time	$t_{d(off)}$	-	tbd	-	ns	I_D= 4 A; R_{ON}=10 Ohm; R_{OFF}=10 Ohm; R_{SS}=680 Ohm; C_C=1.5 nF; V_{DRV}=12 V; see Table 8
Rise time	t_r	-	tbd	-	ns	I_D= 4 A; R_{ON}=10 Ohm; R_{OFF}=10 Ohm; R_{SS}=680 Ohm; C_C=1.5 nF; V_{DRV}=12 V; see Table 8
Fall time	t_f	-	tbd	-	ns	I_D= 4 A; R_{ON}=10 Ohm; R_{OFF}=10 Ohm; R_{SS}=680 Ohm; C_C=1.5 nF; V_{DRV}=12 V; see Table 8

3) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V

4) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	3.4	-	nC	V_{GS}=0 to 3 V; V_{DS}=400 V, I_D=4 A

Table 7 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.2	2.5	V	V_{GS}=0 V; I_{SD}=4 A
Pulsed current, reverse	$I_{SD,pulse}$	-	-	30	A	I_G=13 mA
Reverse recovery charge [5]	Q_{rr}	-	0	-	nC	I_{SD}=4 A; V_{DS}=400 V

5) Excluding Qoss

4 Test Circuits

Table 8 Reverse Channel Characteristics Test

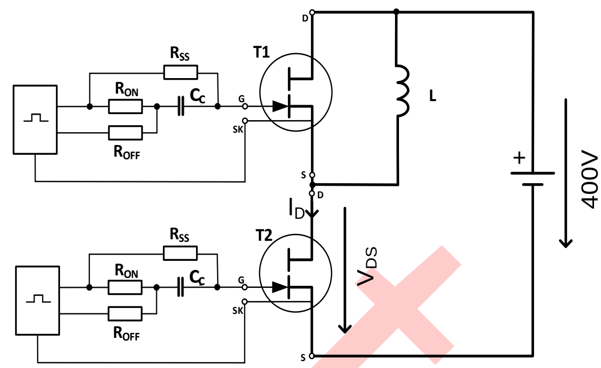
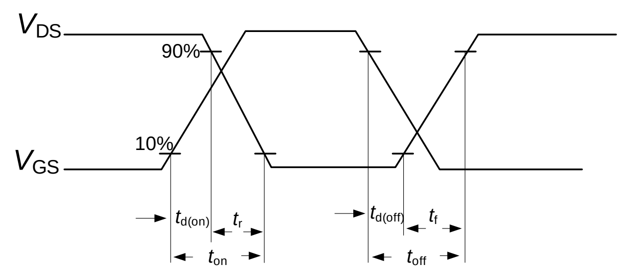
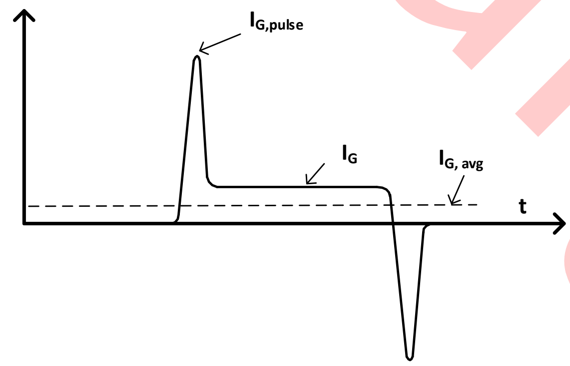
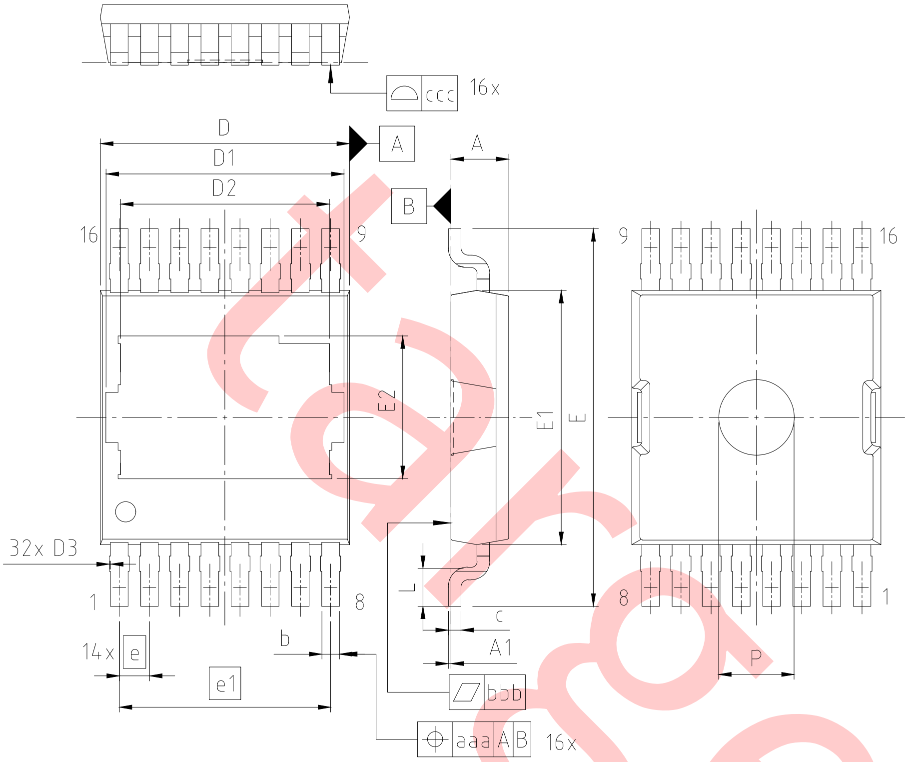
Switching times with inductive load	Switching times waveform
	

Table 9 Gate current switching waveform

Gate current switching waveform


5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-HDSOP-16-U05				
DIMENSIONS	**MILLIMETERS** MIN.	MAX.	**DIMENSIONS**	**MILLIMETERS** MIN.	MAX.
A	2.25	2.35	**e**	1.20	
A1	0.01	0.16	**e1**	8.40	
b	0.60	0.80	**L**	1.40	1.60
c	0.40	0.60	**P**	2.90	3.10
D	9.70	10.10	**aaa**	0.25	
D1	9.46		**bbb**	0.02	
D2	8.20	8.40	**ccc**	0.10	
D3	0.15				
E	14.80	15.20			
E1	10.00	10.30			
E2	5.57	5.77			

NOTES:
ALL METAL SURFACES TIN PLATED EXCEPT AREA OF CUT

Figure 1 Outline PG-HDSOP-16, dimensions in mm

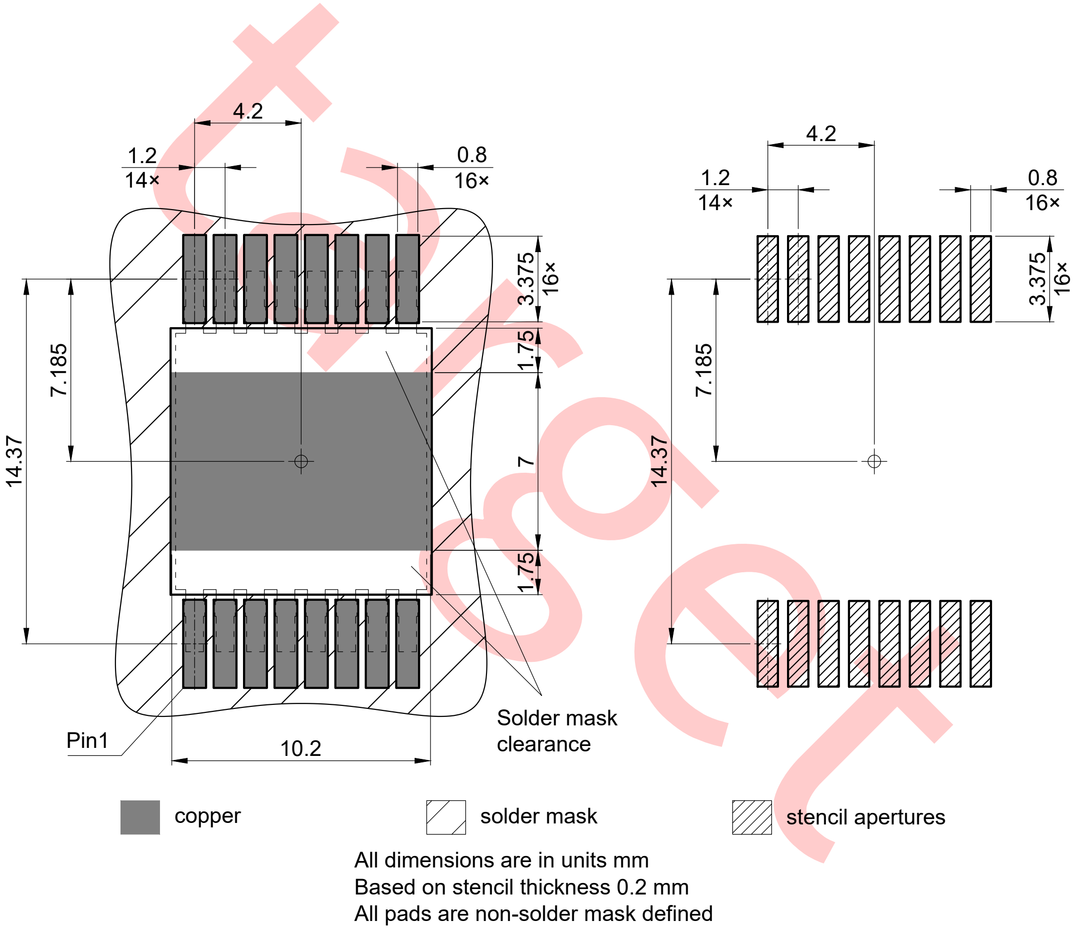


Figure 2 Outline PG-HDSOP-16, dimensions in mm

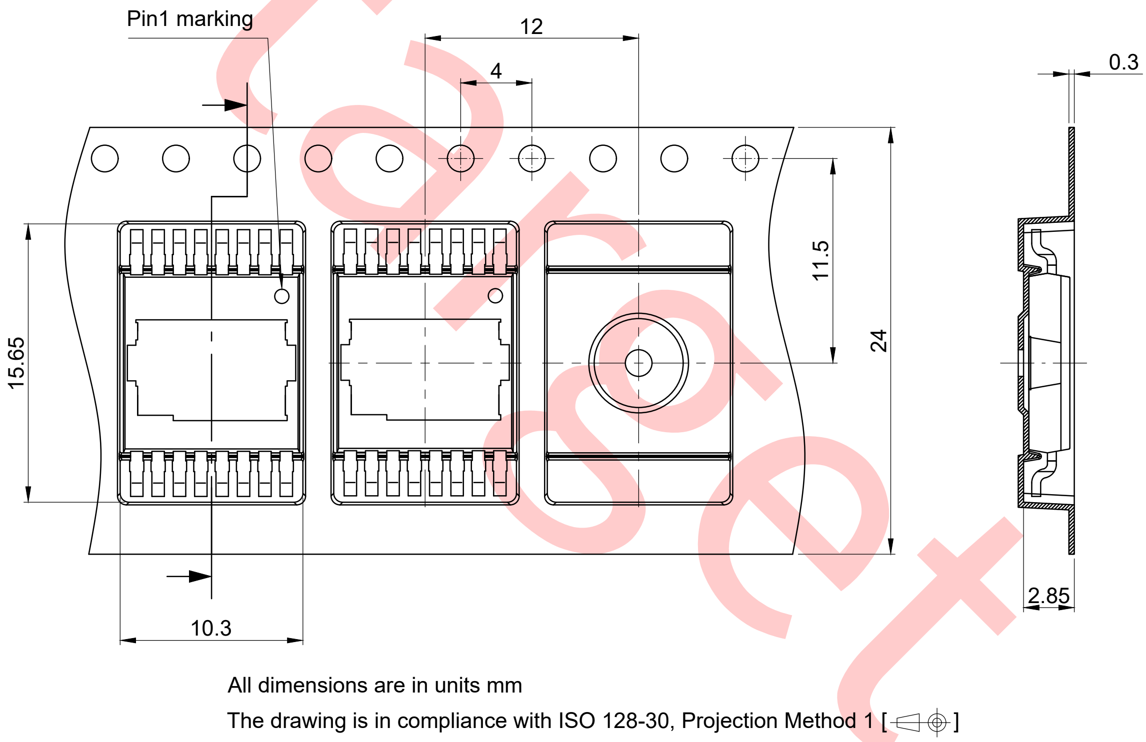


Figure 3 Outline PG-HDSOP-16, dimensions in mm

6 Apendix A

Table 10 Related Links

- IFX CoolGaN^{TM} GaN 650 V webpage
- IFX CoolGaN^{TM} GaN 650 V reliability white paper
- IFX CoolGaN^{TM} GaN 650 V gate driver application note
- IFX CoolGaN^{TM} GaN 650 V applications information

Revision History

IGLT65R110D2

Revision 2024-04-15, Rev. 0.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
0.1	2024-04-15	Release of target

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