XDP™ XDP710-002 evaluation PCBA user guide

About this document

Scope and purpose

This document describes how to set up the XDP™ XDP710-002 Evaluation Board and configure the internal registers to evaluate the performance of the XDP710-002 hot-swap controller for positive rail.

Intended audience

This document is intended for test engineers who want to evaluate the performance of the XDP710-002 hot-swap controller.

Important notice

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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems

Table 1 Safety precautions

	**Warning**: *The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

Table of contents

1 Introduction

Infineon's XDP™ XDP7x0-002 family (XDP700-002 and XDP710-002) are highly integrated wide-input voltage system monitoring and protection devices, which are digitally configurable and use a power management bus (PMBus) communication interface to access their register map to configure all of their features.

The USB007A series dongle is a PC-USB COM port to PMBus bridge dongle that allows access to the XDP710-002 registers from the PC software configurator.

This document describes how to set up the evaluation board and configure the internal registers to evaluate the performance of XDP710-002 to limit inrush current (regulation on programmed FET safe operating area (SOA)) during startup and also highlights the fault detection and control.

2 Hardware and software requirements

The following hardware and software are required for the setup:

- XDP710-002 Evaluation Board V 2.0.
  - **Order code**: EVAL_XDP710_V2
- XDP™ Designer USB dongle USB007 or higher.
  - **Order code**: USB007A1
- XDP™ Designer graphical user interface (GUI).
  - Download from Infineon Development Center

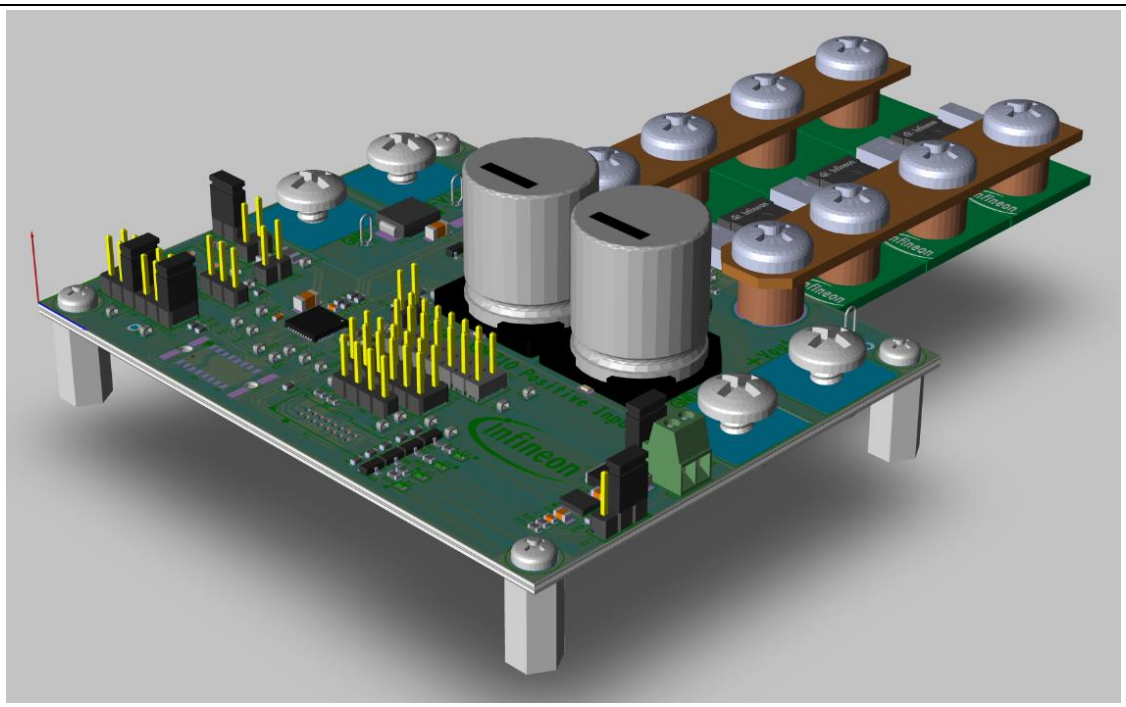

Figure 1 XDP710-002 Evaluation Board

Figure 2 USB007A1 dongle

Hardware and software requirements

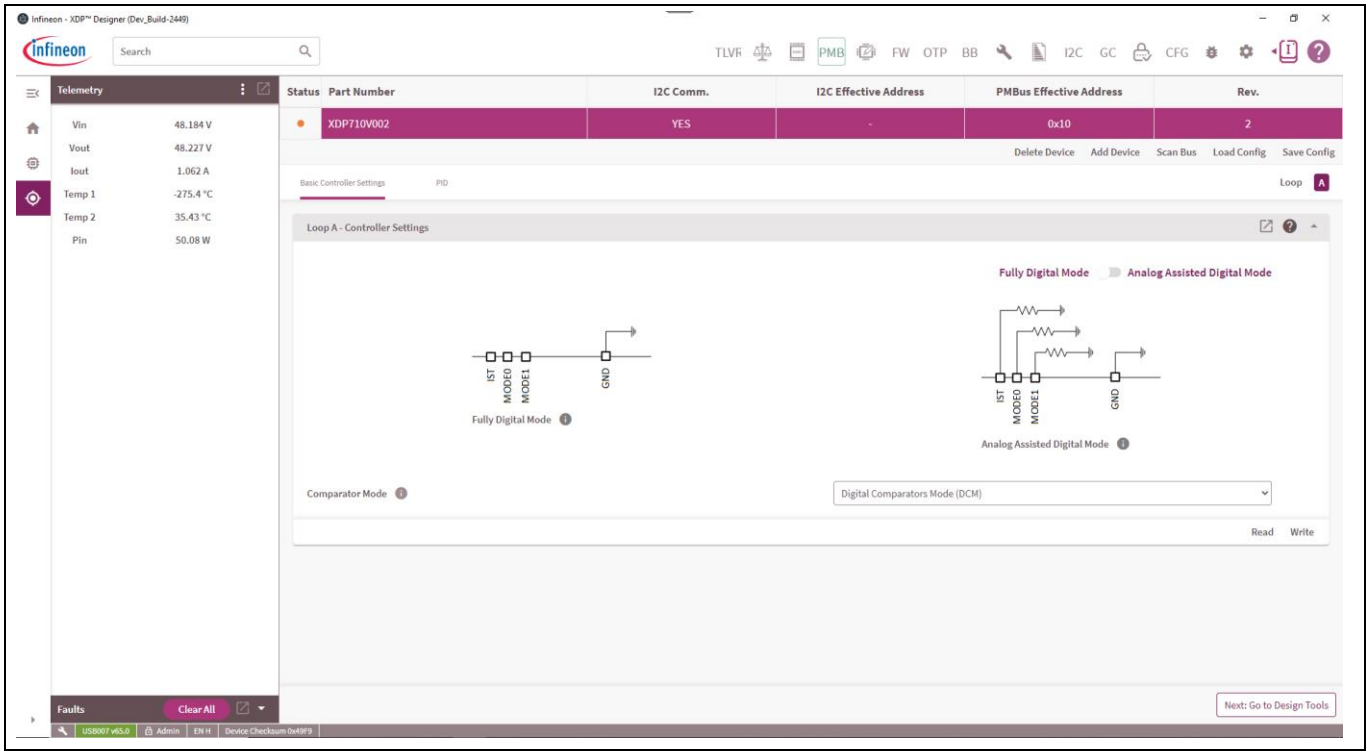

Figure 3 XDP™ Designer GUI

3 XDP710-002 evaluation platform

The following sections describe the XDP710-002 Evaluation Board highlighting the electrical specifications, block diagram, schematics, layout, bill of materials (BOM), and different configuration settings that could be used on this evaluation board.

3.1 Electrical specifications

- Input and output voltage range is 12 V DC to 80 V DC.
- The input current range is up to 50 A but can be varied by the number of paralleled MOSFET adapter boards.
- The MOSFET adapter boards can be removed and added to the evaluation board based on the required current level.

3.2 Block diagram

The XDP710-002 evaluation platform consists of:

- **XDP710-002 Evaluation Board**: Positive input hot-swap controller and eFuse circuitry designed to run a single-channel controller including its corresponding FET. Additionally, communication, control, and protection circuitry is included.
- **USB007A1 dongle**: It is an interface between the PC and XDP710-002 that communicates via the USB dongle. The commands are sent by the XDP™ Designer GUI to the XDP710-002, which are received via the PMBus communication. The USB007A1 dongle translates from USB to PMBus; enabling the XDP710-002.
- **XDP™ Designer GUI**: It is a software GUI tool for XDP710-002 PMBus communication that commands configuration and general control.

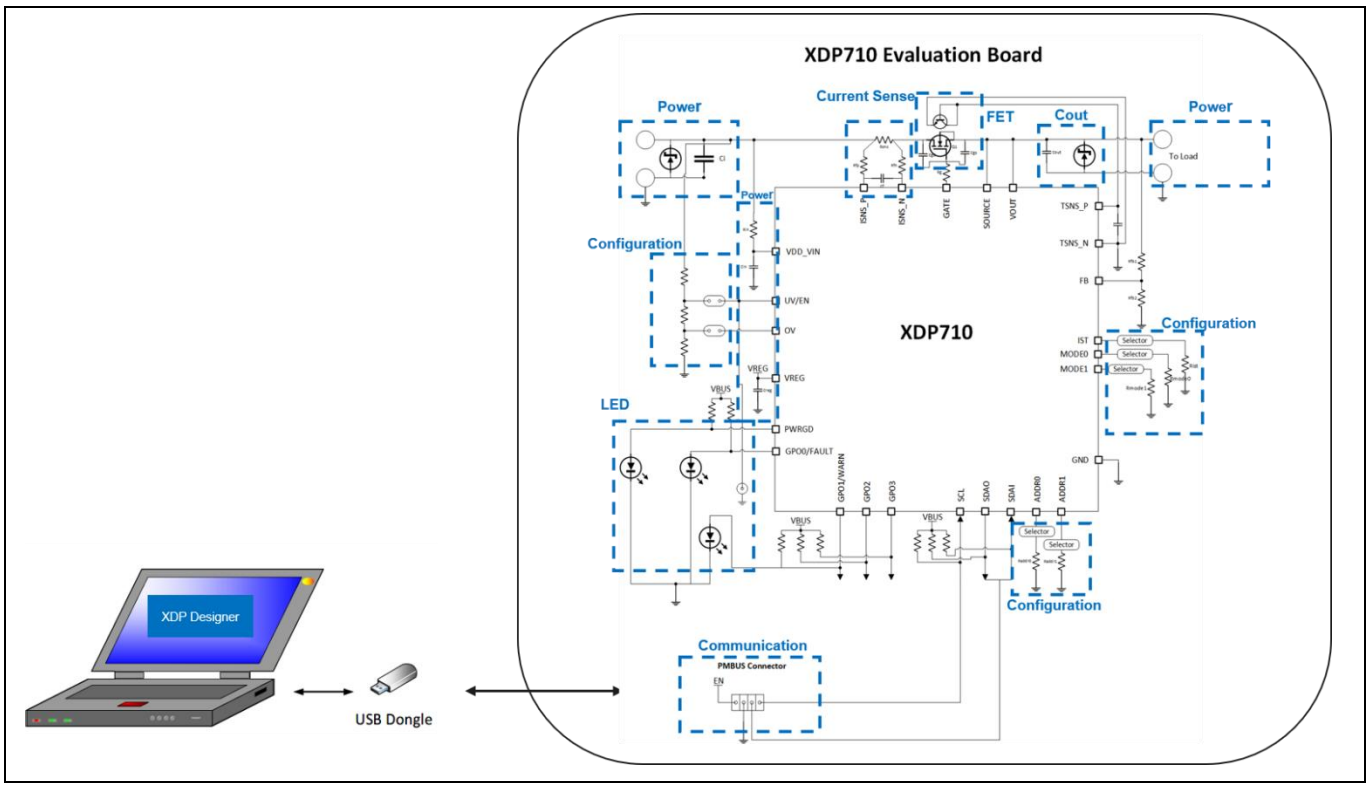

Figure 4 XDP710-002 evaluation platform

3.3 XDP710-002 Evaluation Board schematics

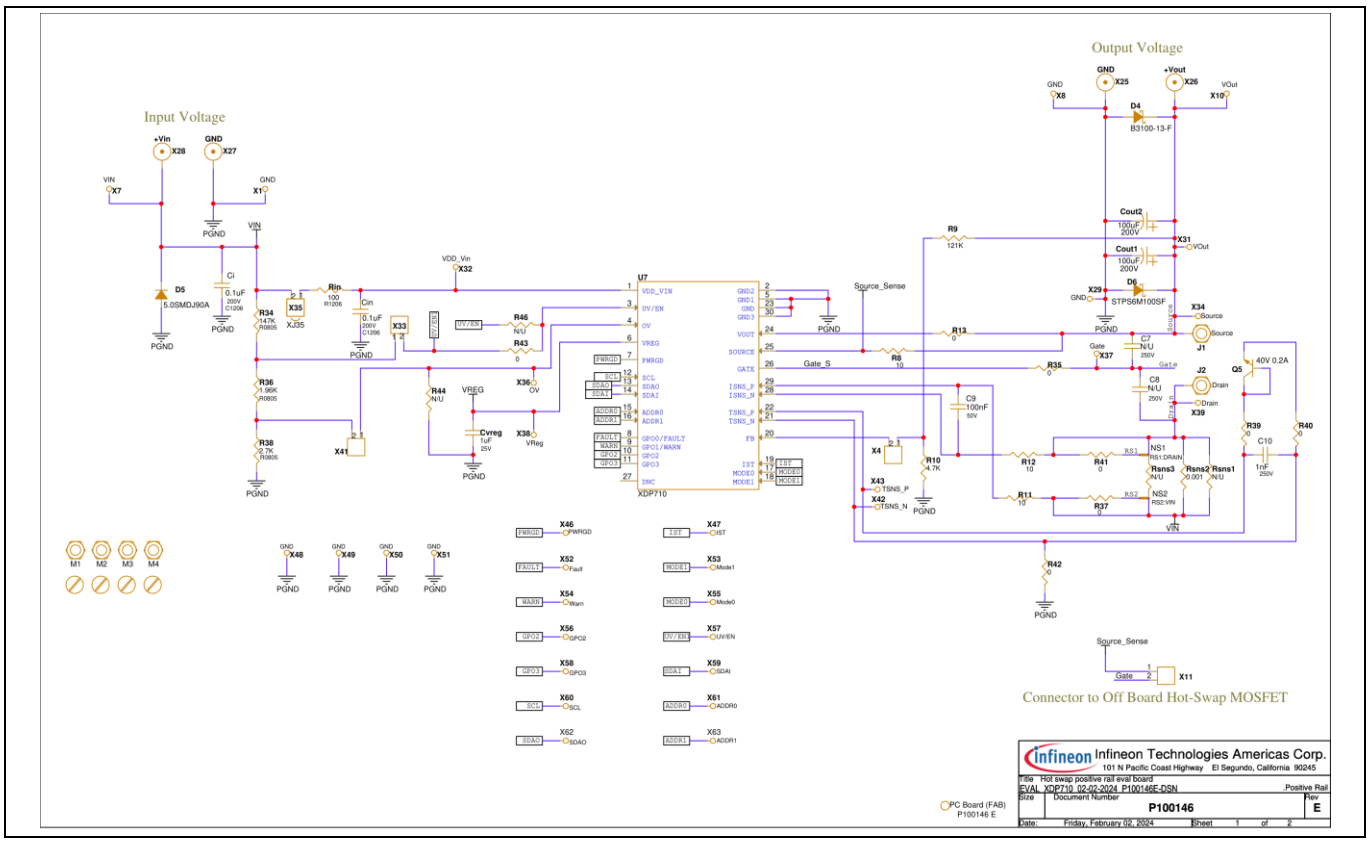

Figure 5 Main IC

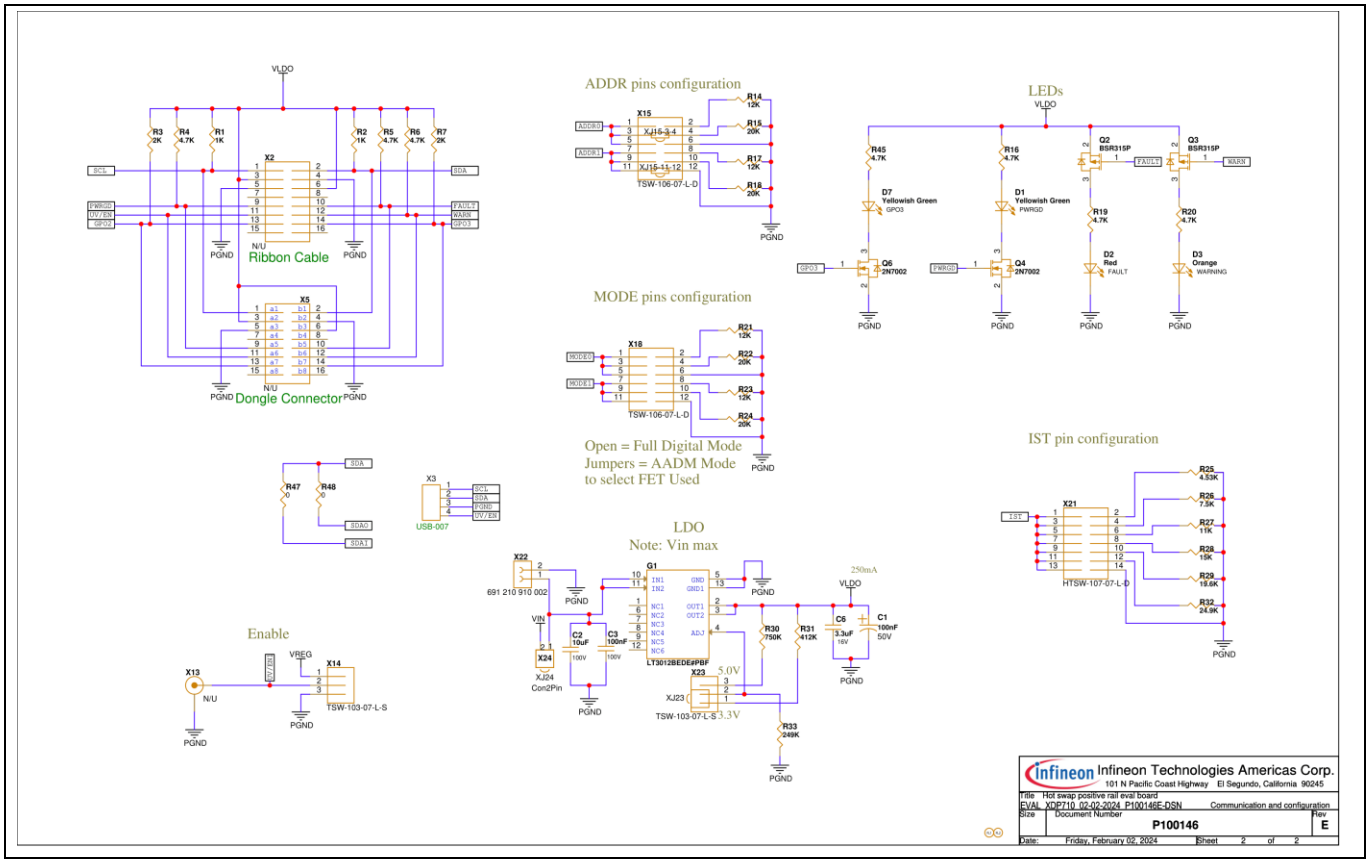

Figure 6 Main PCBA ports

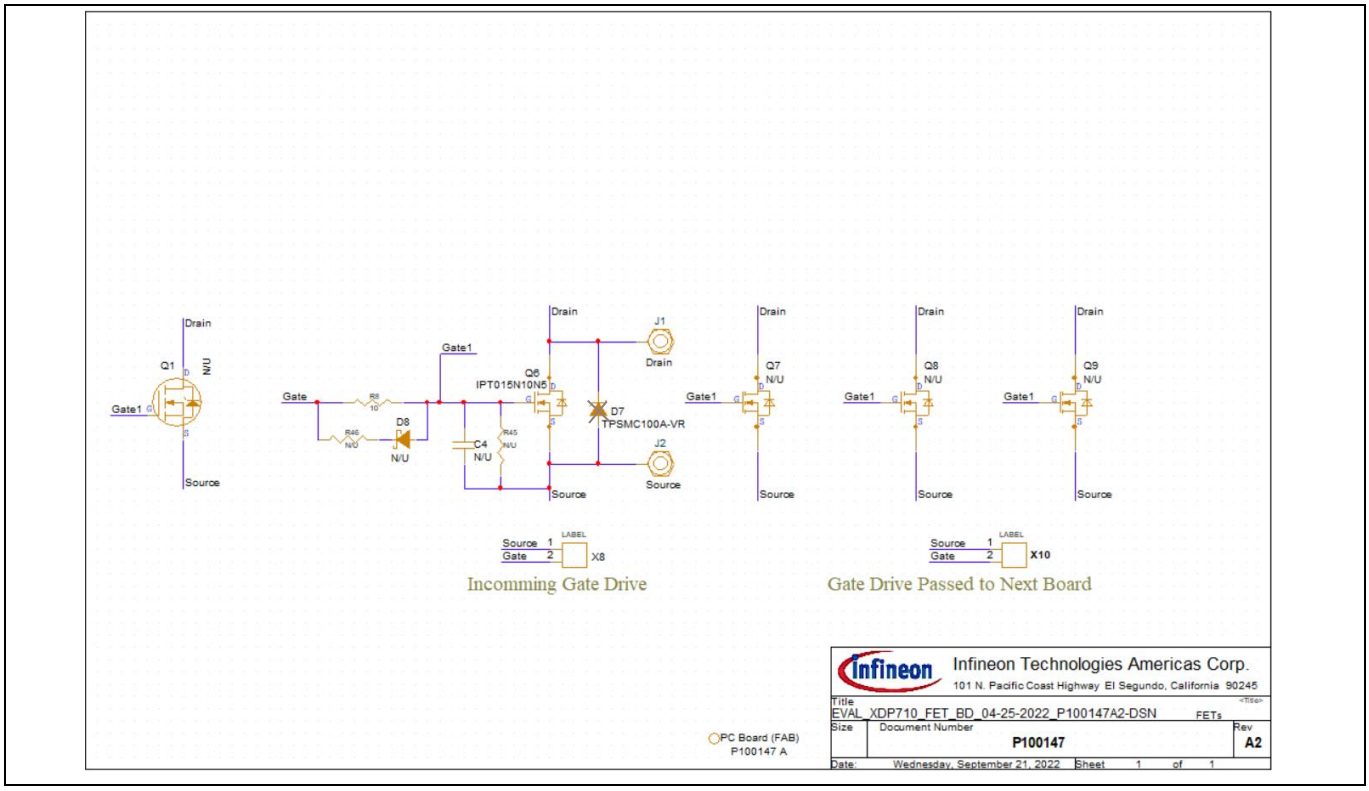

Figure 7 MOSFET PCBA

3.4 XDP710-002 Evaluation Board layout

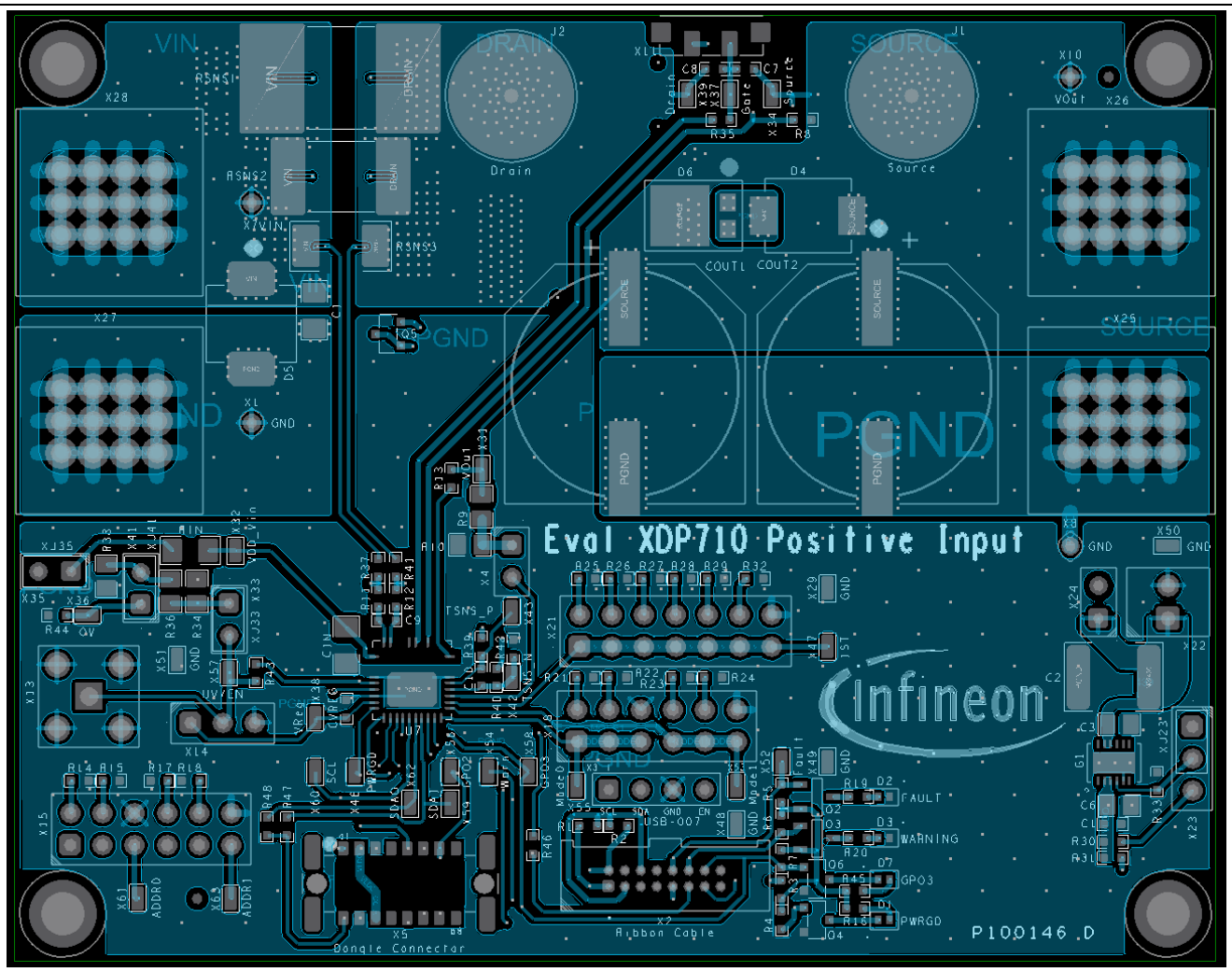

Figure 8 Top layer layout of main PCB

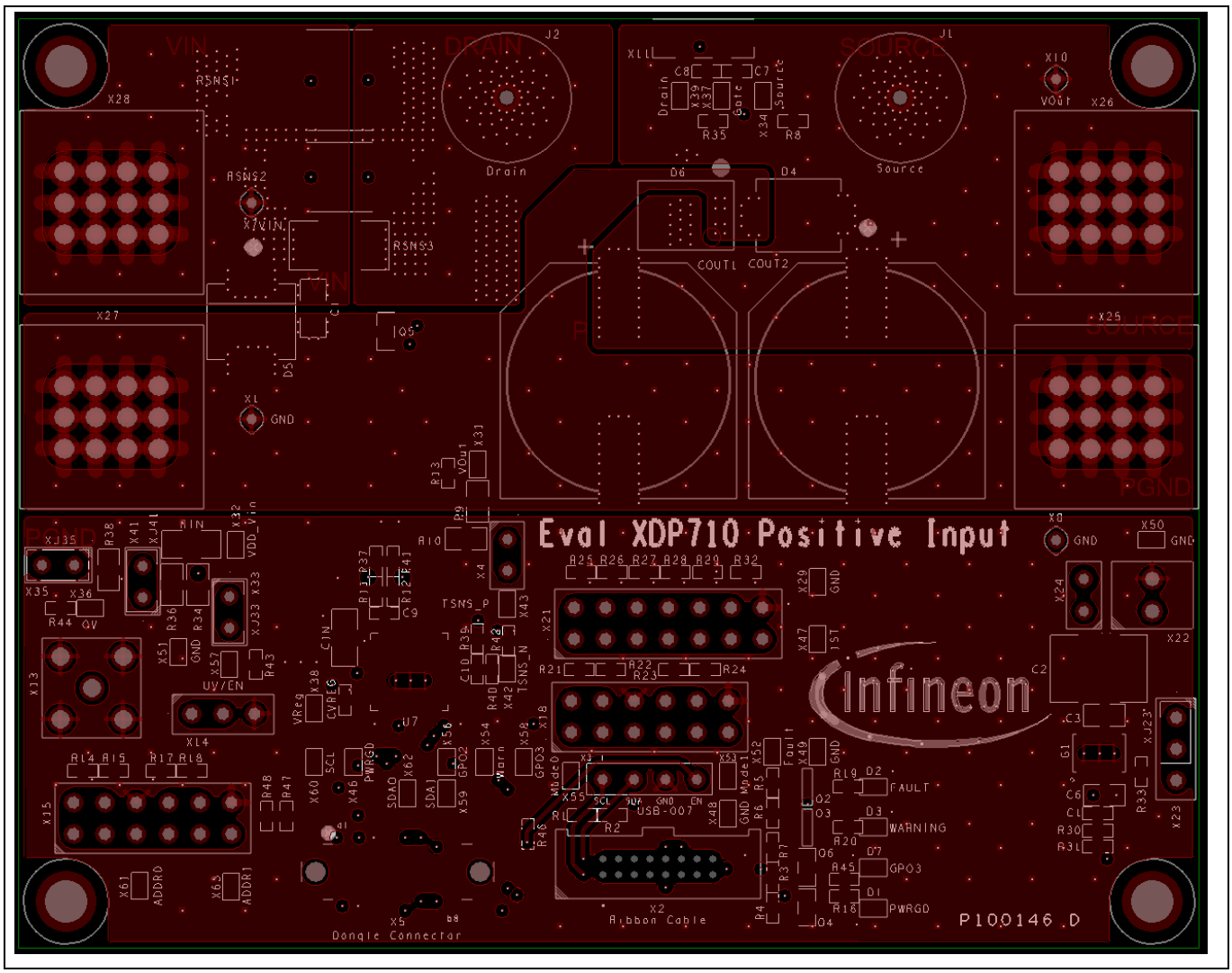

Figure 9 Mid 1 layer layout of main PCB

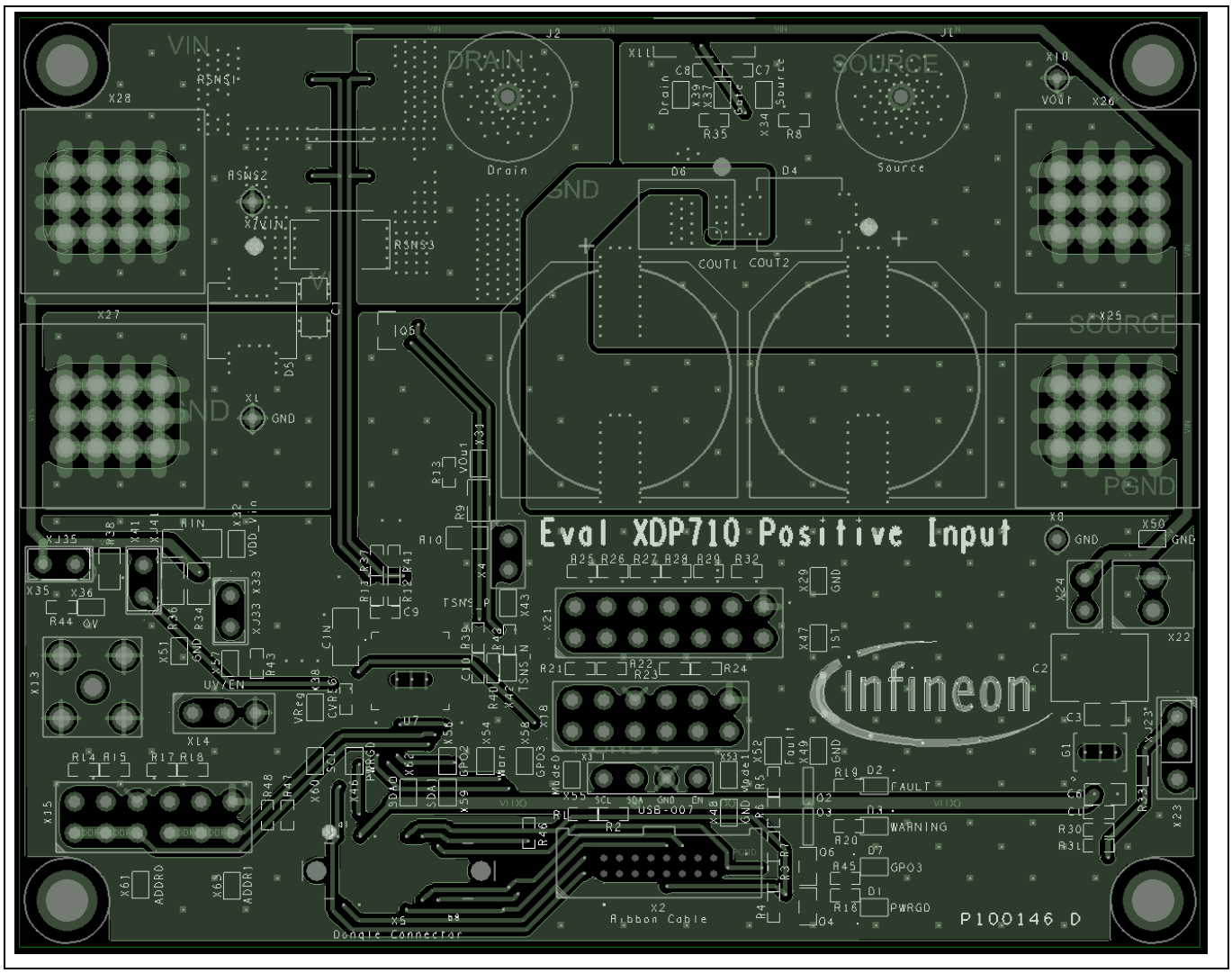

Figure 10 Mid 2 layer layout of main PCB

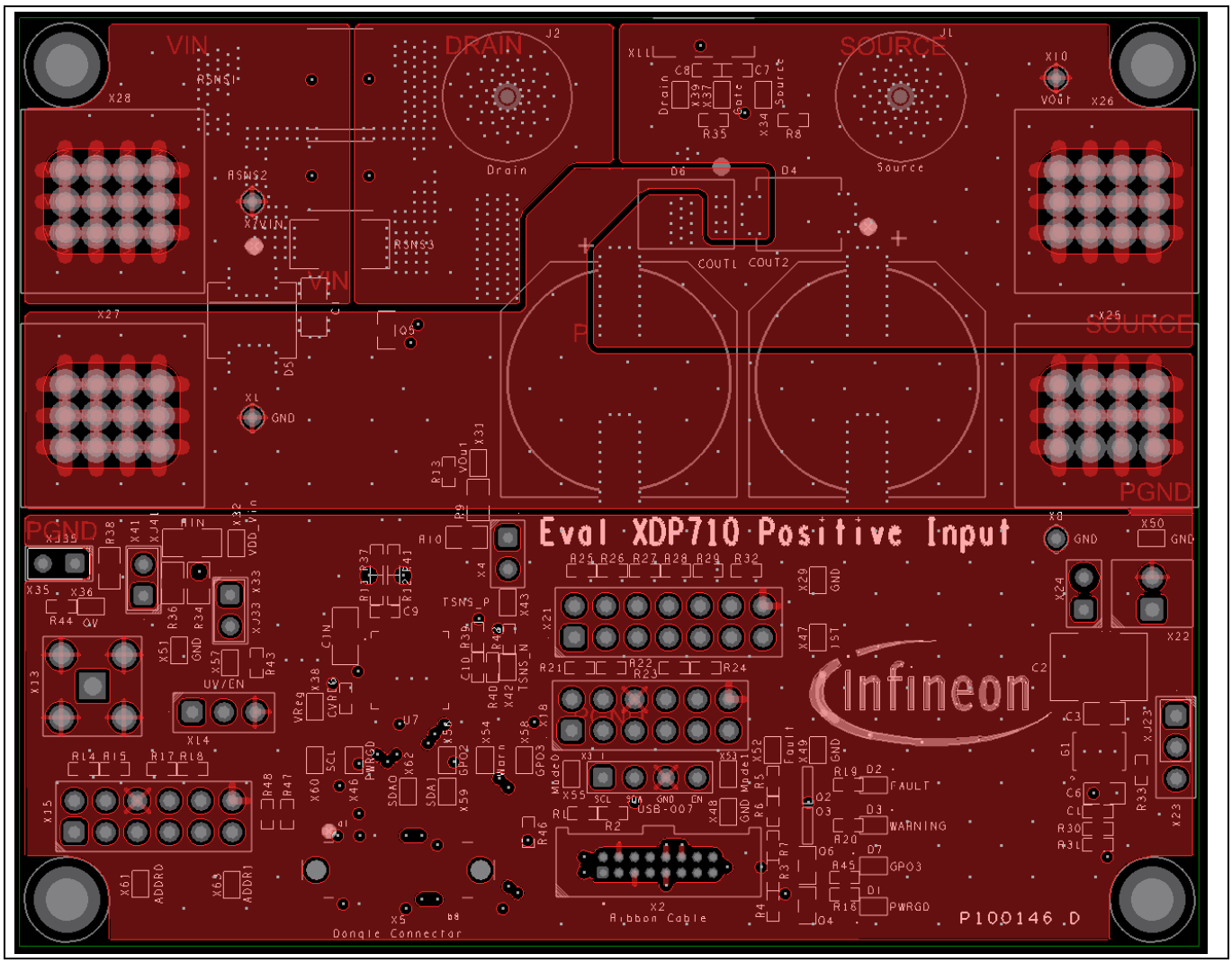

Figure 11 Bottom layer layout of main PCB

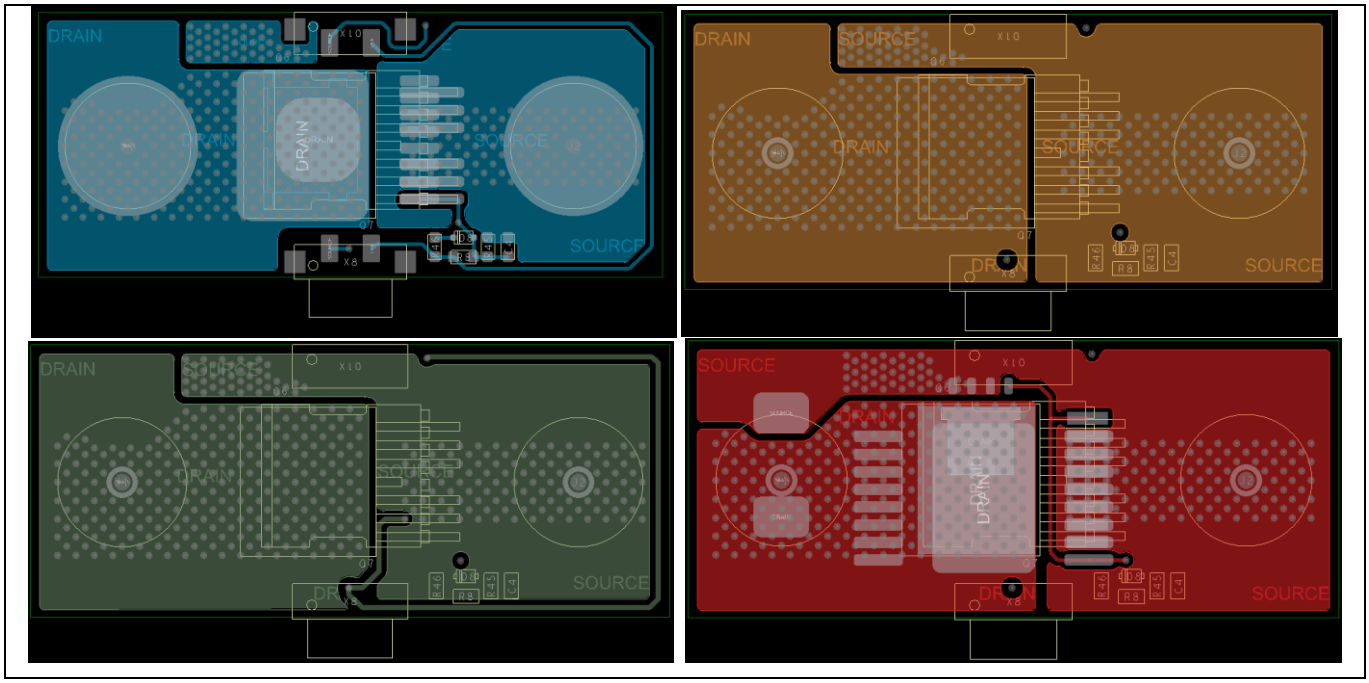

Figure 12 Top, Mid 1, Mid 2, and bottom layer layouts of MOSFET PCB

3.5 XDP710-002 Evaluation Board bill of materials

Table 2 BOM for the main PCBA

Item	Qty	Reference designator	Value	Characteristics	Manufacturer	Part number
1	2	Cin, Ci	0.1 µF	200 V X7R	Murata	GRM31CR72D104KW03L
2	2	Cout1, Cout2	100 µF	200 V Elect.	Panasonic	EEVEB2D101M
3	1	Cvreg	1 µF	25 V X7R	Murata	GRM188R71E105KA12
4	2	C1, C9	100 nF	50 V X7R	Murata	GRM188R71H104JA93
5	1	C2	10 µF	100 V X7S	TDK	C5750X7S2A106M230KB
6	1	C3	100 nF	100 V X7R	Kemet	C0805X104K1RACTU
7	1	C6	3.3 µF	16 V X7R	Murata	GRM21BR71C335KA99
8	2	C7, C8	N/A	–	–	N/A
9	1	C10	1 nF	250 V X7R	Murata	GRM188R72E102KW07
10	2	D1, D7	Yellowish green	–	Rohm Semiconductors	SML-P11MTT86R
11	1	D2	Red	–	Rohm Semiconductors	SML-P11UTT86R
12	1	D3	Orange	–	Rohm Semiconductors	SML-P11DTT86R
13	1	D4	B3100-13-F	–	Diodes Incorporated	B3100-13-F
14	1	D5	5.0SMDJ90A	–	Bourns	5.0SMDJ90A
15	1	D6	STPS6M100SF	–	STMicroelectronics	STPS6M100SF
16	1	G1	LT3012BEDE#PBF	–	Analog Devices	LT3012BEDE#PBF
17	2	J1, J2	SO-M5	–	Würth Elektronik	7466105R
18	4	M1, M2, M3, M4	MTG _Standoff	–	Keystone	2203
19	4	M5, M6, M7, M8	Screw PHMS 4-40 x 1/4	–	Keystone	9900
20	2	Q2, Q3	BSR315P	–	Infineon	BSR315P
21	2	Q4, Q6	2N7002	–	Infineon	2N7002
22	1	Q5	40 V 0.2 A	–	Nexperia	MMBT3904,215
23	1	Rin	100	1%	Panasonic	ERJ-8ENF1000V
24	1	Rsns1	N/A	9 W 1%	Bourns	Not used
25	1	Rsns2	0.001	8 W 1%	Bourns	CSS2H-3920R-1L00F

XDP710-002 evaluation platform

Item	Qty	Reference designator	Value	Characteristics	Manufacturer	Part number
26	1	Rsns3	N/A	6 W 1%	Bourns	Not used
27	2	R1, R2	1k	1%	Panasonic	ERJ-3EKF1001V
28	2	R3, R7	2k	1%	Panasonic	ERJ-3EKF2001V
29	7	R4, R5, R6, R16, R19, R20, R45	4.7k	1%	Panasonic	ERJ-3EKF4701V
30	3	R8, R11, R12	10	1%	Panasonic	ERJ-3EKF10R0V
31	1	R9	121k	1%	Vishay	CRCW0805121KFK
32	1	R10	4.71k	1%	Yageo	RC0603FR-074K7L
33	10	R13, R35, R37, R39, R40, R41, R42, R46, R47, R48	0	1%	Panasonic	ERJ-3GEY0R00V
34	4	R14, R17, R21, R23	12k	1%	Panasonic	ERJ-3EKF1202V
35	4	R15, R18, R22, R24	20k	1%	Panasonic	ERJ-3EKF2002V
36	1	R25	4.53k	1%	Panasonic	ERJ-3EKF4531V
37	1	R26	7.5k	1%	Panasonic	ERJ-3EKF7501V
38	1	R27	11k	1%	Panasonic	ERJ-3EKF1102V
39	1	R28	15k	1%	Panasonic	ERJ-3EKF1502V
40	1	R29	19.6k	1%	Panasonic	ERJ-3EKF1962V
41	1	R30	750k	1%	Panasonic	ERJ-3EKF7503V
42	1	R31	412k	1%	Panasonic	ERJ-3EKF4123V
43	1	R32	24.9k	1%	Panasonic	ERJ-3EKF2492V
44	1	R33	249k	1%	Panasonic	ERJ-3EKF2493V
45	1	R34	147k	1%	Vishay	CRCW0805147KFK
46	1	R36	1.96k	1%	Vishay	CRCW08051K96FK
47	1	R38	2.7k	1%	Vishay	CRCW08052K70FK
48	1	R43	N/A	1%	–	Not used
49	1	R44	N/A	1%	–	Not used
50	1	U7	XDP710-002	–	Infineon Technologies	XDP710-002
51	4	XJ23, XJ33, XJ35, XJ41	CON2_Jumper	–	Sullins	SPC02SYAN
52	4	X1, X7, X8, X10	Loop	–	Keystone	5020
53	1	X2	N/A	–	Samtec	SHF-108-01-L-D-TH

Item	Qty	Reference designator	Value	Characteristics	Manufacturer	Part number
54	1	X3	Con4	–	Würth Elektronik	61300411121
55	5	X4, X24, X33, X35, X41	Con2Pin	–	Harwin	M20-9770246
56	1	X5	N/A	–	Harwin	M55-7001642R
57	1	X11	SOC2	–	AVX	209159002101916
58	1	X13	N/A	–	Samtec	SMA-J-P-H-ST-TH1
59	2	X14, X23	TSW-103-07-L-S	–	Samtec	TSW-103-07-L-S
60	2	X15, X18	TSW-106-07-L-D	–	Samtec	TSW-106-07-L-D
61	1	X21	HTSW-107-07-L-D	–	Samtec	HTSW-107-07-L-D
62	1	X22	691 210 910 002	–	Würth Elektronik	691210910002
63	4	X25, X26, X27, X28	PEM NUT 8-32 SCREW 8-32 x 3/8	–	PEM McMaster-Carr	KF2-832-ET 91241A652
64	28	X29, X31, X32, X34, X36, X37, X38, X39, X42, X43, X46, X47, X48, X49, X50, X51, X52, X53, X54, X55, X56, X57, X58, X59, X60, X61, X62, X63	SMD loop	–	Harwin	S2761-46R

Table 3 BOM for MOSFET PCBA

Item	Qty	Reference designator	Value	Voltage	Manufacturer	Part number
1	1	BRD1	PC board (FAB)	–	–	P100147 A
2	1	C4	N/A	X7R	Murata	Not used
3	1	D7	N/A	–	Littelfuse	Not Used
4	1	D8	N/A	–	–	Not used
5	1	Q1	N/A	100 V 147 A	Infineon	Not used
6	1	Q6	IPT015N10N5	100 V 300 A	Infineon	IPT015N10N5ATMA1
7	1	Q7	N/A	100 V 300 A	Infineon	Not used
8	1	Q8	N/A	100 V 300 A	Infineon	Not used

Item	Qty	Reference designator	Value	Voltage	Manufacturer	Part number
9	1	Q9	N/A	100 V 354 A	Infineon	Not used
10	1	R8	10	1%	Panasonic	ERJ-3EKF10R0V
11	1	R45	N/A	1%	–	Not used
12	1	R46	N/A	1%	–	Not used
13	1	X8	PLUG2	–	AVX	109159002101916
14	1	X10	SOCK2	–	AVX	209159002101916

3.6 XDP710-002 Evaluation Board default settings

See the jumpers on the board as shown in Table 4.

Table 4 Jumper settings

Reference designator	Default configuration	Usage
X4	Open	• **Shorted**: Connects FB to voltage divider for over/undervoltage sensing • **Open**: This header can be left open for digital comparator mode (DCM)
X14	Open	• **Shorted 1 to 2**: Connects UV/EN to VREG • **Shorted 2 to 3**: Connects UV/EN to GND • **Open**: UV/EN can be driven by an SMA connector or dongle
X15	Between pins 5 and 6 and in between pins 11 and 12	ADDRx pins configuration to 0x10. Move the jumpers to change the PMBus address.
X18	Open	MODEx pins configuration. Leave them open for fully digital mode (FDM).
X21	Open	IST pin configuration
X23	Shorted 1 to 2	• **Shorted 1 to 2**: VLDO = 3.3 V • **Shorted 2 to 3**: VLDO = 5 V This header must not be left open
X24	Shorted	• **Shorted**: LDO is supplied by VIN • **Open**: LDO is supplied by external source connected to X22
X33	Open	• **Shorted**: Connects UV/EN to voltage divider • **Open**: UV/EN can be driven by SMA or dongle
X35	Shorted 1 to 2	• **Shorted**: VDD_VIN is connected to the input voltage • **Open**: A current meter can be connected to this header
X40	Open	R_{sns} voltage drop sense
X41	Open	• **Shorted**: Connects OV to voltage divider • **Open**: This header can be left open for DCM

Table 5 Resistors and capacitors

Reference designator	Default configuration	Notes
R8, R35	Check depending on FET	R8 = D^2PAK or TOLL R35 = SSO8
C7, C8	DNF (remove if populated on board)	C_{gd} and C_{gs} of FET
R37, R41, R12, R11	Check depending on sense resistor	Can be always populated: 0 Ω
C9	DNF	R_{sns} filter
R39, R40	Shorted 0 Ω	Temperature sensor filter
C10	1 nF	Temperature sensor filter
R46	0 Ω	• **Populate**: If EN is driven by dongle • **DNF**: If EN is driven by header or SMA
R43	DNF	• **Populate**: If EN is driven by header or SMA • **DNF**: If EN is driven by dongle
Rin	100 Ω	Or lower depending on test slew rate requirements
R30, R31, R33	820 k, 470 k, 270 k, respectively	LDO feedback voltage dividers
R11, R12	10 ohm	For high dV/dt application to avoid damage to the SENSE pins

The rest of the components are populated as specified in the schematics.

3.7 R_{sns}

Three different footprints are provided to support different resistor sizes. The current onboard resistor is 1 mΩ. There are optional footprints that are optimized for resistor packages on board as follows:

- R_{sns1}: 5930, 5931
- R_{sns2}: 3920, 3921, 2818
- R_{sns3}: 2512

3.8 FET board

The XDP710-002 Evaluation Board comes with an option to parallel up to three FET boards to increase the current-carrying capability for testing heavy loads, and shows the capability of driving multiple parallel N-channel MOSEFTs. Necessary heatsinking is provided via a copper bus bar but forced cooling is needed if operating at currents greater than 50 A.

3.9 Different FET footprint options on FET board

The FET footprint supports D^{2}PAK, TOLL, and SS08 packages in the following positions:

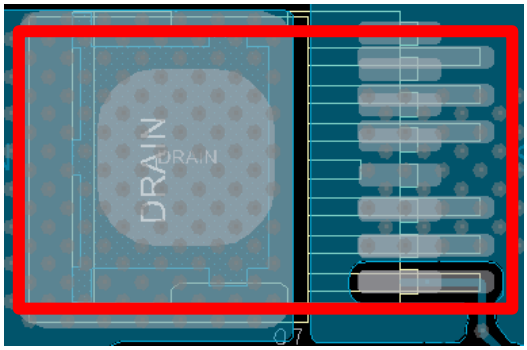

Figure 13 D2PAK and D2PAK7 position (top side)

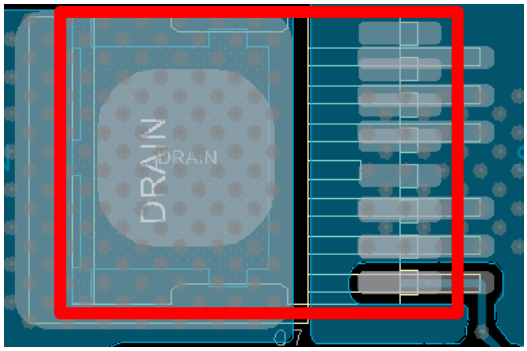

Figure 14 TOLL position (top side)

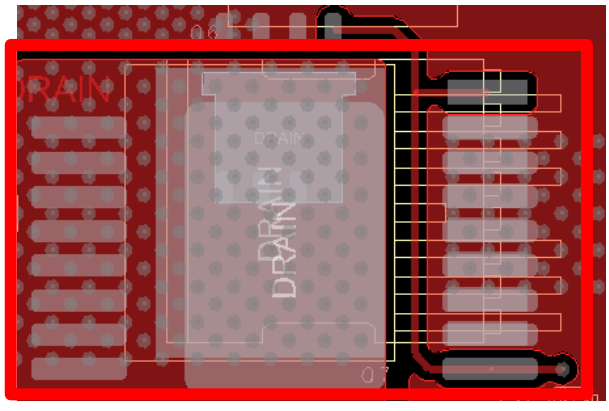

Figure 15 SS08 position (bottom side)

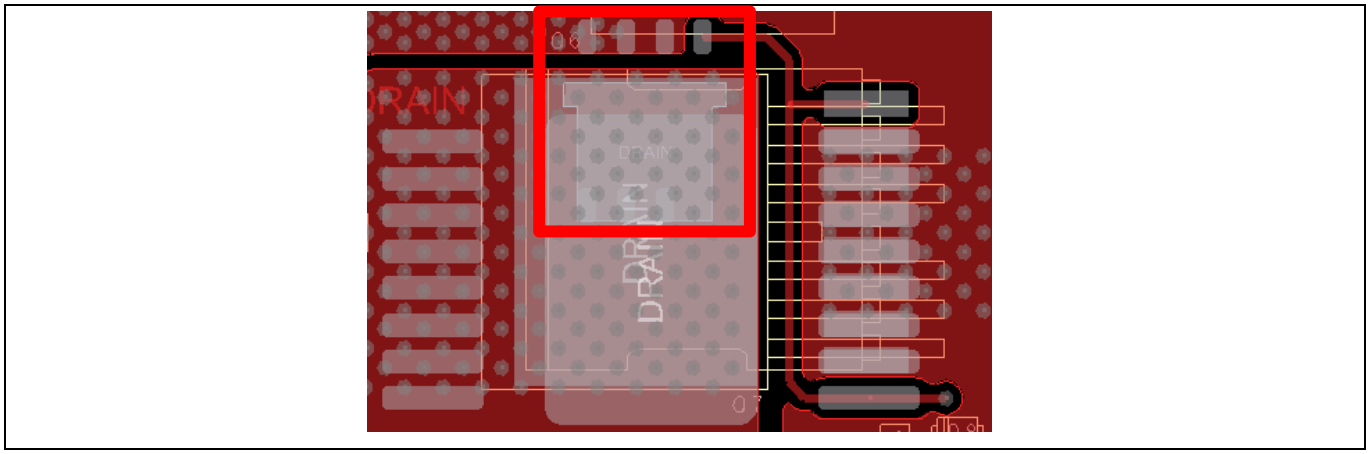

Figure 16 PG-TSON-8-3 position (bottom side)

3.10 USB007A dongle schematics

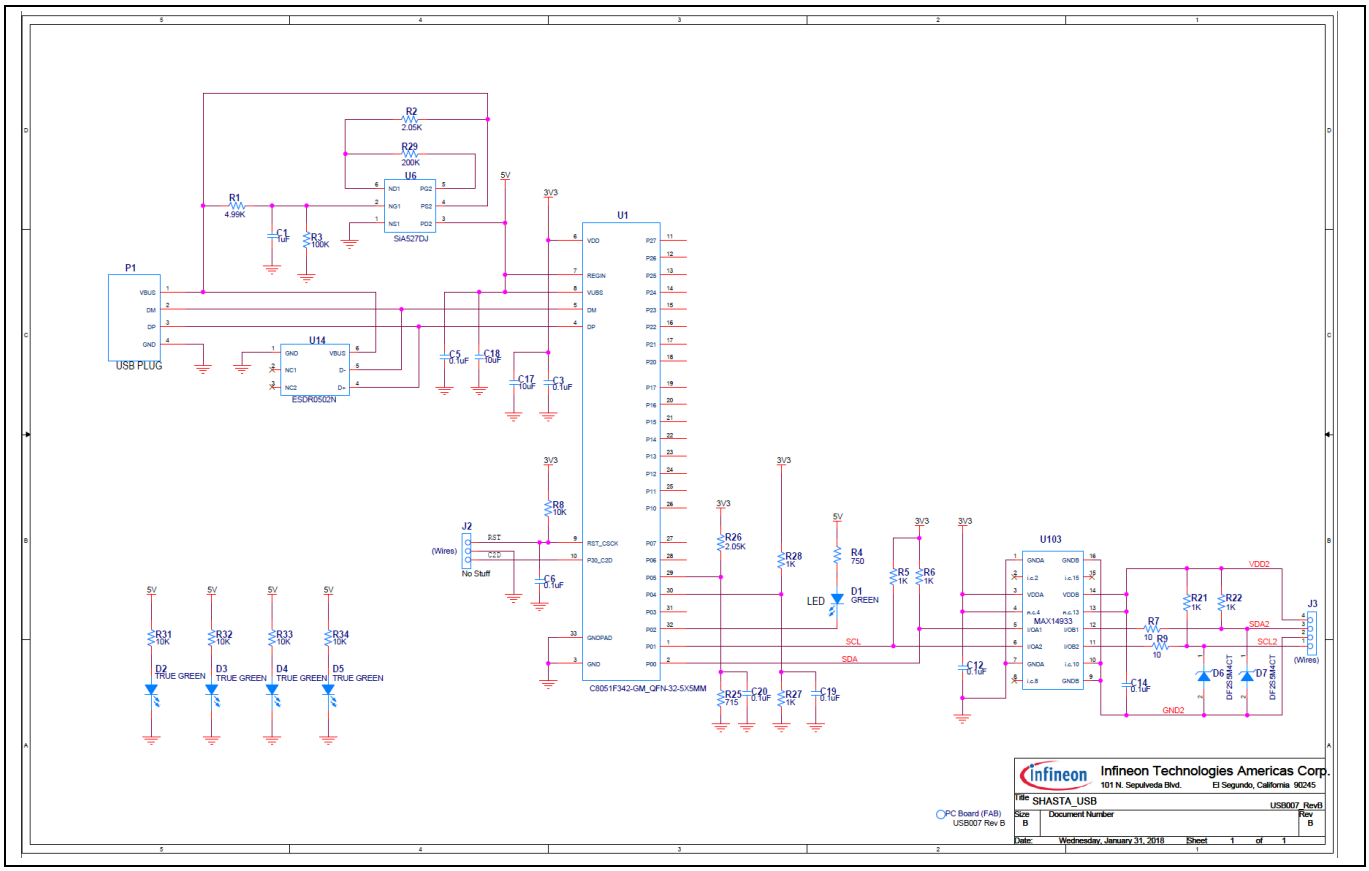

Figure 17 USB007A1 dongle schematics

4 Programming, setup, and turn-on instructions

Set up the system as follows:

- Connect the USB007 dongle to the XDP710-002 Evaluation Board X3 as shown in Figure 18.
- Connect the USB007 dongle to a PC USB port.
- Ensure that the jumpers are connected properly.
- Connect 48 V from VDD_VIN (X28 connector) to the GND (X27) on the left of the board.

XDP710-002 powers up as soon as VDD_VIN is equal to or greater than 5.5 V. At this point, communication and programming is possible, but the FET will be off. To turn on the FET, a minimum of 9 V is required, after which the following registers must be programmed at a minimum to turn on the device.

- FET select
- R_{sns}

The UV/EN is controlled by a dongle; it will hold the signal down until it is toggled manually or can be controlled by the UV/EN1, which is controlled by the X14 header. It must be held low until the necessary registers are written. Use one signal at a time.

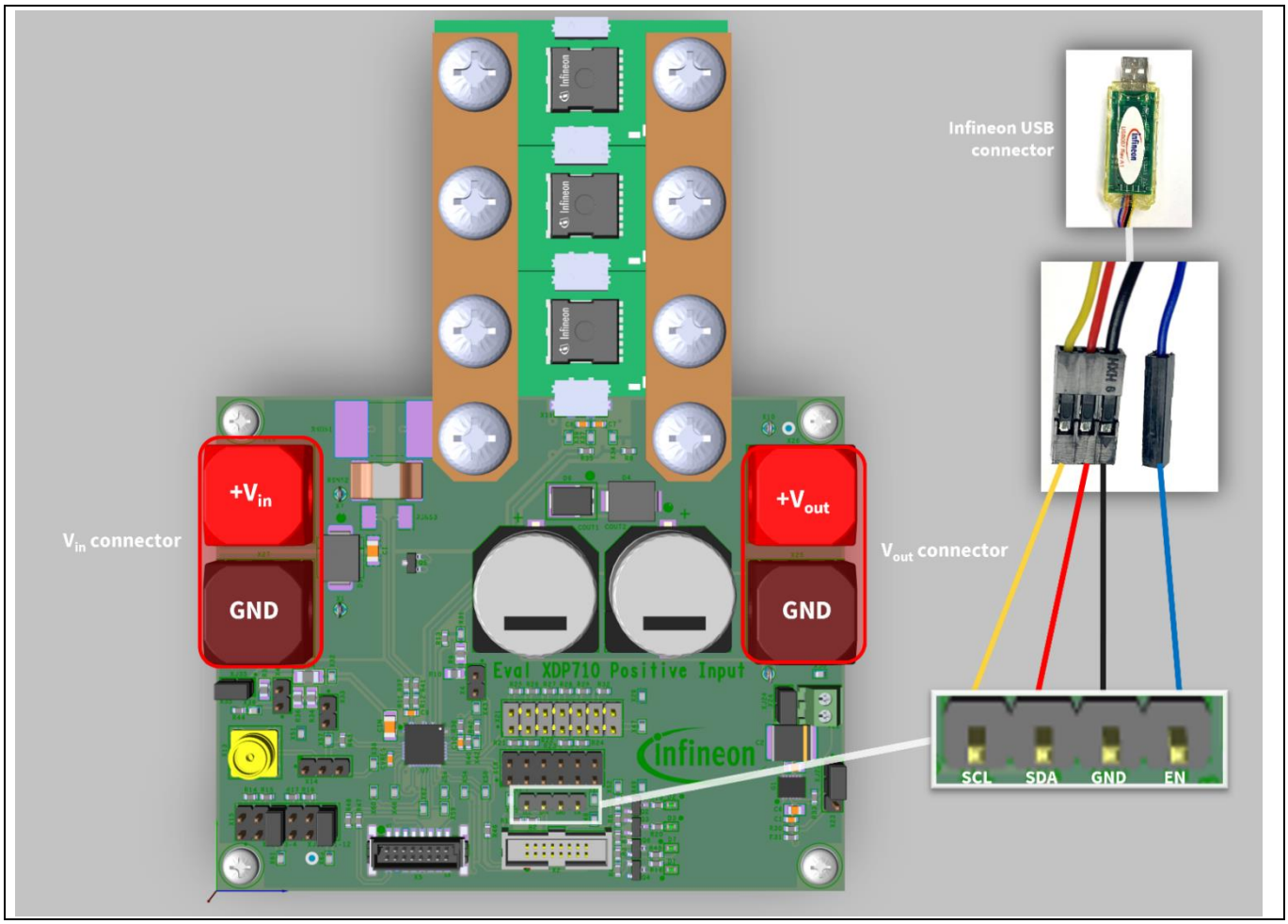

Figure 18 XDP710-002 Evaluation Board and dongle setup

4.1 XDP™ Designer communication setup

Install the XDP™ Designer from the Infineon Development Center.

The following sections explain how to configure and test the evaluation board and dongle using the XDP™ Designer software.

4.1.1 Dongle connection in XDP™ Designer

- Open the XDP™ Designer GUI and then wait for a few moments and check the bottom status bar for the dongle connection.
- If the highlighted area, as shown in Figure 19, turns green and displays **USB007**, then the dongle has been successfully detected by the GUI.
- Ensure that the enable signal is low (EN L); if not then click on it to toggle to **EN L** from EN H.

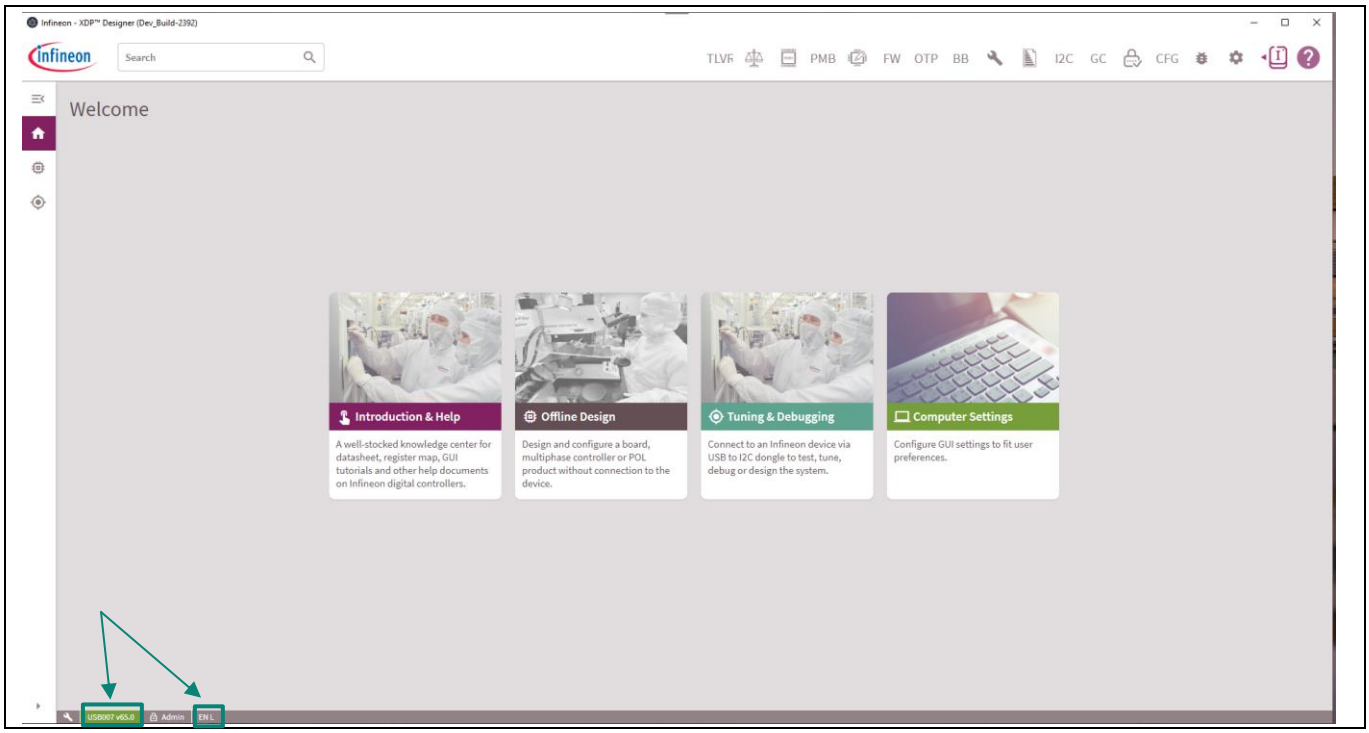

Figure 19 USB007A1 detection on XDP™ Designer

4.1.2 Detecting XDP710-002

- Click the button highlighted in Figure 20 and then wait for a few seconds; the device should be detected by the GUI automatically. If the device is not detected on its own, then click **Scan For Devices**, as shown in Figure 21.

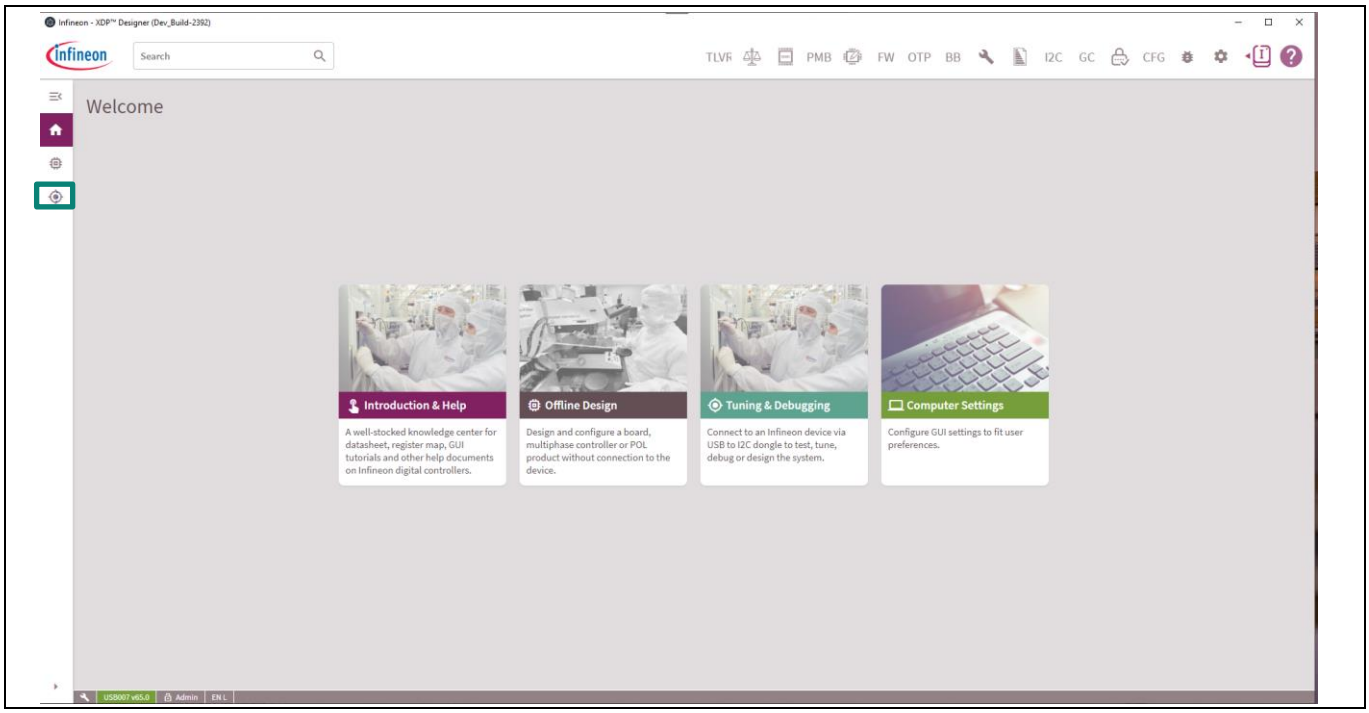

Figure 20 XDP710-002 detection

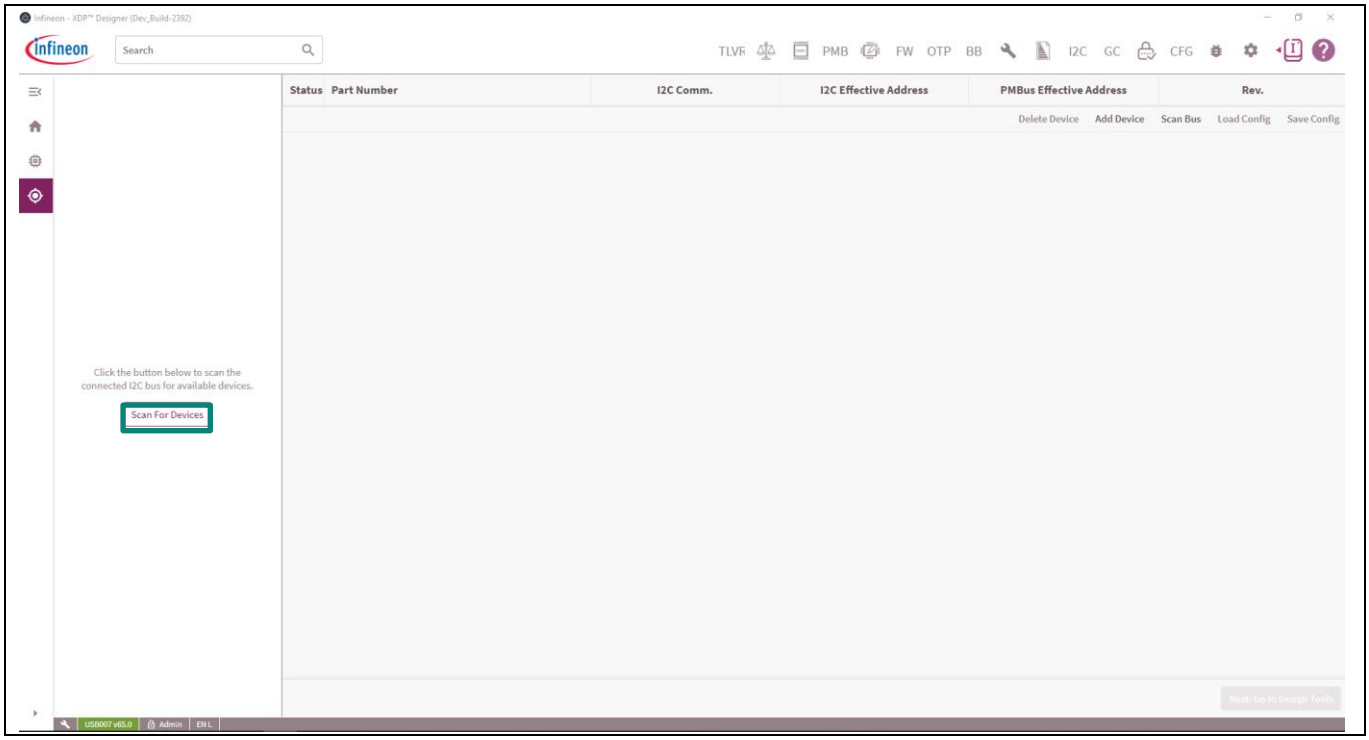

Figure 21 Scan For Devices to find XDP710-002

- The detected device will be XDP710V002, with the **Telemetry** displayed on the left as shown in Figure 22.

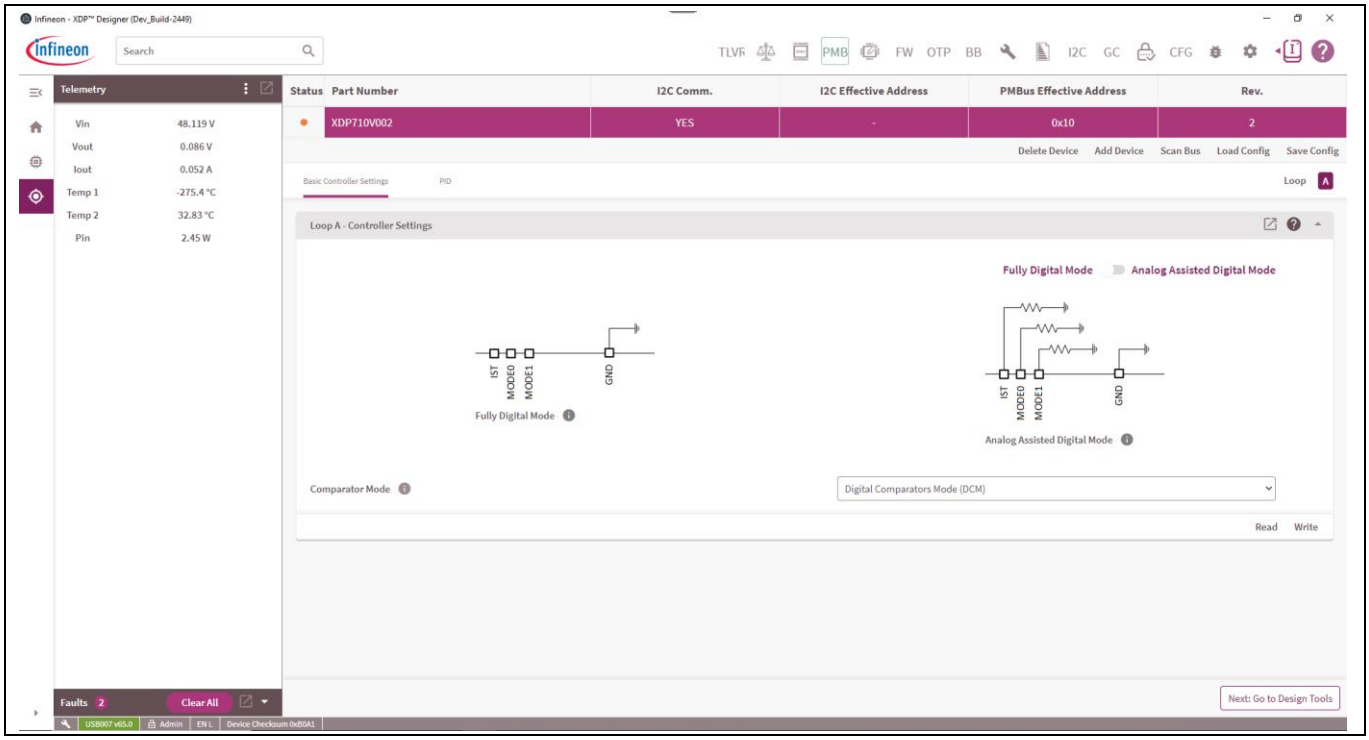

Figure 22 Live telemetry of the connected XDP710-002

- To see the register values currently stored on the device; click **PMB** button to see all the PMBus registers and the stored values in it, as shown in Figure 23.

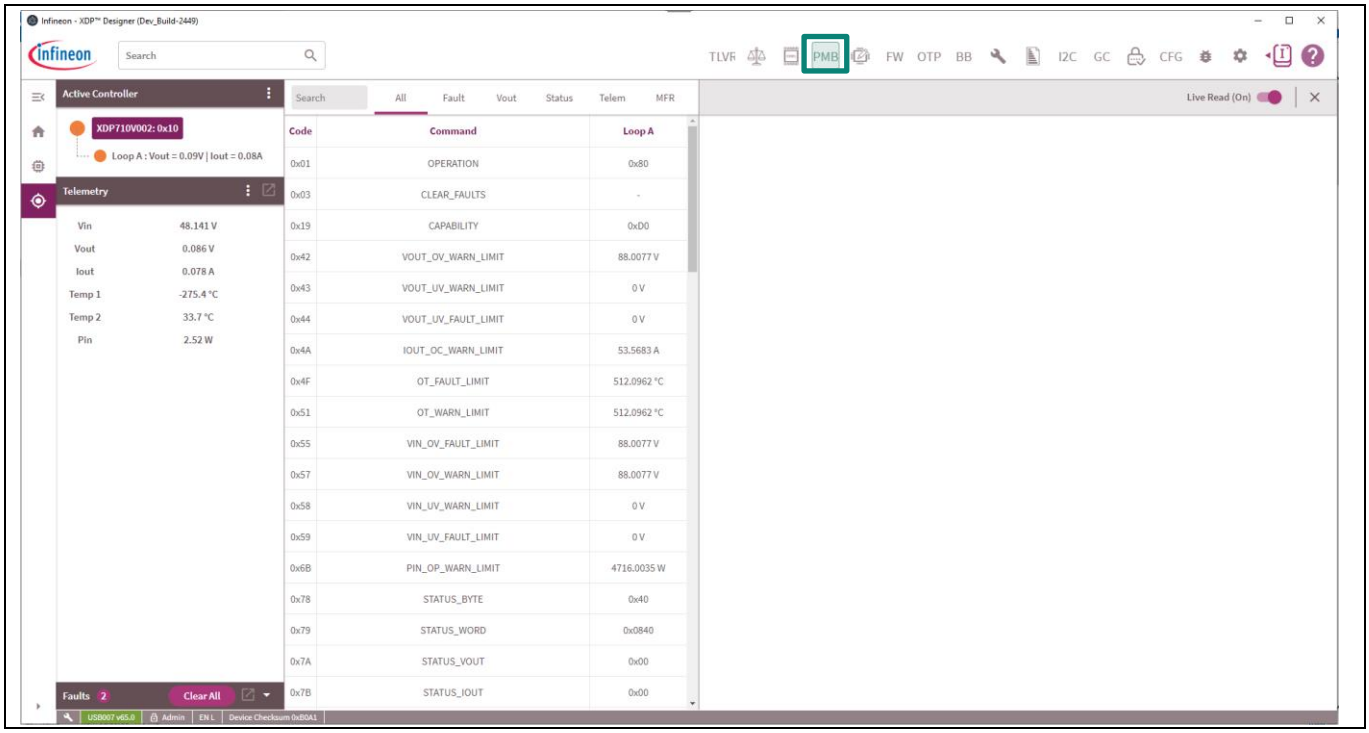

Figure 23 XDP™ Designer displaying all the PMBus registers of the connected XDP710-002

4.1.3 Reading and writing registers

- For editing any register individually, click on the corresponding PMBus register, make the necessary changes, and then click **Write** as shown in Figure 24.

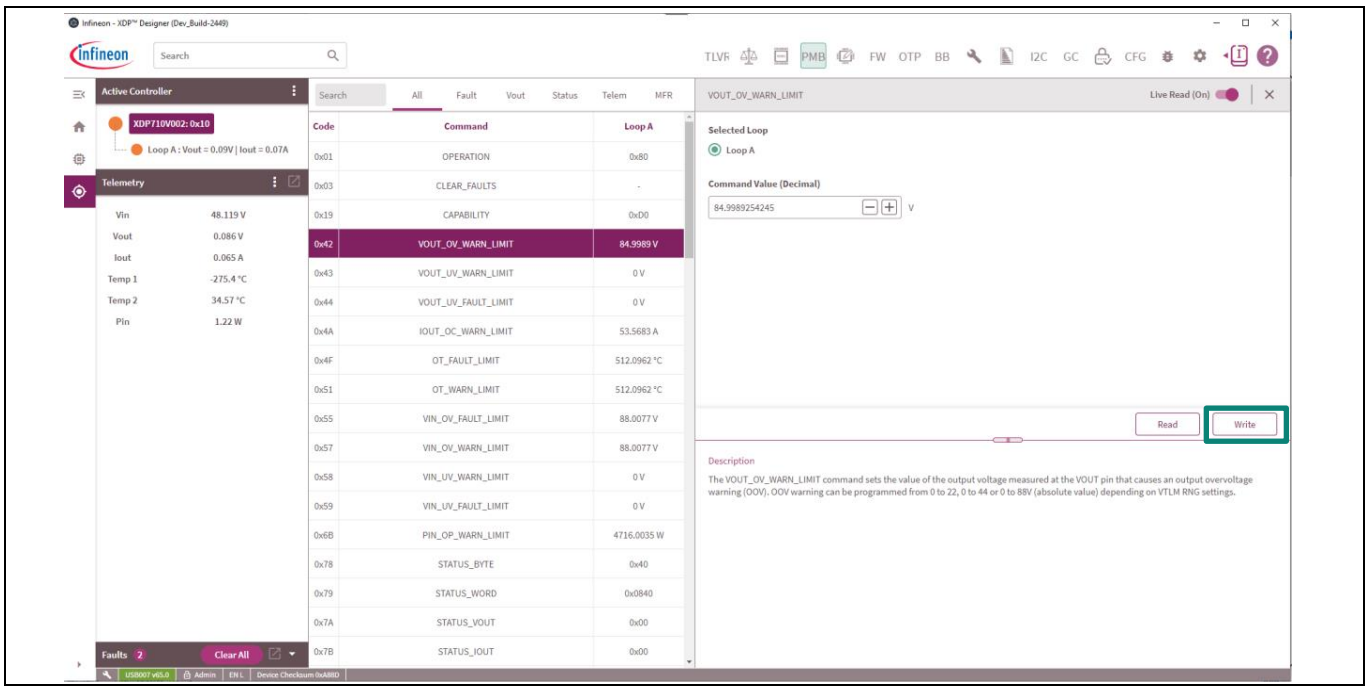

Figure 24 Editing VOUT_OV_WARN_LIMIT

- Most of the registers are updated automatically, but to read the latest values click **Read** to read the corresponding register values, as shown in Figure 25.

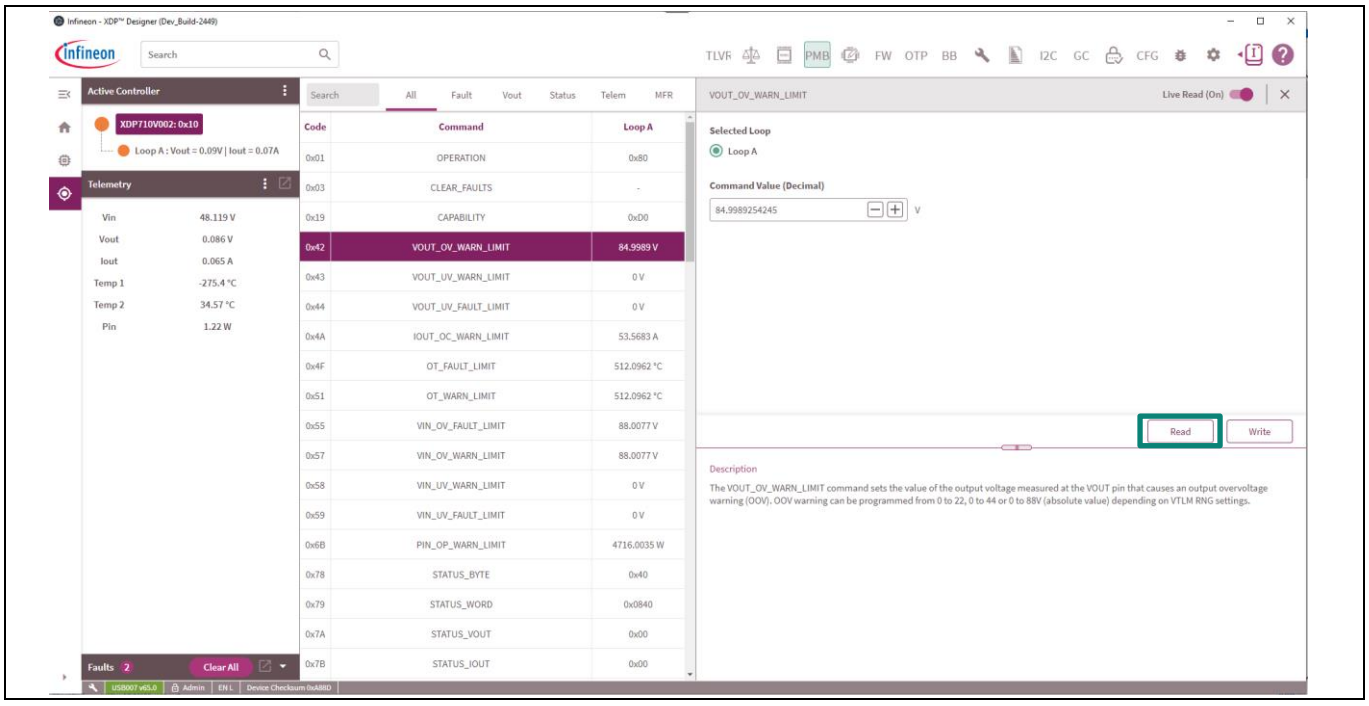

Figure 25 Reading VOUT_OV_WARN_LIMIT

4.1.4 Program FET

- If using analog-assisted digital mode (AADM), the FET will be pre-programmed, and skip this step.
- If using FDM, the FET must be programmed in the FET_SELECT bits of the MODE register (0xD1) according to the one populated on the board.
- The board has FET **IPT015N10N5** populated and to select this FET, the FET_SELECT bit should be modified to 0xA, then click **Write** as shown in Figure 26.

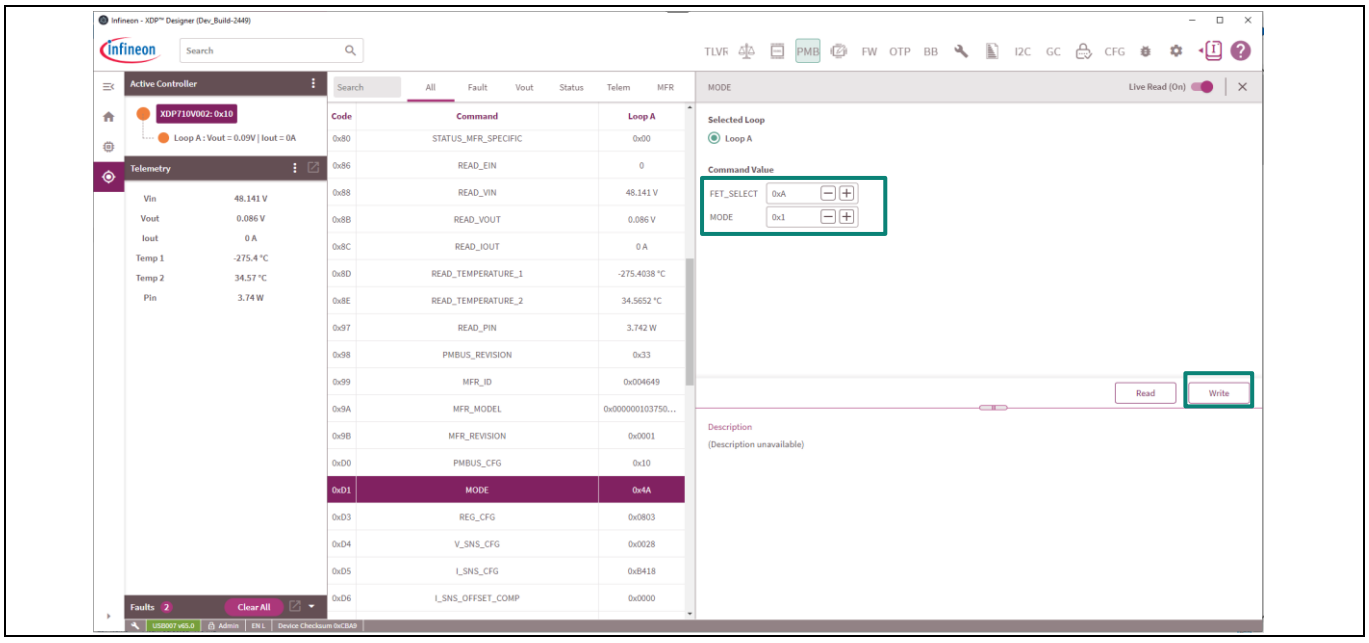

Figure 26 FET selection in FDM

4.1.5 Program Rsns

- The sense resistor value must be programmed in the R_{sns} bits of the REG_CFG register according to the one populated on the board.
- The board has R_{sns} **1 mΩ** populated. To select this resistor, modify the R_{sns} bit to 0xD, and then click **Write** as shown in Figure 27.

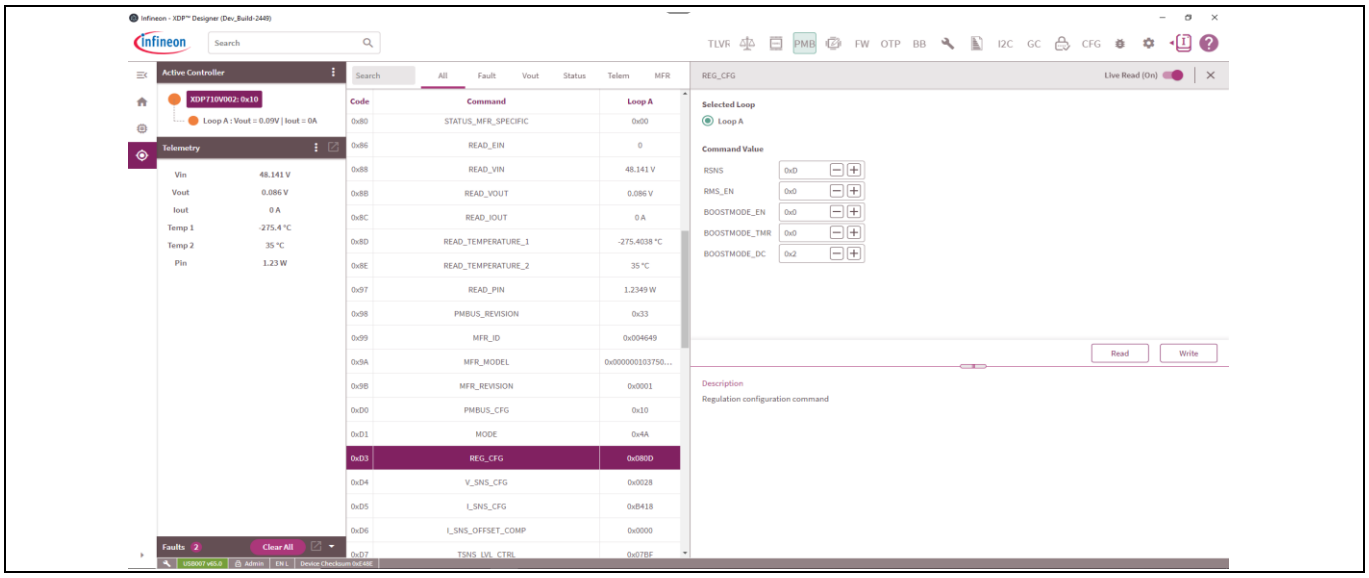

Figure 27 R_{sns} selection

4.1.6 Watchdog timer selection

Set the watchdog timer higher than the turn-on time to ensure that the watchdog timer does not expire before the turn-on and should also not be set much longer than the turn-on time to prevent damage to the FET in the event of a short-circuit during a turn-on. Leave the watchdog at the default value of 500 ms as shown in Figure 28.

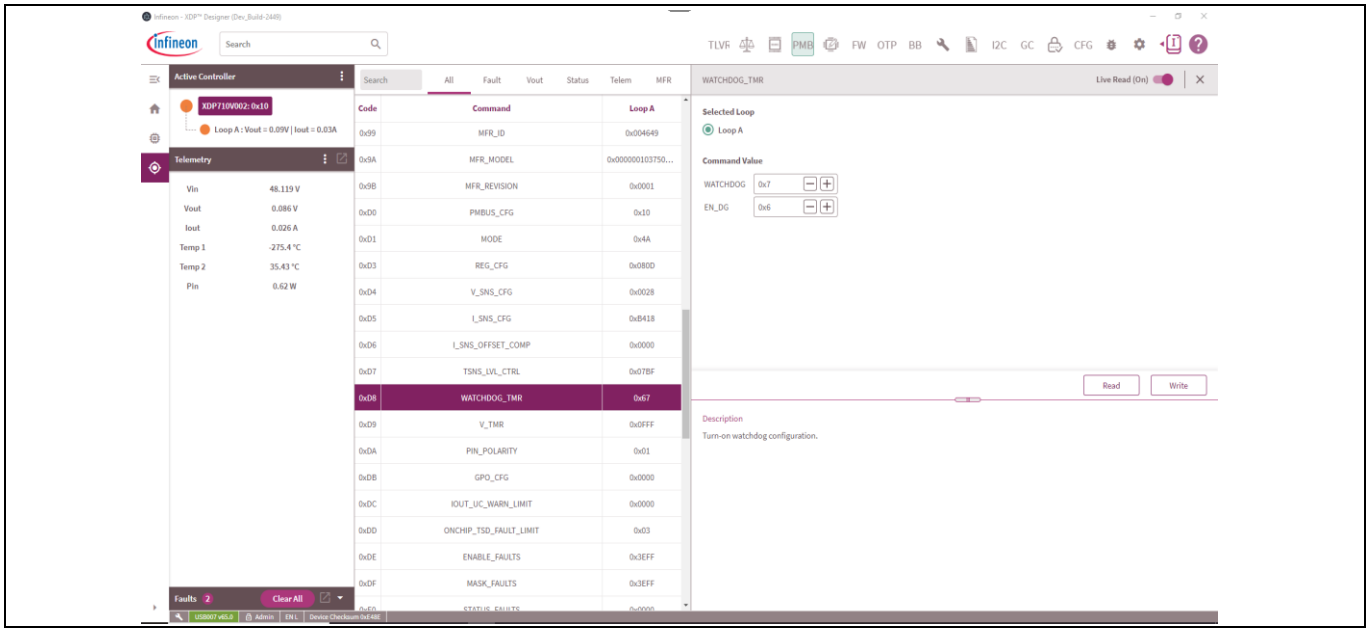

Figure 28 Watchdog timer selection

4.1.7 Program current sense range (CS_RNG) and start-up current limit (IST)

If using AADM, skip this step, as the resistor on the IST pin selects the start-up current limit and current sense range. In FDM, program the desired current sense range and start-up current limit in the I_SNS_CFG register (0x59), as shown in Figure 29.

Note: Do not set the current sense range as 100 mv with 1 mohm sense resistor. The SOA regulation loop does not work when (Current Sense Range/ R(mohm)) > 83.333 A.

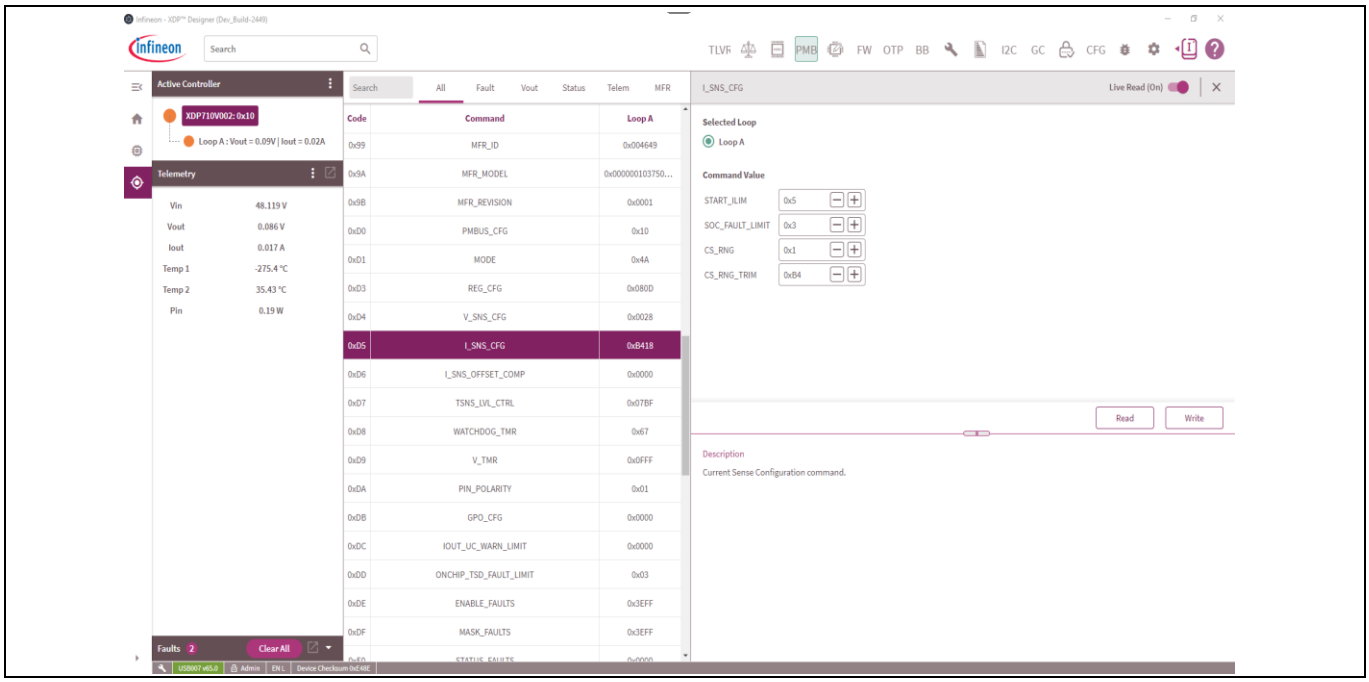

Figure 29 Current sense range and start-up current limit setting

4.1.8 Program VIN_UV_FAULT_LIMIT

If using AADM or ACM, skip this step, as the input undervoltage (UV) fault limit is set by external resistors on the UV pin. In the DCM, program the desired UV fault limit in the VIN_UV_FAULT_LIMIT register (0x59). If the UV fault is not used, the register can be programmed to 0 V, or the fault can be disabled.

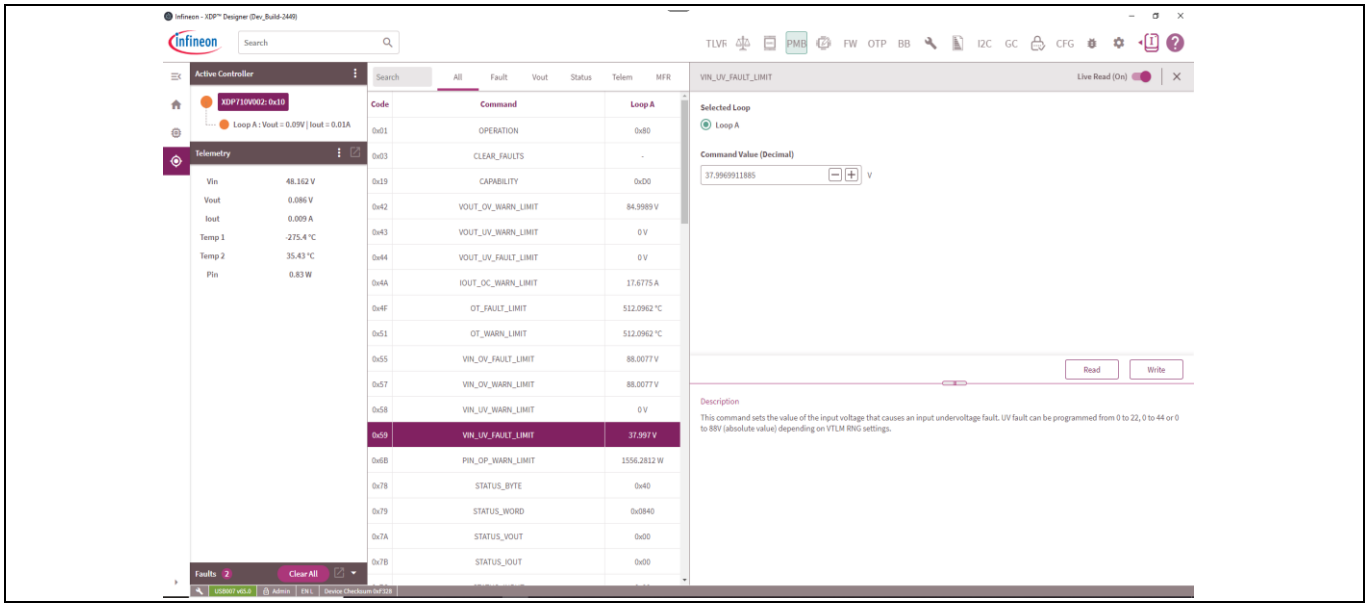

Figure 30 Program VIN_UV_FAULT_LIMIT

4.1.9 Program VIN_OV_FAULT_LIMIT

If using AADM or ACM, skip this step, as the input overvoltage (OV) fault limit is set by external resistors on the OV pin. In the DCM, program the desired OV fault limit in the VIN_OV_FAULT_LIMIT register (0x55). If the OV fault is not used, the register can be programmed to 88 V, or the fault can be disabled.

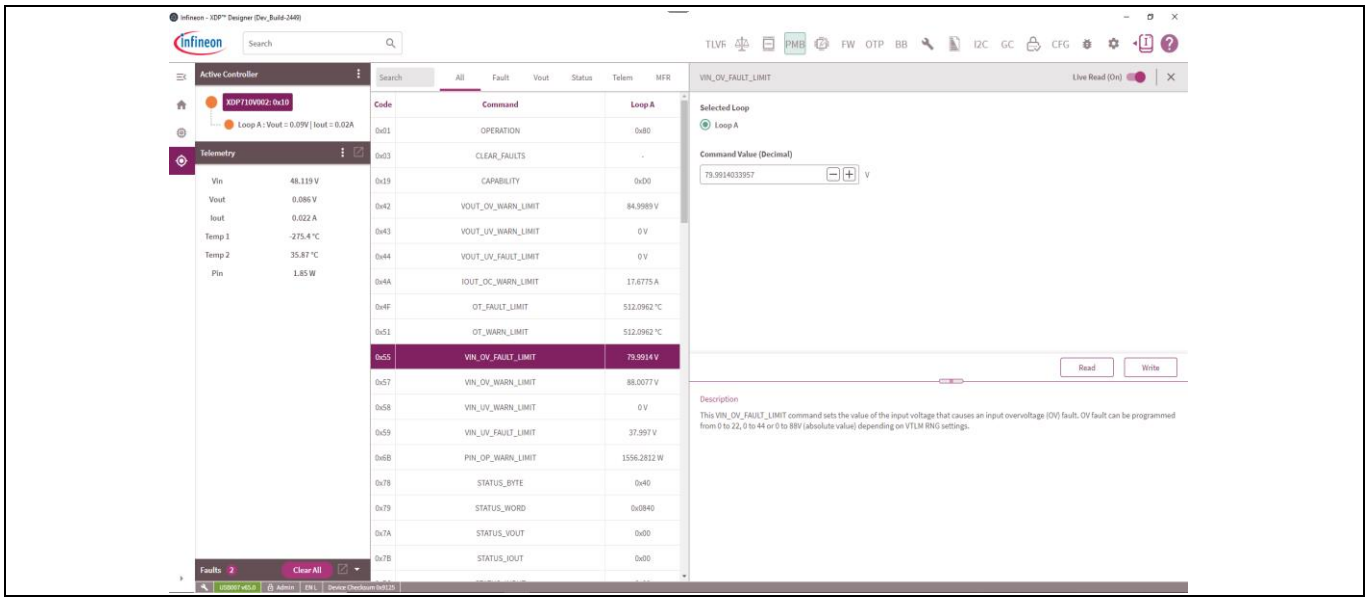

Figure 31 Program VIN_OV_FAULT_LIMIT

4.1.10 Program VOUT_UV_FAULT_LIMIT

If using AADM or ACM, skip this step, as the output UV fault limit is set by external resistors on the FB pin. In the DCM, program the desired output UV fault limit in the VOUT_UV_FAULT_LIMIT register (0x44). If the UV fault is not used, the register can be programmed to 88 V, or the fault can be disabled.

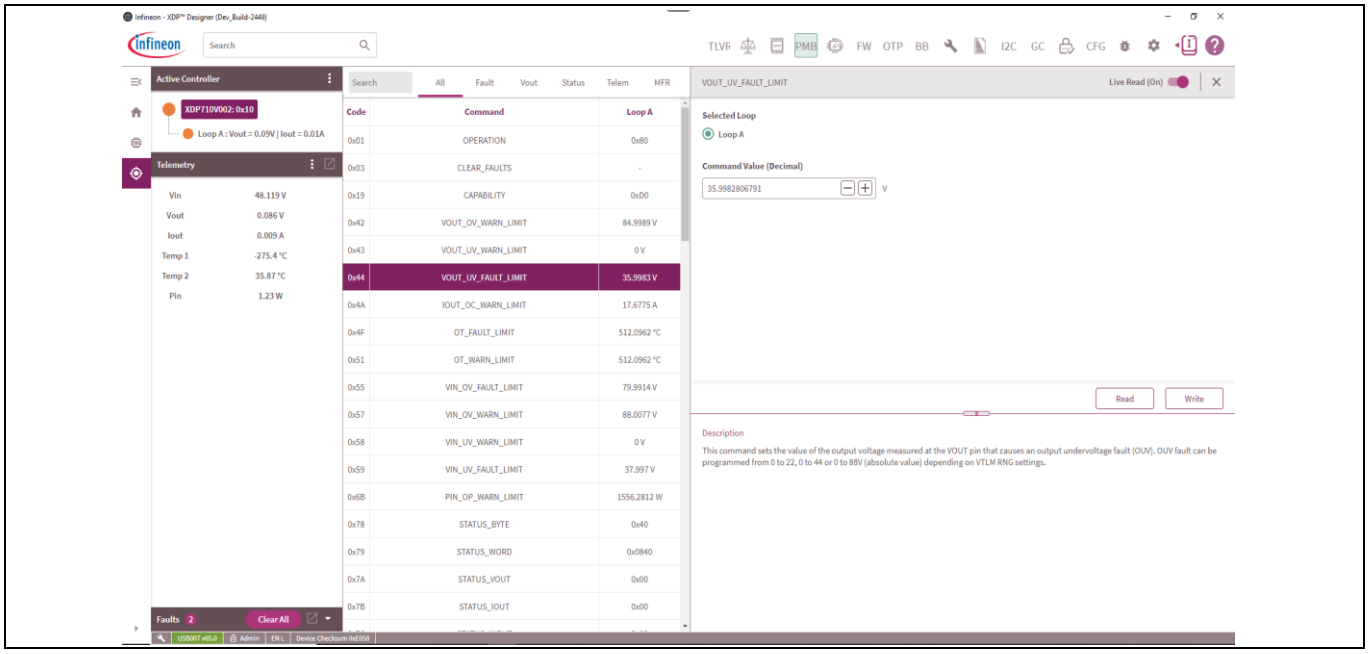

Figure 32 Program VOUT_UV_FAULT_LIMIT

4.2 XDP710-002 programming under different modes

There are two different modes in which the XDP710-002 can be operated; namely FDM and AADM. FDM has two selections: DCM and ACM. AADM or FDM can be selected based on the resistor connected on the Mode 0 and Mode 1 pins on the evaluation board. Based on the mode selected, different PMBus registers need to be configured.

4.2.1 FDM

FDM lets you select the FET, start-up current limit and current sense range via PMBus registers. In the DCM, the input and output voltage fault sensing is done via digital comparators and is based on the telemetry of the device, therefore, reducing the amount of analog circuitry needed while in an ACM. External voltage dividers are needed on the UV, OV, and FB pins, and the voltage on the divider is compared with the internal threshold to detect the faults. Voltage warnings are still set internally. The following registers in the PMBus need to be programmed in FDM for both DCM and ACM:

- FET_SELECT: See Section 4.1.4
- R_{sns}: See Section 4.1.5
- Watchdog (optional): See Section 4.1.6
- Current sense range (CS_RNG) and start-up current limit (IST): See Section 4.1.7
- Telemetry enable
- Enabling warnings (if needed)
- Setting warnings (if needed)

4.2.2 FDM (DCM)

If the device is programmed using DCM, select the DCM in register 0xD1 and modify bit '7' to '1'. The following register needs to be modified to detect the necessary faults if the corresponding fault bits are enabled in PMBus register (0xDE):

- VOUT_UV_FAULT_LIMIT (0x44): See Section 4.1.10
- VIN_OV_FAULT_LIMIT (0x55): See Section 4.1.9
- VIN_UV_FAULT_LIMIT (0x59): See Section 4.1.8

To turn on the FET, toggle the enable signal to high on the GUI, as shown in Figure 33.

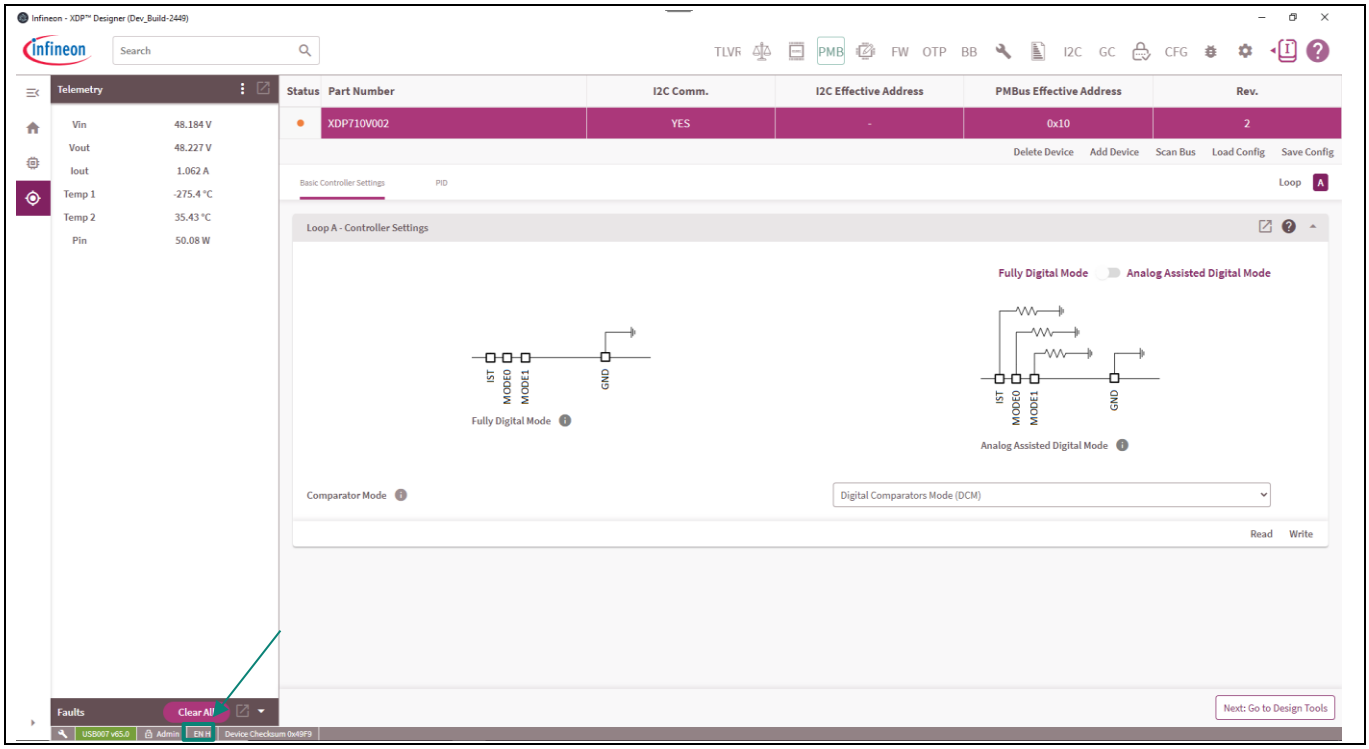

Figure 33 Enabling FET by toggling enable signal high

4.2.3 FDM (ACM)

If the device is programmed using an ACM, select the ACM in register 0xD1 and modify bit '7' to '0'. In this mode, all the voltage faults are sensed using external resistors, and so the following jumpers need to be placed on the evaluation board to detect necessary faults if the corresponding fault bits are enabled in the PMBus register (0xDE):

- **VOUT_UV_FAULT_LIMIT (FB pin)**: Jumper is required on connector X4; the output UV fault limit can be modified by modifying R9 and R10.
- **VIN_OV_FAULT_LIMIT (OV pin)**: Jumper is required on connector X41; the input OV fault limit can be modified by modifying R34, R36, and R38.
- **VIN_UV_FAULT_LIMIT (UV pin)**: Jumper is required on connector X33. If UV_FAULT is disabled, then ensure that the UV pin gets the necessary enable signal voltage to turn on the FET.

4.2.4 AADM

AADM lets you select the FET, start-up current limit and current sense range via external resistors connected on pins Mode 0, Mode 1, and IST. For the evaluation board, the settings are done as shown in Table 6.

Table 6 AADM selection resistors

Connector	Jumper position (resistor)	Function
X18 (mode pins)	Between 3 and 4 (Mode 0: 20 kΩ (2.0 V))	Selects the FET IPT015N10N5ATMA1
	Between 9 and 10 (Mode 1: 20 kΩ (2.0 V))	
X21 (IST pins)	Between 7 and 8 recommended (IST: 15 kΩ (1.5 V))	25 mV current sense range is selected and 12.5 percent of overcurrent (OC) level is selected.

The following jumpers need to be placed on the evaluation board to detect necessary faults if the corresponding fault bits are enabled in PMBus register (0xDE):

- **VOUT_UV_FAULT_LIMIT (FB pin)**: Jumper is required on connector X4; the output UV fault limit can be modified by modifying R9 and R10.
- **VIN_OV_FAULT_LIMIT (OV pin)**: Jumper is required on connector X41; the input OV fault limit can be modified by modifying R34, R36, and R38.
- **VIN_UV_FAULT_LIMIT (UV pin)**: Jumper is required on connector X33. If UV_FAULT is disabled, then ensure that the UV pin gets the necessary enable signal voltage to turn on the FET.

Modify the necessary PMBus registers for proper operation:

- R_{sns}: See Section 4.1.5
- Watchdog: See Section 4.1.6
- Telemetry enable
- Enabling warnings (if needed)
- Setting warnings (if needed)

5 Loading configuration file

This section describes how to load the configuration file directly into the device; eliminating the need to manually modify the required register. The configuration file can be loaded into the device as follows:

- Click **Load Config**, as shown in Figure 34.
- Click **Browse** and select the *.txt* file that needs to be loaded onto the device, as shown in Figure 35.
- click **Load** to load the necessary configuration onto the device, as shown in Figure 36.

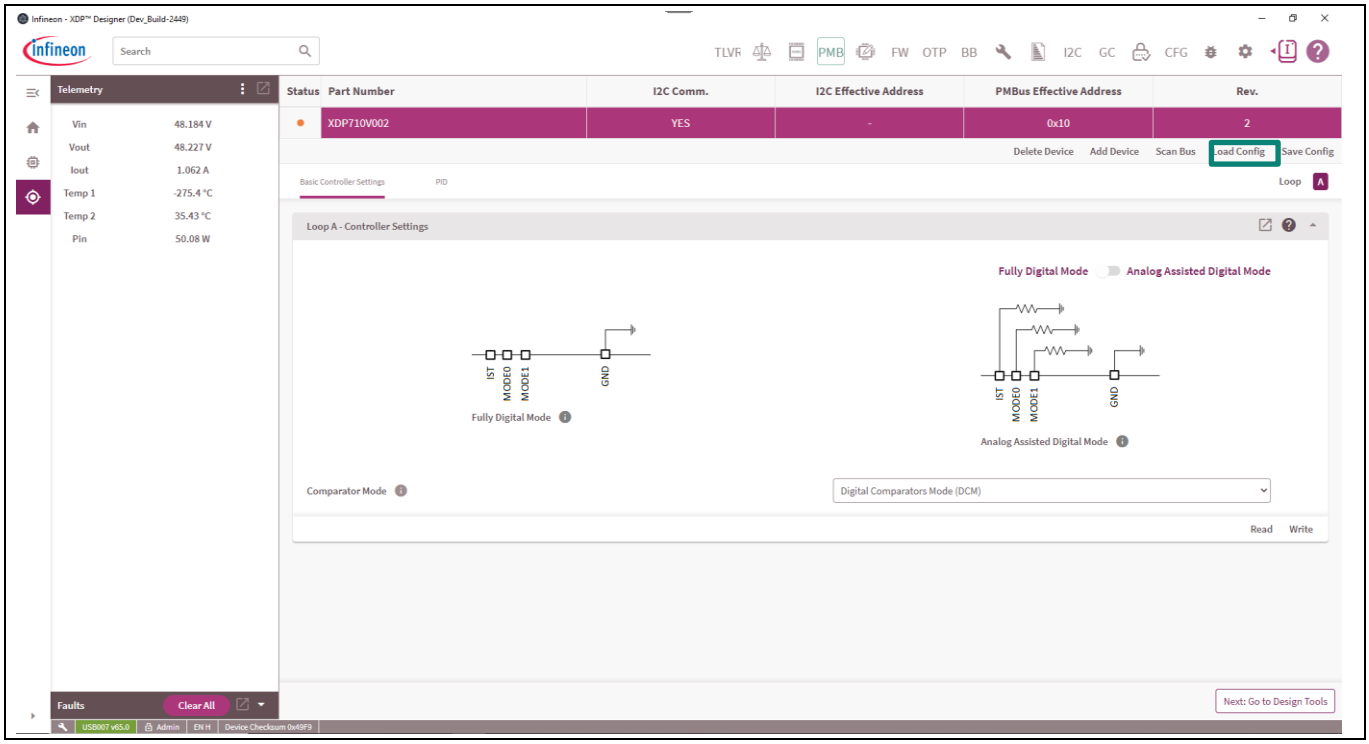

Figure 34 Select Load Config option

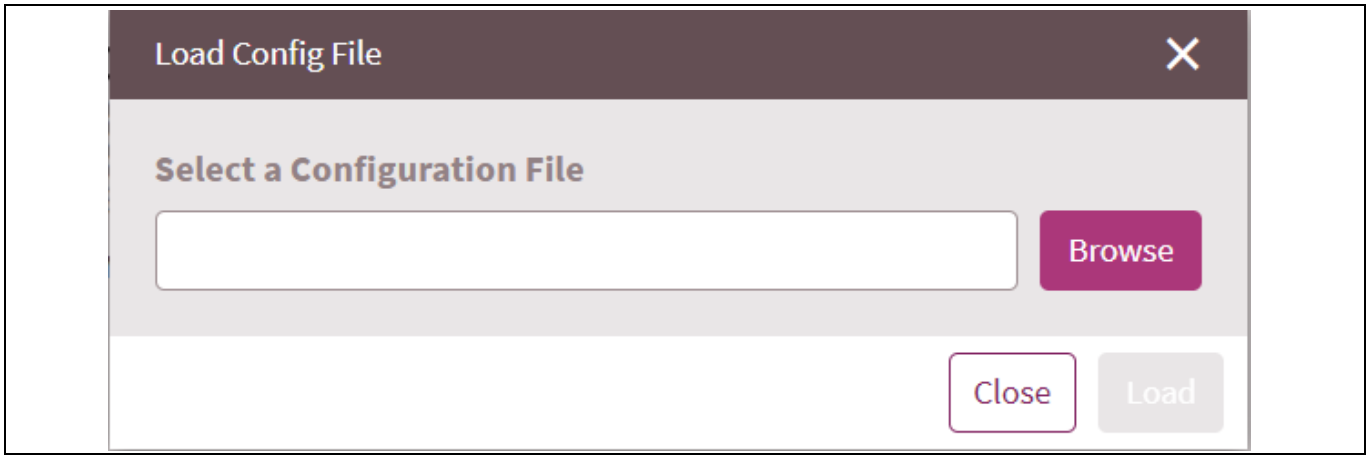

Figure 35 Browse to select the necessary configuration file

Loading configuration file

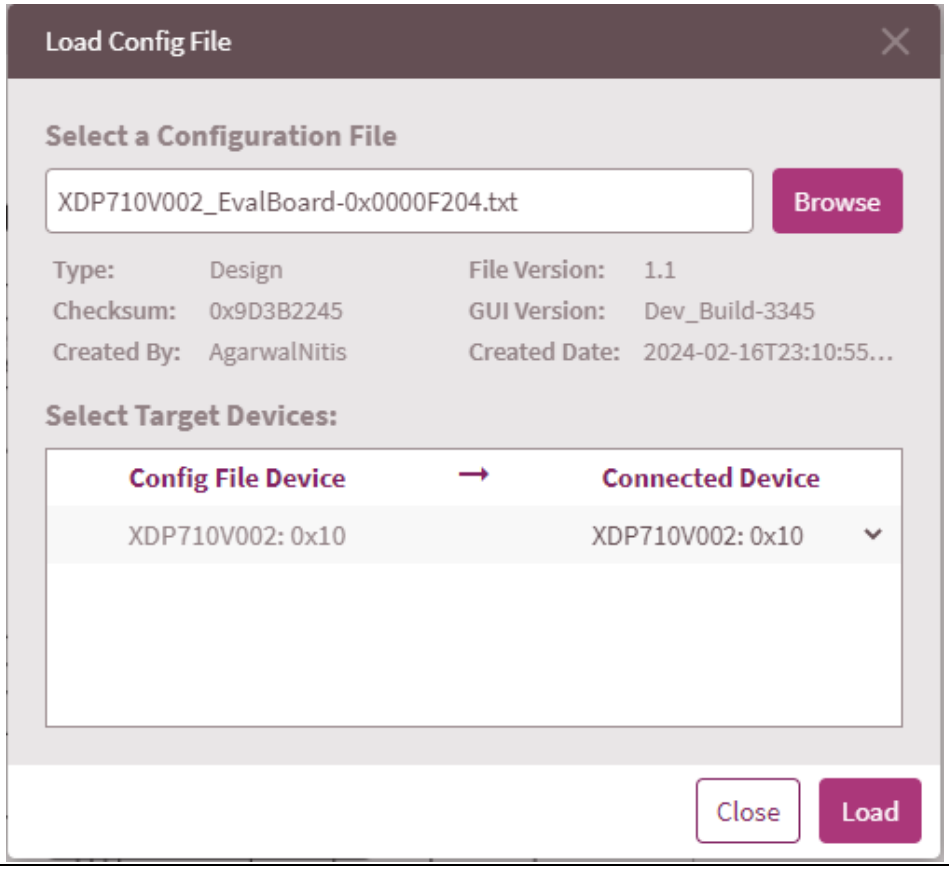

Figure 36 Load the selected configuration file

An example configuration file in .txt format can be found on the XDP710-002 Evaluation Board page [2] as *XDP710V002_EvalBoard-0x0000F204.txt*. This configuration file is compatible with the evaluation board in the default configuration.

6 XDP710-002 evaluation

For this section, it is assumed that the proper input voltage (48 V) is available on the input of the evaluation board and the example config is loaded onto the device and the device is not yet enabled.

6.1 Turn on FET test

FET is turned on by toggling the enable signal to High as shown in Figure 37.

Note: Ensure that the load is not on when enabling the FET as it could lead to watchdog timer fault and the FET will not be able to turn.

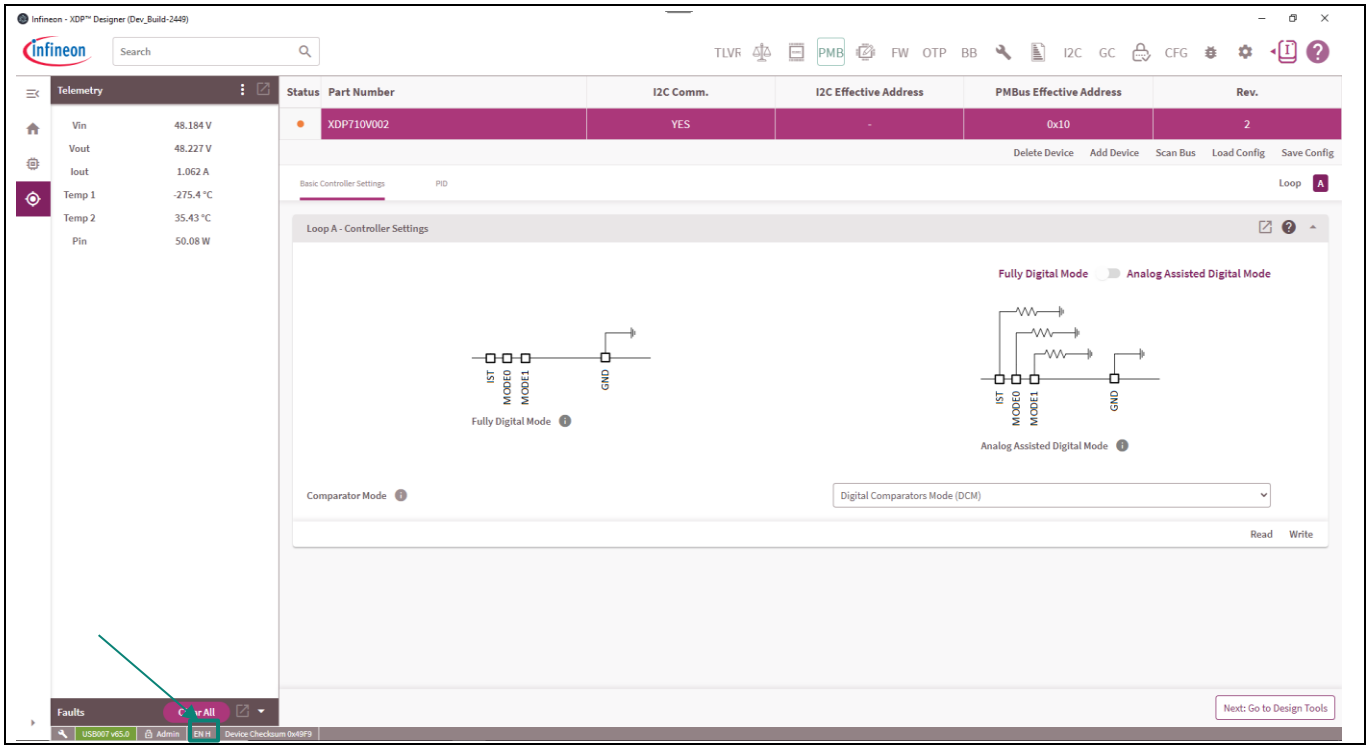

Figure 37 Enabling FET by toggling enable signal high

The turn on waveforms is shown in Figure 38. It is observed that the startup current follows the programmed SOA of the FET shown in Figure 38 closely and ensures that the FET SOA is not violated during turn-on operation; therefore, providing a safe and fast turn-on. Additionally, the maximum startup current observed is 2.776 A at an IST setting of 25%. Figure 39 highlights the regulation current at various VDS levels based on the SOA of IPT015N10N5.

Note: In Figure 38, the turn-on waveform is for three FETs connected in parallel highlighting the active startup current regulation feature of XDP710-002.

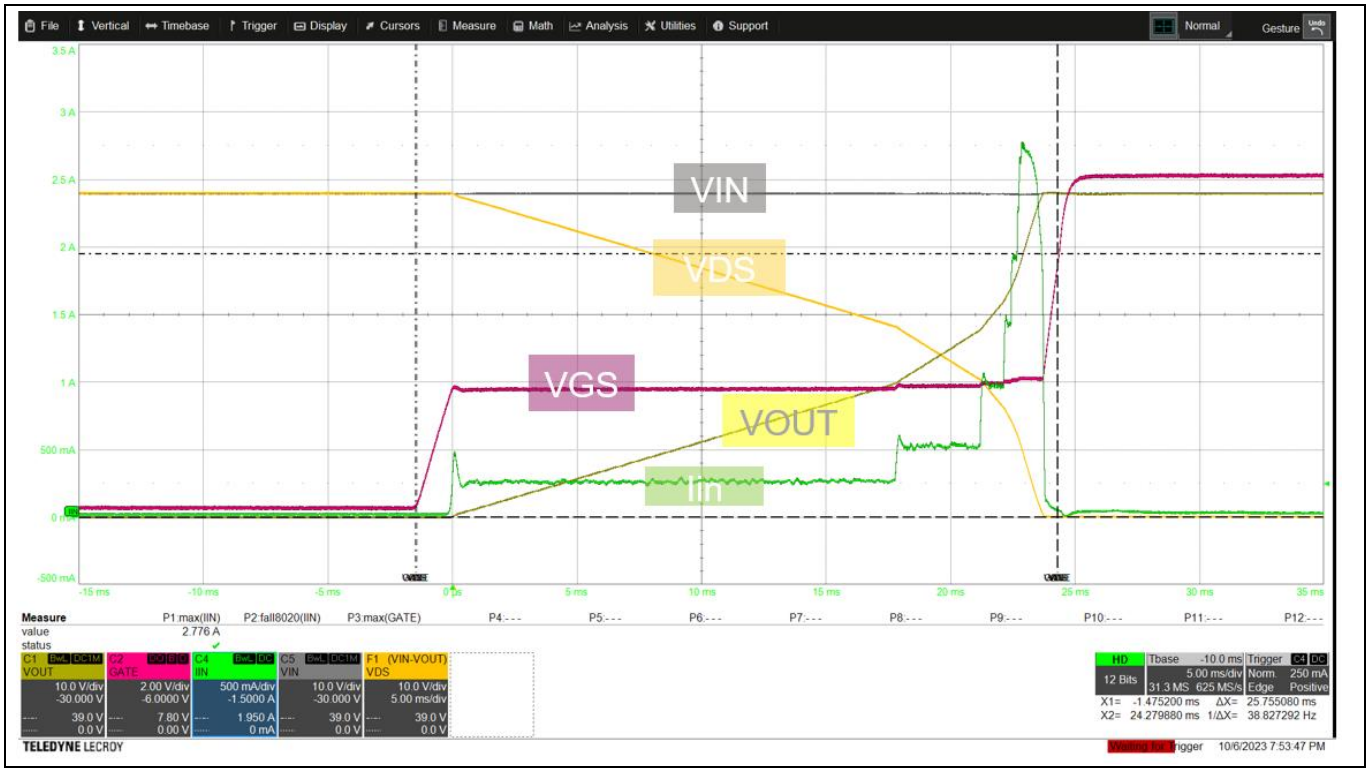

Figure 38 Startup current waveform at 48 V input

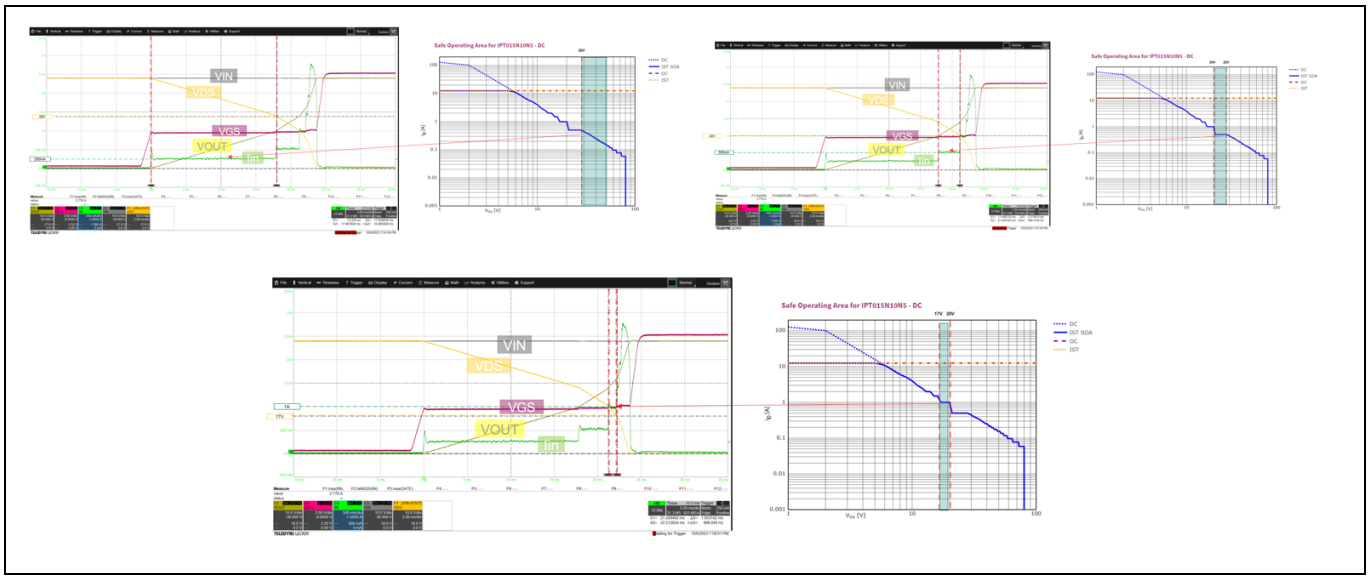

Figure 39 Startup current regulation at various VDS levels

6.2 Boost mode test

For FETs with weaker SOA with current capability of less than 0.25 A at higher voltages, it is recommended to turn on the FET with boost mode. In the following example, the boost mode is enabled and set the parameters as follows:

- Type of boost mode: Automatic boost mode
- SOA line: 1 ms
- Duty cycle: 20%

If the SOA is below 0.5 A, then boost mode is activated and the controller sends out gate pulses allowing the drain current for only 1 ms with its limit restricted to 8x the programmed SOA level. When the regulation current reaches 0.5 A, then boost mode is turns off and the FET is regulated with regular SOA. Figure 40 shows the startup behavior with automatic boost mode and at V_{DS} = 28 V, where I_{SOA} = 0.5 A, the controller resumes with regular current regulation.

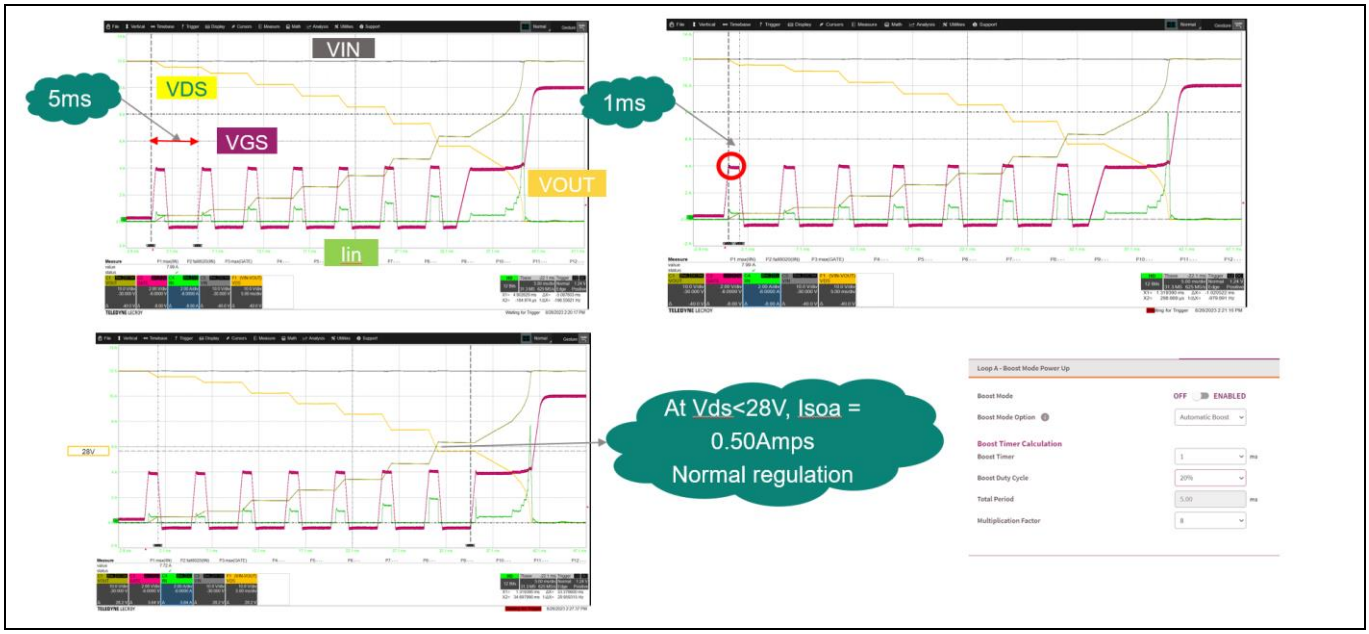

Figure 40 Automatic boost mode operation

Attention: ***Set the duty cycle according to C_{gs} to provide sufficient time for the gate to discharge to avoid double pulses and violation of SOA on 1 ms line.***

6.3 Overcurrent (OC) fault test

The overcurrent (OC) fault test is performed and the overcurrent fault module is set to the following settings:

- Overcurrent level: 12 A
- SOA Deglitch timer (SOAD_TMR): 1 ms
- SOA Regulation timer (SOAR_TMR): 10 ms

From Figure 41, it can be observed that when the current reaches a level of 12 A, then it is blanked for 1 ms as set by the SOAD_TMR. After SOAD_TMR expires, the gate voltage is reduced to regulate the current at 12 A for defined time of 10 ms set by the SOAR_TMR. During this time, if the current does not go below 12 A, then the FET is turns off and OC fault is declared.

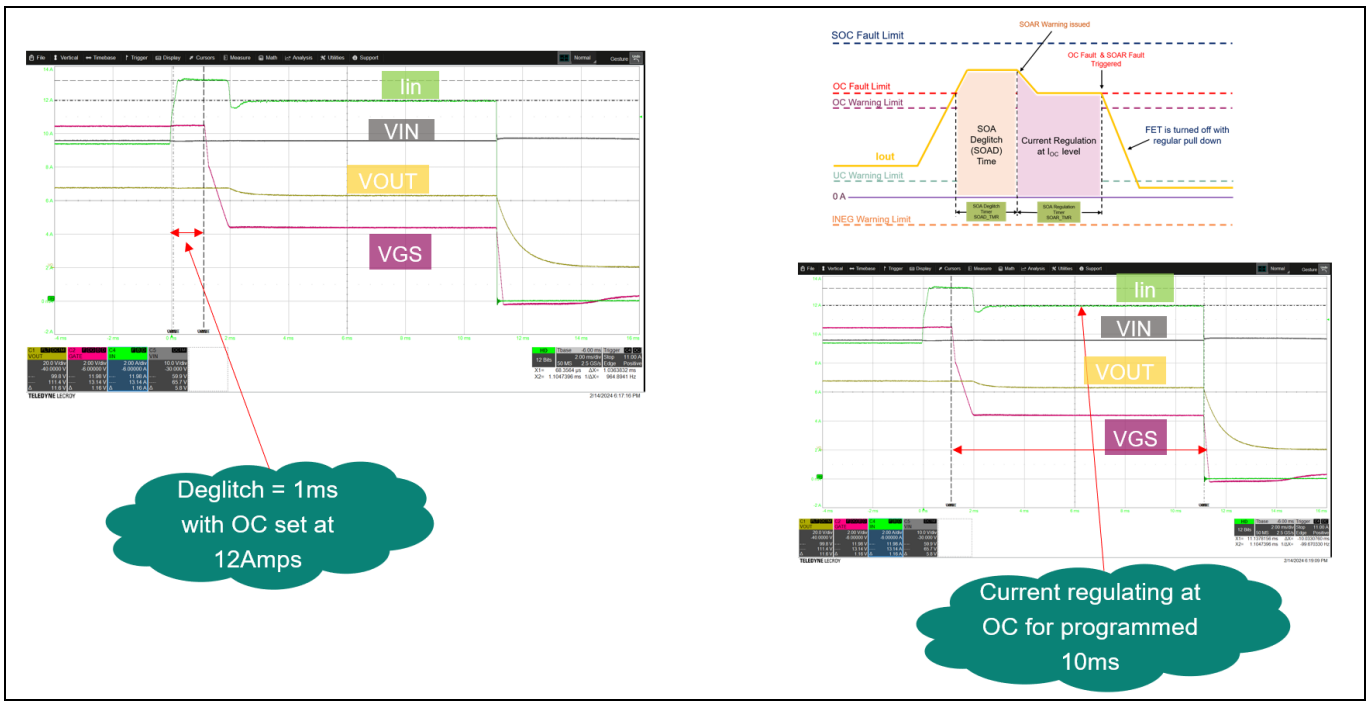

Figure 41 Overcurrent fault and regulation

6.4 Severe overcurrent (SOC) fault test

XDP710-002 provides fast detection of severe overcurrent faults by turning off the FET within 1 µs from detection to full turn-off by sinking 1.5 A of current out from the gate. This level can be adjusted as explained in Section 6.5. The SOC fault module is set as follows in the example file:

- SOC fault limit: 18.75 A
- SOC_DG_TMR: 500 ns
- SOC_TMR: 0 µs
- One step shutdown

Figure 42 shows the SOC fault detection and the fast turn-off feature of XDP710-002. Note that the deglitch is added to highlight the feature of XDP710-002 to ignore noise if expected. It is observed that, after the deglitch time of 500 ns , the FET is turned off within 475 ns and SOC fault is declared.

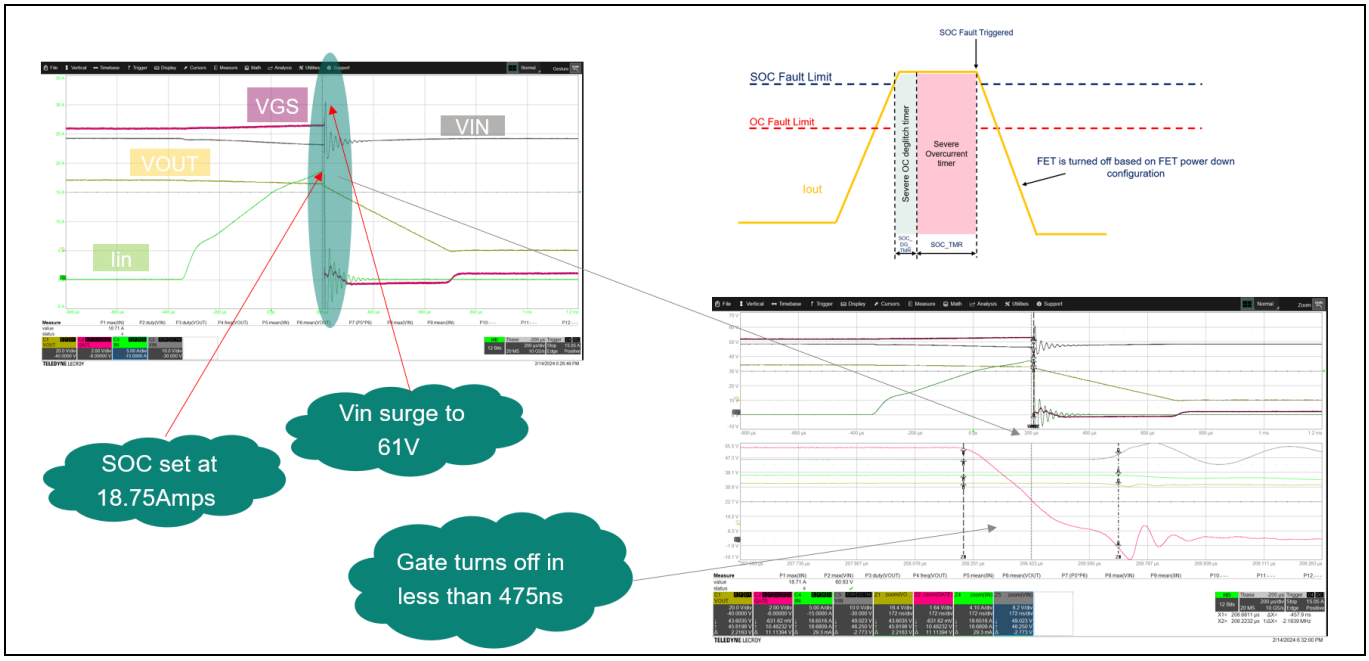

Figure 42 Severe overcurrent fault detection

6.5 Two-step turn-off test

It is observed from Figure 42 when the FET is turns off with a strong pulldown then due to inductance of input lines, the voltage spikes are induced on the input voltage (Vin) and add stress on the FET and the system. In a two-step shutdown, the turn-off process is split into two sinks levels, the internal 200 Ω resistors is turns on for the time defined by the GATE_PD_TMR and after timer expires, then the sink level is switched to current defined by the GATE_SLOW_PD (250 µA, 500 µA, 750 µA, or 1250 µA).

For testing, the two-step shutdown is set with GATE_PD_TMR = 4000 ns and GATE_SLOW_PD= 750 µA. The Figure 43 shows the two-step gate turn-off and it is observed that the ringing on Vin has been significantly reduced at the expense of increasing turn-off time.

Figure 43 Two-step shutdown to turn off MOSFET after SOC fault

7 Programming SOA, OTP, and MTP

As specified in the XDP710-002 datasheet [1], to program the desired settings in internal commands or OTP at power-up, follow these steps:

- Apply a voltage at the VDD_VIN and ISNS_P pins:
  - At least 5.5 V to program commands into volatile memory
  - At least 20 V to program OTP or MTP
- Keep the UV/EN pin at chip GND potential.
- Communication via PMBus is possible as soon as the STANDBY state is entered. At this point, commands, OTP, or MTP can be programmed.
- For a successful programming, the internal temperature of the device must stay below 125°C at all times.

To program OTP or MTP sections:

1. Program the commands in volatile memory as desired.
2. Click the button highlighted as shown in Figure 44.

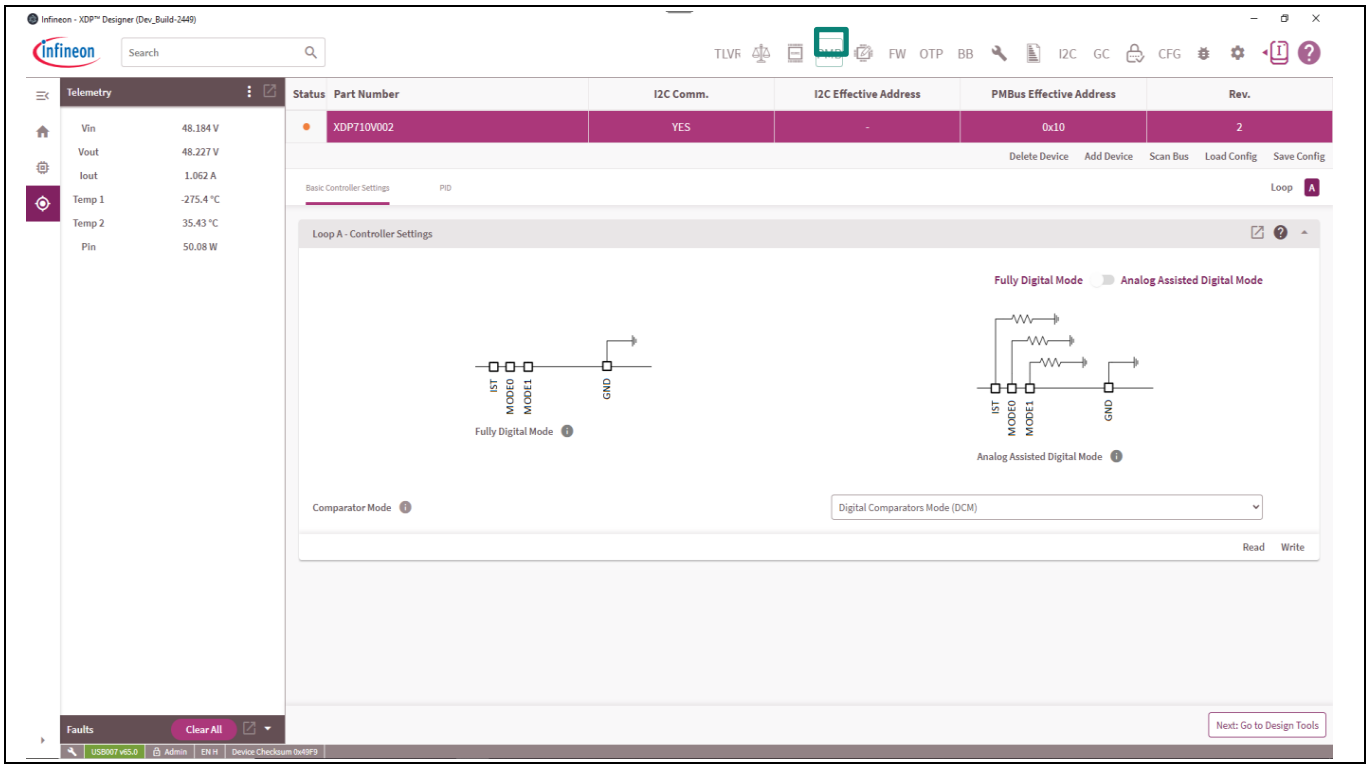

Figure 44 Programming tab

3. Set the program from **Registers**, select the memory section that needs to be programmed and then click **Program to OTP**, as shown in Figure 45.

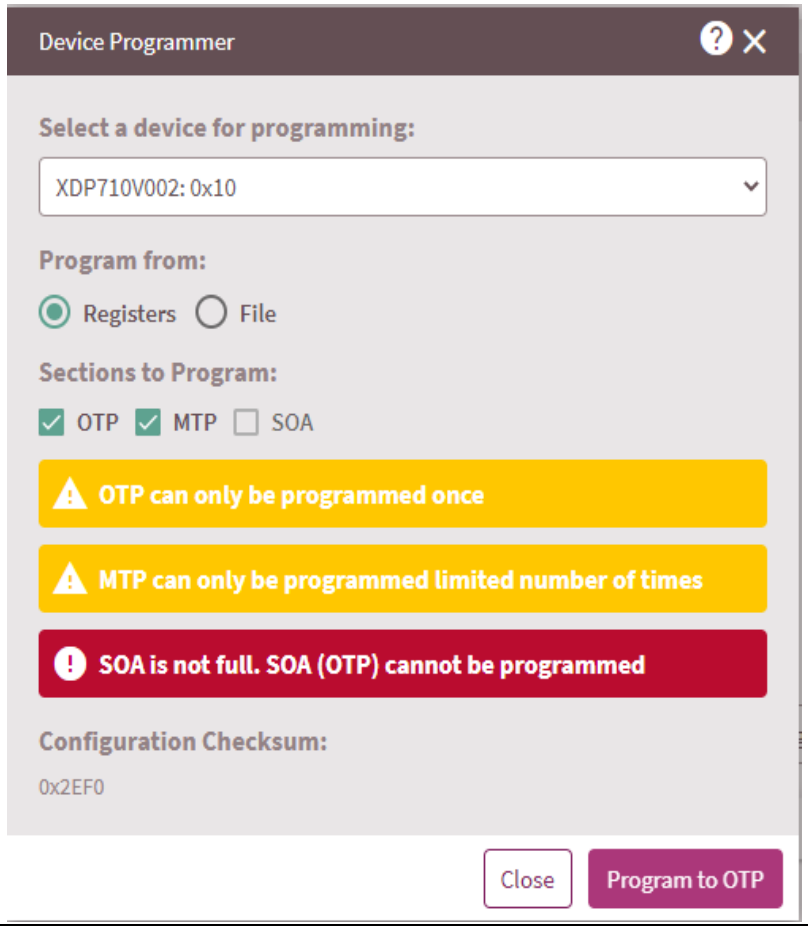

Figure 45 OTP and MTP programming

4. The command configuration will be automatically copied to the selected memory section.

References

[1] Infineon Technologies AG: *XDP710-002 hot-swap controller datasheet;* Available online

[2] Infineon Technologies AG: *XDP710-002 Evaluation Board webpage*; Available online

Revision history

Document revision	Date	Description of changes
V 1.0	2023-08-11	Initial release
V 1.1	2024-03-26	Added XDP710-002 evaluation section Updated configuration file

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