EVAL_6EDL7151_36V_1kW: Smart gate driver evaluation board

About this document

Scope and purpose

This document describes the functionalities of the EVAL_6EDL7151_36V_1kW motor drive board for battery-powered brushless DC (BLDC) motor drives with sensorless field-oriented control, used in battery powered motor control applications. This solution combines an XMC1400 series microcontroller, with the 6EDL7151 three-phase smart driver IC and Infineon OptiMOS™ BSC014N06NSSC dual-side cooling power MOSFETs. The 6EDL7151 reduces system component count and development time-to-market, while significantly increasing the power density, system performance, and peak power pulse capabilities. Additionally, the ModusToolbox™ Motor Suite GUI (graphical user interface), a software tool designed for configuring the 6EDL7151, will also be introduced.

Intended audience

This document addresses the market for cordless power tools, robotics, and other battery-powered motor drive applications, targeting designers who aim to provide a high-performance system solution while reducing system costs. It is intended for design engineers, applications engineers, and students.

Infineon components featured

- BSC014N06NSSC (OptiMOS™ 60 V 1.4 mΩ 5x6 dual-side cooling PQFN package)
- 6EDL7151 three-phase half-bridge MOSFET gate driver and motor control IC
- XMC1404-VQFN64-200 kB 32-bit microcontroller with Arm® Cortex®-M0 (XMC™)

Table of contents

1 Introduction

1.1 Brushless motors

BLDC and PMSM motors are commutated by controlled switching of the inverter instead of using mechanical brushes. Windings are energized in a determined sequence to generate a rotating magnetic field. As the rotor's permanent magnet attempts to align with the stator field, it generates torque and rotary motion. The torque control in BLDC and PMSM motors is achieved by controlling the motor currents, which is achieved by switching the inverter in a particular sequence to control both the magnitude and phase angle of the motor current, also known as the vector control or field-oriented control.

1.2 EVAL_6EDL7151_36V_1kW motor drive board

This application note describes Infineon's EVAL_6EDL7151_36V_1kW motor drive evaluation board, optimized for battery-powered tools operating with sensorless FOC. The design considers the electrical driving capabilities for PMSM/BLDC machines with three shunts for phase current measurement to estimate rotor position and speed.

The board utilizes BSC014N06NSSC OptiMOS™ 60 V 1.4 mΩ DSC power MOSFETs in 5x6 PQFN, dual-side cooled SuperSO8 packages. A detachable heatsink can be mounted to the top side or bottom side of the board to enable improved thermal management and increased power handling capability.

The demo board includes an on-board isolated debugger, ready for direct connection to a PC via a USB Type-A port. The source code is implemented using the Infineon Eclipse-based IDE, ModusToolbox™ Software (development platform for XMC™ microcontroller). The firmware is developed using the XMC1400 microcontroller family.

With this kit, users can evaluate the 6EDL7151-based motor drive system using the control capabilities of the XMC1400 using a control algorithm with customized features for power tool applications. The board includes a switch for changing the motor direction and a POT1 for speed control. Configuration and control are also possible through the dedicated GUI, which connects to the demo board through a USB cable interfacing with an on-board programmer/debugger.

The evaluation boards have a 3-shunt configuration for current measurement and runs sensorless FOC algorithm. However, the same board can be used to evaluate 1-shunt trapezoidal control for BLDC motors. To evaluate the board under a trapezoidal control scheme, it is recommended to remove the shunts on the U, and W phases and connect the jumpers at the appropriate locations on the evaluation kit.

Introduction

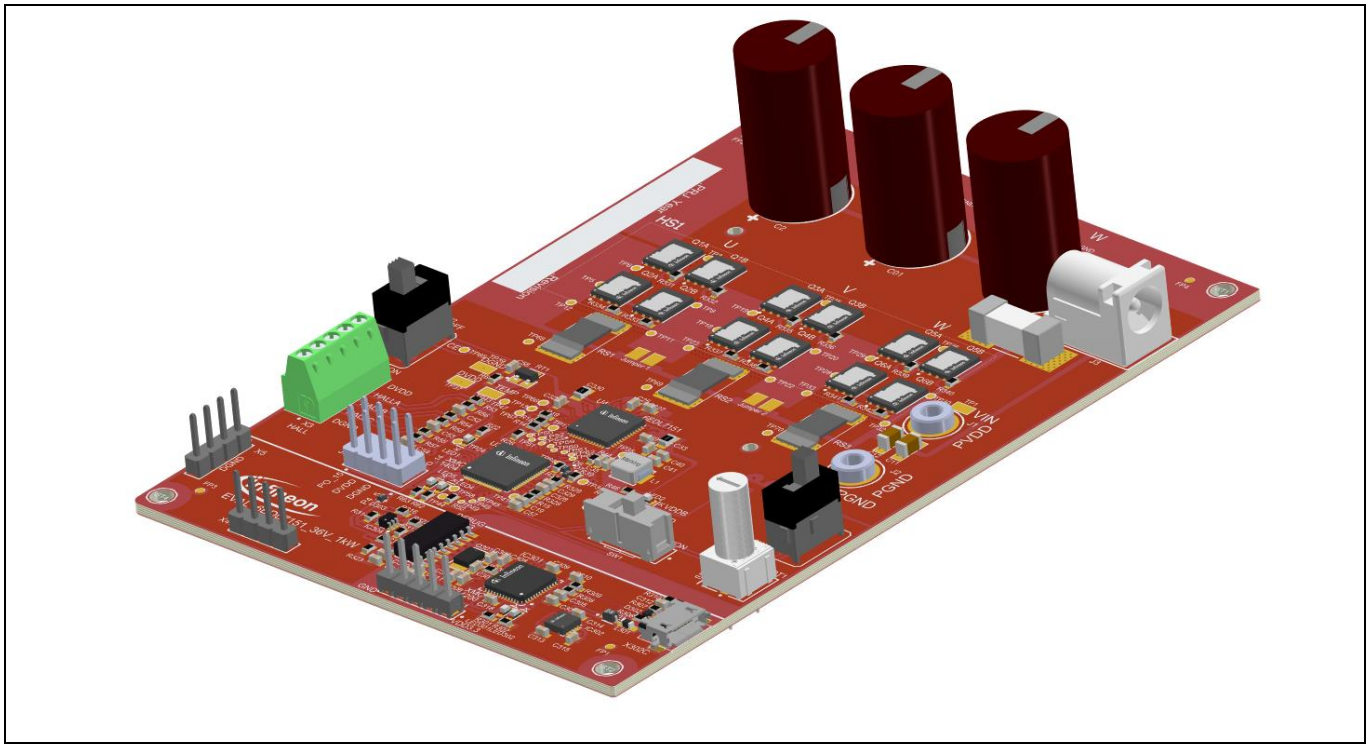

Figure 1 EVAL_6EDL7151_36V_1kW demo board

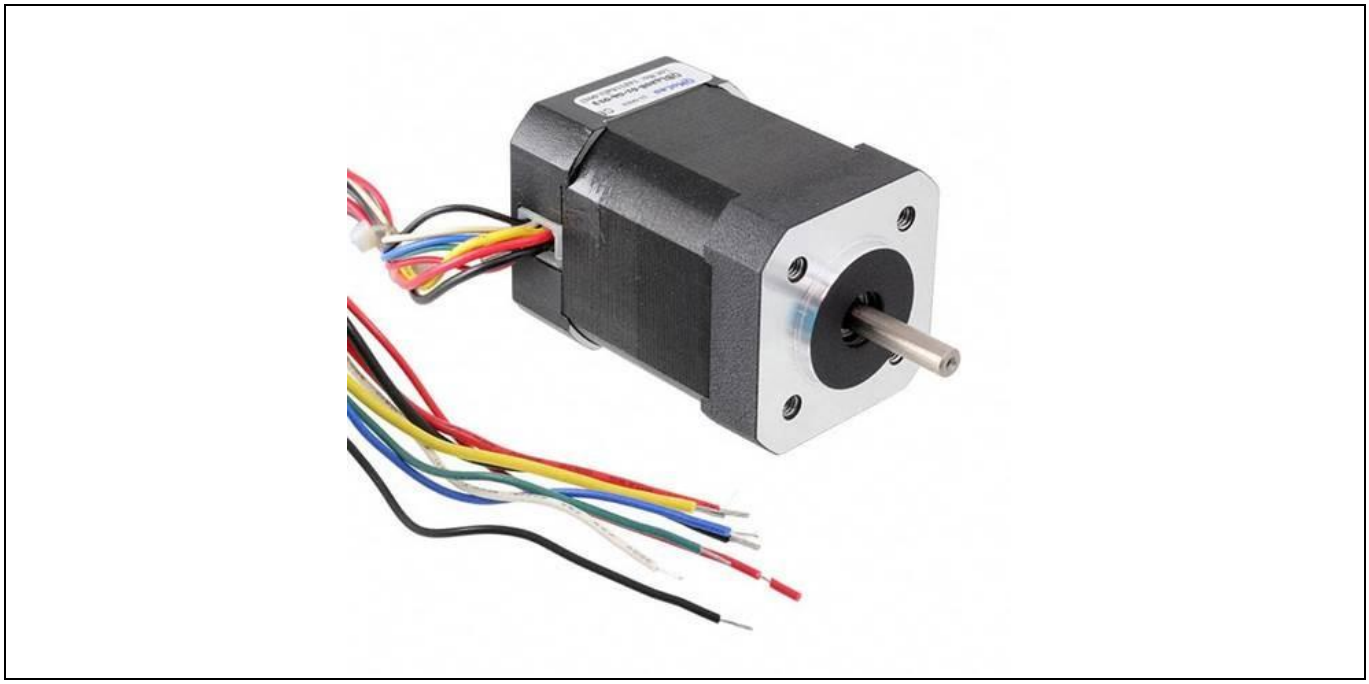

Figure 2 BLDC motor example

Introduction

The motor drive system level block diagram excluding the on-board debugger is shown below.

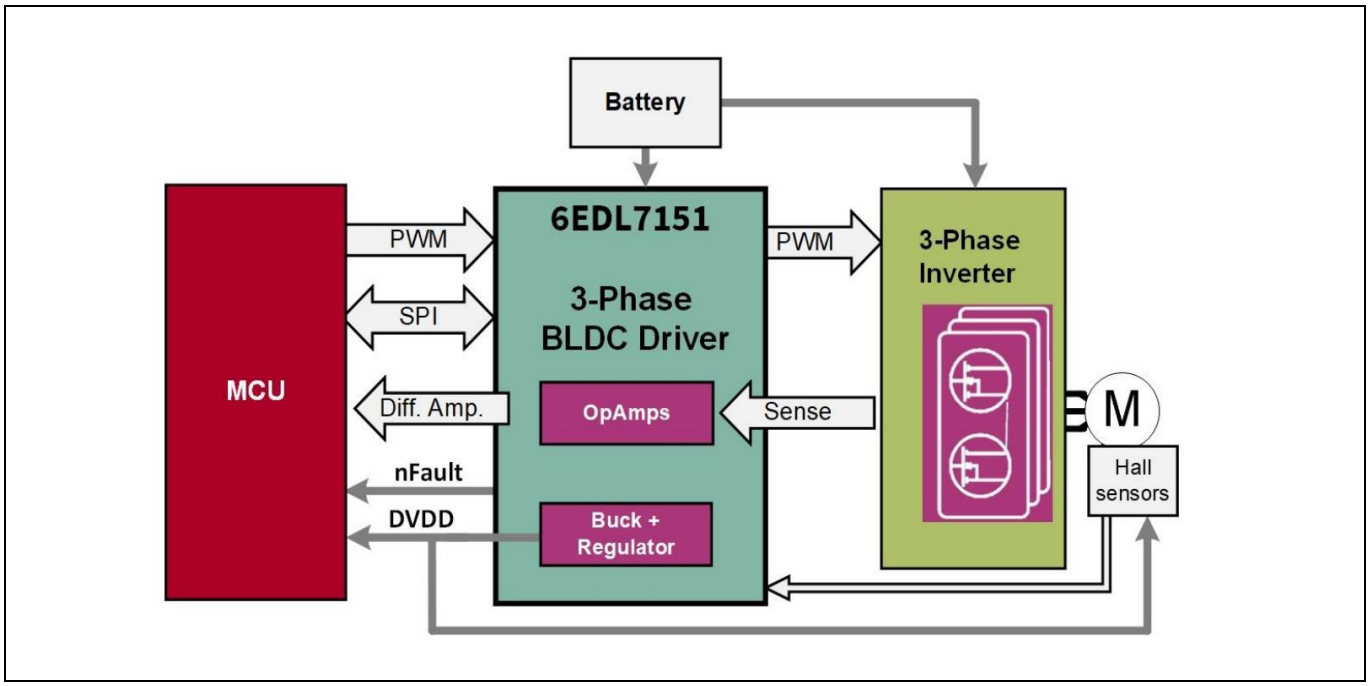

Figure 3 Simplified system block diagram

Rotary velocity plotted against torque, measured with a 24 V supply voltage for the example motor, is shown below. The blue area represents the region where the motor may be safely used without overheating the stator coils.

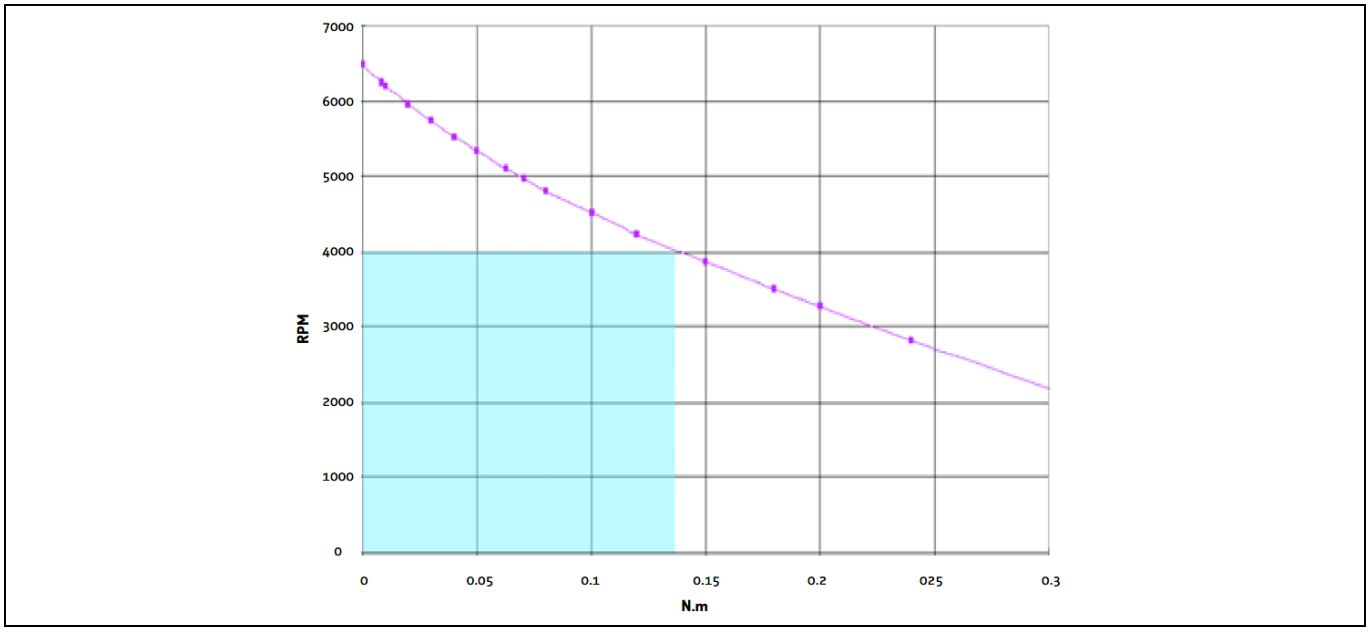

Figure 4 Rotary velocity vs. torque curve for example BLDC motor

1.3 6EDL7151 functional overview

The 6EDL7151 is a three-phase smart gate driver in a 48-pin VQFN package for brushless DC or permanent magnet synchronous motor drive systems. It is designed to operate in conjunction with a microcontroller and as an example, Infineon's XMC1400 series microcontroller is used in this EVAL board. The 6EDL7151 consists of a configurable three-phase half-bridge gate driver able to operate in multiple PWM modes. It also features an integrated DC-DC synchronous buck converter, a low drop-out linear voltage regulator, and configurable precision current sense amplifiers. There are many configuration options available, which can be set via an advanced microcontroller interface in conjunction with a PC-based GUI. Configuration settings can be made permanent by storing in the built-in one-time programmable memory.

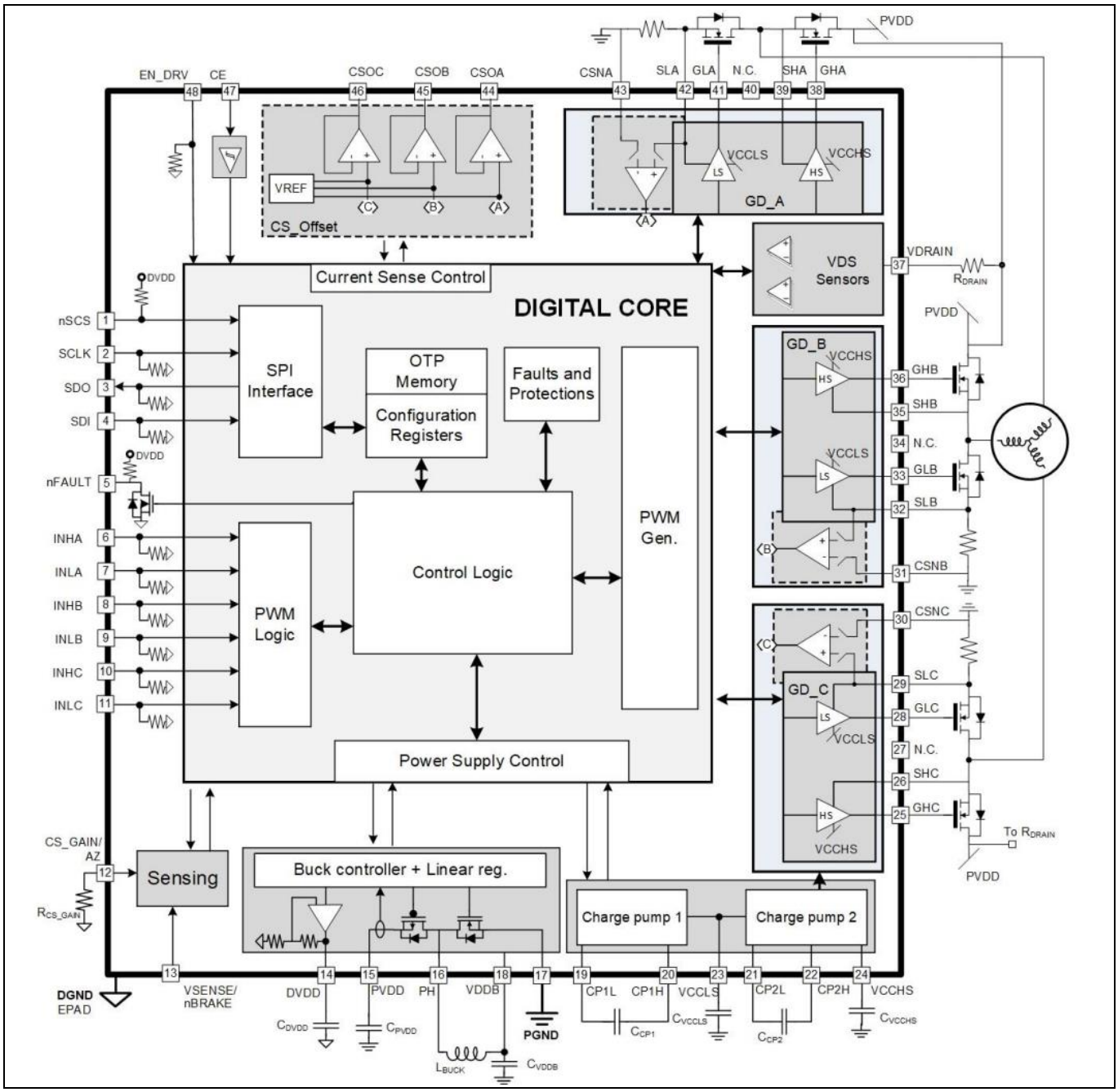

Figure 5 6EDL7151 internal block diagram

Introduction

The microcontroller communicates with the 6EDL7151 via an SPI to enable configuration. PWM signals from the microcontroller provide the gate drive control pulses, which can be decoded in multiple ways. The 6EDL7151 provides gate drive pulses to the three-phase inverter low- and high-side MOSFETs. The gate drive output voltages (PVCC) can be selected to several different levels between 7 V and 15 V. The switch-on and switch-off profiles can be optimized to minimize EMI and switch-off transients by configuring the gate drive current during four different time intervals of the switching process. This also eliminates the need for resistor-diode gate drive networks. Configuration of the gate driver and slew rate control is explained in Section 4.1.

The 6EDL7151 also includes a complete power system infrastructure as shown in Figure 6. The first stage is based on the synchronous buck regulator, which operates in an Adaptive Constant-On-Time scheme. This efficiently converts the battery voltage to an internal voltage, which is set to 6.5 V, 7 V or 8 V depending on the gate drive voltage setting. The buck regulator is capable of supplying up to 600 mA and requires only an inductor and capacitor. The buck regulator supplies the linear regulator, which can provide a noise-free 3.3 V or 5 V supply for the digital circuitry and microcontroller. The output of the linear regulator can be set by the value of the resistor during start-up or through configuration via the GUI. Configuration of the buck and linear regulator is explained in Section 4.2.

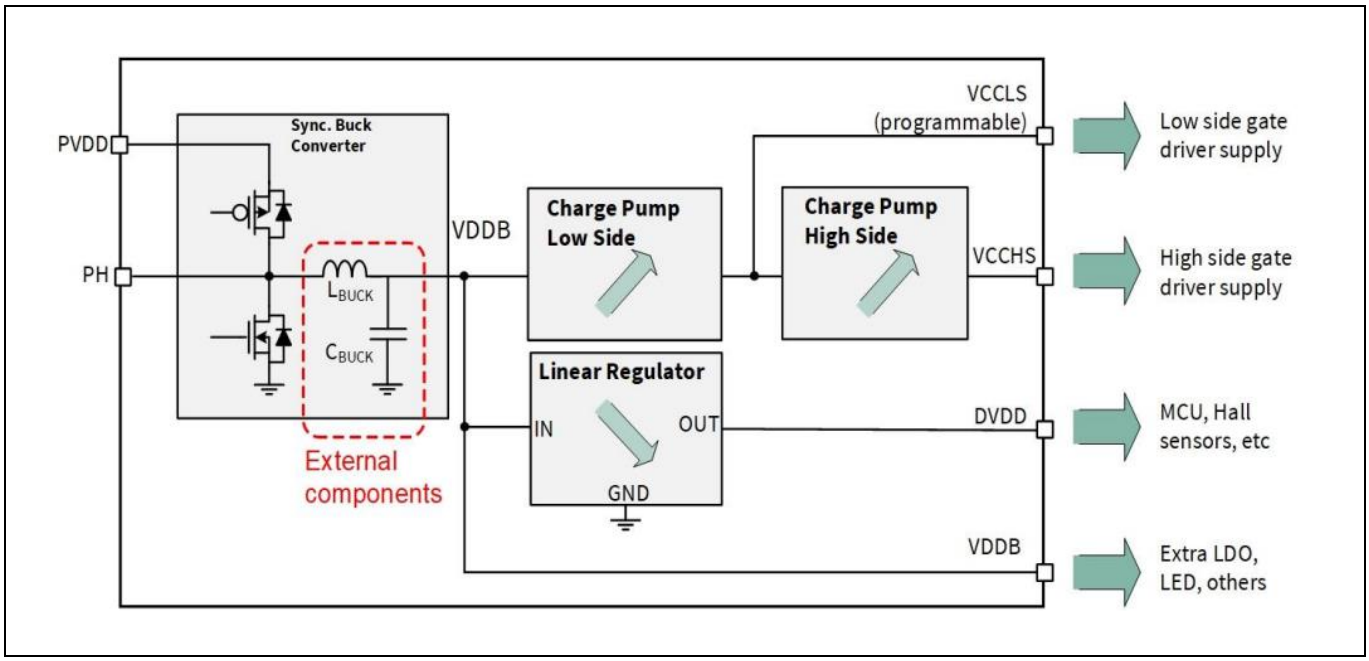

Figure 6 6EDL7151 integrated power supplies

Also, the 6EDL7151's integrated low-side and high-side charge pumps, supplied from the buck regulator, provide the gate driver supply voltages, enabling duty cycles up to 100 %. Each charge pump uses an external switched capacitor (CP1 for the low-side and CP2 for the high-side) to transfer charge from the buck converter output to the gate driver bias supplies, VCCLS, and VCCHS. VCCLS is referenced to the system zero-volt rail, while VCCHS is referenced to the system positive supply rail. Unlike conventional half-bridge drivers, the 6EDL7151 includes an advanced high-side driver scheme that enables VCCHS to be able to supply the switch-on voltage and current to the high-side gate drivers for all three phases without the need for separate floating supplies for each phase. The values of the switched capacitors and bias supply capacitors, CVCCLS and CVCCHS, must be selected according to the datasheet instructions for the charge pumps to operate correctly. The charge pump clock frequency is selectable from at 195.3 kHz, 390.6 kHz, 781.3 kHz, or 1.56 MHz with optional frequency modulation to reduce EMI. The configuration of the charge pump is explained in Section 4.3.

The 6EDL7151 integrates three precision current sense amplifiers, which can be used to measure the current in the inverter via shunt resistors. It supports single-, double-, or triple-shunt measurements and each current

sense amplifier can be enabled individually. The gain and offset are configured internally and can be set via the user interface. An additional output buffer allows adding a variable-offset voltage to the sense amplifier output, which can be set to four different values by programming the internally generated level so that negative current in current shunts can also be measured.

A positive overcurrent comparator detects an overcurrent condition on a motor winding for a positive shunt voltage. This comparator can be used to apply PWM cycle-by-cycle pulse truncation, terminating the gate drive to limit the maximum motor current. An additional negative overcurrent comparator is also used for detecting the overcurrent condition on motor winding for negative shunt currents. A built-in DAC is used for programming the thresholds of the overcurrent comparators. The different sub-systems in the current sense stage are shown in Figure 7. Configuration of the current sense amplifier is explained in Section 4.4.

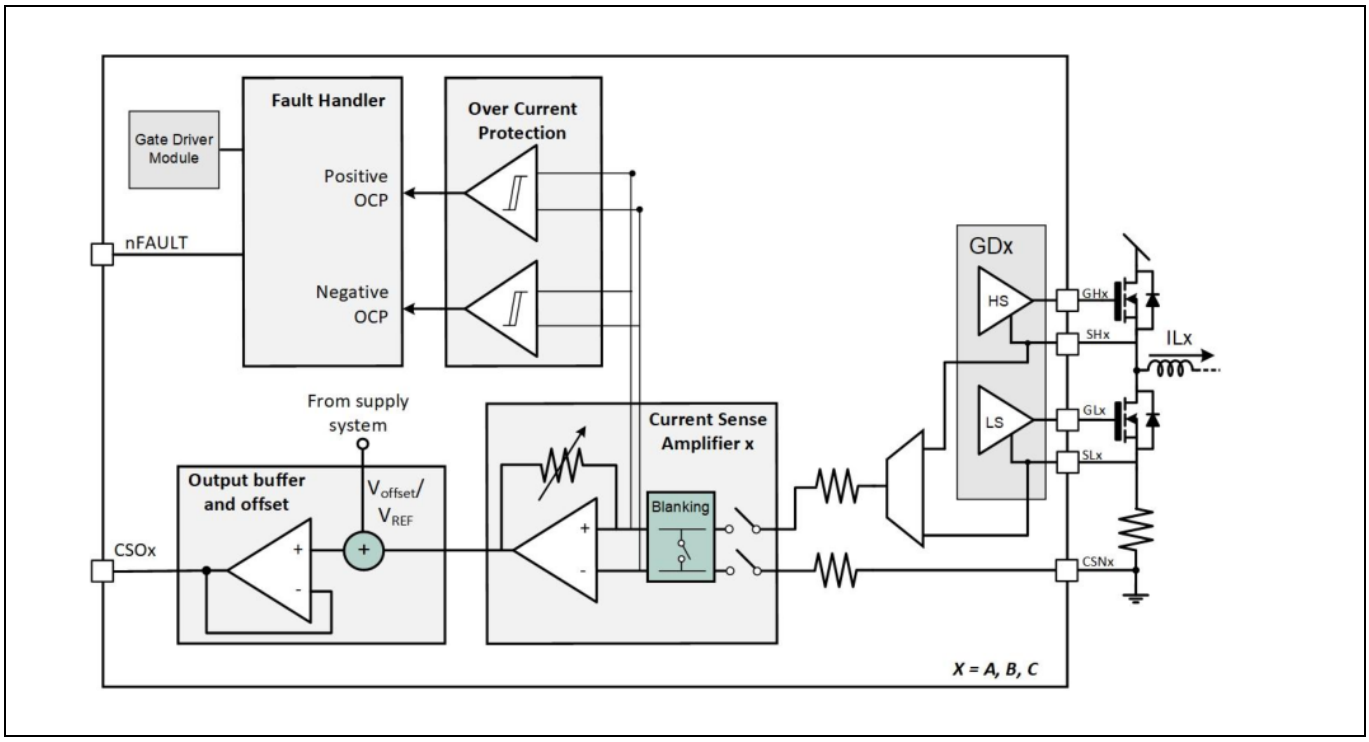

Figure 7 6EDL7151 current sense amplifiers and comparators

The 6EDL7151 also integrates the VDS sensor system as shown in Figure 8. The VDS sensors provide the possibility to monitor the status of the external MOSFETs and detect potential fault conditions. One VDS sensor is provided for each MOSFET in the 3-phase inverter, three for low-side MOSFETs and three for high-side MOSFETs. The Drain to Source voltage across the MOSFET is monitored, when the measured voltage exceeds the programmed threshold voltage a fault is detected and PWM input to the inverter is stopped. The fault is reported on nFault pin. The VDS sensor of a MOSFET is enabled only when that MOSFET is activated. During turn-off periods of the MOSFET, the VDS sensor for the corresponding MOSFET is switched off as well. The VDS sensor system is explained in detail in Section 4.5 along with the off-state diagnostics feature, which is extremely useful to avoid deep discharge of the battery when one of the MOSFETs has failed.

Introduction

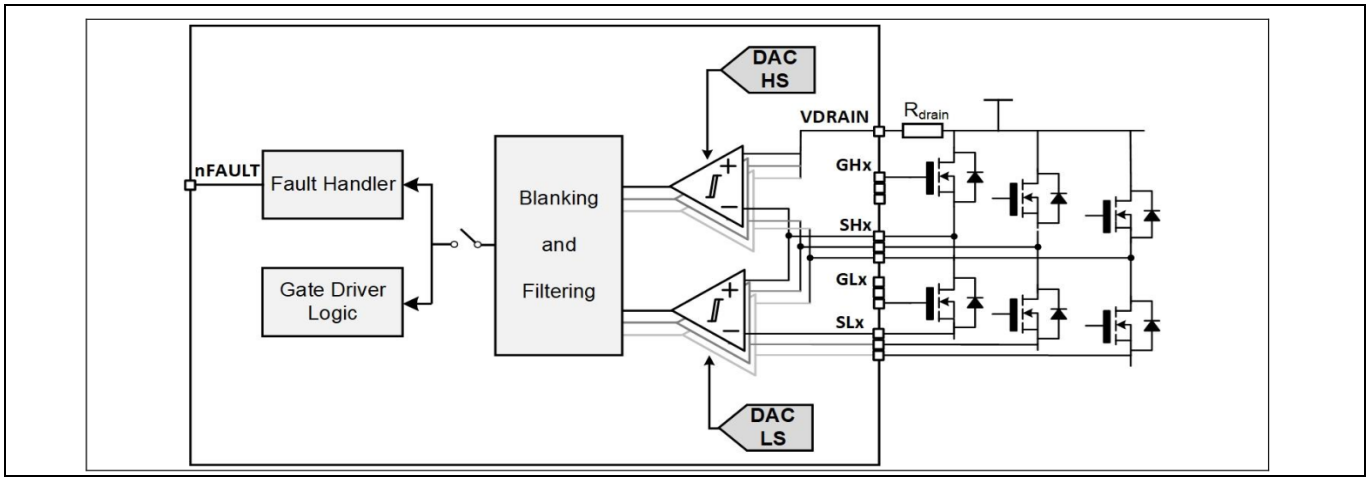

Figure 8 VDS sensor block diagram

The 6EDL7151 supports several PWM modes, which can be selected. These include:

- 6PWM
- 3PWM
- 1PWM and commutation pattern
- 1PWM with Hall sensor commutation
- 1PWM mode with Hall sensor commutation and alternating recirculation.

This allows the designer flexibility in terms of microcontroller selection to cover a variety of different applications. In one and three PWM modes, the dead-time is configurable in the 6EDL7151.

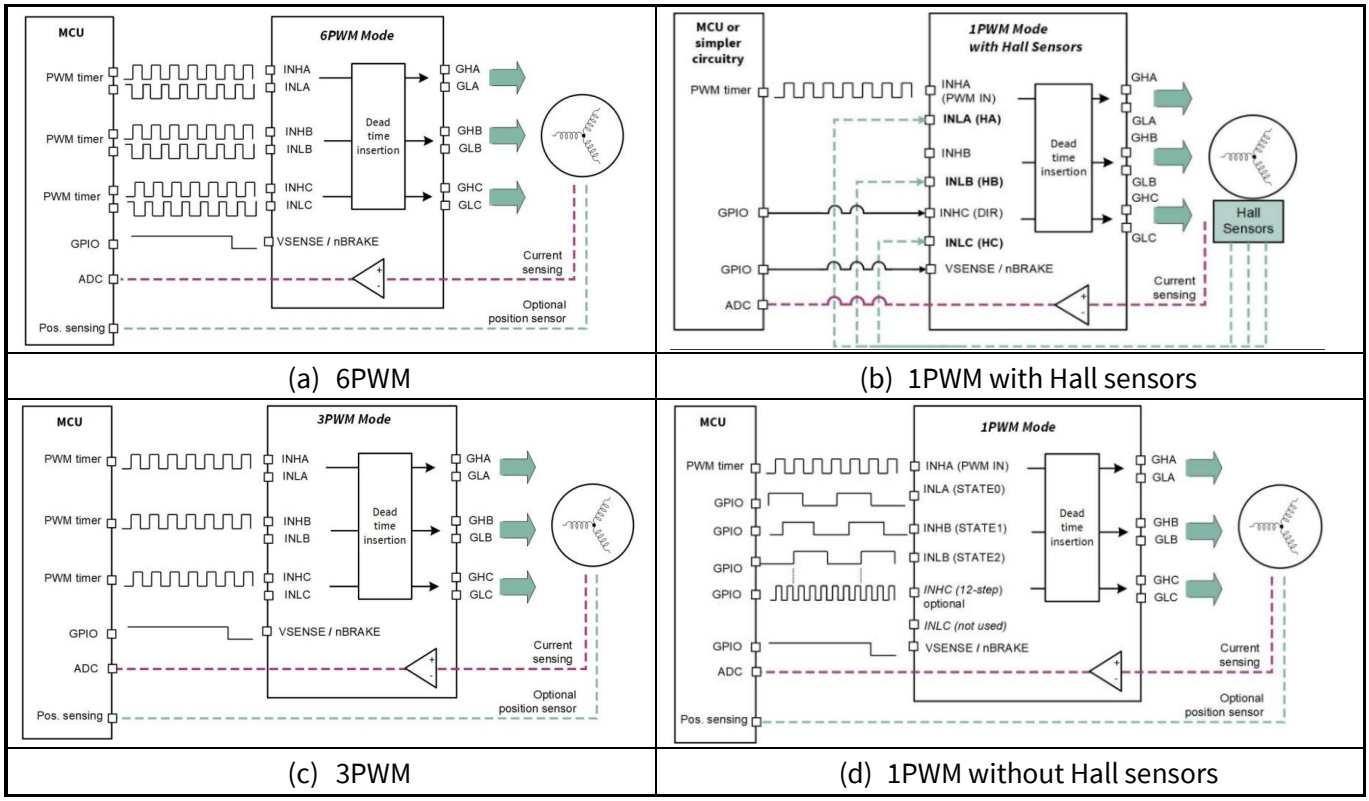

Figure 9 PWM switching modes supported by the 6EDL7151

Introduction

The EVAL_6EDL7151_36V_1kW evaluation board operates using the 6PWM mode with the firmware supplied.

The 6EDL7151 also incorporates several protection functions, including:

- Overcurrent protection for the internal power supplies and inverter phases
- Undervoltage lock-out for the input bus voltage and digital supply voltage
- VDS Sensor System for protection of external inverter MOSFETs
- Overtemperature detection, warning, and shut down
- A configurable watchdog timer
- Locked rotor detection based on Hall sensor inputs and memory fault detection
- OTP memory fault detection

  Section 3.14 of the 6EDL7151 datasheet explains the protections and fault handling in detail.

2 Specifications

Input and output in normal operation:

- DC input voltage: 12 V to 36 V
- Maximum input current 50 A
- Output voltage three-phase sinusoidal voltage FOC
- Maximum output current per phase 75 A_{RMS}
- Maximum output continuous power 1000 W

Control scheme:

- Sensorless FOC
- Switching frequency 20 kHz
- Three current shunts

Protection features:

- VDS Sensor system to detect fault conditions in external MOSFETs
- Input fuse
- Input reverse polarity
- Output overcurrent
- Thermal shutdown

Maximum component temperature:

In an ambient temperature of 30°C, the maximum allowed component temperatures are as follows:

- Resistors less than 100°C
- Ceramic capacitors, film capacitors and electrolytic capacitors less than 100°C
- MOSFET transistors and diodes less than 100°C
- ICs less than 100°C

Dimensions of evaluation board:

Maximum width 3.3 inches/83.6 mm, maximum length 4.8 inches/121.96 mm.

Attention: ***The board should be tested only by qualified engineers and technicians.***

3 Schematics

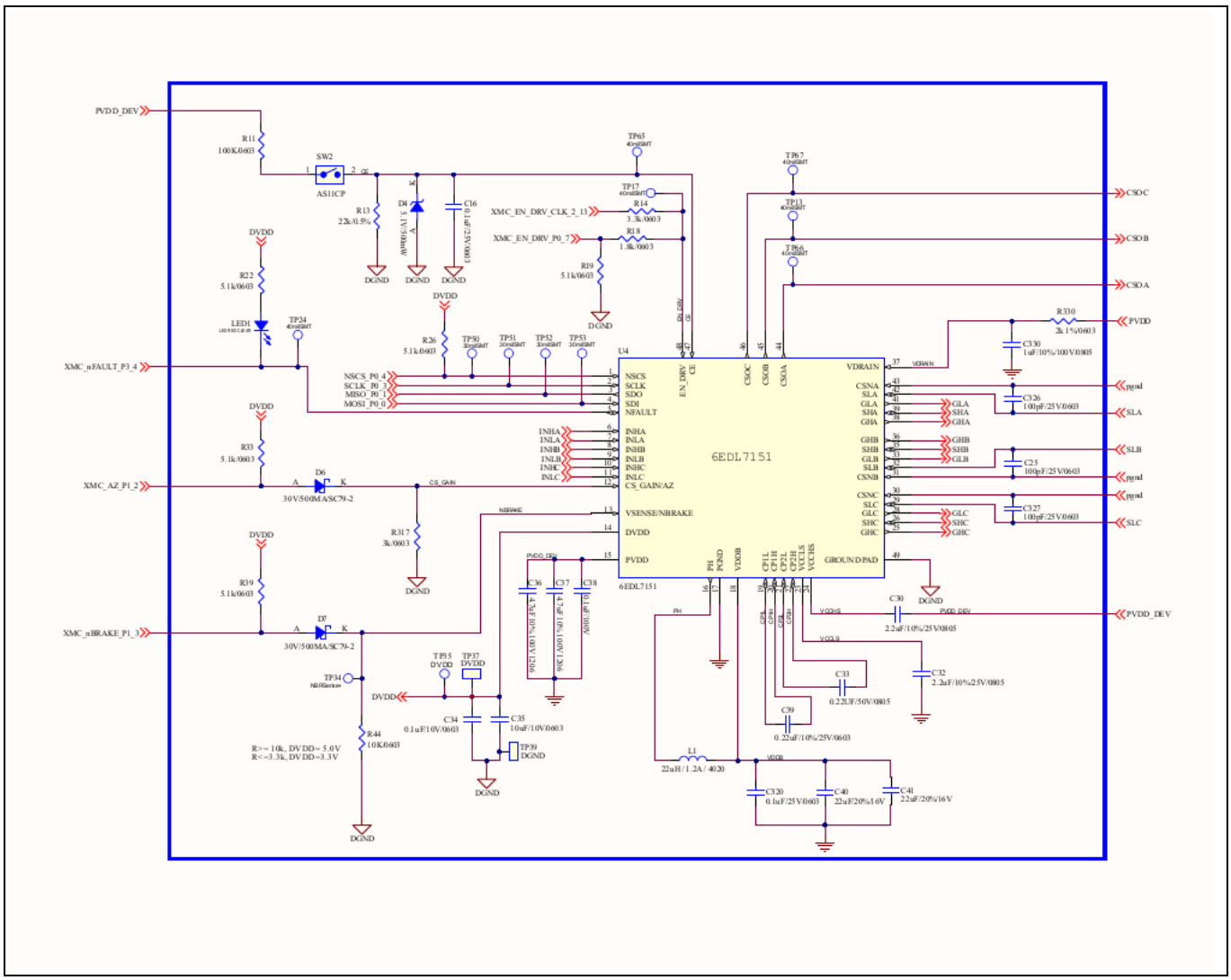

Figure 10 EVAL_6EDL7151_36V_1kW schematic – 6EDL7151 gate driver section

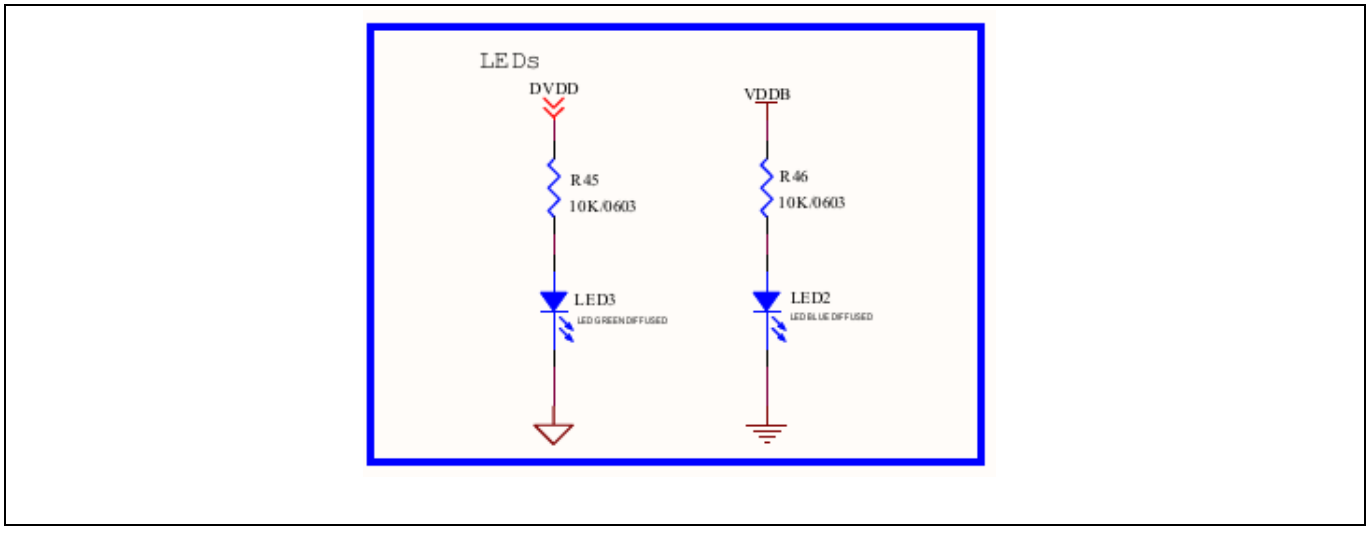

Figure 11 EVAL_6EDL7151_36V_1kW schematic – power LED indicators and connections

Schematics

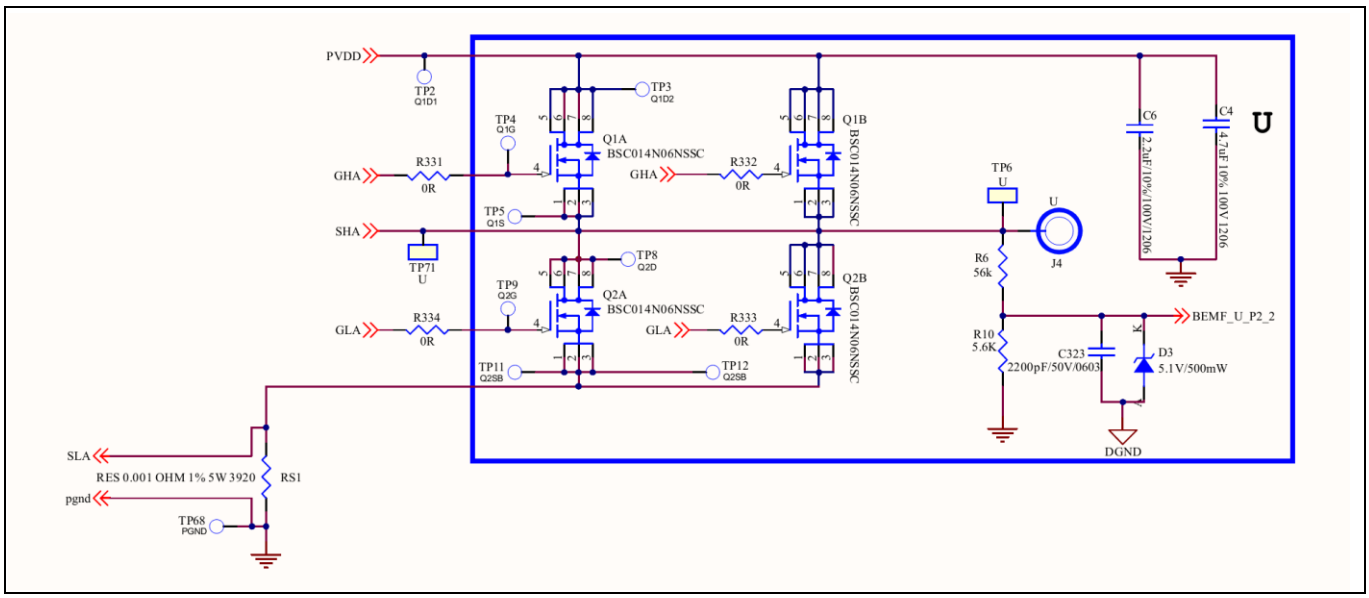

Figure 12 EVAL_6EDL7151_36V_1kW schematic – power stage, phase “U”

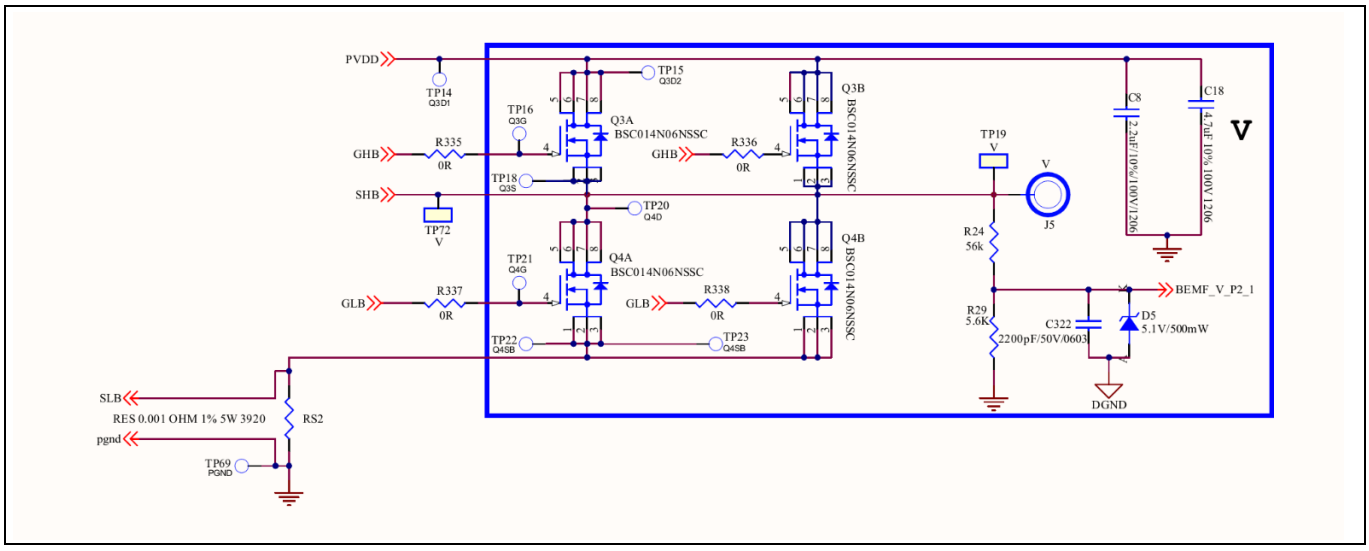

Figure 13 EVAL_6EDL7151_36V_1kW schematic – power stage, phase “V”

Schematics

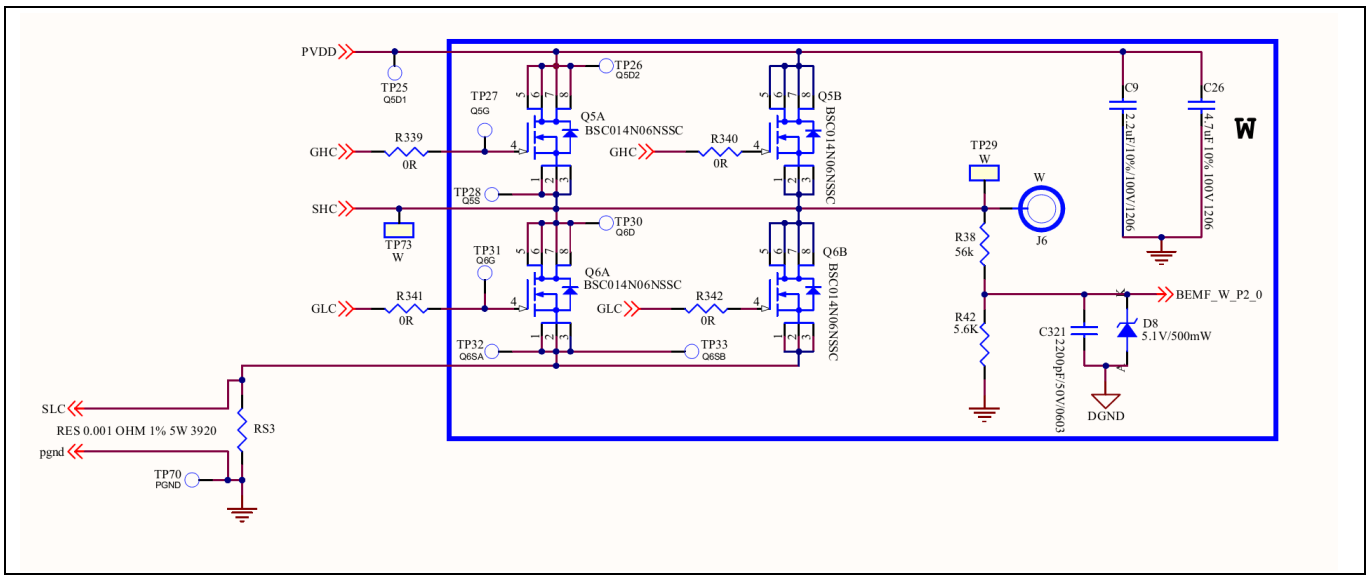

Figure 14 EVAL_6EDL7151_36V_1kW schematic – power stage, phase “W”

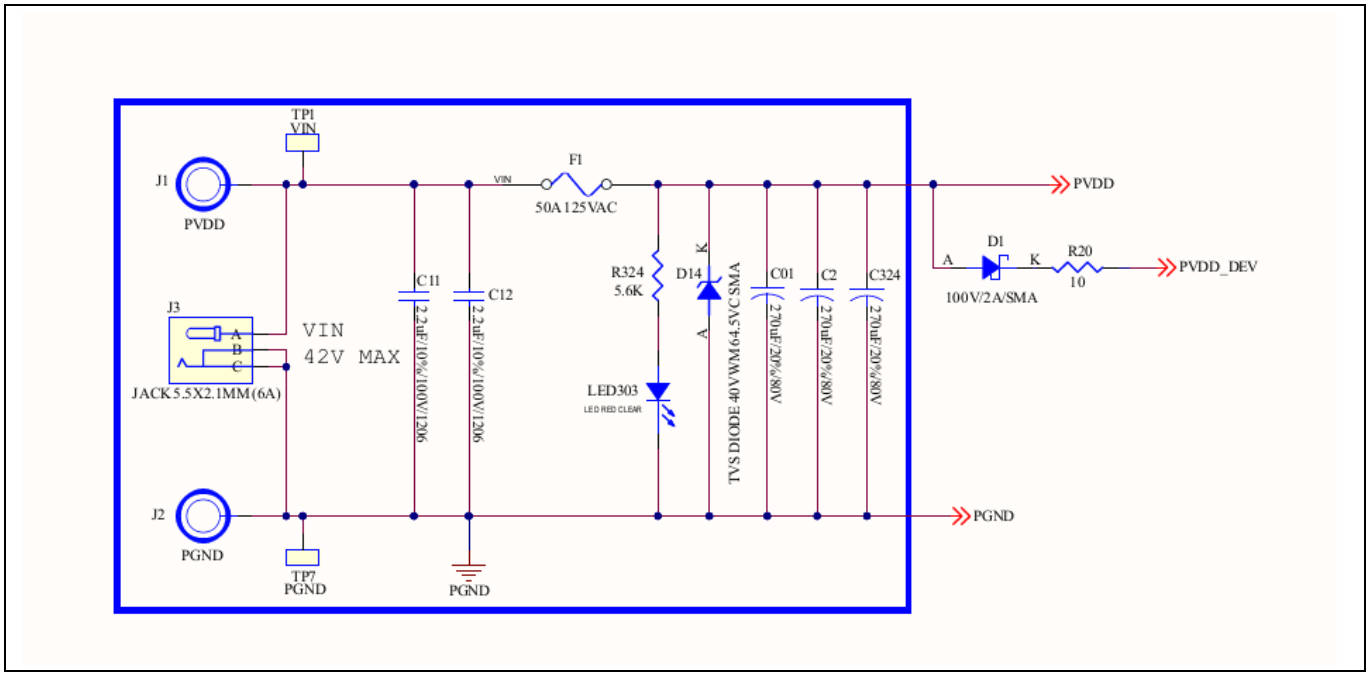

Figure 15 EVAL_6EDL7151_36V_1kW schematic – DC input

Schematics

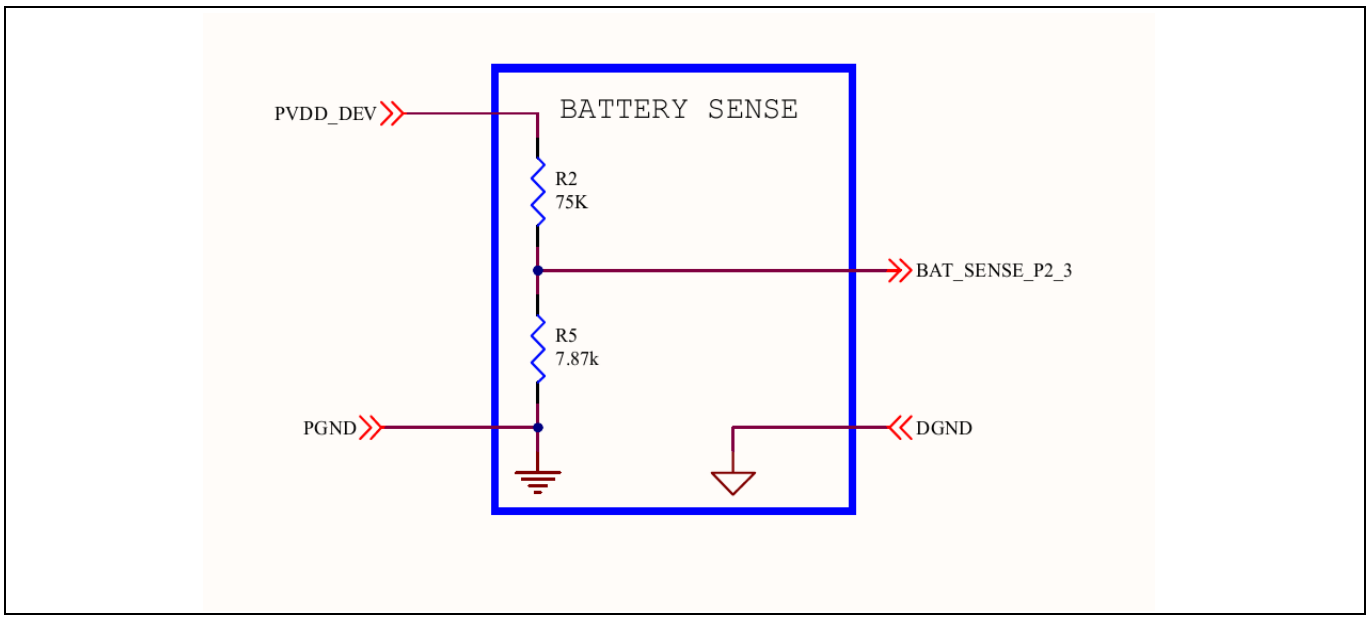

Figure 16 EVAL_6EDL7151_36V_1kW schematic – voltage sensing

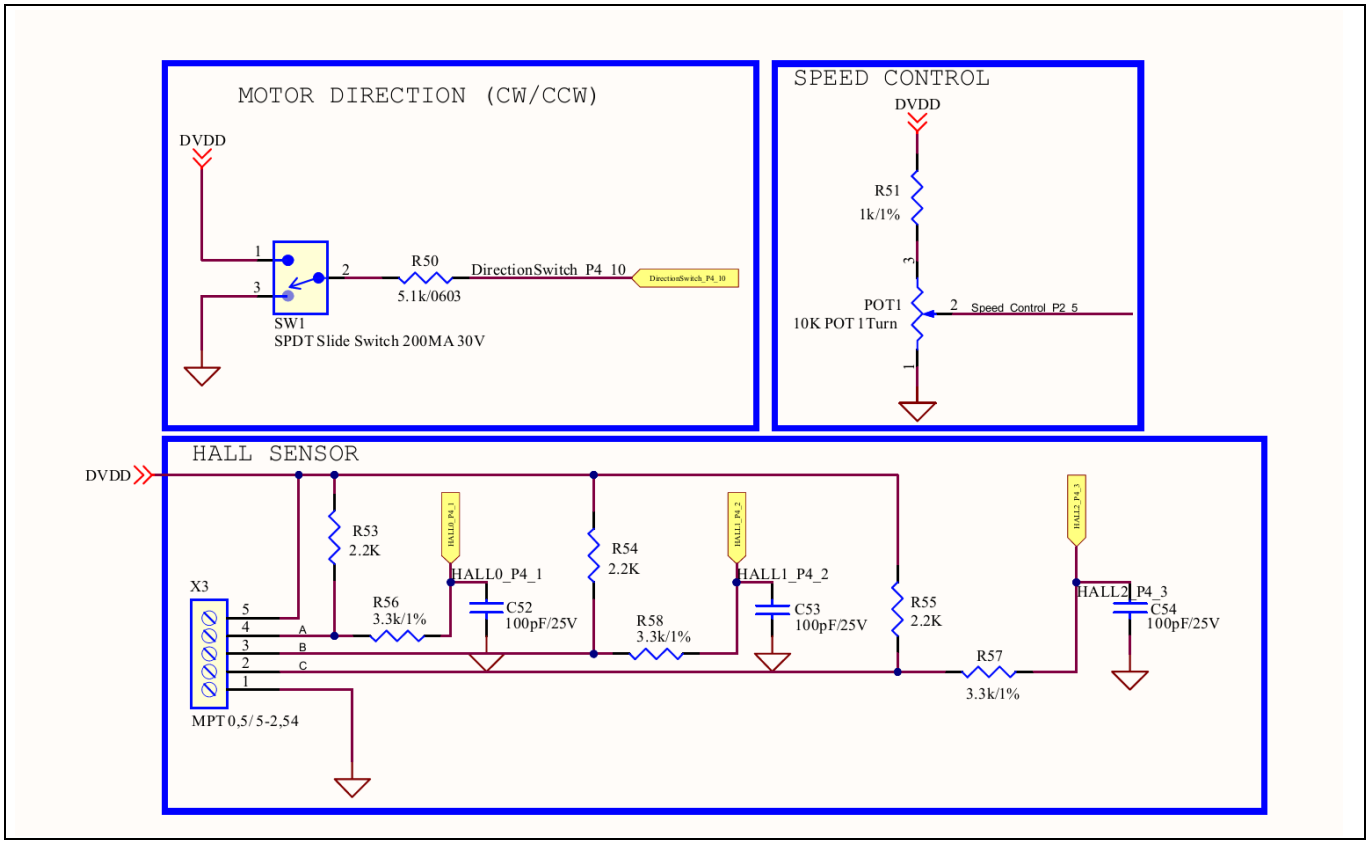

Figure 17 EVAL_6EDL7151_36V_1kW schematic – direction switch, speed control and Hall sensor inputs

Schematics

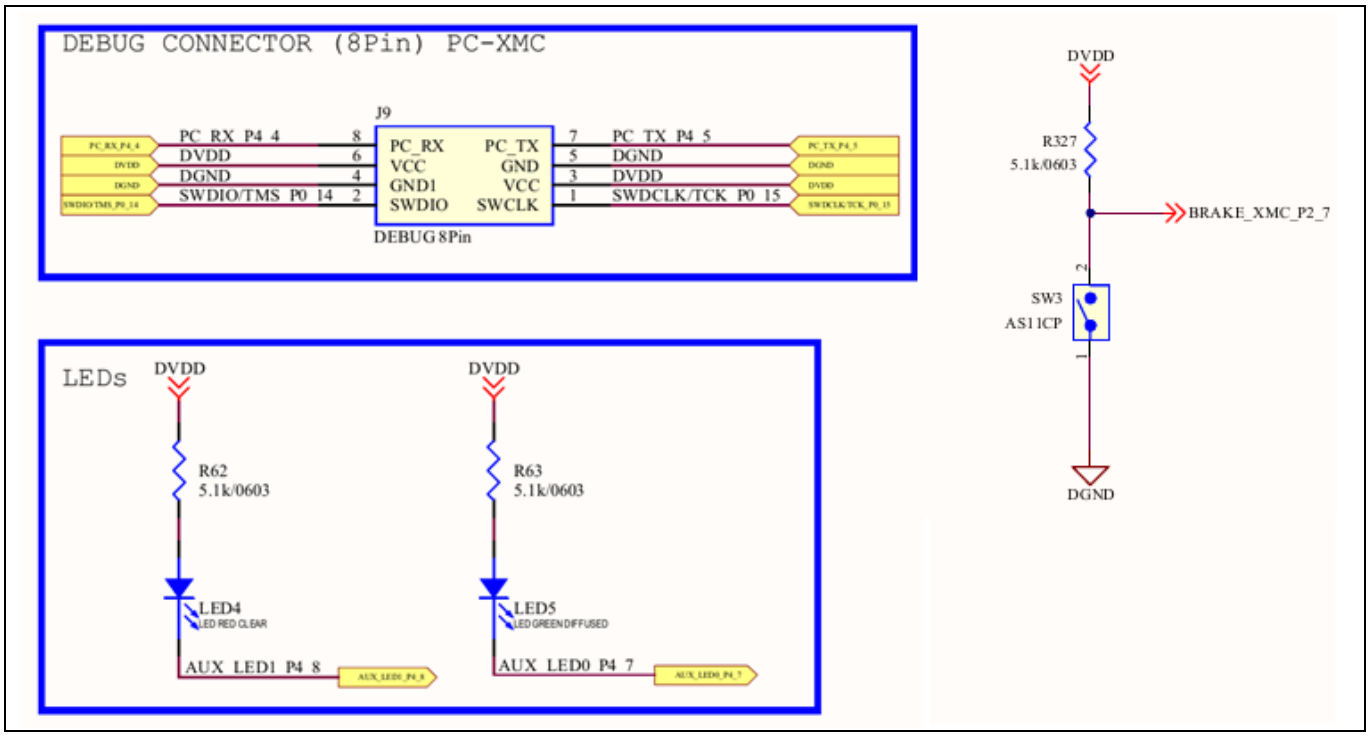

Figure 18 EVAL_6EDL7151_36V_1kW schematic – LED indicators, Brake, and external debugger

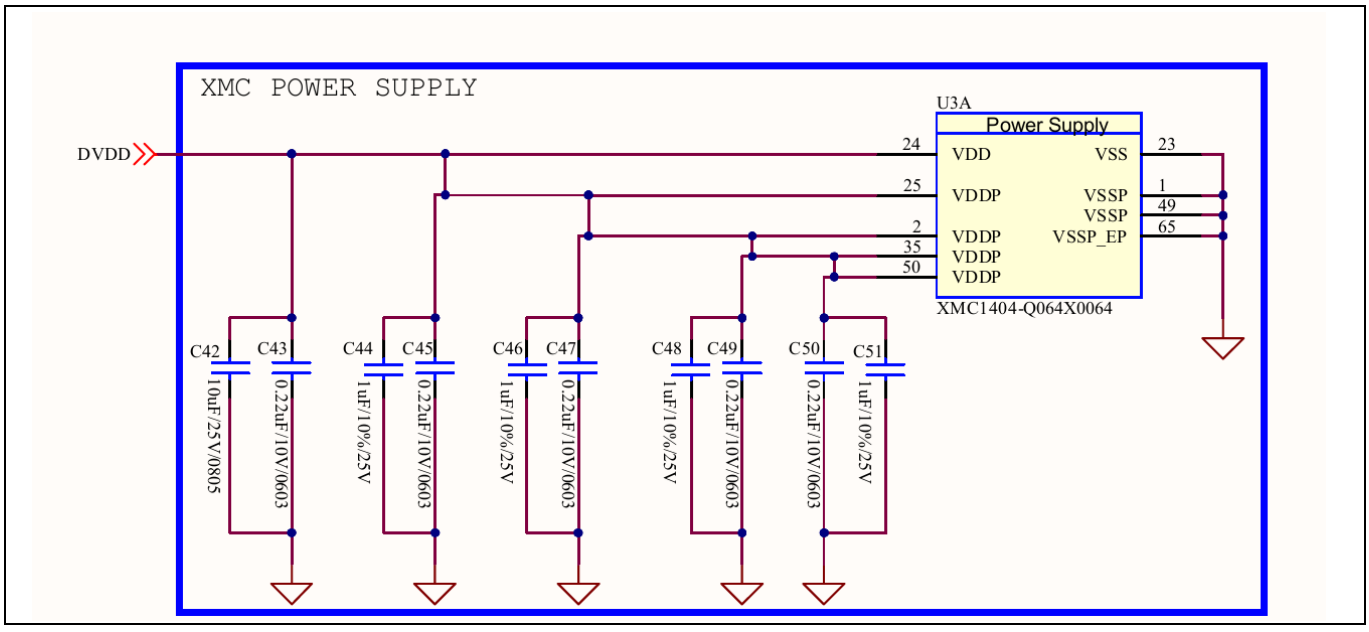

Figure 19 EVAL_6EDL7151_36V_1kW schematic – XMC1404 main controller power supply

Schematics

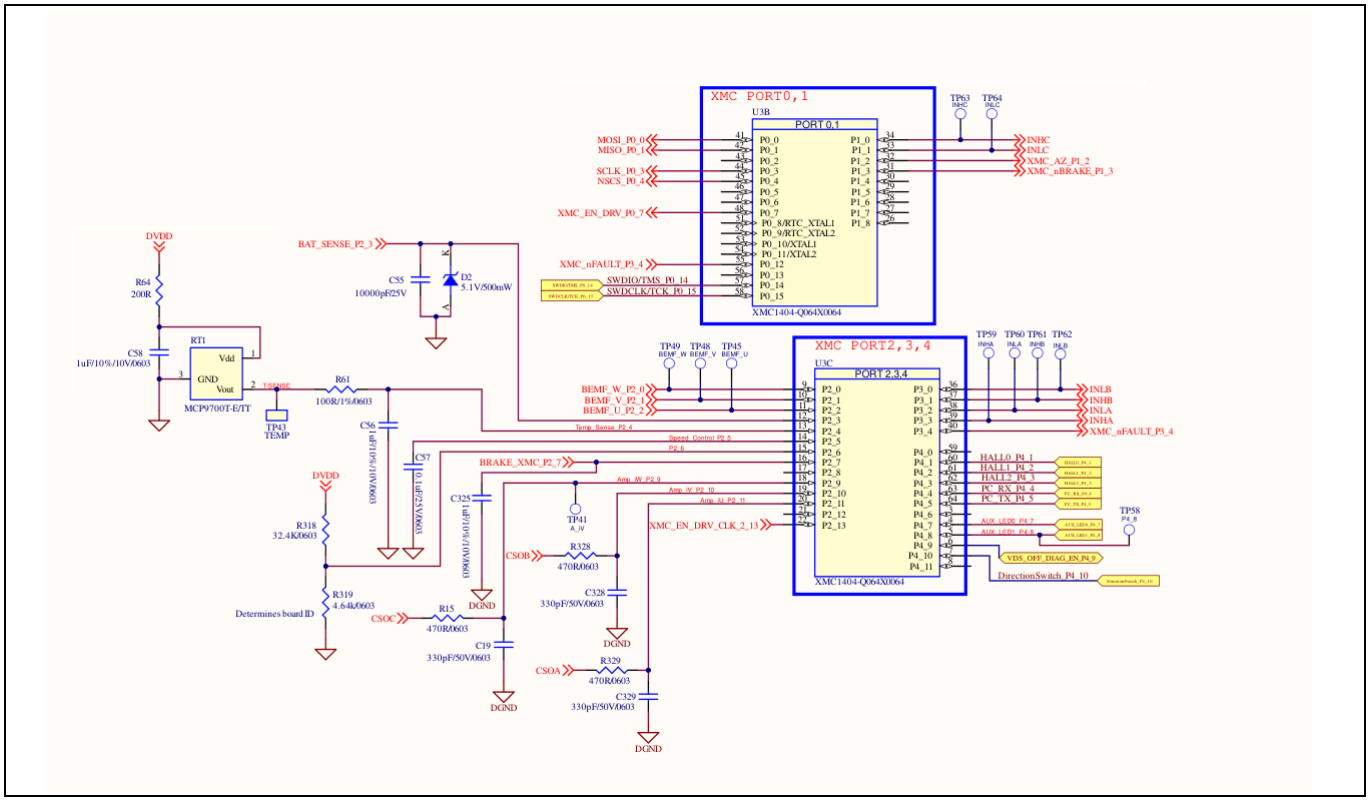

Figure 20 EVAL_6EDL7151_36V_1kW schematic – XMC1404 main controller connections

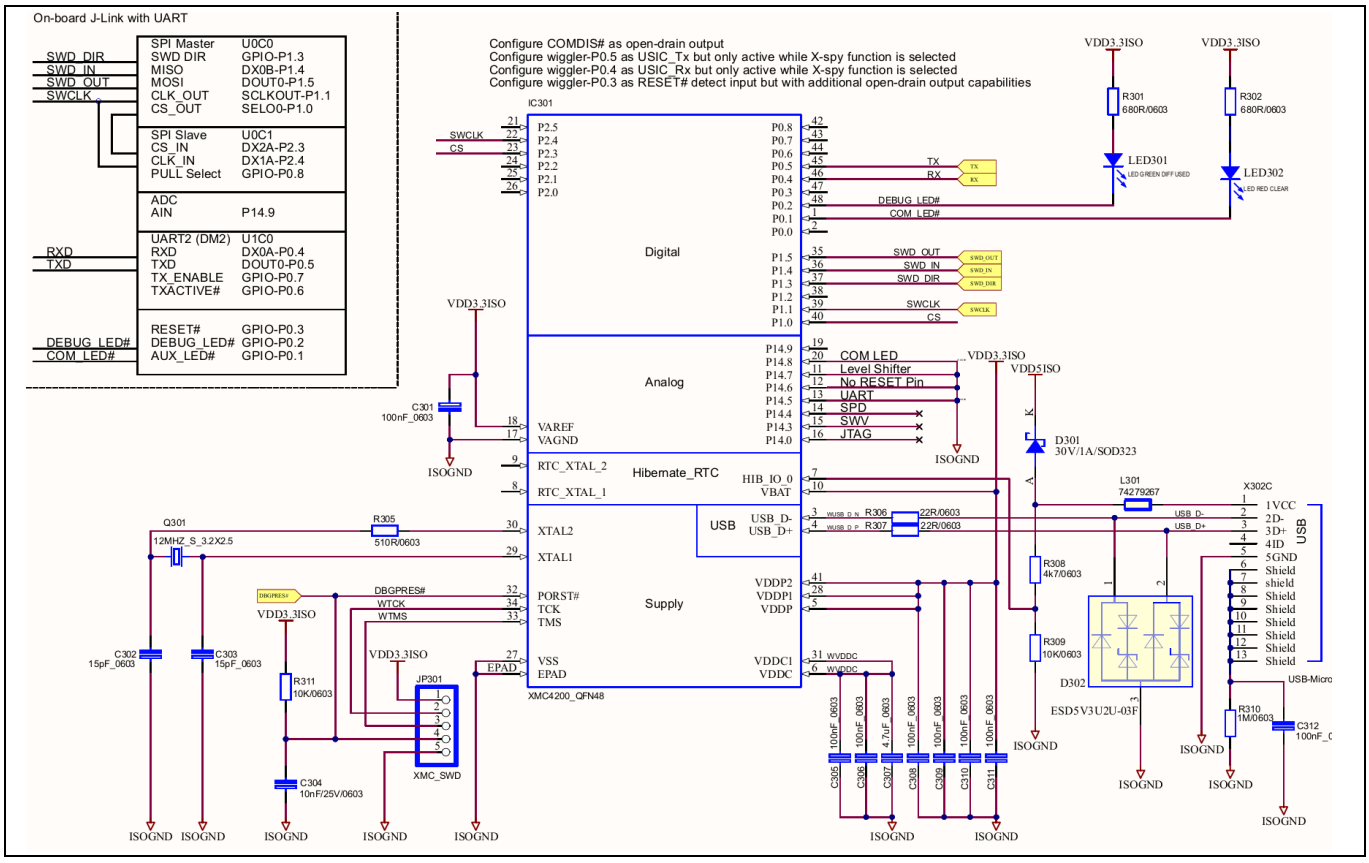

Figure 21 EVAL_6EDL7151_36V_1kW schematic – debugger controller section

Schematics

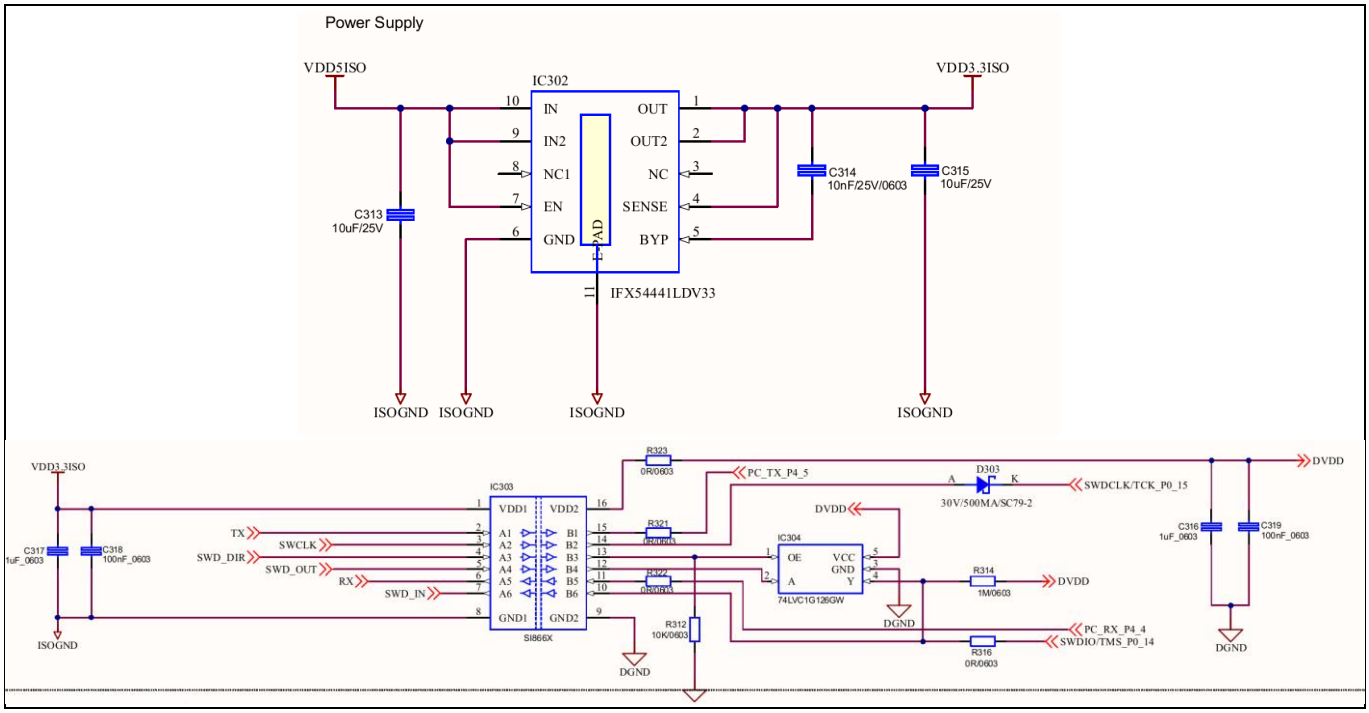

Figure 22 EVAL_6EDL7151_36V_1kW schematic – debugger power supply and isolators

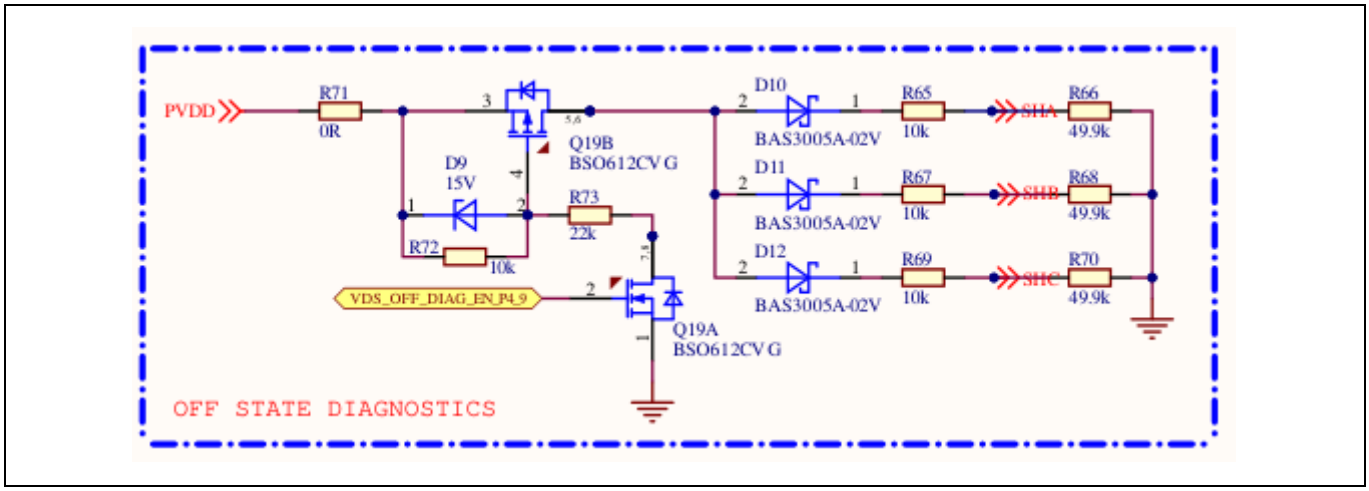

Figure 23 Off state diagnostics circuit

4 6EDL7151 smart gate driver

Optimized gate drive pulses to the high- and low-side MOSFETs in each phase are provided by the 6EDL7151 smart gate driver (U4). Logic-level switching PWM pulses are supplied to the 6EDL7151 from the XMC1404 microcontroller (U3). The high- and low-side gate drivers allow operation over the full duty-cycle range up to 100 percent. The gate drive voltages can be set to different levels, including 7 V, 10 V, 12 V, and 15 V. One benefit of the charge pumps is that voltage levels can be maintained even if the battery voltage drops to a lower level, allowing standard gate-level MOSFETs to be used.

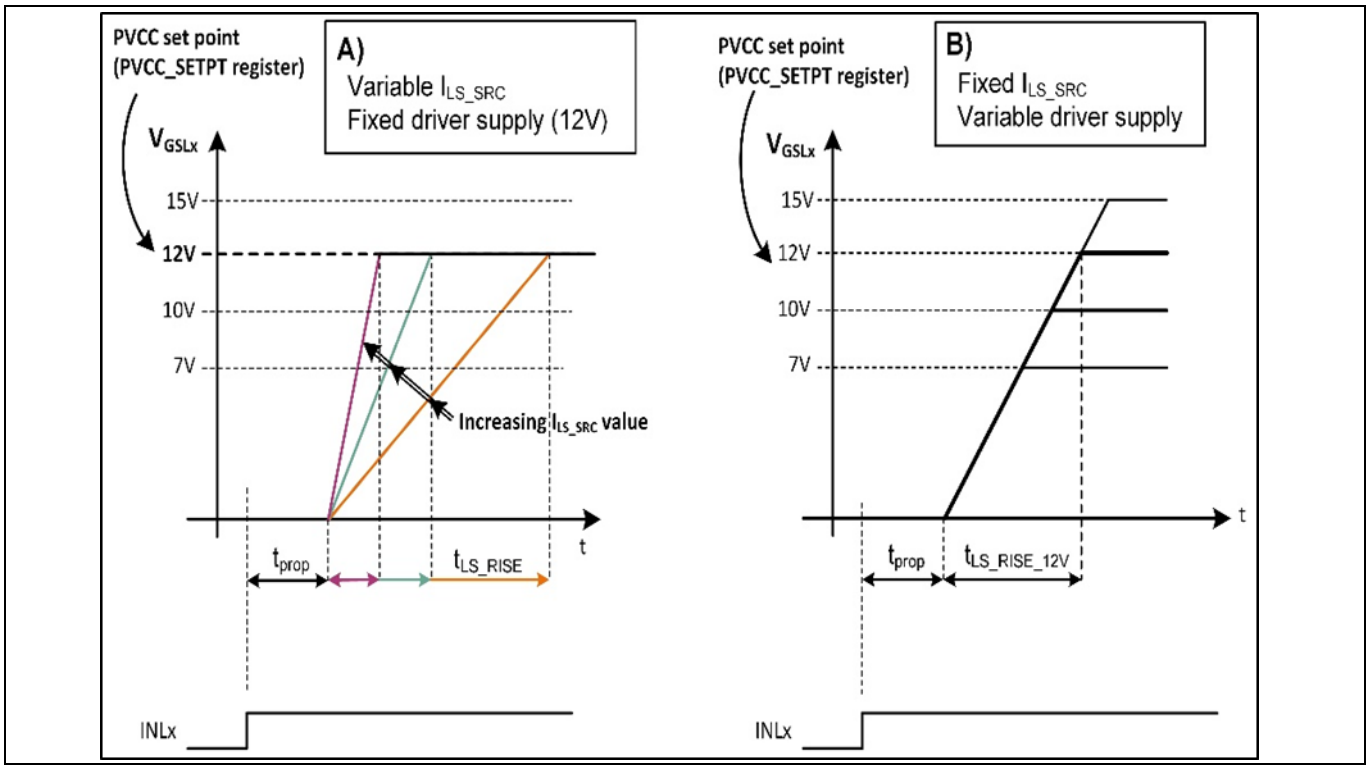

Figure 24 6EDL7151 gate drive control

Control of the drain-source rise and fall times is one of the most important parameters for optimizing drive systems, affecting critical factors such as switching losses, dead-time optimization and drain voltage ringing that can lead to possible MOSFET avalanching. Correct configuration of the gate drive also helps to minimize EMI emissions. The 6EDL7151 can control the slew rate of the driving signal to control the rise and fall slew rates of the drain-to-source voltage by adjusting the gate drive sink and source currents during different time segments during the switch-on and switch-off processes. This permits the designer to eliminate diode resistor networks commonly used in gate drive circuits. In most cases, gate resistors can be removed altogether, reducing component count and at the same time simplifying and allowing further optimization of the circuit layout.

4.1 Configuration of the gate driver

4.1.1 Gate drive current and timing

The gate driver implementation overview is illustrated in Figure 25. The EVAL_6EDL7151_36V_1kW evaluation board utilizes the 6PWM mode, in which the microcontroller inserts a specific dead-time between the INHx and INLx signals generated by its PWM modules. This driving scheme is also applicable to other PWM modes.

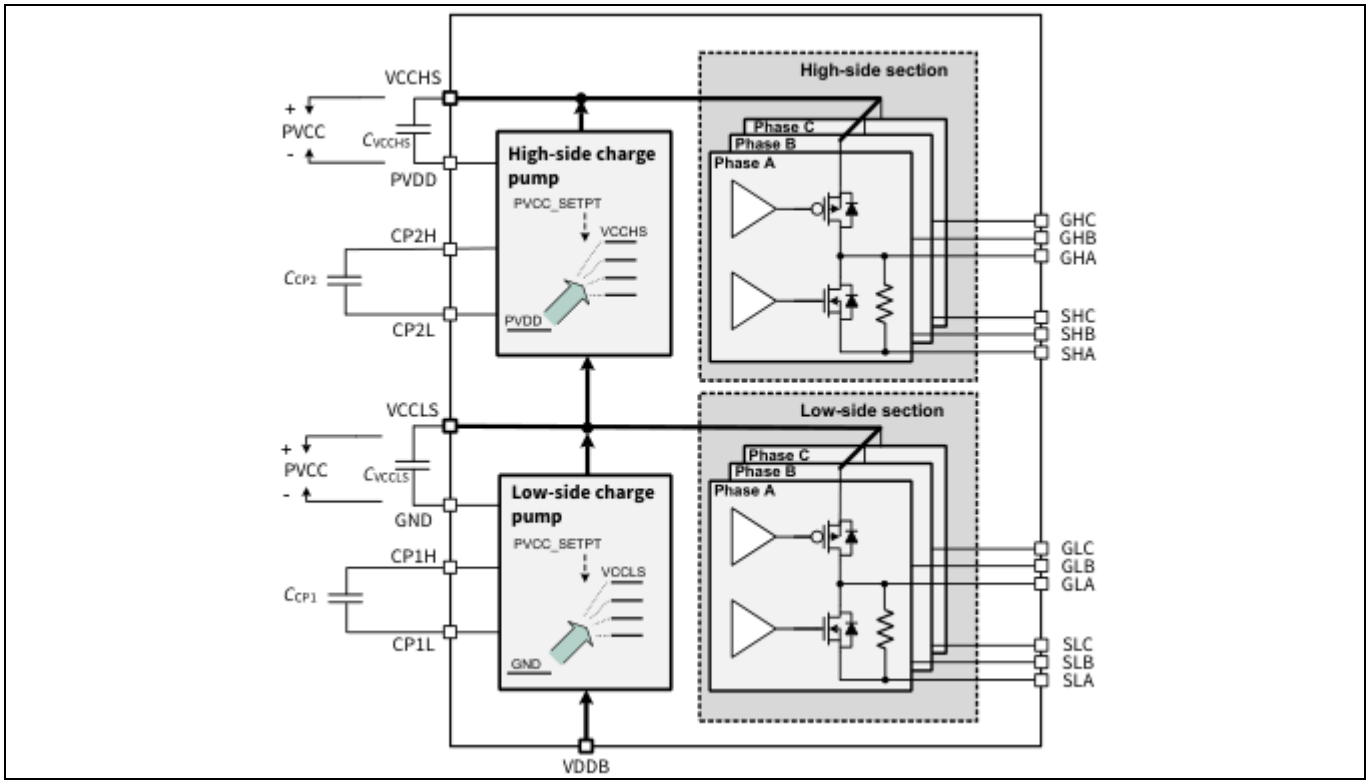

Figure 25 6EDL7151 Gate driver architecture

Using the GUI tool, the designer can configure the gate driver current and timings with the following parameters via SPI accessible registers:

Table 1 Gate drive parameters[1]

Parameter	Description	Minimum	Maximum
I_{HS_SRC}	Source current value for switching on high-side MOSFETs	10 mA	0.5 A
I_{HS_SINK}	Sink current value for switching off high-side MOSFETs	10 mA	0.5 A
I_{LS_SRC}	Current value for switching on low-side MOSFETs	10 mA	0.5 A
I_{LS_SINK}	Current value for switching off low-side MOSFETs	10 mA	0.5 A
I_{PRE_SRC}	Pre-charge current value for switching on both high- and low-side	10 mA	1.5 A
I_{PRE_SNK}	Pre-charge current value for switching off both high- and low-side	10 mA	1.5 A
T_{DRIVE1}	Amount of time that I_{PRE_SRC} is applied. Shared configuration between high and low.	0 ns	2.59 µs

[1] Available current and time delay values are listed in Section 3.16 “Register Map” of the 6EDL7151 datasheet [1].

6EDL7151 smart gate driver

Parameter	Description	Minimum	Maximum
T_{DRIVE2}	Amount of time that I_{HS_SRC} and I_{LS_SRC} are applied. Shared configuration between high-side and low-side drivers.	0 ns	2.55 µs
T_{DRIVE3}	Amount of time that I_{PRE_SNK} is applied. Shared configuration between high- and low-side drivers.	0 ns	2.59 µs
T_{DRIVE4}	Amount of time that I_{HS_SINK} and I_{LS_SINK} and are applied. Shared configuration between high-side and low-side drivers.	0 ns	2.55 µs

Figure 26 shows the slew rate control timing for a complete switching cycle on a 6PWM mode. Propagation delays are not shown for simplification of the diagram. When the input signal from the microcontroller transitions from low to high, the gate driver switch-on sequence is triggered. The gate drive output first applies a constant current defined by the user-programmable value I_{PRE_SRC} for a time defined by T_{DRIVE1}, at the end of which the MOSFET gate voltage should have reached the threshold voltage $V_{GS(TH)}$. The next period of the gate switch-on sequence is defined by the parameter T_{DRIVE2}, which begins immediately after the completion of T_{DRIVE1}. The current applied during T_{DRIVE2} determines both the dI_D/dt and dV_{DS}/dt of the MOSFETs, as it will supply the current to charge the Q_{SW} of the MOSFET being driven.

In the three-phase motor drive configuration, each half-bridge operates in continuous mode with hard switch-on of either the high-side or the low-side depending on the direction of current in the motor windings. Once the T_{DRIVE2} period has elapsed, the gate driver applies full current (1.5 A) to ensure the fastest full turn-on of the MOSFET by supplying the remaining charge required to raise V_{GS} to the programmed PVCC value ($Q_{OD} = Q_G - Q_{SW} - Q_{G(TH)}$).

A similar process takes place during the switch-off of the MOSFET, in which the parameters T_{DRIVE3} and T_{DRIVE4} determine the periods for which the programmed discharge currents are applied.

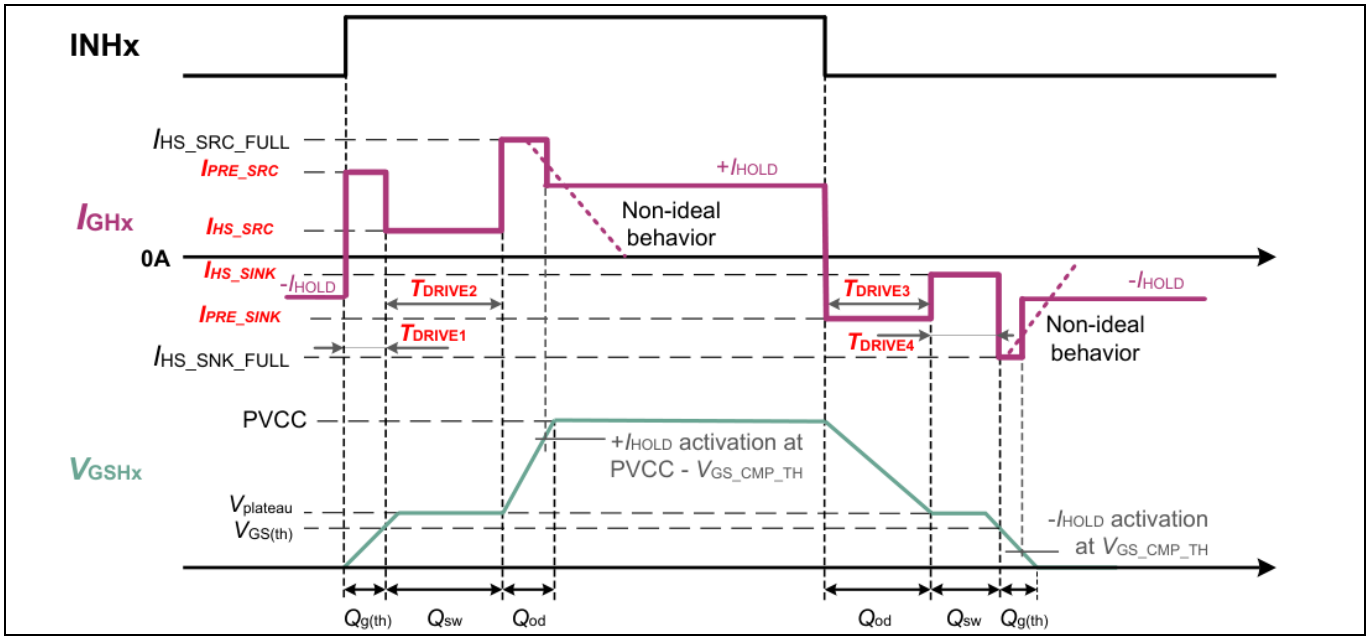

Figure 26 6EDL7151 gate drive profile

Figure 26 shows the V_{GS} charging and discharging transitions for a high-side MOSFET in one of the inverter phases during a typical hard-switched transition. The different charging and discharging phases of the MOSFET switch-on and switch-off are illustrated above. Thanks to the flexible timing structure provided by the 6EDL7151 gate driver with its high $T_{DRIVE(X)}$ resolution and ability to set the current during each interval, the designer can configure and optimize the switch-on and switch-off operations without the need for any external gate drive components.

During hard switching, the controlled gate drive currents enable adjustment of the slew rate dV_{DS}/dt, by controlling the gate drive current in periods T_{DRIVE2} and T_{DRIVE4} during which the charge Q_{SW} is injected or extracted from the gate as V_{DS} transitions. Higher currents can be used for fast charging and discharging of $Q_{GS(TH)}$ and Q_{OD}, since neither dI_D/dt nor dV_{DS}/dt are affected during these periods.

The pre-charge current can be selected from 17 available values, of which 16 of them are defined by $I_{PRE\_SRC/SNK}$ with an additional 1.5 A option, which is the maximum current capability of the gate driver. In cases where larger MOSFETs with relatively high gate charge are used, $Q_{G(TH)}$ during turn-on or Q_{OD} during turn-off may benefit from using the full gate driver capability. Full strength during the pre-charge may be selected via the GUI. In cases where $Q_{G(TH)}$ is too small to apply a larger current than the one used for slew rate control, the user can set T_{DRIVE1} to value zero, resulting in the gate driver going immediately to the beginning of the T_{DRIVE2} period with its corresponding gate current setting. This enables optimization for both large and small MOSFETs covering different technologies such as OptiMOS™ or StrongIRFET™. The T_{DRIVE1} and/or T_{DRIVE3} can be set to zero, resulting in those intervals being skipped if required.

Note: When adjusting the slew rate, it is necessary to set the dead-time greater than the sum of T_{DRIVE1} and T_{DRIVE2} (low to high transition) or T_{DRIVE3} and T_{DRIVE4} (high to low transition), or whichever is greater if both dead-times are equal.

4.1.2 Gate drive voltage

As described previously, motor drive systems utilize a range of different MOSFET sizes and technologies. Generally, increasing the driving voltage reduces the $R_{DS(on)}$ and associated power loss. But also increases the switching rise and fall times, leading to higher switching losses. However, 6EDL7151 has programmable currents during turn on and turn-off times, which leads to reduction in the effective rise and fall times even with increased gate drive voltage.

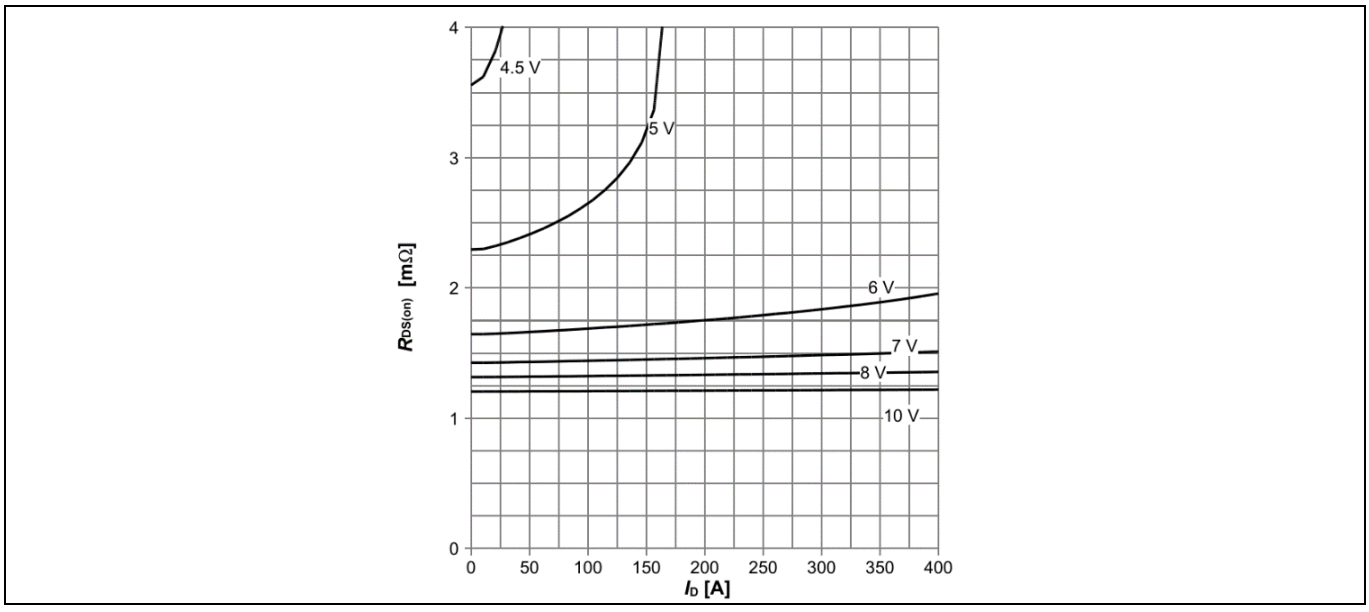

Figure 27 BSC014N06NSSC $R_{DS(on)}$ vs. V_{GS} characteristic

6EDL7151 smart gate driver

The 6EDL7151 offers the designer several driving voltage options to select from depending on the system requirements, allowing them to adjust the MOSFET driving voltage (PVCC voltage) via SPI registers. The same-value PVCC applies to both high- and low-side charge pumps with four possible values: 7 V, 10 V, 12 V, and 15 V. This is done by setting the bit field PVCC_SETPT via the GUI, where the default value is 12 V. Gate drive outputs include undervoltage lockout (UVLO) protection.

The MOSFETs in an inverter can be exposed to non-zero gate-source voltage levels when gate drivers are not activated. In some cases, such voltages can be high enough to pass the MOSFET gate turn-on threshold, partially switching on the device. If a high- and low-side MOSFET in an inverter phase were to switch on at the same time, the resulting high current could destroy the devices. To prevent this, it is common to add weak pull-down resistors between the gates and sources of each MOSFET. The 6EDL7151 avoids the need for these resistors by integrating the following functions into its gate driver outputs:

- Weak pull-down: A weak pull-down (RGS_PD_WEAK) is always connected between gate and source of each gate driver output. This ensures a weak pull-down during states where the gate driver is off, either because EN_RV is turned off or because the device is fully off (CE off). This mechanism is similar to the ones described above.
- Strong pull-down: During gate driver off periods, if the external gate-to-source voltage increases for any reason, a strong pull-down (RGD_PD_STRONG) is activated, ensuring a tight pull-down to prevent any partial turn-on.

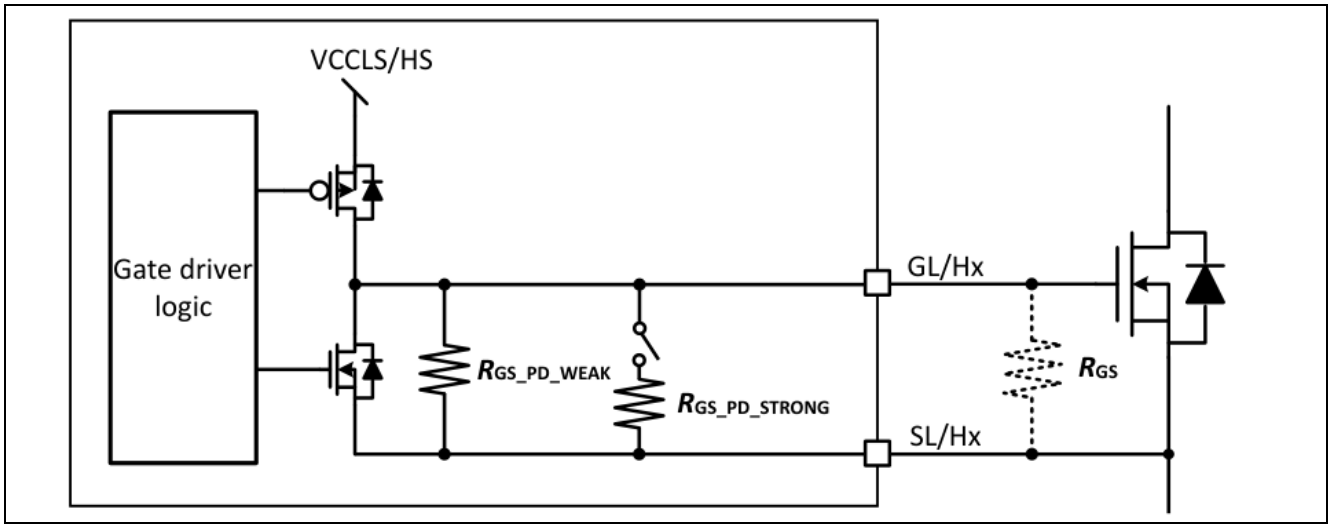

Figure 28 In-built pull-downs in 6EDL7151

4.1.3 Setting driver parameters

As described in the previous section, setting the right values of all the TDRIVEx, Dead times, and Source and Sink currents is a crucial set during the design phase. This involves calculating the values using a MOSFET datasheet, which can be a tedious task. However, this task is simplified with the ModusToolbox™ Motor Suite using the MOSFET tuning feature.

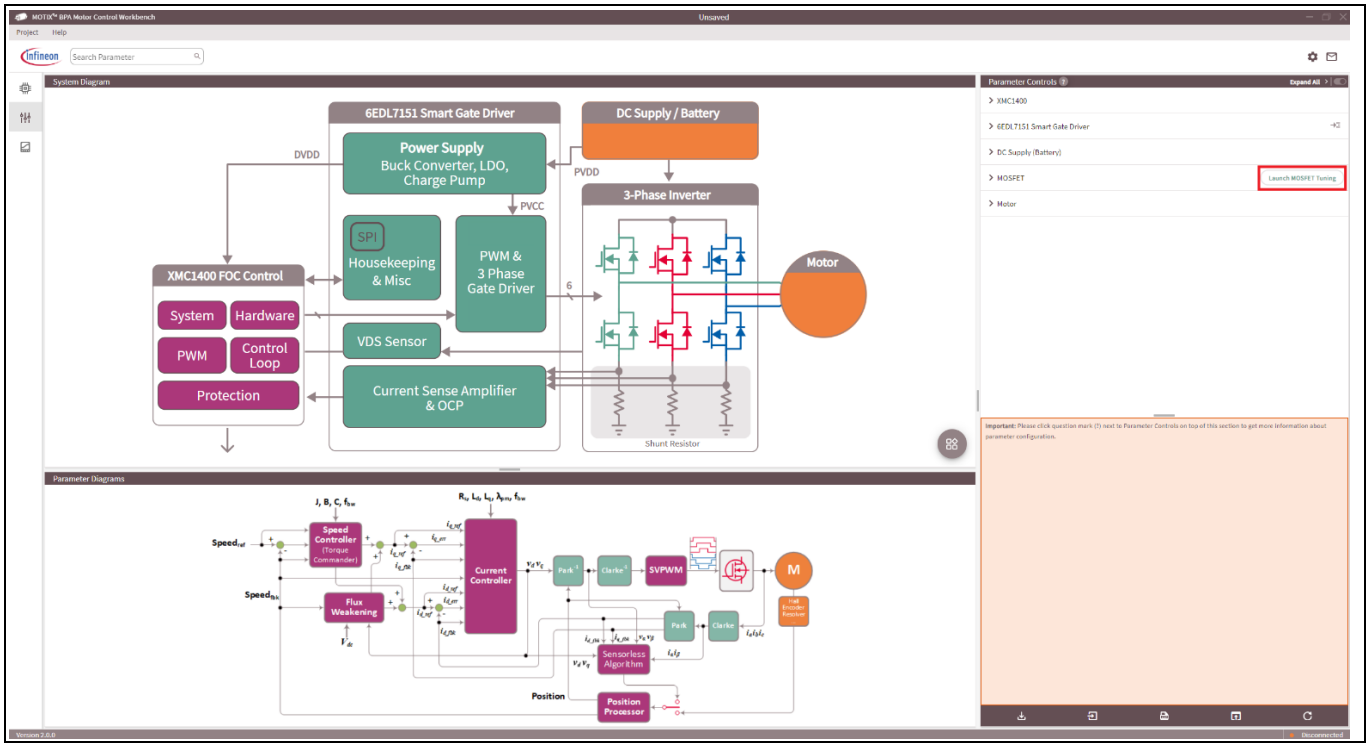

Figure 29 MOSFET tuning in GUI

By selecting the right Infineon MOSFET from the dropdown list and entering the minimal details about the operating conditions as shown in the Figure 30, the tool will calculate all the required parameters. This is especially useful as the MOSFET tuning tool takes actual test data from the Infineon database.

6EDL7151 smart gate driver

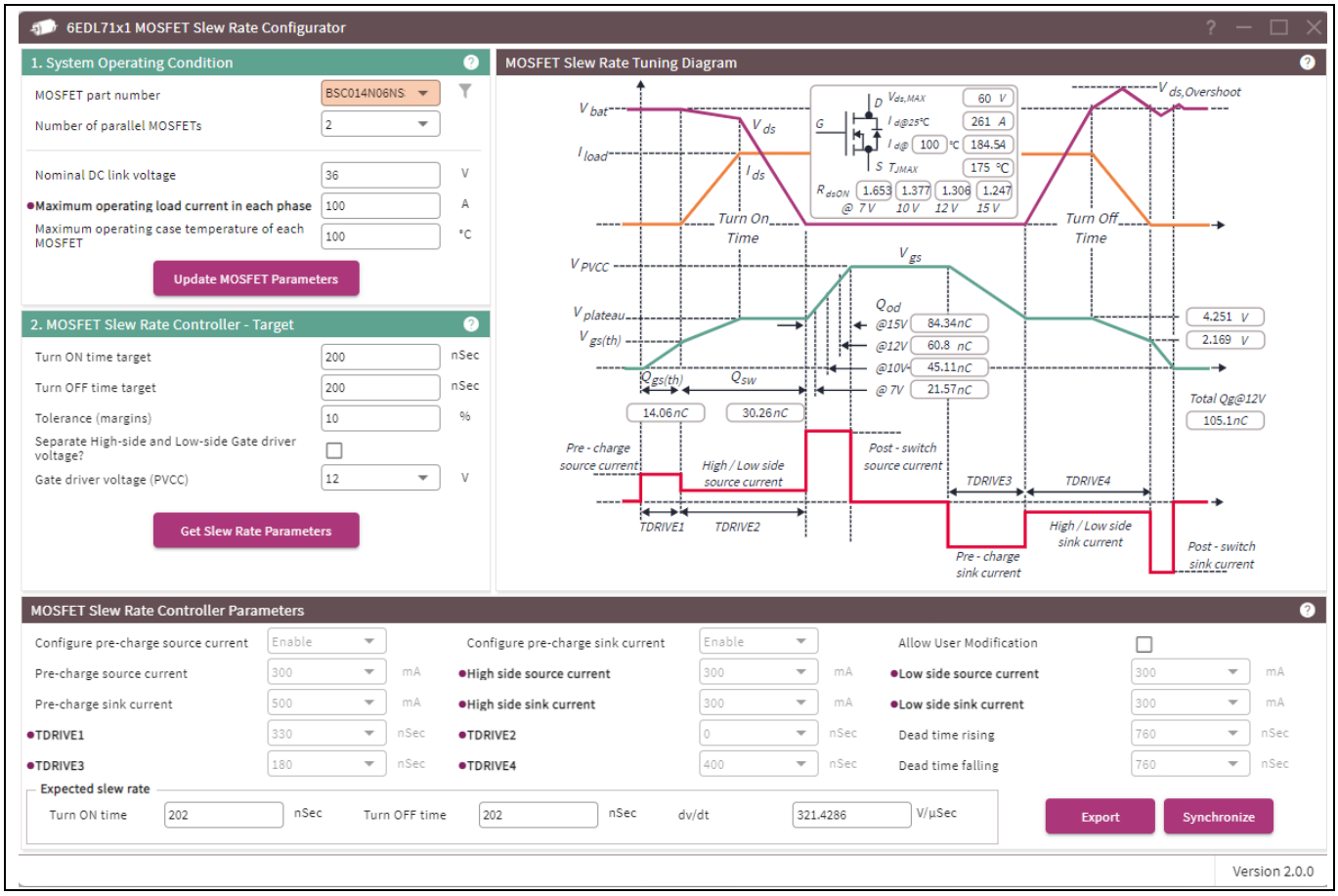

Figure 30 Setting the value of gate drive parameters of 6EDL7151

These values should be considered as the initial estimates for fine-tuning based on bench data, because the calculations do not take the parasitics of the PCB into account. Table 5 list the configuration used for capturing the test results in this document.

4.2 Configuration of the buck and linear regulators

The VDDB output can be used to supply external components as long as the current limits of the buck converter, charge pumps, and linear regulator are not exceeded. The maximum average current of the buck converter is 600 mA. The voltage may be set to 6.5 V, 7 V, or 8 V, depending on the gate drive voltage selection. The overcurrent protection (OCP) is also implemented for the buck converter to prevent any damage to the device if the VDDB output becomes overloaded.

Two different switching frequencies, 500 kHz or 1 MHz, can be selected via the GUI. In this evaluation board, the buck inductor L1 value is 22 µH for 500 kHz switching. If switching at 1 MHz is desired, a 10 µH inductor needs to be used. The values for the buck output capacitors C40 and C41 are 22 µF with an additional 0.1 µF ceramic capacitor C320 added to reduce high-frequency noise. Both the synchronous buck converter and linear voltage regulator circuits are shown in the Figure 31. The high-side switch inside the buck is a p-FET, this eliminates the need for an additional bootstrap capacitor to drive the high-side switch. The buck converter operates in an Adaptive Constant on time (ACOT) scheme.

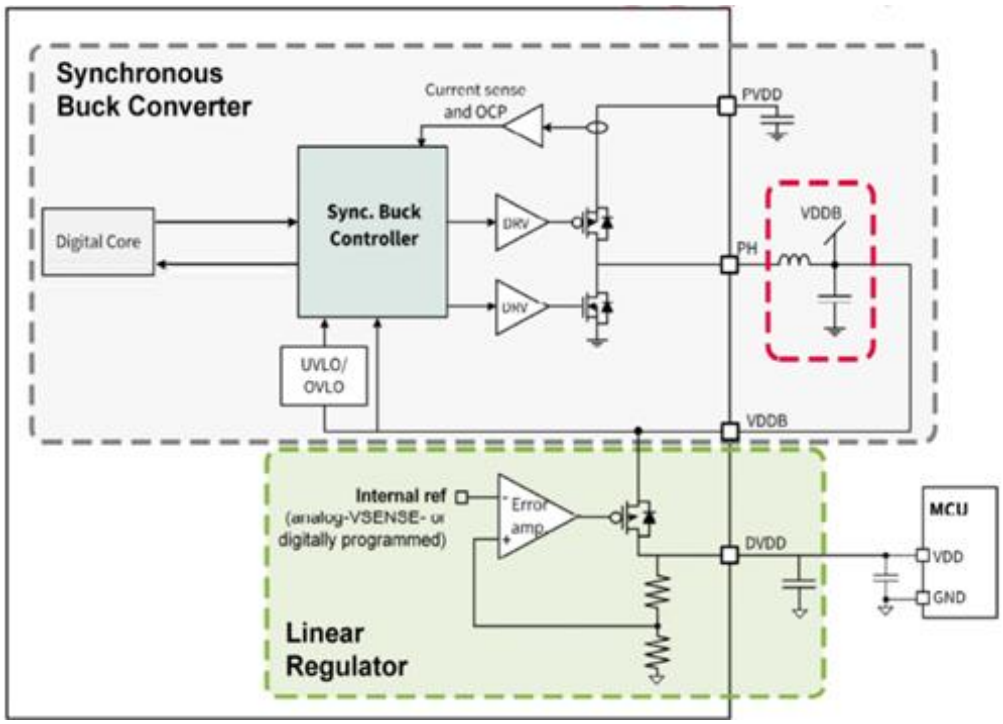

Figure 31 Detail of integrated synchronous buck converter and linear regulator

The following protections are implemented to ensure correct operation of the buck converter:

- Output UVLO
- Output overvoltage lockout (OVLO)
- OCP, cycle by cycle

If the current exceeds the OCP level, the buck converter controller terminates the high-side gate drive pulse until the start of the next PWM period. The low-side operates accordingly after insertion of the dead-time. Once the OCP event takes place, a counter increments each consecutive period that the peak current is reached. After 16 switching cycles, the buck OCP fault is triggered and the nFAULT pin is set low to signal the MCU. The

buck converter will continue operation in current limitation to ensure that the MCU remains powered. If the OCP is not triggered for three consecutive PWM periods, the counter resets.

The output of the buck converter VDDB is the input for the linear regulator. The integrated linear regulator output DVDD can be set to either 3.3 V or 5 V by means of an external resistor R44. On the evaluation board, R44 is set to 10 kΩ, which sets DVDD to 5 V. A 10 µF (C34) and a 0.1 µF(C35), two capacitors are connected to the DVDD pin. It is possible to override this hardware setting through the GUI, which can also read back the value set by the hardware. The LDO output supplies the internal sub-systems of the 6EDL7151, and this can also be used to power an external microcontroller if needed, as in the case of this evaluation board. The linear regulator can also be used to provide an offset to the current sense amplifiers to allow negative current measurements.

DVDD OCP can be configured between four different levels: 50 mA, 150 mA, 300 mA, or 450 mA, with 450 mA being the default value. If the OCP level is reached a fault is reported through the nFAULT pin. The DVDD OCP works in two different stages:

1. Pre-warning mode at 66% of the selected OCP levels:
   The nFAULT pin is pulled down to signal the controller that an OCP warning has occurred. If the current level reduces before reaching the 100% level, the operation will continue normally, releasing the nFAULT pin. The pre-warning allows some extra time for the microcontroller to make a decision on how to react to the possible OCP event.
2. Current limiting mode at 100% of the selected OCP level:
   If current increases beyond the configured OCP level, the DVDD regulator limits its output current. This causes the DVDD voltage to drop, eventually resulting in a DVDD UVLO fault if the UVLO threshold is crossed. This protects DVDD against a short-circuit condition.
   Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device should be operated only under the recommended operating conditions as specified in the datasheet [1].

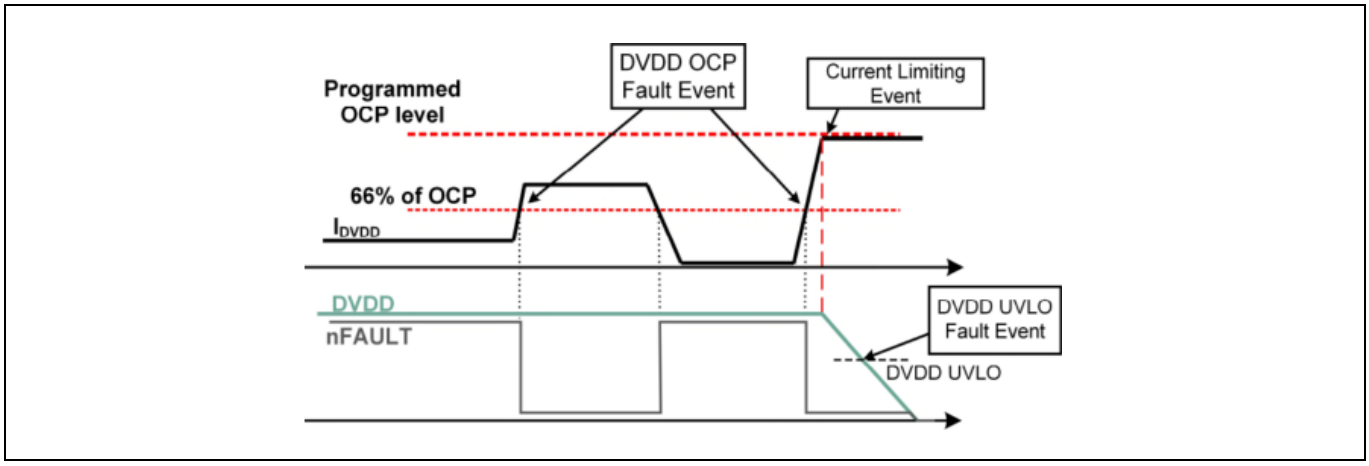

Figure 32 DVDD OCP behavior including pre-warning and current limiting modes

4.3 Configuration of the charge pumps

The gate drive voltage is generated from two separate charge pumps, VCCLS for low-side and VCCHS for high-side. The output voltage of the charge pump, i.e. the gate drive voltage (PVCC), can be set to 7 V, 10 V, 12 V, or 15 V through the GUI. The high- and low-side gate driver charge pumps are based on switched capacitor circuits that operate at a determined switching frequency. Selection from one of four frequencies, 781.3 kHz, 390.6 kHz, 195.3 kHz, and 1.56 MHz, allows flexibility for EMC optimization, with 781.3 kHz being the default setting. Another useful feature in reducing the EMI impact of the charge pump is the spread spectrum feature, which

can also be enabled and disabled via the GUI. This function is enabled by default to provide a frequency variation into the charge pump clock signal in order to distribute emissions over a wider frequency range, thereby reducing peaks in the EMI spectrum.

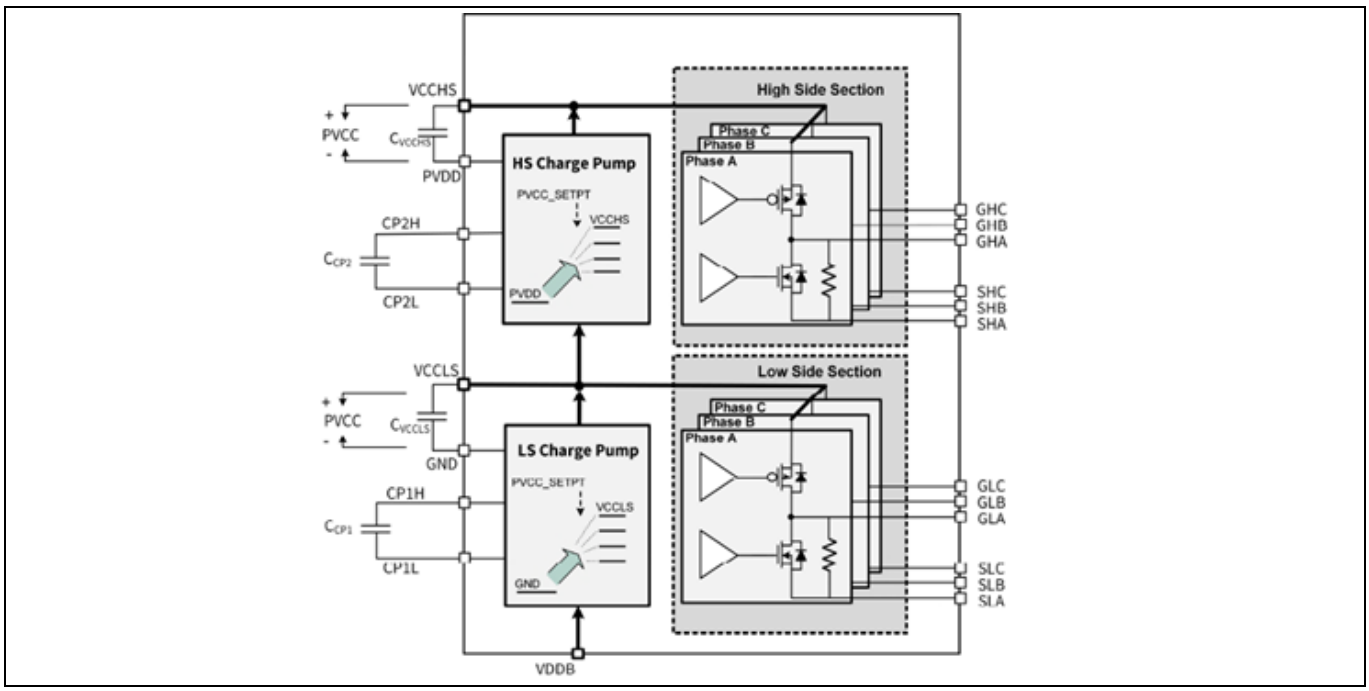

Figure 33 6EDL7151 integrated charge pumps and gate drivers

The selection of charge pump flying capacitors C33 and C39 are set at 0.22 µF and the tank capacitors C30 and C32 are set to 2.2 µF. The 6EDL7151 provides pre-charging of the charge pump output capacitors (C32) to a voltage just below the buck converter output voltage (VDDB) before the EN_DRV pin is activated. In this way, the charge pump start-up time and therefore the system start-up time are reduced. In this case, when EN_DRV is activated by the microcontroller to enable the gate driver stage, the charge pumps need only to ramp up the voltage from the existing pre-charge voltage to the selected target value. Pre-charge is disabled by default and can be enabled via the GUI.

The start-up time for the charge pumps, defined as the time that the gate drive supply voltages require to get to the target programmed voltage, depends on several factors:

- Target voltage: The higher it is, the longer the start-up time for the gate drivers.
- Charge pump clock frequency: Higher clock frequency results in faster start-up time.
- Charge pump tank capacitor values: A smaller value results in faster ramp-up time but higher ripple.
- Charge pump flying capacitors: Smaller capacitors lead to slower start-up time.

The charge pumps feature the UVLO protection VCCLS UVLO and VCCHS UVLO. The UVLO prevents the gate driver from propagating PWM signals if the drive voltage is not above the UVLO threshold. If UVLO occurs on either VCCLS or VCCHS, the nFAULT pin is pulled low so the microcontroller in the system can action to be performed.

4.4 Configuration of the current sense amplifiers

The 6EDL7151 integrates three current sense amplifiers that can be used to measure the current in the inverter via shunt resistors (Figure 37) or can be configured to sense voltage across the $R_{DS(on)}$ of the low side MOSFETs

(Figure 36). Single-, double-, or triple-shunt measurements are supported, as shown in Figure 34. Each current sense amplifier can be enabled individually with programmable gain and offset are generated internally.

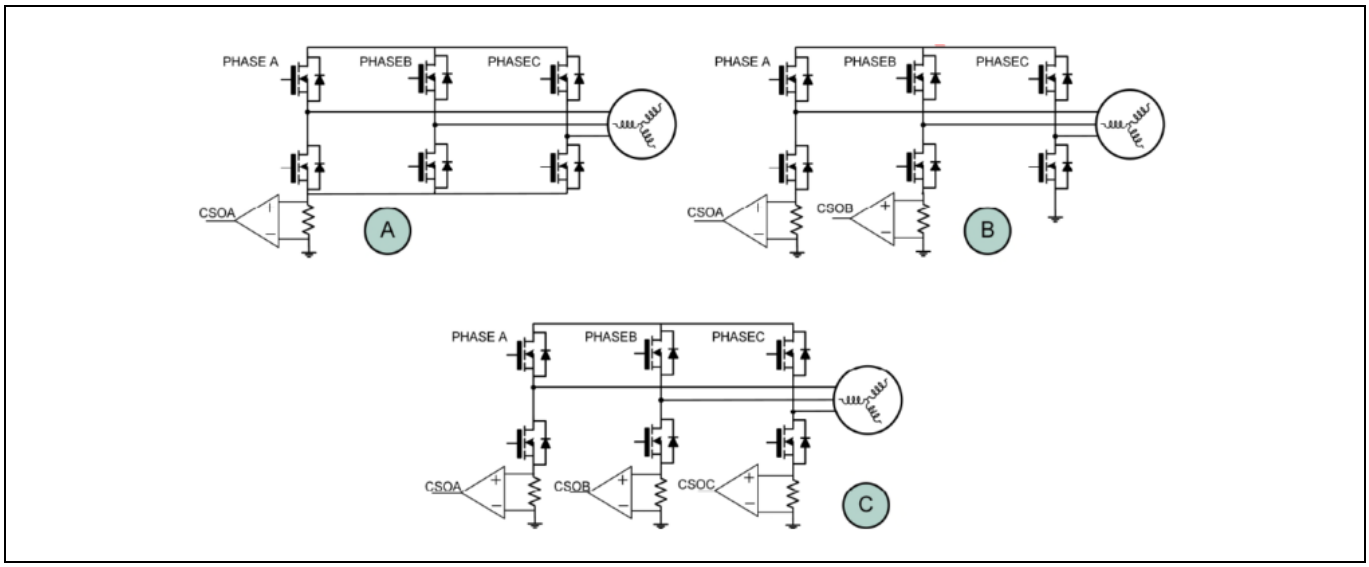

Figure 34 Single- (A), dual- (B) and triple- (C) shunt current sensing configurations

The current sense amplifier block contains the following sub-blocks, explained in detail in this section:

- Current sense amplifier: Connected to external shunt resistor or internally to an SHx pin for $R_{DS(on)}$ sensing. This module amplifies the shunt voltage or $V_{DS(on)}$ voltage to a level suitable for a microcontroller ADC input. It includes leading-edge blanking of the signal synchronized to the gate drive, which is active during periods to eliminate noise.
- Output buffer: Allows adding a variable offset voltage to the sense amplifier output. The offset amount can be set to one of four different values, programming the internally generated level. With this implementation, negative shunt currents can also be measured.
- Positive overcurrent comparator: Used for detecting the overcurrent conditions on motor windings for positive shunt voltage. This comparator causes the gate drive pulse to be terminated, thus limiting the motor current.
- Negative overcurrent comparator: Used for detecting the overcurrent condition on motor windings for negative shunt currents.
- OCP DAC: Used for programming the overcurrent comparator thresholds. One sets the positive level and a second sets the negative level, which is shared among the different OCP comparators.

The current sense amplifier architecture includes an “auto-zero” function. This takes place during 6EDL7151 start-up and operation to maintain accuracy of measurements during the lifetime of the device. If no GHx rising edge happens for a given time (tAUTO_ZERO_CYCLE), i.e., if the low-side is fully turned on for a long period in a six-step commutation, then an internal watchdog timer triggers an auto-zero compensation. Auto-zero is continuous during the standby state and can be disabled via the GUI. In addition, the 6EDL7151 includes a current sense amplifier user calibration mode that can be used to measure and compensate for offset at a time when the shunt current is known to be zero, i.e., when all of the gate drives are low.

6EDL7151 smart gate driver

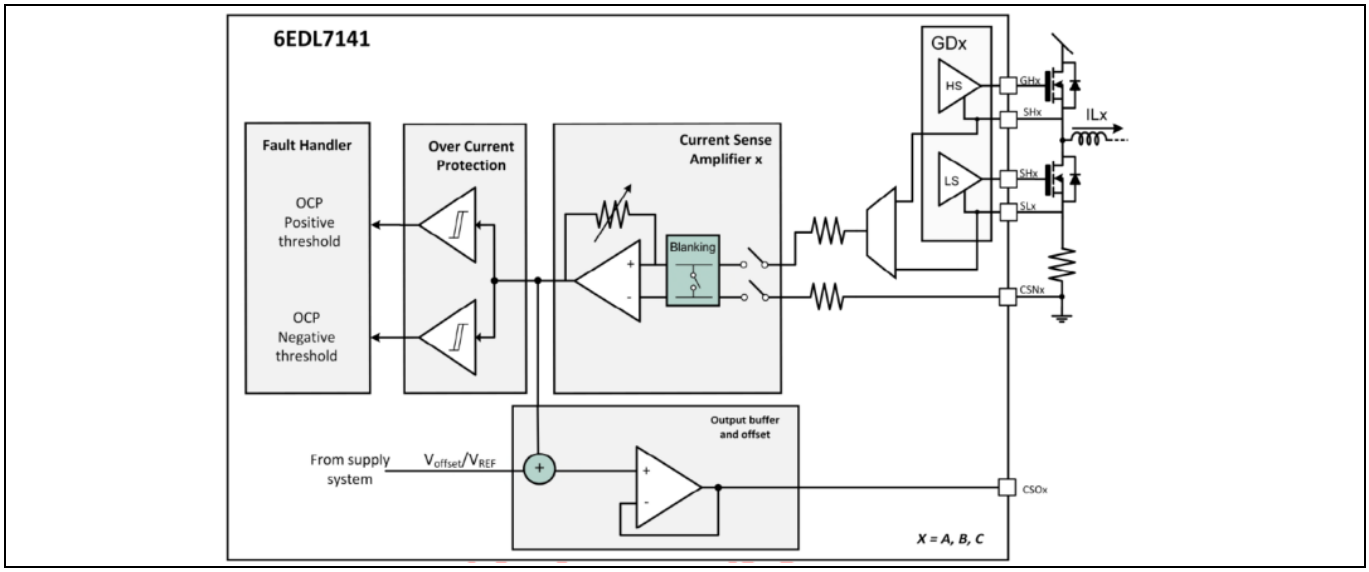

Figure 35 Current sense amplifier simplified block diagram

The current sense amplifiers in 6EDL7151 can be configured for $R_{DS(on)}$ sensing to avoid the use of shunt resistors as shown in Figure 36. However, this function is not used in the EVAL_6EDL7151_36V_1kW board, which uses a single 1 mΩ shunt resistors RS1, RS2, and RS3. In this implementation one current sense amplifier is required for each phase.

The current sense amplifiers have a default voltage gain of 12. This can be changed via the GUI to any of the following values: 8, 12, 14, 20, 24, 32 or 64. Alternatively, the gain can be selected by connecting an external resistor from pin CS_GAIN to the ground. In order to enable analog programming of the current sense amplifier via an external resistor, the designer must ensure that the bit field CS_GAIN_ANA is set accordingly. The value of RGAIN is read during the start-up sequence of the 6EDL7151. Table 9 in the datasheet [1] provides the resistor values and register settings for gain selection in both analog and digital modes.

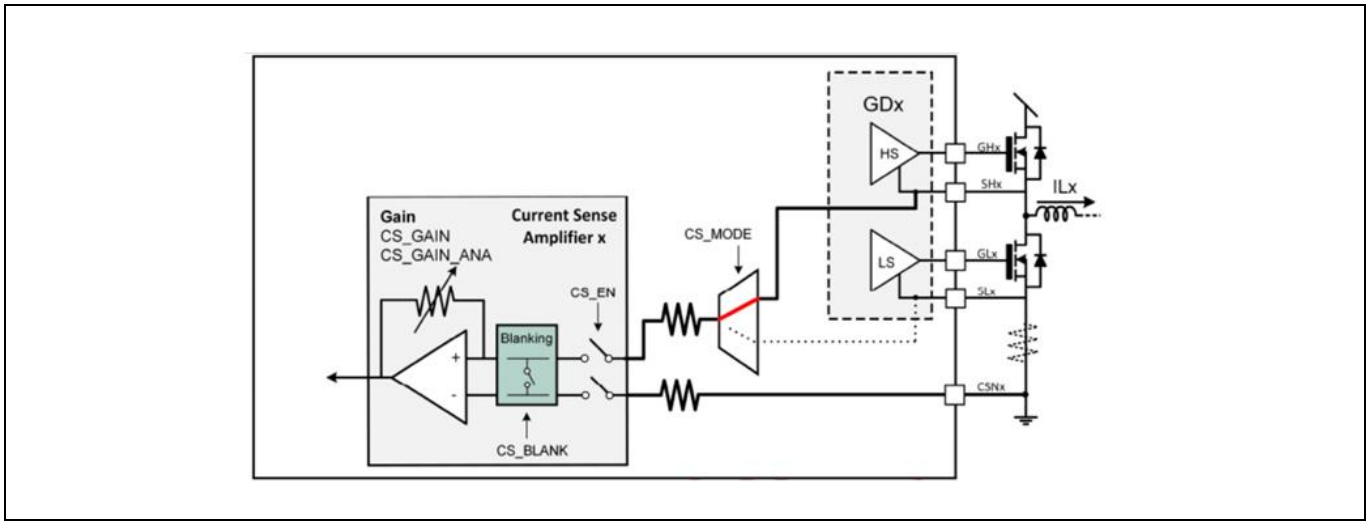

Figure 36 System diagram of a low-side $R_{DS(on)}$ current sensing configuration (not used here)

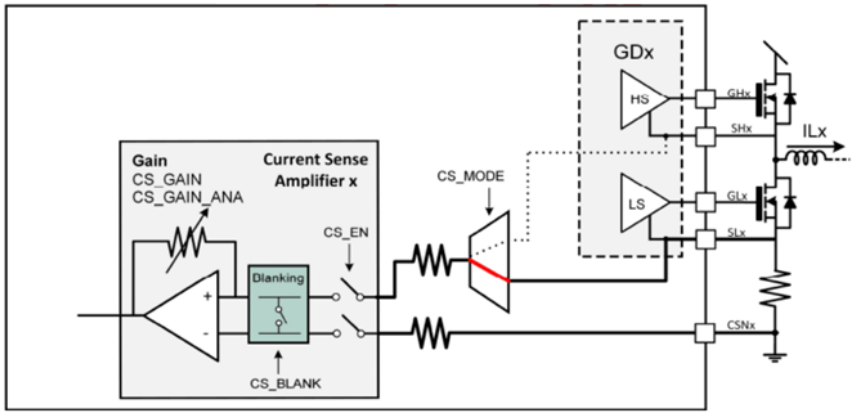

Figure 37 System diagram of an external shunt current sensing configuration

In many motor drive inverters such as this evaluation board, the current is sensed via shunt resistors. In this case, the voltage across the shunt needs to be amplified only when the low-side MOSFET is switched on. In other cases, it might be useful to monitor the signal continuously. The 6EDL7151 supports four different modes of operation of the current sense amplifiers regarding when the output is connected to the amplifier, which can be selected through the GUI. GL ON mode is the default mode in the evaluation board.

The four modes are:

- Always OFF: Current sense amplifier output disabled. This is achieved by disabling the amplifier in register CSAMP_CFG via bit field CS_EN.
- GL ON (default mode): In this mode, the CSOx pin is connected to the amplifier only when the corresponding GLx signal is active. In single-shunt mode, the CSOx is connected according to the ORing of all two or three GLx signals. If two or three amplifiers are enabled, then the signals for enabling CSOx come from the corresponding GLx signal. This mode is mandatory if $R_{DS(on)}$ sensing is selected to avoid overvoltage damage to the internal circuitry.
- GH OFF: Similar to GL ON, this mode exposes the output to GL ON period but extends the sensing period to the dead-times, both rising and falling.
- Always ON: This mode connects the activated amplifier CSOx signals continuously to the amplifier independently of PWM signals.

The programmable leading-edge blanking function can be configured in the current sense amplifiers. Since both phase node voltage SHx and SLx pins (CSNy) are subject to ringing due to the switching activity, the blanking module disconnects the inputs for a configurable time (CS_BLANK). The default blanking time is zero, and values between 50 ns and 8 µs can be selected via the GUI. The 6EDL7151 internal linear voltage regulator (DVDD) can be used for offset generation for current sense amplifiers. The default value is 1/2DVDD; values of: 5/12, 1/3 and 1/4DVDD are also available.

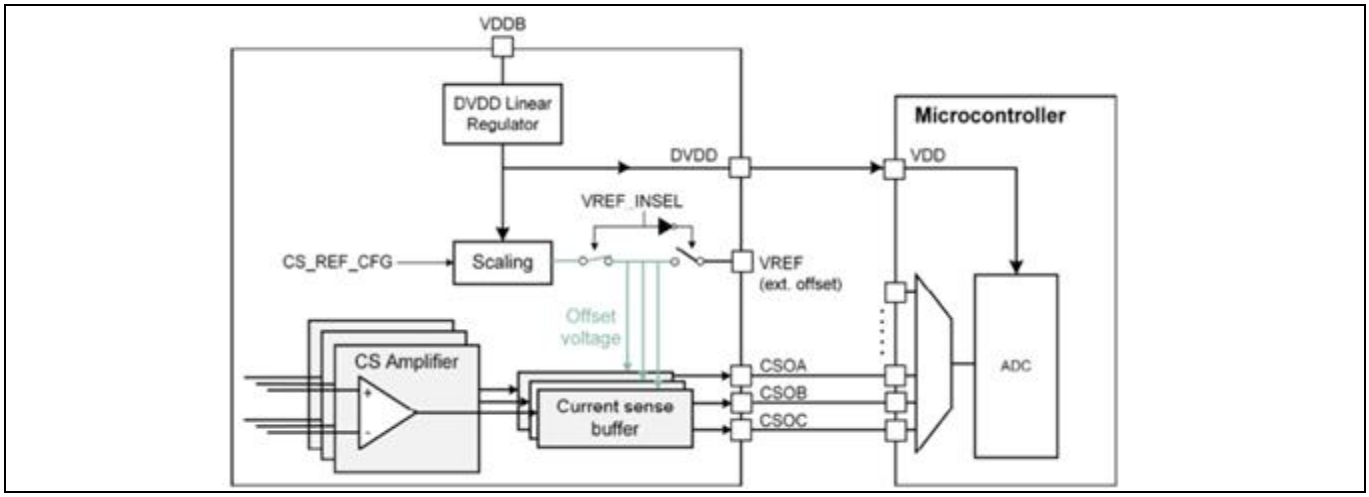

Figure 38 Current sense amplifier offset generation block diagram

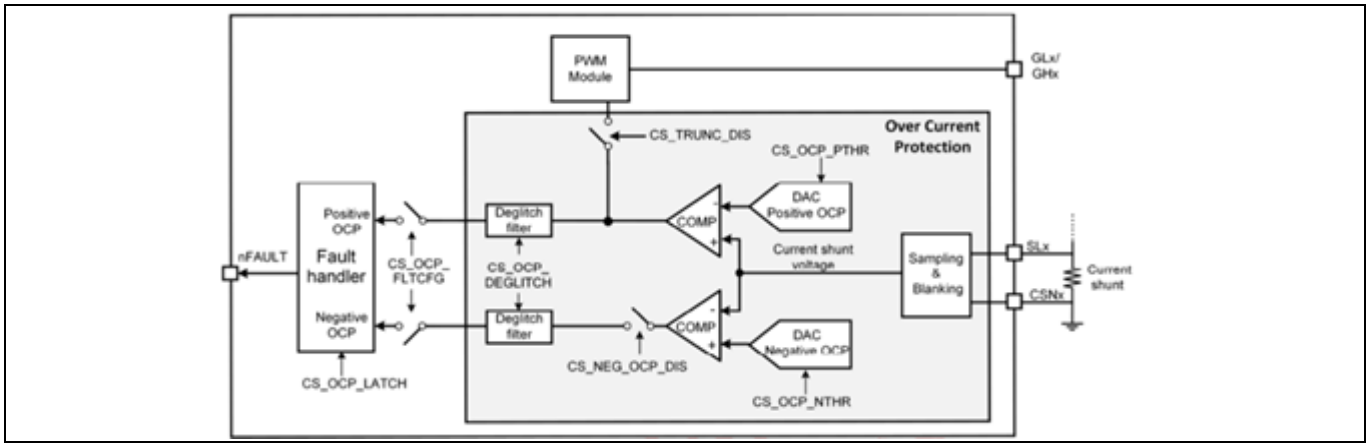

Figure 39 Current sense amplifier architecture

The 6EDL7151's response to an OCP event can be programmed via the GUI, allowing for customization to suit different application needs.

- Apply PWM truncation immediately after OCP event and report on nFAULT pin after OCP event – deglitching is disabled if truncation is enabled. If a positive OCP event occurs, the high-side PWM is truncated. The result is that the high-side MOSFETs are all switched off and the current flowing in the motor windings therefore recirculates through the low-side MOSFET body diodes.
- Disable reporting but keep truncation of PWM.
- Trigger a configurable brake action upon OCP event. If truncation is not desired, a brake event can be configured using one of the available braking modes.
- Disable OCP protection, both nFAULT reporting and truncation of PWM. In this case, OCP is ignored.

It is also possible to select whether the OCP fault is latched or not via the GUI. In a latch configuration, the nFAULT pin is held low until the fault is cleared via an SPI command or after a power cycle. If the OCP fault is configured as non-latched, the nFAULT pin remains low while the fault is being detected but will pull up again when the OCP condition is no longer present. Configuration allows the user to set a target number of consecutive events (PWM cycles) required to activate the nFAULT fault signaling.

In the evaluation board default configuration PWM truncation, OCP fault latching and Brake on OCP is disabled.

4.5 VDS sensor system

The VDS sensors provide the possibility to monitor the status of the external MOSFETs and detect potential fault conditions. One VDS sensor is provided for each MOSFET in the 3-phase inverter, three for low-side MOSFETs and three for high-side MOSFETs. Each VDS sensor monitors the drain and source voltage of a single MOSFET, using the drain and source terminals as inputs.

Programmable thresholds, independent for high-side and low-side MOSFETs, allow to adapt the detection level to the operating conditions. A blanking circuit is present to disable the VDS sensors during a programmable time, where the MOSFETs are expected to switch from battery voltage to ground or vice versa. Finally, to avoid wrong triggering due to noise, a deglitching filter is also configurable via the SPI register. Figure 40 shows the block diagram of the VDS sensor module in 6EDL7151.

Once the VDS sensor is activated, the drain to source voltage is monitored and compared against the programmable DAC value VDSVTH_LS for low side and VDSVTH_HS for high side. When the comparator output is high for longer than VDS_FILTER time (SPI configurable), the VDS fault will be triggered, stopping the inverter operation and reporting on the nFAULT pin. The filter function deglitches the OCP functions and avoids noise, glitches, or too short overcurrent events are detected as faults. The filter functionality is shown in Figure 41. The filtering time is the minimum time for which the fault condition should persist in order to detect the fault. A microcontroller can check for detected faults by polling the status register and by monitoring the nFAULT pin. Status bits are available for each of the six VDS sensors. These faults are latched, and operation can be resumed only if the MCU clears the fault or if there is a power cycle. The report behavior of the faults is configured via the bitfield VDS_FAULT_CFG. Additionally, if one comparator detects a fault condition, the device will switch off all gate driver outputs into a safe state. All the voltage thresholds and timings can be configured under the VDS sensor section from the GUI as shown in Figure 42.

Note: The VDS sensor is enabled by default.

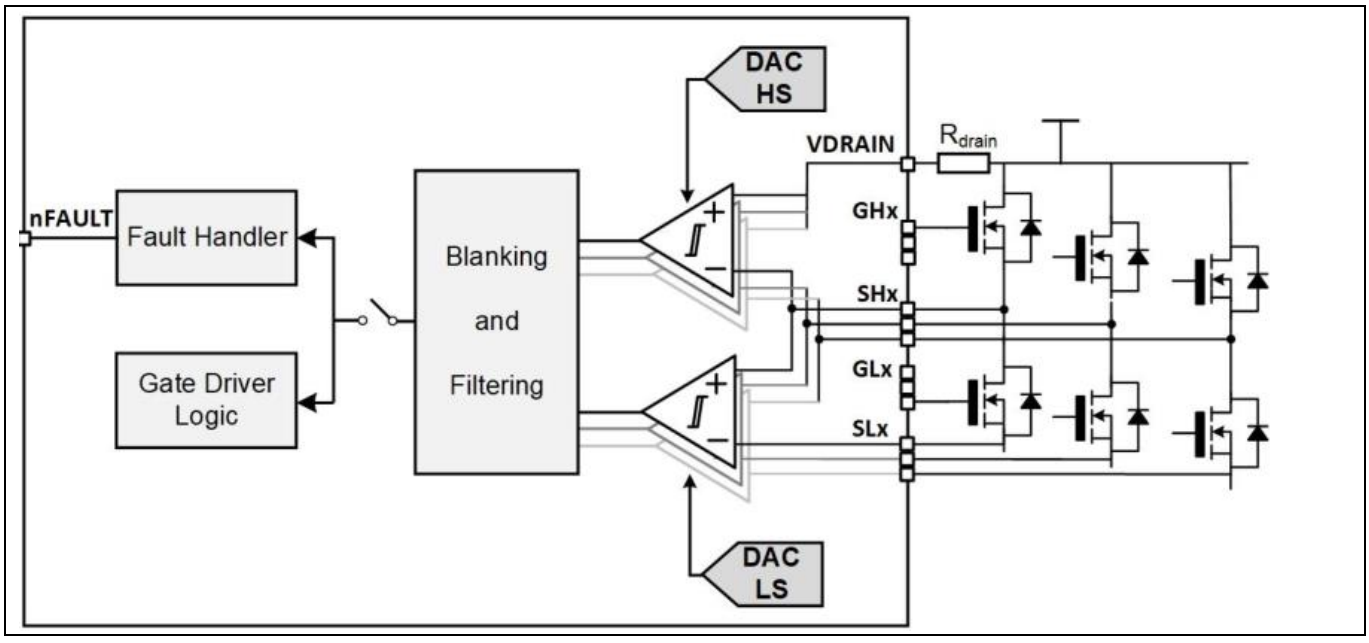

Figure 40 VDS sensor system

6EDL7151 smart gate driver

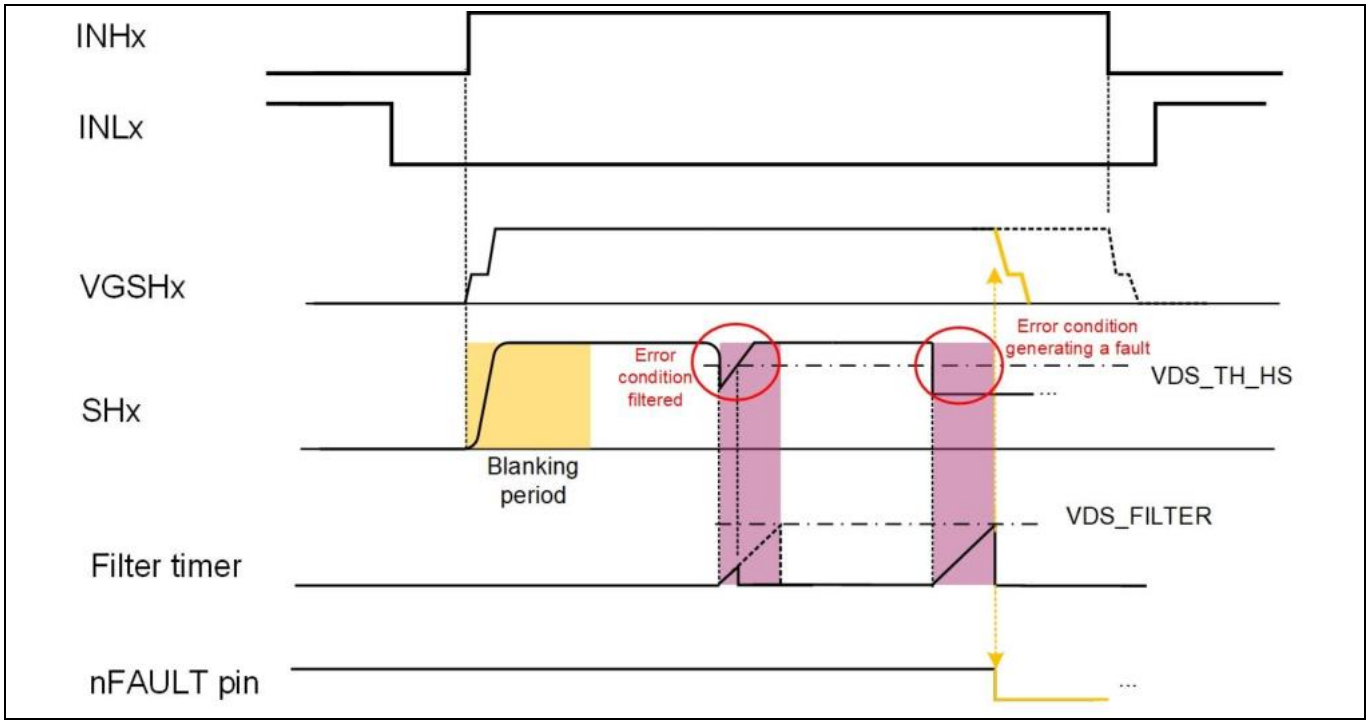

Figure 41 VDS sensor blanking behavior and operation waveforms

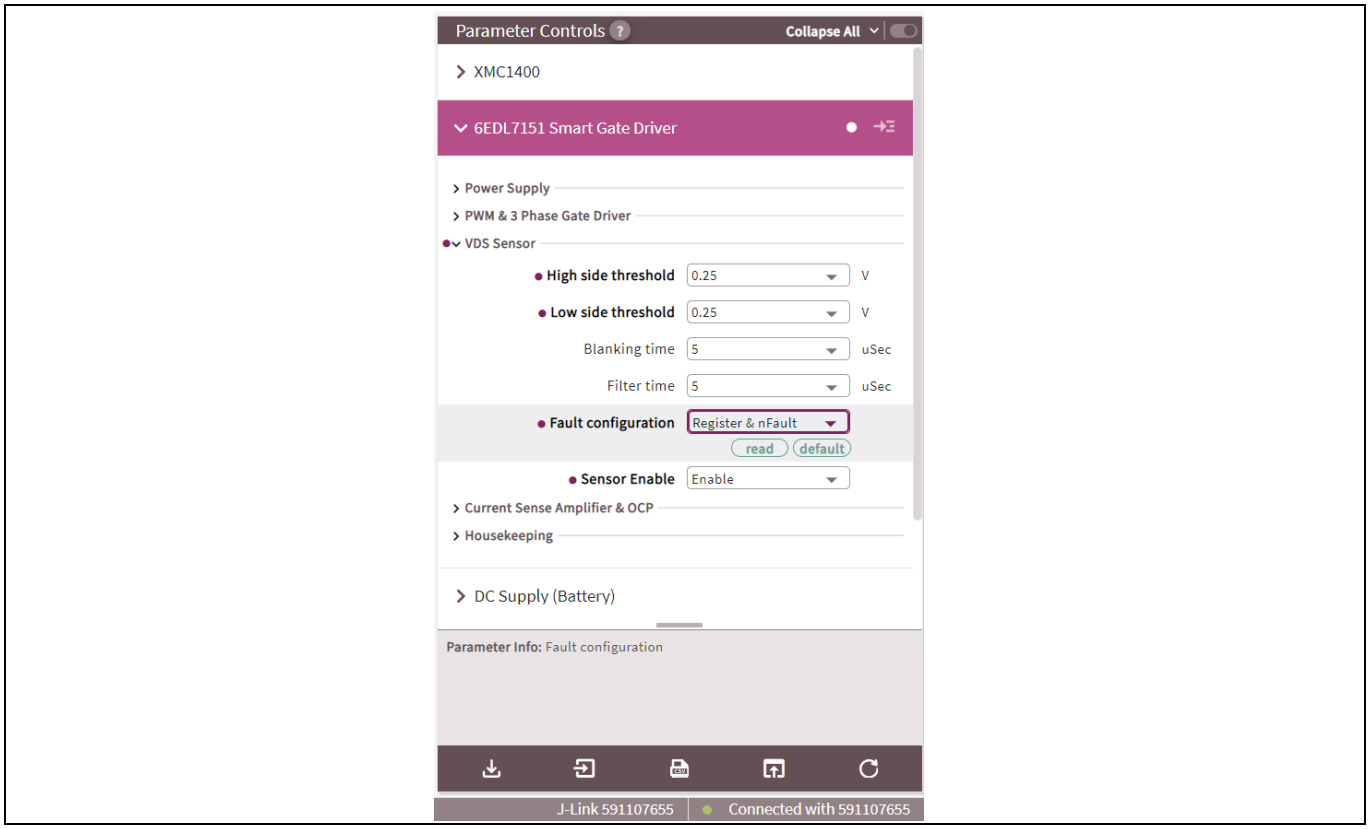

Figure 42 VDS sensor configuration from GUI

4.5.1 Off-state diagnostics

Off-State Diagnostics is a firmware feature that uses VDS sensor of 6EDL7151 and additional hardware to determine the failure(s) or short(s) of the external MOSFETs before the normal operations. This feature will protect the battery from deep discharge.

The evaluation board has the required additional hardware to enable this feature as shown in Figure 43. The circuit consists of resistor dividers to bias the MOSFET VDS and a switch Q19 to enable this part of the circuit during Off-state diagnostics.

To run the off-state diagnostics, the Q19A (n-MOSFET) needs to be turned on from the XMC1400 microcontroller, which turns on the Q19B (p-MOSFET) and PVDD will be available for the resistive voltage divider. If any of the MOSFETs are shorted from drain to source, then the voltage read across that MOSFET by the VDS sensor would be 0 V. Now, the firmware/GUI reads the status of FUNCT_ST register and EN_DRV signal is held low, implies the MOSFETs will not turn on causing a dead short circuit condition, which would result in deep discharge of the battery.

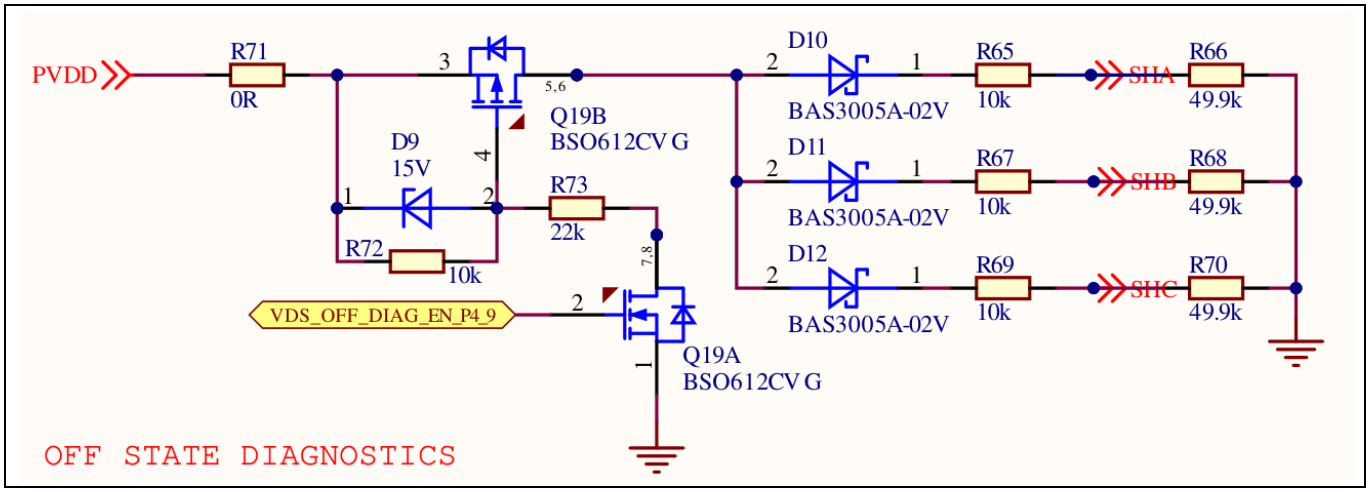

Figure 43 Off-state diagnostic circuit

To evaluate the feature in the ModusToolbox™ Motor Suite GUI, a radio button is provided at the bottom-left corner of the Testbench. If no faults are found the message is displayed on the bottom-right corner as a pop-up message as shown in Figure 44. If the diagnostic tool detects a fault, a fault message appears in as shown in Figure 45.

When a motor is connected, a short-circuit in one of the MOSFETs will make the VDS sensors of other two MOSFETs on the same side to report fault. This is because the motor winding impedance makes all the three MOSFETs of the same side to appear in parallel when there is no back EMF. If one of the MOSFETs is shorted, it needs to be removed from the PCB.

6EDL7151 smart gate driver

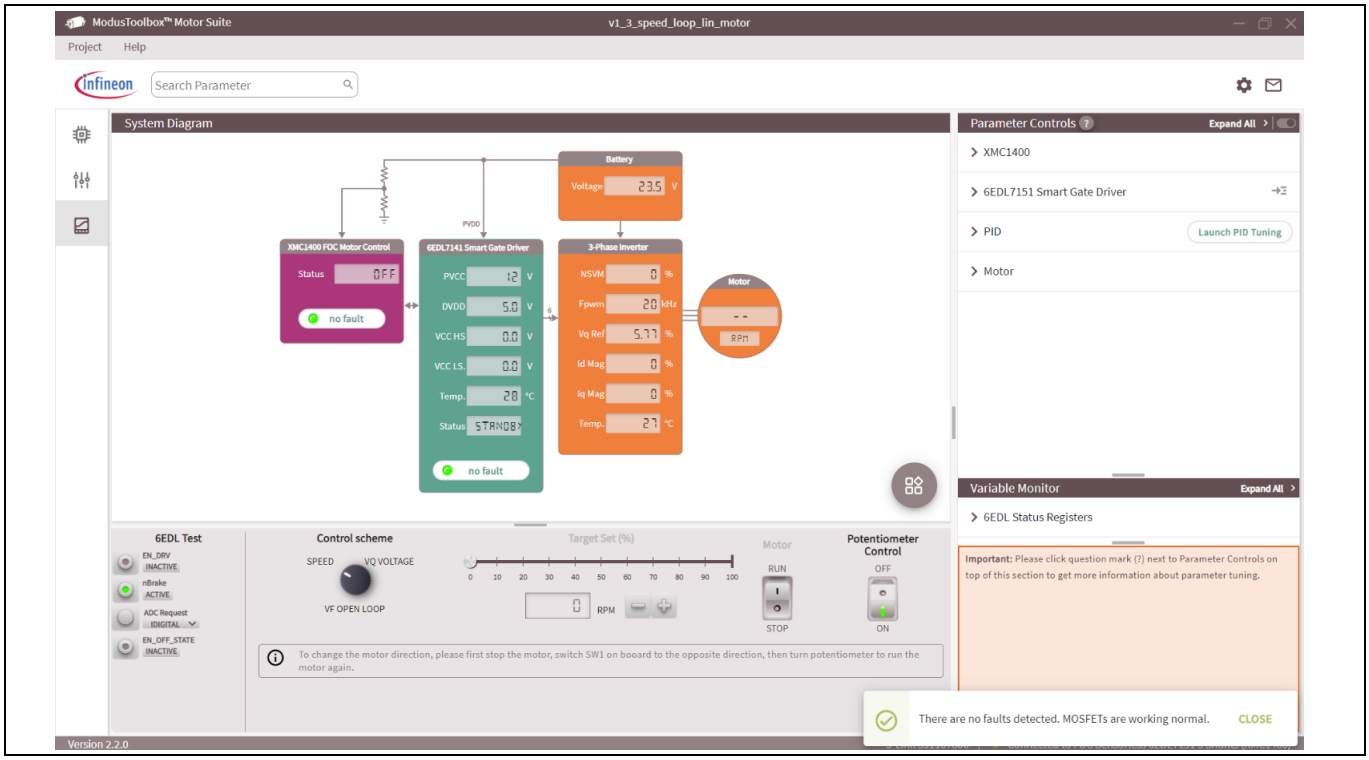

Figure 44 GUI: Off-state diagnostics without fault

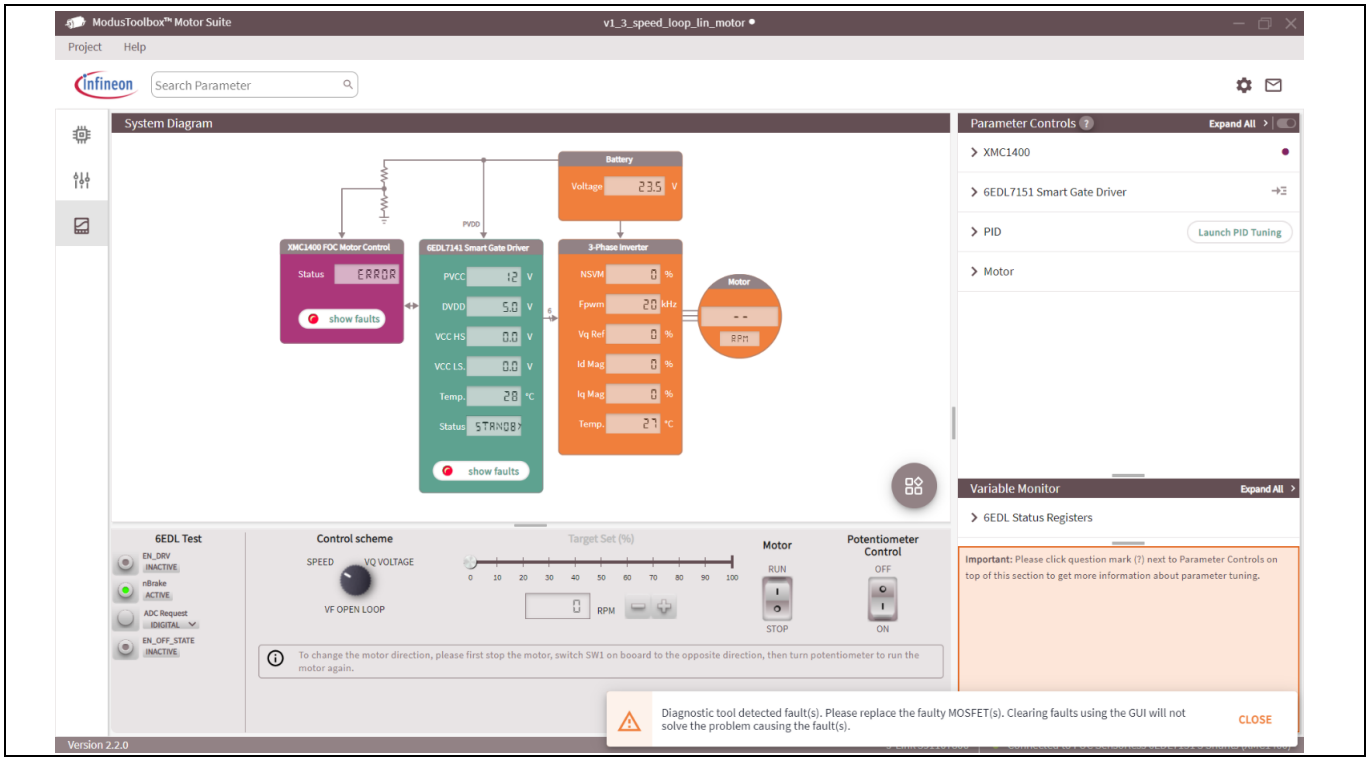

Figure 45 GUI: Off-state diagnostics with fault

4.6 XMC1404-VQFN64-200kB microcontroller

The evaluation board has a XMC1404-Q064X0200 microcontroller to control the motor drive system. This is a 32-bit Arm® Cortex®-M0 microcontroller optimized for motor control. This microcontroller interacts with the system through the following inputs and outputs:

Table 2 Microcontroller inputs and outputs

Port	Configuration	Description
P0.7	Digital input	Enable
P2.7	Digital input	Braking switch
P4.1	Digital input	Hall sensor input – phase A
P4.2	Digital input	Hall sensor input – phase B
P4.3	Digital input	Hall sensor input – phase C
P4.10	Digital input	Motor direction
P2.3	Analog input	Battery voltage sense
P2.9	Analog input	Shunt current sense through amplifier (Phase W)
P2.10	Analog input	Shunt current sense through amplifier (Phase V)
P2.11	Analog input	Shunt current sense through amplifier (Phase U)
P2.5	Analog input	Potentiometer voltage sense
P2.2	Analog input	Back EMF sense – phase U
P2.1	Analog input	Back EMF sense – phase V
P2.0	Analog input	Back EMF sense – phase W
P2.4	Analog input	Temperature sensing
P3.2	PWM output	Low-side gate pulse – phase U (INLA)
P3.3	PWM output	High-side gate pulse – phase U (INHA)
P3.0	PWM output	Low-side gate pulse – phase V (INLB)
P3.1	PWM output	High-side gate pulse – phase V (INHB)
P1.1	PWM output	Low-side gate pulse – phase W (INLC)
P1.0	PWM output	High-side gate pulse – phase W (INHC)
P1.3	Digital output	Brake command
P1.2	Digital output	Auto zero command
P0.12	Digital output	Fault indicator
P3.4	Digital output	Fault indicator (nFAULT) (LED1)
P4.7	Digital output	LED indicator (LED5)
P4.8	Digital output	LED indicator (LED4)
P4.4	Debug	PC_RX
P4.5	Debug	PC_TX
P0.14	Debug	SWDIO/TMS
P0.15	Debug	SWDCLK/TCK
P4.9	Digital output	VDS Off-state diagnostics enable

4.7 Board connections and controls

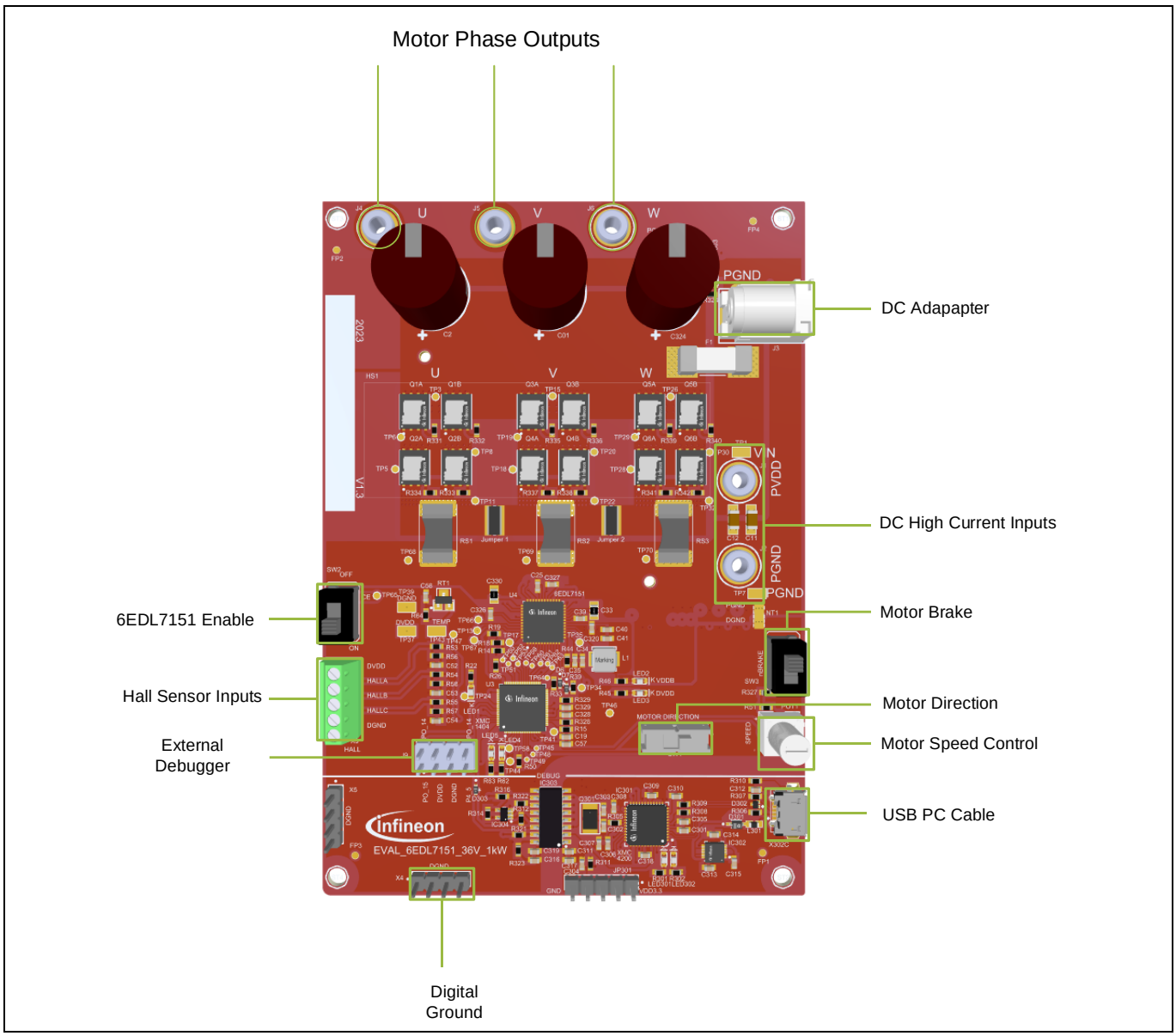

Figure 46 EVAL_6EDL7151_36V_1kW external connections and controls

4.8 On-board programmer/debugger

The EVAL_6EDL7151_36V_1kW board includes an on-board debugger, which is located near the white line shown on the top-side component legend (see Figure 46). This is connected to a PC through a USB cable to enable control, programming and debugging via a dedicated GUI or firmware development tool such as ModusToolbox™.

4.9 External programmer/debugger

If for any reason the user wishes to use an external debugger such as the XMC™ Link, this can be connected via the 4 x 2-way header indicated on the top-side of the PCB.

5 Inverter, Control, and firmware

The main hardware blocks consist of three-phase inverter power stage, the 6EDL7151 three-phase smart gate driver and the XMC1400 series 32-bit microcontroller with Arm® Cortex®-M0.

5.1 Three-phase inverter stage:

The three-phase inverter switching devices are BSC014N06NSSC (DSC OptiMOS™ 60 V 1.4 mΩ 5x6 PQFN) power MOSFETs optimized for battery-powered power tool applications. The demo board operates at a switching frequency of 20 kHz in 6PWM mode. That is, all the 6 PWM signals are generated from the Space Vector Modulation algorithm implemented inside the XMC1400 microcontroller firmware. The duty cycle will vary as per the reference set in the control loop to generate a sinusoidal current in the stator winding. The winding inductances remove most of the PWM frequency component, leaving a small amount of ripple.

The 6EDL7151_36V_1kW evaluation board allows heatsinks to be attached directly on the MOSFETs on the board to extract heat from the MOSFETs, allowing higher power drive to the motor without overheating.

The sensorless FOC needs current information on each inverter leg and this is achieved by measuring the shunt voltages (RS1, RS2, RS3) on all the three inverter legs.

5.2 Field Oriented Control:

PMSM and BLDC are a special type of AC synchronous machines, which has permanent magnets to produce the field instead of separate field windings as in case of DC machines or conventional synchronous machines. The simplest way to control PMSM/BLDC is by implementing a block commutation algorithm. Although the performance is acceptable for power tools, block commutation is known to create a torque ripple with six times the frequency of the electrical rotary frequency of the 3-phase motor. This leads to vibrations and acoustic noise due to the discrete switching between the phases such that the stator and rotor fields are not always perpendicular to each other. This generates high torque ripples, resulting in some inevitable vibration and noise.

Field Oriented control (FOC) is a technique used to control the stator current and hence the stator flux in such a way that the stator flux is always orthogonal to rotor flux. Generally, the permanent magnets are on rotor and a 3-phase winding on the stator. By controlling stator current through switching inverter, FOC enables a precise control of motor torque. FOC decouples stator and rotor fields results in superior transient response, improved steady state performance, and higher efficiency.

FOC implementation requires information about the position of the rotor, which can be either measured or estimated from phase current information. The example project available on ModusToolbox™ Motor Suite GUI implements estimation of rotor position based on phase currents, i.e. sensorless FOC. However, the evaluation board has provision to interface encoders for sensored FOC.

FOC implementation requires a series of mathematical computations to be performed on a microcontroller. The evaluation board has an XMC1400 series microcontroller to perform the computation, which has sufficient processing power to execute this control algorithm.

As shown in Figure 47, the fundamental component of all the phase voltages has a sinusoidal shape, resulting in a sinusoidal current and sinusoidal back-EMF shape in the machine.

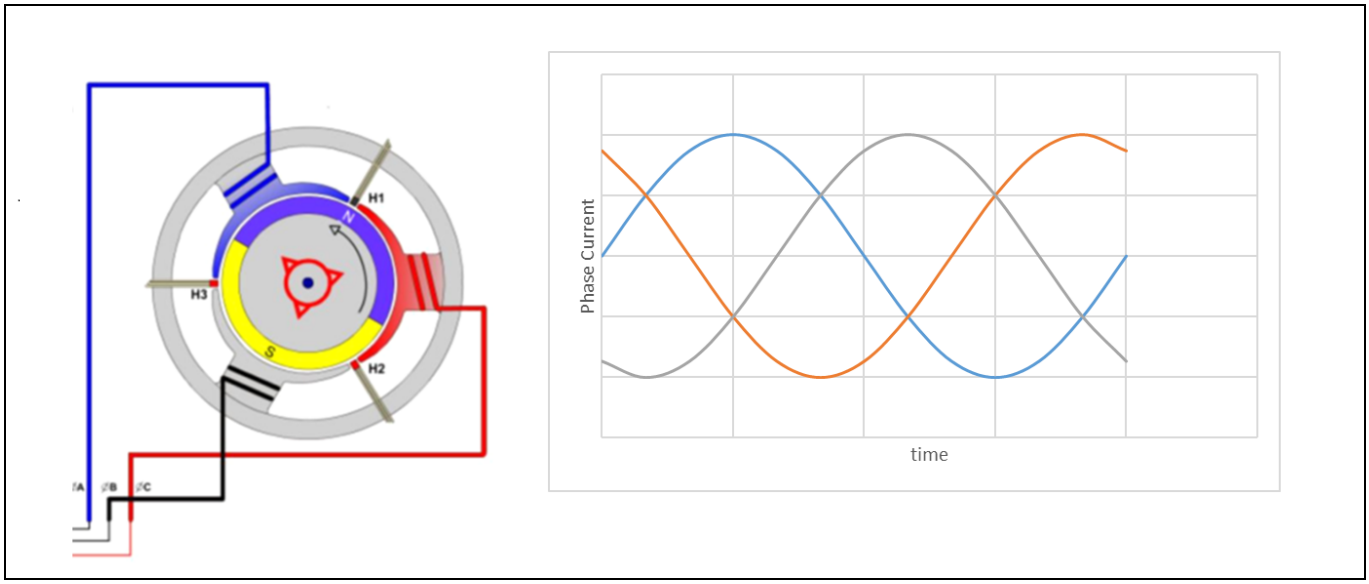

Figure 47 Sinusoidal phase currents in FOC

The 3-phase stator voltage reference is computed and at the final stage, it is converted into PWM signals using SVM, generating complementary outputs with dead time to drive the 3-phase Inverter.

The block diagram of PMSM FOC Sensor less control is shown below. In the EVAL6EDL7151_36V_1kW implementation, the 6PWM mode is used, where all the high- and low-side gate drive pulses are generated by the microcontroller. The firmware on the evaluation board supports two types of SVM implementation as summarized in the GUI. The SVM switching scheme can be selected under the XMC1400 in parameter controls pane of the GUI.

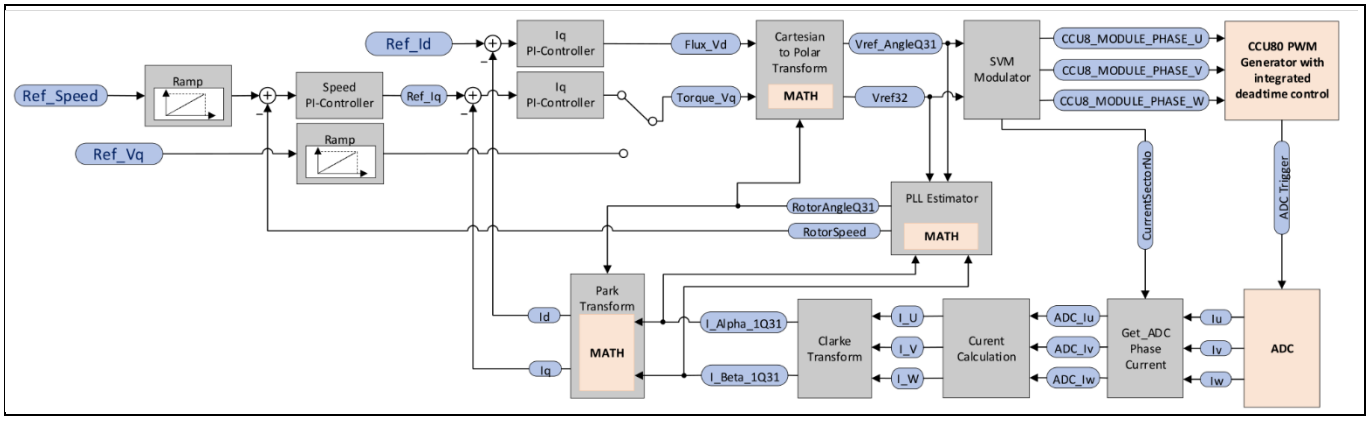

Figure 48 Block diagram of PMSM FOC Sensor less Implementation

Table 3 Supported SVM Switching schemes

Modulation scheme	Description
5 Segment SVM	Modulation is applied to the low-side switches
7 Segment SVM	Modulation is applied to the high-side switches

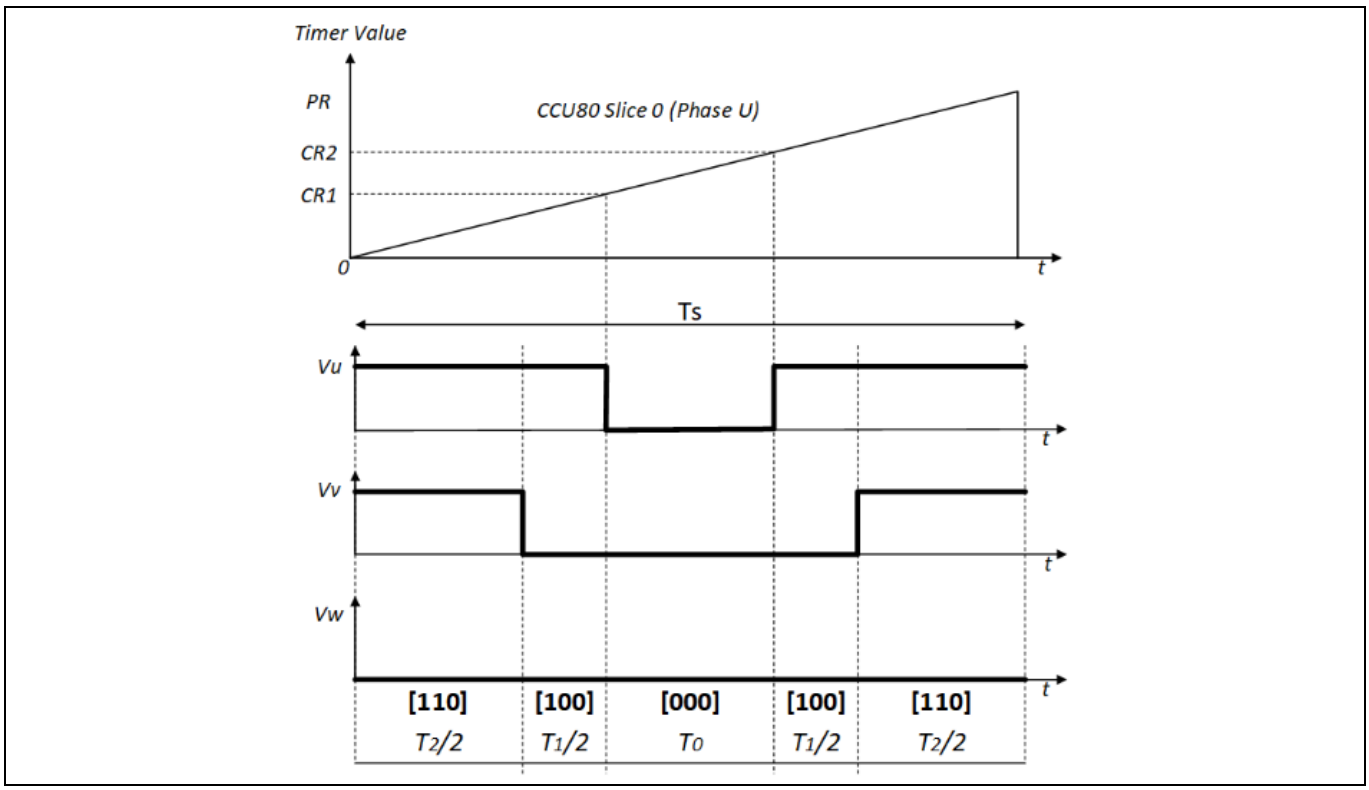

Figure 49 5 Segment SVM

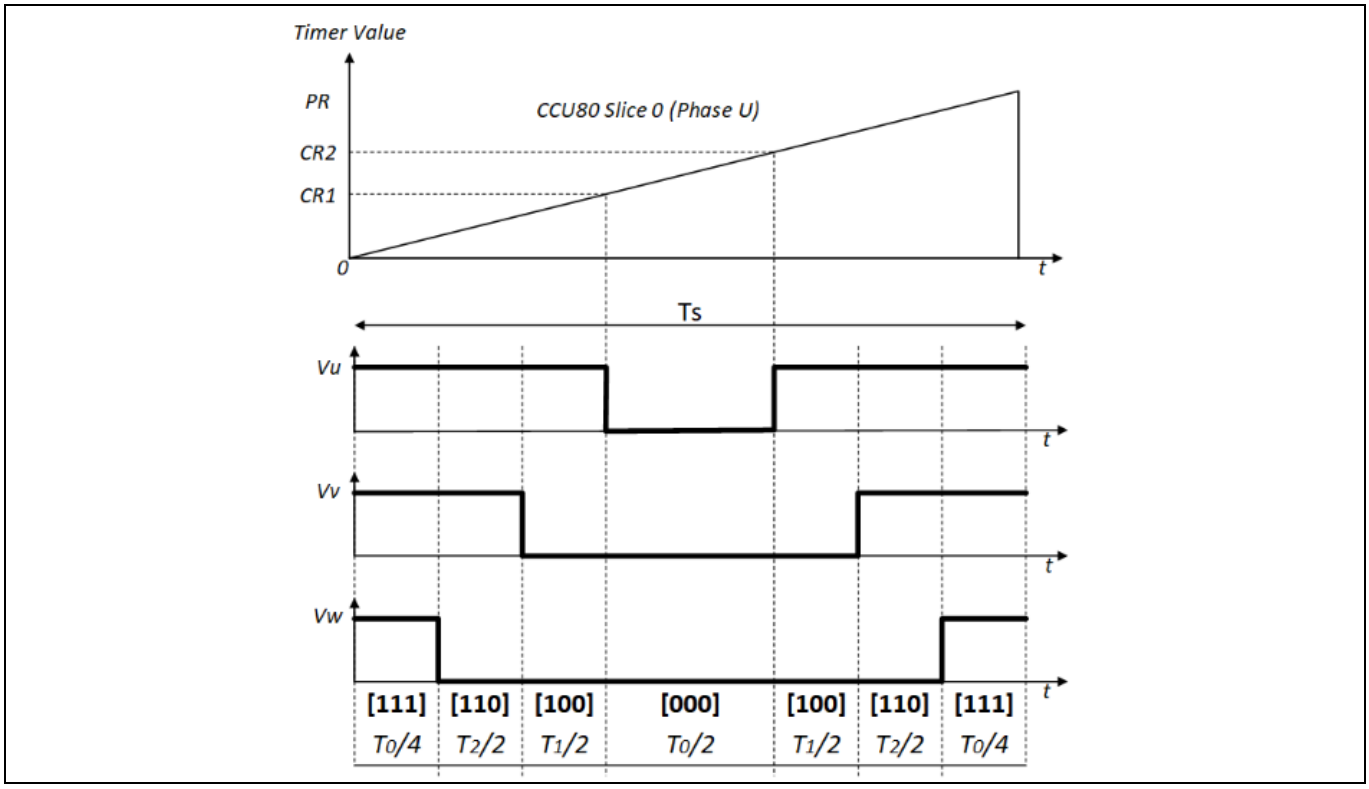

Figure 50 7 Segment SVM

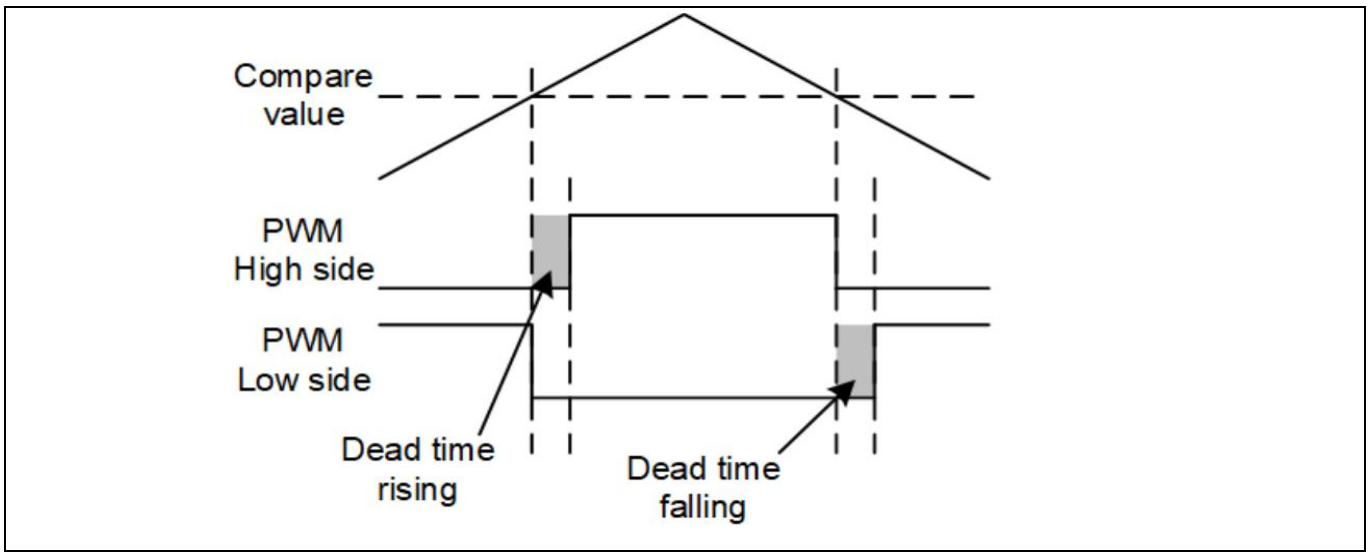

Figure 51 Dead time between High Side and Low Side gate signals

During SVM modulation with synchronous rectification the switching dead-time is inserted between the rising and falling edges of the PWM signals to prevent the high-side and low-side MOSFETs of each inverter phase from being on at the same time during switching transitions (shoot-through condition). The body diode of each MOSFET conducts current when the MOSFET is off. This dead time is configurable from the GUI.

5.3 PI compensation

As illustrated in the block diagram in Figure 52, a closed-loop control system is used to regulate the motor voltage, current, or speed. Speed control is the default control method set by the GUI and selected in the pre-installed firmware. A command value is applied to the system through the potentiometer on the board or from the GUI in test bench mode via the slider control. The firmware implements a proportional-integral (P-I) control loop as shown in Figure 52.

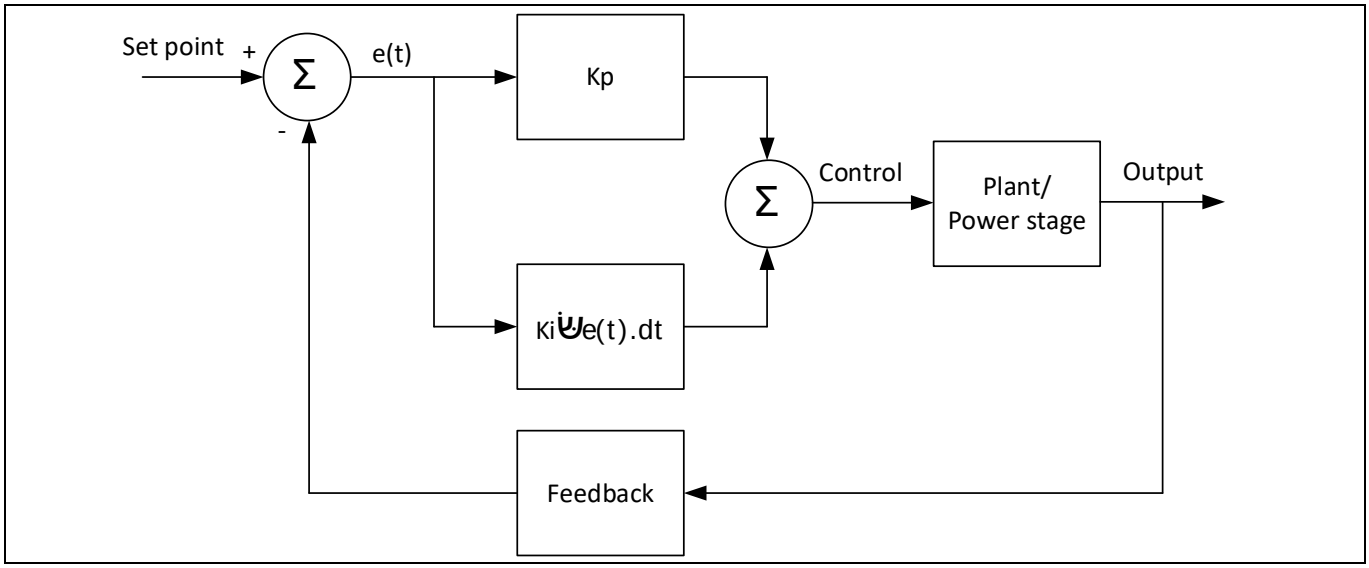

Figure 52 P-I control block diagram

Inverter, Control, and firmware

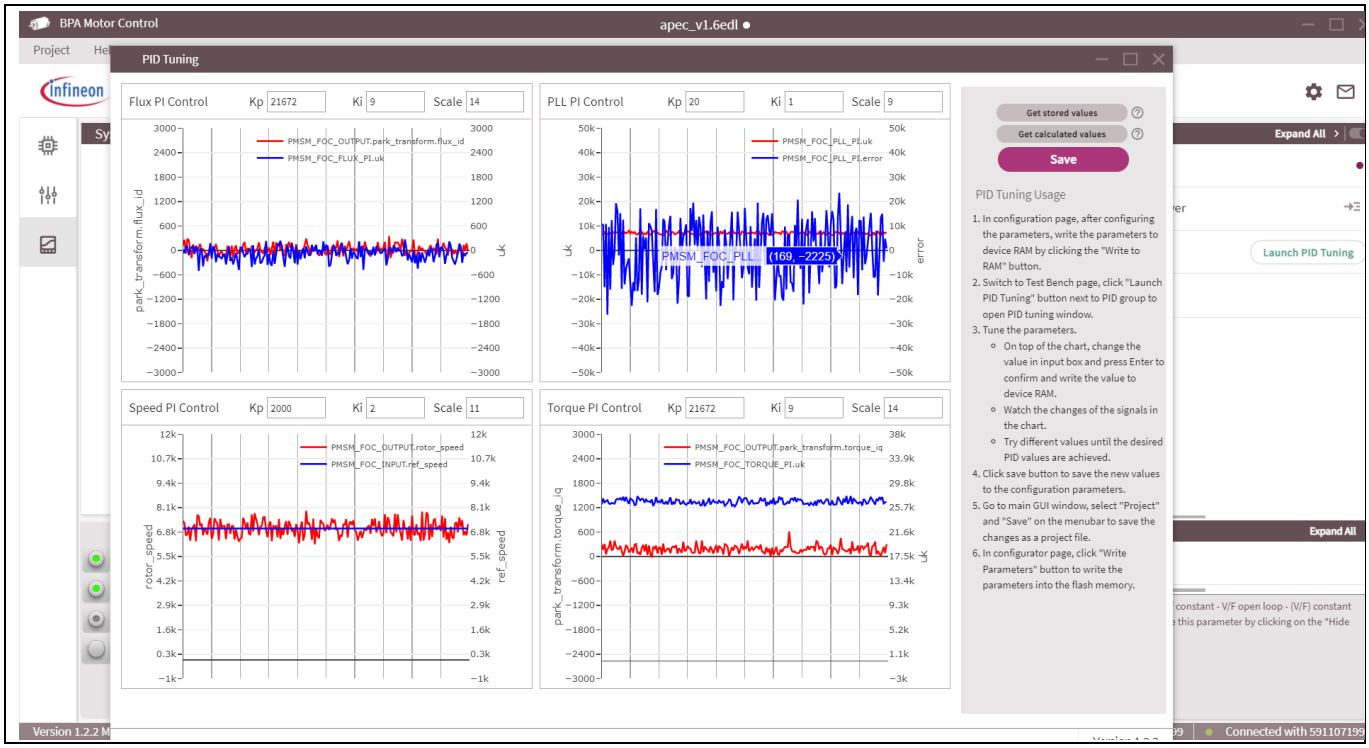

Figure 53 PID Tunning tool in GUI

The P-I controller is a widely used feedback control mechanism, which continuously calculates an error value e(t) as the difference between the setpoint and the actual measured value of the measured output quantity. In this case, the speed is estimated by the firmware from the phase current sensed signals. The error value is fed to the proportional calculator where it is multiplied by K_P and to the integral calculator where it is integrated with respect to time and the result multiplied by K_I. These two results are then summed together to provide a control value, which is applied to the power stage to provide a correction that will adjust the output to match the setpoint. The goal is to optimize the values of K_P and K_I for the specific system (inverter and motor) to achieve minimal delay and overshoot when changes are made to the commanded speed. The $K_{proportional\ gain} = Kp/2^{Scale}$ and $K_{integral\ gain} = Ki/2^{Scale}$ where Kp, Ki, and scale are integer values represented in the source code for proportional gain, integral gain, and scale calculation, respectively. The tuning of the gain factors, K_P and K_I, for different loops via the ModusToolbox™ Motor Suite GUI is very intuitive. The tuning of PI controllers can be performed by opening PID Tuning inside the Test Bench as shown in Figure 53.

6 Graphical user interface

The ModusToolbox™ Motor Suite downloads the control firmware and configuration settings for the 6EDL7151 on motor control boards operating with Sensorless field-oriented control with three shunts. Once the parameters for a particular project have been selected, the configuration can be saved. The opening screen of the GUI is as shown in Figure 54.

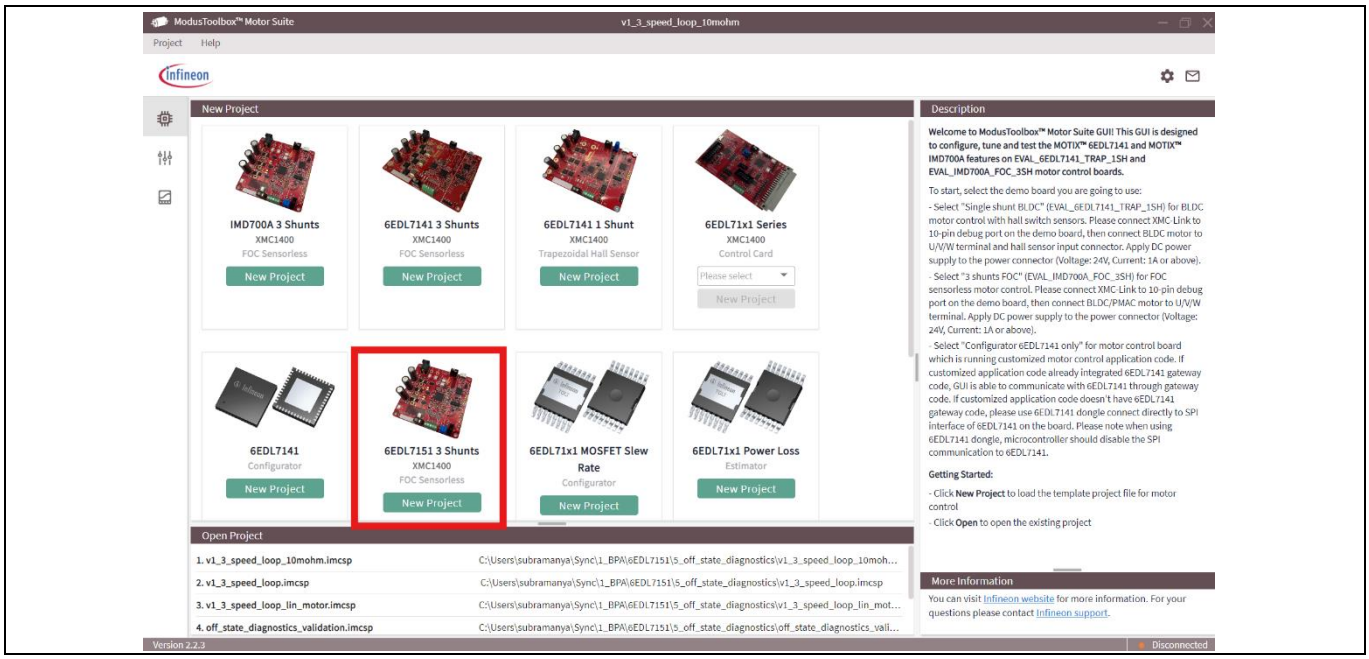

Figure 54 ModusToolbox™ Motor Suite opening screen

To start a **New Project**, first select the **6EDL7151 3 Shunts** configuration from the available options (see Figure 54). The EVAL_6EDL7151_36V_1kW evaluation board features a three-shunt design for PMSM/BLDC operation in sensorless FOC mode , which brings the GUI to the next screen (see Figure 55). You can configure all the crucial parameters needed for executing the FOC algorithm through the **Parameter Control** panel, which also includes a MOSFET tuning panel as explained in the Section 4.1.3.

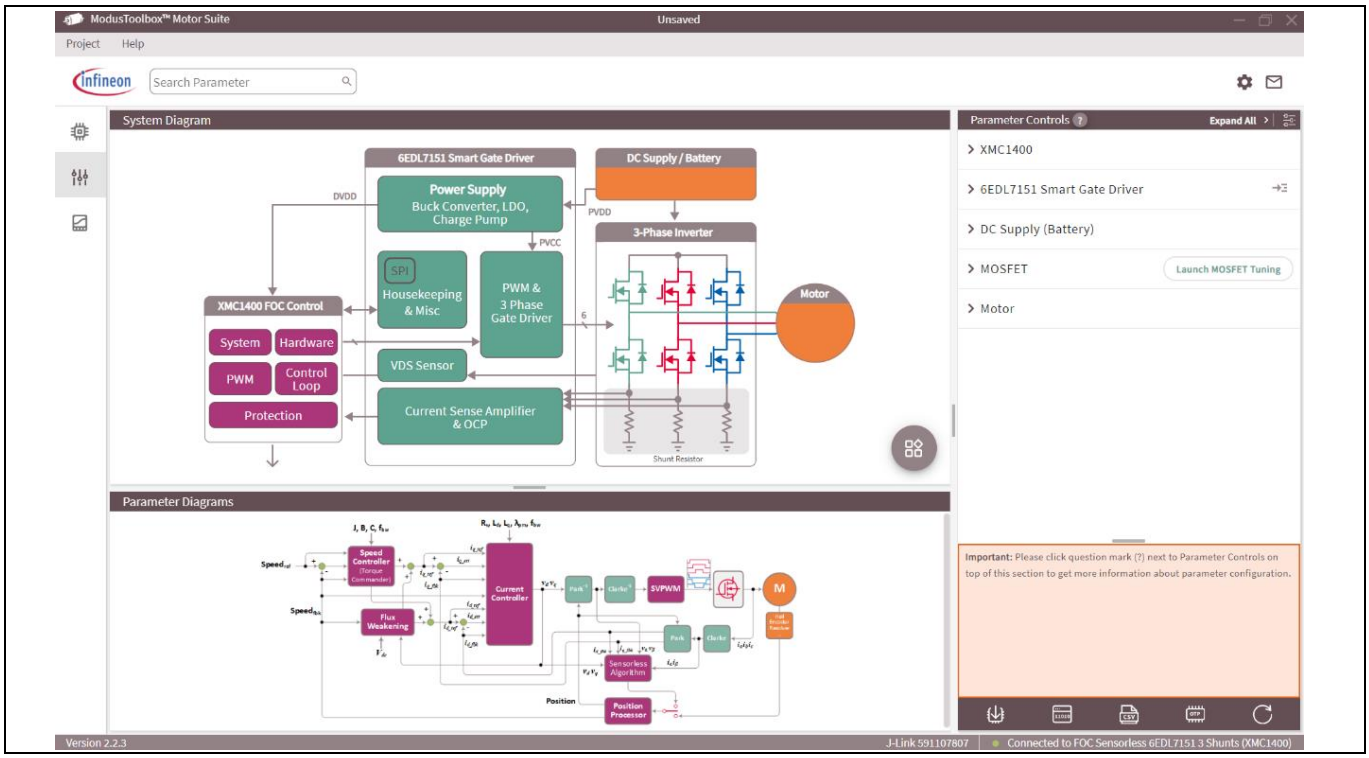

Figure 55 Sensorless FOC control with 3-Shunts firmware configuration menu

6.1 Downloading the firmware from the GUI

In order to support the transfer of 6EDL7151 parameters from the GUI, the firmware must include the functions that support configuring 6EDL7151 via SPI. The EVAL_6EDL7151_36V_1kW board is pre-installed with the correct firmware and parameters.

The GUI includes a suite of firmware options that can be downloaded to any compatible motor drive board, which uses the XMC1400 microcontroller with the 6EDL7151. Once a new project is created, the Parameter controls panel allows for configuring parameters using the drop-down list in each sub-section. These parameters are related to the evaluation board components, motor, and performance specific variables such as startup method, PWM settings, and Protection trigger levels.

Graphical user interface

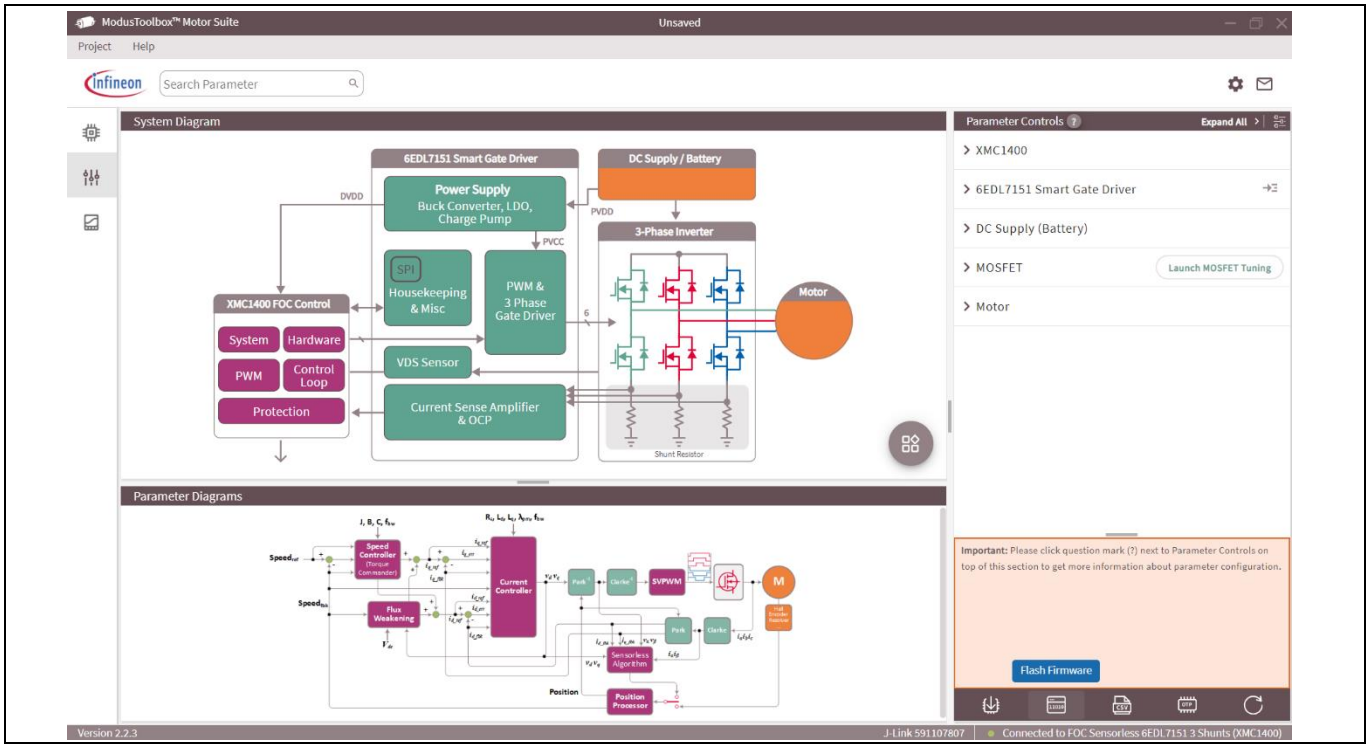

Figure 56 Firmware options and download

The various firmware parameters that were used for testing the eval board are listed in the following table. To download the firmware to the board via USB cable, select the desired parameters in the GUI and click the 'Flash Firmware' button. A confirmation message will appear once the firmware has been successfully programmed onto the microcontroller.

Table 4 List of firmware parameters

Component	Block	Parameter	Value	Unit
XMC1400	Hardware	ADC reference voltage	5	V
XMC1400	Hardware	Shunt resistor	3	mΩ
XMC1400	System	Control scheme	SPEED_INNER_CURRENT_CTRL	_
XMC1400	System	Potentiometer control	Disable	_
XMC1400	Protection	DC link over/under voltage	Enable	_
XMC1400	Protection	Over voltage threshold	50.4	V
XMC1400	Protection	Under voltage threshold	21.6	V
XMC1400	PWM	DC bus compensation	Enable	_
XMC1400	PWM	DQ decoupling	Disable	_
XMC1400	PWM	Deadtime	0.75	µs
XMC1400	PWM	PWM frequency	20000	Hz
XMC1400	Control Loop	Direct FOC startup Vq voltage	0.8	V
XMC1400	Control Loop	Motor Startup method	MOTOR_STARTUP_VF_OPEN_LOOP	_

Graphical user interface

Component	Block	Parameter	Value	Unit
XMC1400	Control Loop	Open loop V/f startup offset voltage	0.5	V
XMC1400	Control Loop	Open loop startup V/f constant	0.3	V/Hz
XMC1400	Control Loop	Pre-alignment ramp rate	100	V/sec
XMC1400	Control Loop	Pre-alignment time	100	ms
XMC1400	Control Loop	Pre-alignment voltage	0.8	V
XMC1400	Control Loop	Rotor Initial Position Detection	ROTOR_PRE_ALIGNMENT	_
XMC1400	Control Loop	SVM switching scheme	STANDARD_SVM_5_SEGMENT	_
XMC1400	Control Loop	Speed control rampdown rate	50	RPM/sec
XMC1400	Control Loop	Speed control ramp up rate	50	RPM/sec
XMC1400	Control Loop	Transition speed from V/F to close loop	400	RPM
XMC1400	Control Loop	V/f speed ramp up rate	50	RPM/sec
DC Supply (Battery)	_	Nominal DC link voltage	36	V
DC Supply (Battery)	_	Voltage divider R_high	75	kΩ
DC Supply (Battery)	_	Voltage divider R_low	7.87	kΩ
Motor	_	Maximum speed	2400	RPM
Motor	_	Minimum speed	100	RPM
Motor	_	Motor per phase inductance	112	µH
Motor	_	Motor per phase resistance	0.1	Ω
Motor	_	Pole pairs	4	_

Motor specifications are given in Chapter 8.

6.2 Configuring the 6EDL7151 parameters

The various sub-systems of the 6EDL7151 gate driver, as explained in Chapter 4, can be configured under “6EDL7151 Smart Gate Driver” in the **Parameter Controls** pane.

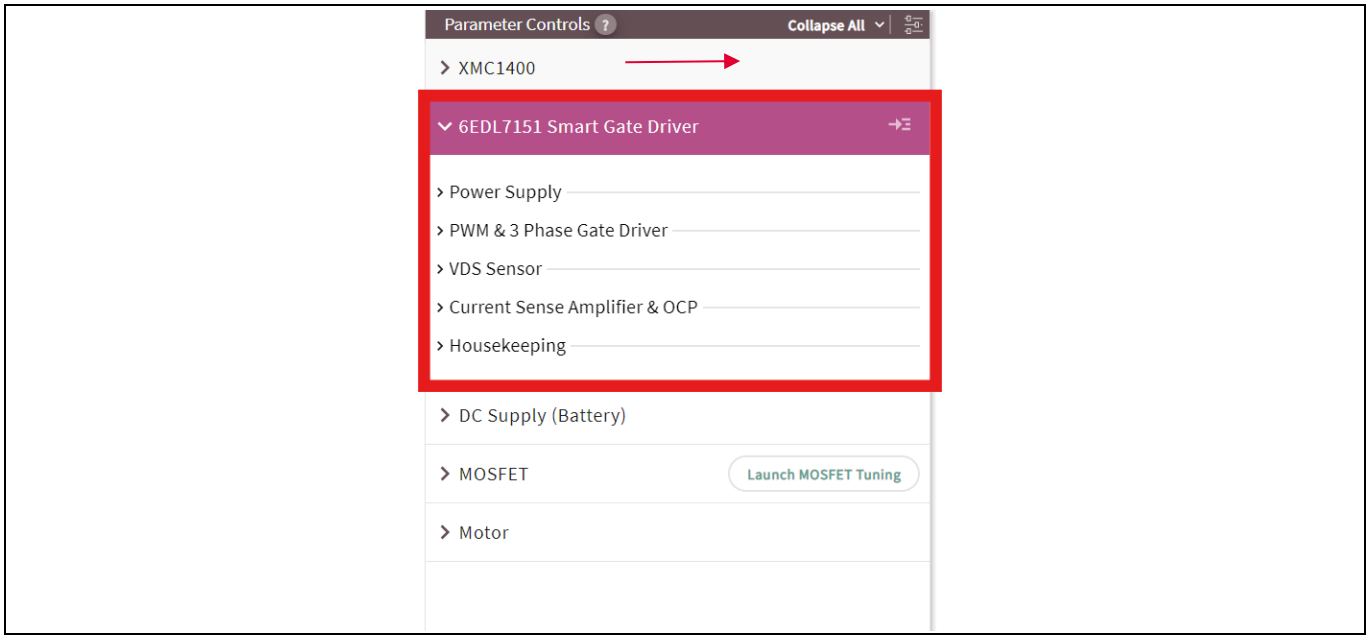

Figure 57 Selecting the gate drive parameters

The GUI enables configuration of all the 6EDL7151 selectable parameters, including the on-board power supply, charge pump settings, the current sense amplifiers, VDS Sensor, and other protection thresholds as discussed in previous sections. The **MOSFET Tuning** tab can be used to calculate the values of different source/sink current and TDRIVEs.

Once all the firmware options and 6EDL7151 parameters have been selected for a design, the project should be saved via the **Project** menu at the top of the screen. The project file has a *.6EDL extension*.

The target board containing the 6EDL7151 can be connected to the PC via an XMC™ Link debugger; however, this is not necessary for the EVAL_6EDL7151_36V_1kW evaluation board, which has its own on-board debugger and can be connected directly to a USB port on the PC. The 6EDL7151 can be programmed with the selected values using the following options shown in Figure 58.

Figure 58 Transferring the settings to the 6EDL7151

The **Write Parameters** option transfers the configuration to volatile memory, which will remain only while the 6EDL7151 is powered. This option should be used during bench testing and optimization until the designer is completely satisfied that all the correct values have been selected. If values are changed during bench evaluation, the project should be saved again. When the designer is sure that the final values have been obtained, the **Burn 6EDL7151 OTP** option may be used to permanently set the configuration in the one-time programmable (OTP) memory.

Graphical user interface

Table 5 List of 6EDL7151 parameters

Parameter Name	Value	Unit
Power Supply		
Buck Converter Frequency	500	kHz
Charge Pump Clock Frequency	781.25	kHz
Charge Pump Pre-Charge	Disable	_
Charge Pump Spread Spectrum	Enable	_
DVDD OCP Threshold	450	mA
DVDD Soft Start Time	100	µs
DVDD Turn On Delay	800	µs
PVCC Set Point	12	V
PWM and 3 Phase Gate Driver		
Alternate Recirculation	Disable	_
Brake Configuration	Low side	_
Configure pre-charge sink current	Enable	_
Configure pre-charge source current	Enable	_
Dead time falling	680	ns
Dead time rising	680	ns
Gate driver clamp feature	Enable	
High side sink current	300	mA
High side source current	300	mA
Low side sink current	300	mA
Low side source current	300	mA
PWM Freewheeling Mode	Diode FW	_
PWM Mode	6 PWM	_
Pre-charge sink current	300	mA
Pre-charge source current	300	mA
TDRIVE1	70	ns
TDRIVE2	230	ns
TDRIVE3	180	ns
TDRIVE4	350	ns
VDS Sensor		
Blanking time	5	µs
Fault configuration	Register	_
Filter time	5	µs
High side threshold	2	V
Low side threshold	2	V
Sensor Enable	Enable	_

Graphical user interface

Parameter Name	Value	Unit
Current Sense Amplifier and OCP		
Amplifier A	Enable	_
Amplifier B	Enable	_
Amplifier Blanking Time	0	ns
Amplifier C	Enable	_
Amplifier DC Calibration	Disable	_
Amplifier Mode	Shunt resistor	_
Amplifier Timing Mode	GLx high	_
Amplifier auto zero	Internal trigger	_
Amplifier gain	12x	_
Brake on OCP	Disable	_
Internal offset selection	1/2 DVDD	_
Negative OCP	Enable	_
OCP Deglitch Time	8	µs
OCP Negative Threshold	-300	mV
OCP Positive Threshold	200	mV
OCP fault latching	Disable	_
OCP fault trigger	8 events	_
PWM truncation	Disable	_
Use external offset	Disable	_
Housekeeping		
ADC Measurement filter	8	_
ADC PVDD Measurement Filter	32	_
Brake on WD timer overflow	Disable	_
Buck converter watchdog	Enable	_
Hall Sensor Deglitch Time	0	ns
Over-temperature Shutdown	Enable	_
Rotor lock detection time	1	s
Rotor lock detection	Disable	_
User ID	0	_
WD DVDD Re-start Attempts	0	_
WD DVDD restart delay	0.5	ms
WD Fault Latching	Disable	_
WD Fault Report	Status Reg Only	_
WD Input Selection	EN_DRV	_
WD Period Time	100	µs
Watchdog Timer	Disable	_

6.3 Using the GUI to control the board

The ModusToolbox™ Motor Suite is also able to operate and monitor a 6EDL7151-based motor drive inverter such as the EVAL_6EDL7151_36V_1kW through its test bench screen, which is shown in the following figure.

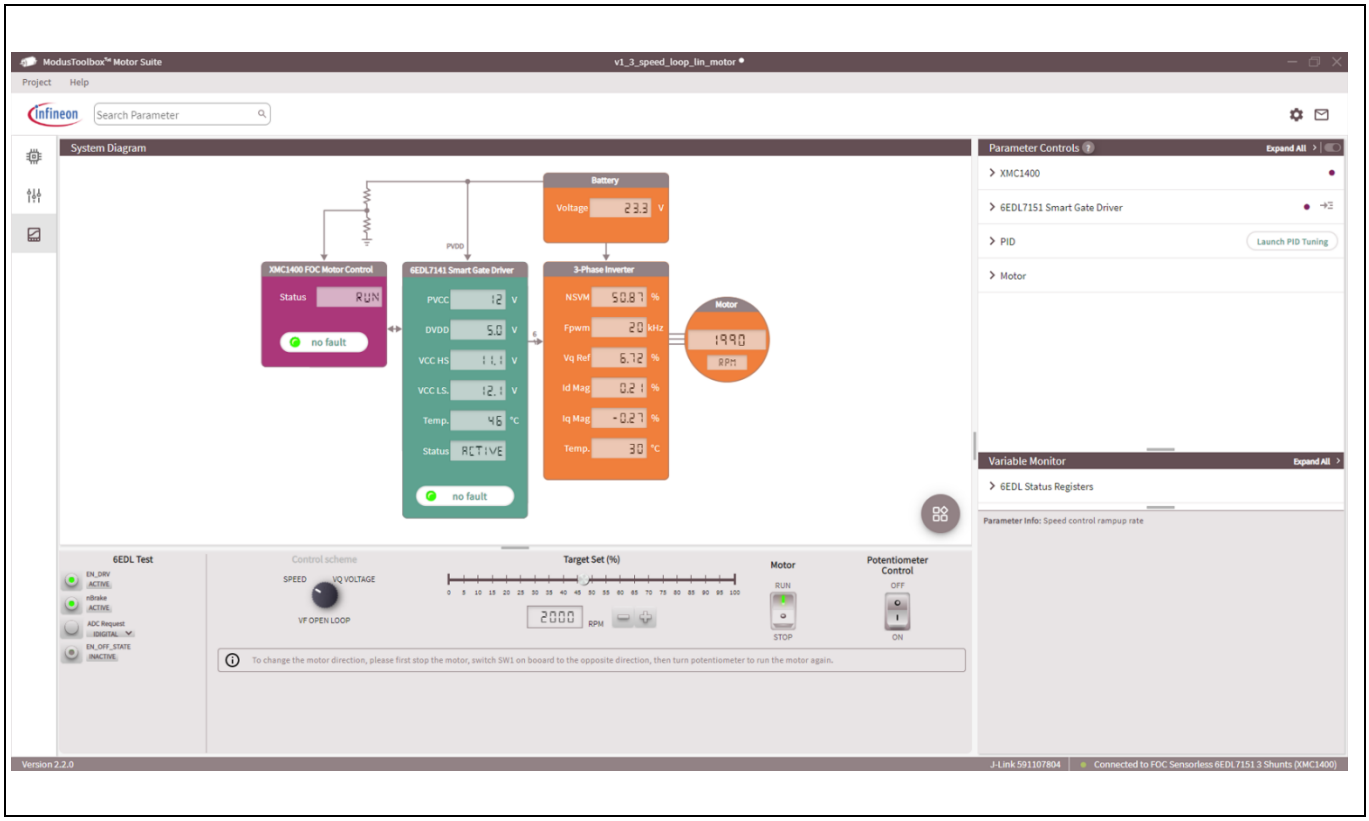

Figure 59 GUI test bench screen

The Test Bench screen provides a real-time display of the system parameters such as the power supply, internal regulator, and charge pump voltages as well as the battery input voltage. It also indicates the rotor revolutions per minute (RPM), the motor current, the PWM switching frequency and duty cycle, and the 6EDL7151's temperature from its integrated sensor. Additionally, a fault status is also indicated for monitoring and diagnosing purposes.

In addition to monitoring, the motor's direction and speed can also be controlled from this GUI screen using the **Target Set** slider control in the lower area of the screen. The motor can be started or stopped via the motor switch and the board-mounted speed control potentiometer can also be enabled and disabled. To control the speed through the GUI, the potentiometer control switch on the right must be in the off position.

7 Bill of materials

Table 6 Bill of materials

Item	Part References	Qty	Description	Manufacturer	Part Number 1
1	C01, C2, C324	3	270uF, 80V, 20%, Radial Cap Alum	United Chemi-Con	EKZN800ELL271MK20S
2	C4, C18, C26, C36, C37	5	4.7uF, 100V, 10% , 1206	Murata	GRM31CC72A475KE11L
3	C6, C8, C9, C11, C12	5	2.2uF,100V,10%, 1206	TDK Corporation	C3216X7S2A225K160AE
4	C16, C57, C320	3	0.1uF, 25V, 10%, 0603	TDK Corporation	CGA3E2X5R1E104K080AA
5	C19, C328, C329	3	330pF, 50V, 10%, 0603	KEMET	C0603C331K5RAC7867
6	C25, C326, C327	3	100pF, 25V, 10%, 0603	KEMET	C0603C101K3GAC7867
7	C30, C32	2	2.2uF, 25V,10%, 0805	Samsung	CL21A225KAFNNNG
8	C33	1	0.22UF, 50V, ±10%, 0805	KEMET	C0805C224K5RACAUTO
9	C34	1	0.1uF, 10V, 10%, 0603	KEMET	C0603C104K8PAC7867
10	C35	1	10uF, 10V, 10%, 0603	Samsung	CL10A106KP8NNNC
11	C38	1	0.1uF ,100V, 10%, 0603	YAGEO	CC0603KRX7R0BB104
12	C39	1	0.22uF,10%,25V, 0603	MURATA	GRM188R61E224KA88D
13	C40, C41	2	22uF,16V, 20%, 0603	Samsung	CL10A226MO7JZNC
14	C42	1	10uF, 25V, 10%, 0805	Samsung	CL21A106KAFN3NE
15	C43, C45, C47, C49, C50	5	0.22uF,10V, 10%, 0603	MURATA	GRM188R61A224KA01D
16	C44, C46, C48, C51	4	1UF, 25V, 10%, X5R 0603	SAMSUNG	CL10A105KA8NNNC
17	C52, C53, C54	3	100pF,25V, ±5% , 0603	AVX	06033A101JAT2A
18	C55	1	10000pF,25V, ±10%, 0603	AVX	06033D103KAT2A
19	C56, C58, C325	3	1uF, 10V, 10%, 0603	MURATA	GRT188C81A105KE13D
20	C301, C305, C306, C308, C309, C310, C311, C312, C318, C319	10	100nF, 25V, 10%, X7R 0603	Kemet	C0603C104K3RAC7867
21	C302, C303	2	15pF, 25V, +-5%, 0603	Kyocera	06033A150JAT2A
22	C304, C314	2	10nF, 25V, 10%, 0603	Kemet	C0603C103K3RAC7411
23	C307	1	4.7uF, 25VDC, 20%, X5R 0603	Taiyo Yuden	TMK107BBJ475MA-T
24	C313, C315	2	10uF, 25V, 10%, 0603	Murata	GRM188R61E106KA73D
25	C316, C317	2	1uF, 6.3V, X5R 0603	Kemet	C0603C105K9PAC7411
26	C321, C322, C323	3	2200pF, 50V, 10%, X5R 0603	TDK Corporation	CGA3E2X5R1H222K080AA

Bill of materials

Item	Part References	Qty	Description	Manufacturer	Part Number 1
27	C330	1	1uF, 100V, 10%, 0805	Murata	GCM21BC72A105KE36L
28	D1	1	100V,2A,SMA	STMicroelectronics	B2100A-13-F
29	D2, D3, D4, D5, D8	5	Zener, 5.1V, 500mW, SOD-523 SMD	On-Semi	MM5Z5V1T1G
30	D6, D7, D303	3	DIODE SCHOTTKY 30V 500MA SC79-2	Infineon Technologies	BAS3005A02VH6327XTSA1
31	D9	1	DIODE ZENER 15V 500MW SOD523	On-Semi	MM5Z15VT1G
32	D10, D11, D12	3	DIODE SCHOTTKY 30V 500MA SC79-2	Infineon Technologies	BAS3005A-02V
33	D14	1	TVS DIODE 40VWM 64.5VC SMA	Eaton - Electronics Division	SMAJE40A
34	D301	1	DIODE SCHOTTKY 30V 1A SOD323	Infineon Technologies	BAS3010A-03W
35	D302	1	TVS DIODE 5.3VWM 15VC TSFP-3	Infineon Technologies	ESD5V3U2U03FH6327XTSA1
36	F1	1	FUSE 50A 125VAC NANO SMD	Littelfuse Inc.	0456050.DRSD
37	HS1	1	Heatsink (60x20x40)mm QSZ39x39	AlphaNovatech	S08CDY15
38		1	QSZ39x39	AlphaNovatech	S001ZB7F
39		2	ANCR-10	AlphaNovatech	S001YZ7A
40	IC301	1	XMC4000 Microcontroller IC 32-Bit 80MHz 256K	Infineon Technologies	XMC4200Q48K256BAXUMA1
41	IC302	1	IC REG LINEAR 3.3V 500MA TSON-10	Infineon Technologies	TLS205B0LDV33XUMA1
42	IC303	1	DGTL ISO 2500VRMS 6CH GP 16SOIC	Skyworks Solutions Inc.	SI8662BB-B-IS1
43	IC304	1	IC BUF NON-INVERT 5.5V 5TSSOP	Nexperia	74LVC1G126GW,125
44	J3	1	CONN JACK R/A PCB 5.5X2.1MM	Tensility International Corp	54-00129
45	J9	1	DEBUG 8Pin	Adam Tech	PH2-08-UA
46	JP301	1	CONN HEADER VERT 5POS 2.54MM	Sam tech	HTSW-105-07-G-S-LL
47	L1	1	FIXED IND 22UH 1.2A 500 MOHM SMD	Bourns	SRP4020TA-220M
48	L301	1	FERRITE BEAD 60 OHM 0603 1LN	Würth Elektronik	74279267

Bill of materials

Item	Part References	Qty	Description	Manufacturer	Part Number 1
49	LED1, LED4, LED302, LED303	4	LED RED CLEAR	Lite-On Inc.	LTST-C190KRKT
50	LED2, LED3	2	LED BLUE DIFFUSED	Osram Opto	LB Q39G-L2OO-35-1
51	LED5, LED301	2	LED GREEN DIFFUSED	Rohm Semiconductor	SML-D12M8WT86
52	NT2, NT3, NT4, NT5	4	#4-40 Hex Nut 0.250" (6.35mm) 1/4"	B&F Fastener Supply	HNSS440
53	POT1	1	TrIMMER 10K OHM 0.5W PC PIN TOP	Bourns Inc.	3362P-1-103TLF
54	Q1A, Q1B, Q2A, Q2B, Q3A, Q3B, Q4A, Q4B, Q5A, Q5B, Q6A, Q6B	12	MOSFET N-CH 60V 261A WSON-8	Infineon Technologies	BSC014N06NSSC
55	Q19	1	MOSFET N/P-CH 60V 3A/2A 8DSO	Infineon Technologies	BSO612CV G
56	Q301	1	CRYSTAL 12.0000MHZ 8PF SMD	Kyocera	CX3225GA12000D0PTVCC
57	R2	1	75K, 1/10W, 1%, 0603	Panasonic	ERJ-3EKF7502V
58	R5	1	7.87K,1/10W,1%, 0603	Yageo	RC0603FR-077K87L
59	R6, R24, R38	3	56K, 1/10W, 1%, 0603	YAGEO	RC0603FR-0756KL
60	R10, R29, R42, R324	4	5.6K, 1/10W, 1%, 0603	Stackpole	RMCF0603FT5K60
61	R11	1	100K, 1/10W, 1% , 0603	Yageo	RC0603FR-07100KL
62	R13	1	22K, 1/10W, 1%, 0603	Yageo	RC0603FR-0722KL
63	R14	1	3.3K, 1/10W, 1% , 0603	Yageo	RC0603FR-073K3L
64	R15, R328, R329	3	470R, 1/10W, 1% , 0603	Panasonic	ERJ-3EKF4700V
65	R18	1	1.8K, 1/10W, 0.1%, 0603	Yageo	RT0603BRE071K8L
66	R20	1	10, 1/2W, 5%, 1210	Yageo	RC1210JR-0710RL
67	R19, R22, R26, R33, R39, R50, R62, R63, R327	9	5.1K, 1/10W, 5%, 0603	Panasonic	ERJ-3GEYJ512V
68	R44, R45, R46, R309, R311, R312	6	10K, 1/10W, 5%, 0603	Yageo	RC0603JR-0710KL
69	R51	1	1K, 1/10W, 1%, 0603	Yageo	RC0603FR-071KL
70	R53, R54, R55	3	2.2K, 1/10W, 1%, 0603	Yageo	RC0603FR-072K2L
71	R56, R57, R58	3	3.3K, 1/10W, 1%, 0603	Yageo	RC0603FR-073K3P
72	R61	1	100R, 1/10W, 1%, 0603	Yageo	RC0603FR-07100RP
73	R64	1	200R, 1/10W, 1%, 0603	Yageo	AC0603FR-07200RL
74	R65, R67, R69, R72	4	10K , 0.1W, 1% , 0603	Vishay Dale	CRCW060310K0FKEA
75	R66, R68, R70	3	49.9K , 0.1W , 1% , 0603	Vishay Dale	CRCW060349K9FK

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Item	Part References	Qty	Description	Manufacturer	Part Number 1
76	R71	1	0 OHM JUMPER 0.1W, 0603	Vishay Dale	CRCW06030000Z0EA
77	R73	1	22K , 0.1W, 1%, 0603	Vishay Dale	CRCW060322K0FK
78	R301, R302	2	680R, 1/10W, 1%, 0603	Yageo	RT0603FRE07680RL
79	R305	1	510R, 1/10W, 1%, 0603	Panasonic	ERJ-3EKF5100V
80	R306, R307	2	22R, 1/10W, 5%, 0603	Panasonic	ERJ-3GEYJ220V
81	R308	1	4.7K, 1/10W, 1%, 0603	Panasonic	ERJ-3EKF4701V
82	R310, R314	2	1M, 1/10W, 1%, 0603	Yageo	RC0603FR-071ML
83	R316, R321, R322, R323	4	0R, 1/10W, JUMPER, 0603	Yageo	RC0603JR-070RP
84	R317	1	3K, 1/10W, 1%, 0603	Panasonic	ERJ-3EKF3001V
85	R318	1	32.4K, 1/10W, 1%, 0603	Panasonic	ERJ-3EKF3242V
86	R319	1	4.64K, 1/10W, 1%, 0603	Yageo	RC0603FR-074K64L
87	R330	1	2K, 1/10W, 1%, 0603	Stackpole Electronics, Inc	RMCF0603FT2K00
88	R331, R332, R333, R334, R335, R336, R337, R338, R339, R340, R341, R342	12	0R, 1/10W, JUMPER, 0603	Yageo	RC0603FR-070RL
89	RS1, RS2, RS3	3	RES 0.001 OHM 1% 5W 3920	Stackpole Electronics Inc	HCS3920FT1L00
90	RT1	1	SENSOR ANALOG -40C-125C SOT23-3	Microchip	MCP9700T-E/TT
91	ST1, ST2, ST3, ST4	4	HEX STANDOFF #4-40 ALUM 1-1/4"	Keystone	8407
92	SW1	1	SWITCH SLIDE SPDT 200MA 30V	E-Switch	EG1218
93	SW2, SW3	2	SWITCH SLIDE SPST 0.4VA 28V	NKK Switches	AS11CP
94	U3	1	32-bit Microcontrollers with ARM® Cortex®-M0	Infineon Technologies	XMC1404-Q064X0200 AA
95	U4	1	Gate driver IC for 3 phase BLDC or PMSM motor drive application	Infineon Technologies	6EDL7151
96	X3	1	CONN TERM BLOCK 2.54MM 5POS	PHOENIX CONTACT	1725685
97	X4, X5	2	Header,4x1,TH,0.025 Sq,100milSP	Adam Tech	PH1-04-UA
98	X302C	1	RCPT, USB2.0, MICRO AB, SMD, RA	Würth Elektronik	6.29105E+11

Bill of materials

Item	Part References	Qty	Description	Manufacturer	Part Number 1
99	Jumper1, Jumper 2 (Do not populate)	2	0, 3/4W, Jumper 2010	YAGEO	RC2010JK-070RL

8 Motor specifications

The motor used for obtaining the results presented in this application note is CMP1424X1E-202409 (BASE MOTOR: MPP1424C1E-KPSN) manufactured by Parker Hannifin Corp. The specifications are as follows:

Table 7 Motor technical data

MOTOR DATA @	48	VDC	
MOTOR PARAMETERS		UNITS	VALUE
HORSEPOWER	HP RATED	Hp	4.29
KILOWATTS	KW RATED	KW	3.2
MAX. OPERATING SPEED	N MAX	RPM	2635
SPEED @ RATED TORQUE	N RATED	RPM	2431
CONTINUOUS RATED TORQUE @ 2431RPM		IN-LBS[Nm]	110.2 [12.45]
CONTINUOUS STALL TORQUE		IN-LBS[Nm]	112 [12.66]
CONTINUOUS LINE CURRENT		A(rms)	60.0
PEAK TORQUE	Tpk	IN-LBS[Nm]	454.3[51.33]
PEAK CURRENT		A(rms)	282.4
TORQUE SENSITIVITY	Kt	IN-LBS/AMP[Nm/A(rms)]	1.534 [0.212]
BACK EMF (LINE TO LINE)	± 10%	Vrms/Krpm	12.84
D.C. RESISTANCE (P-P)	± 10%	OHMS	0.01238
INDUCTANCE (P-P)	± 10%	MILLIHENRIES	0.213
ROTOR INERTIA	Jm	IN-LBS-SEC²[Kg-M²]	0.0130[0.001469]
STATIC FRICTION	Tf	IN-LBS[Nm]	0.469[0.0530]

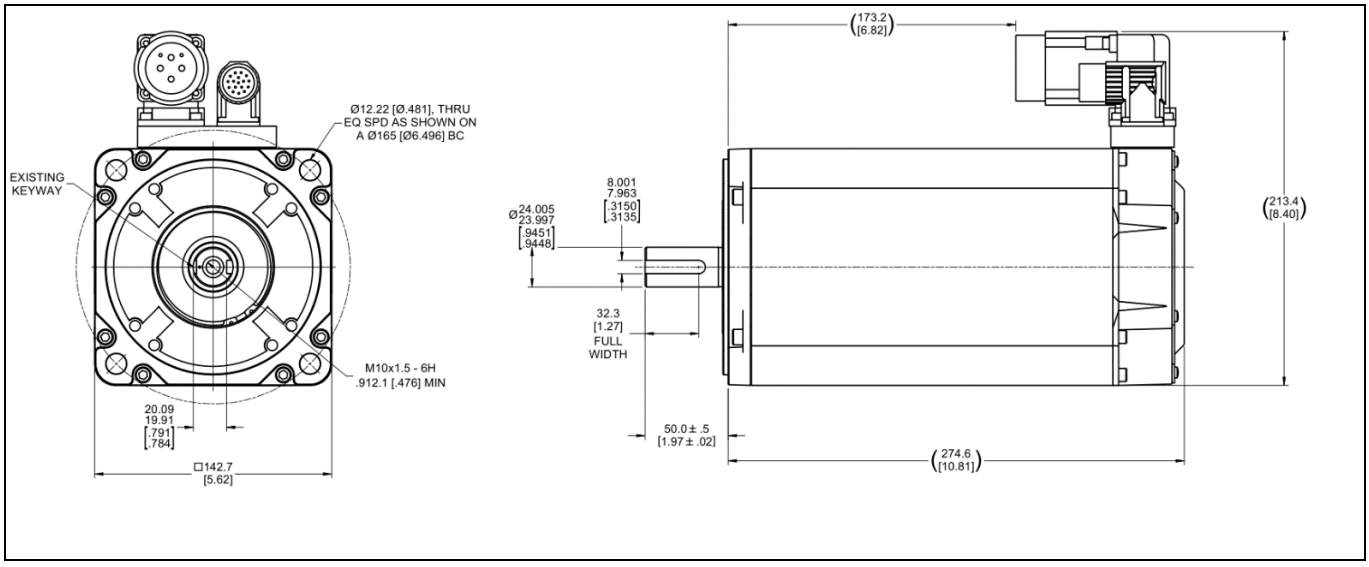

Figure 60 CMP1424X1E-202409 motor dimensions

9 PCB layout

The EVAL_6EDL7151_36V_1kW evaluation board utilizes a six-layer PCB with 2 oz. copper on the top and bottom layers and 1 oz. copper on the internal layers. The components are mounted on the top and bottom sides. The width is 3.3 inches/84 mm, and the length is 4.7 inches/120 mm.

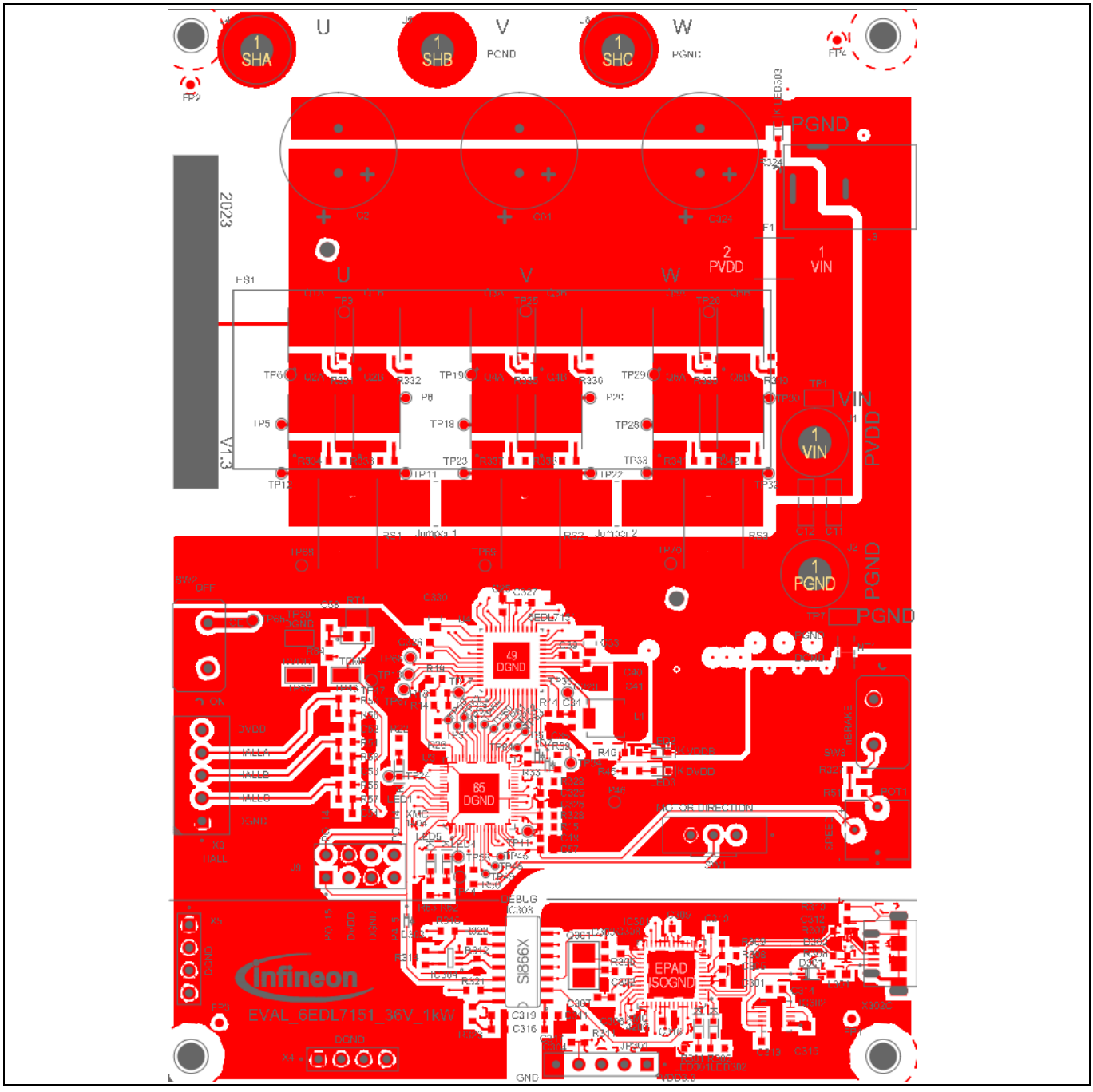

Figure 61 EVAL_6EDL7151_36V_1kW PCB top layer with silkscreen

PCB layout

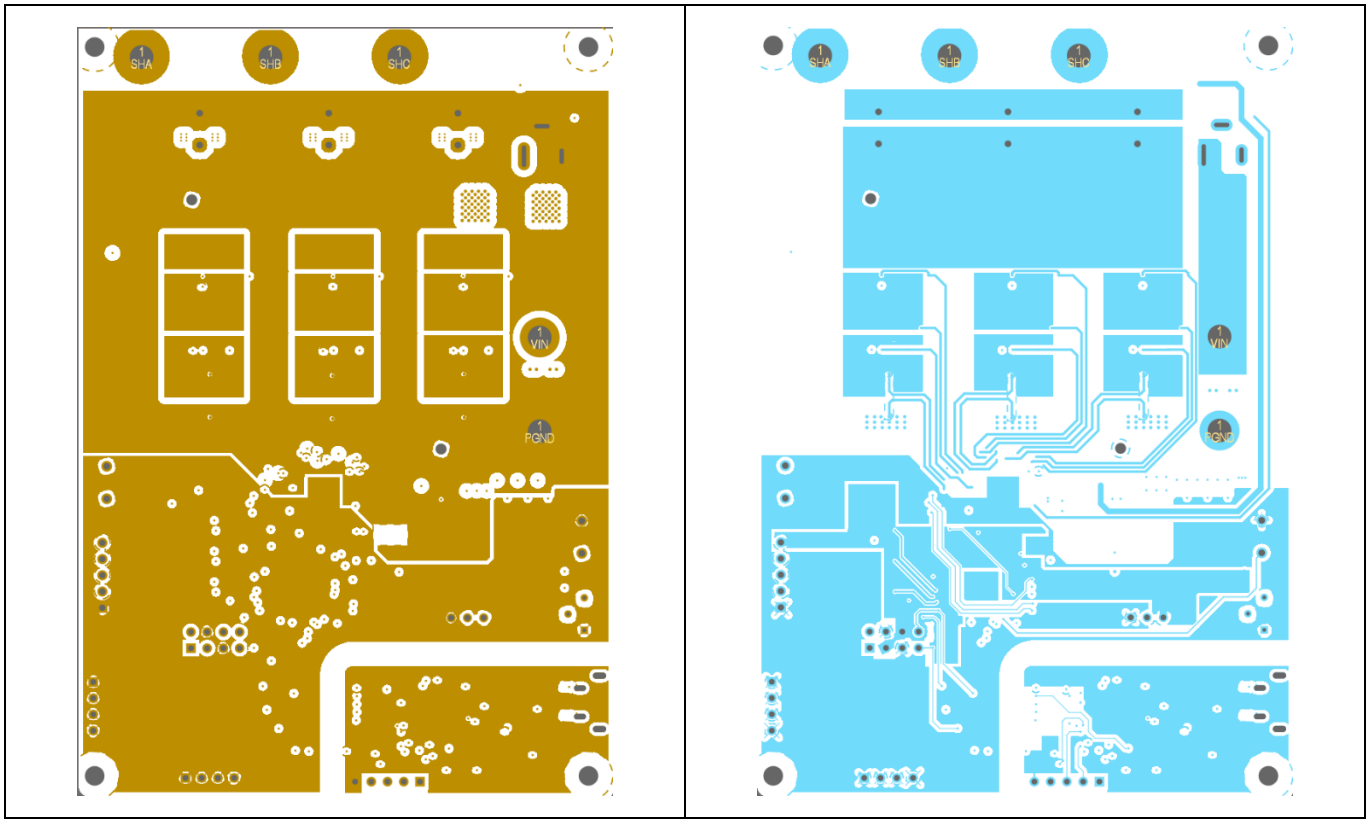

Figure 62 EVAL_6EDL7151_36V_1kW PCB internal layers 1 (left) and 2 (right)

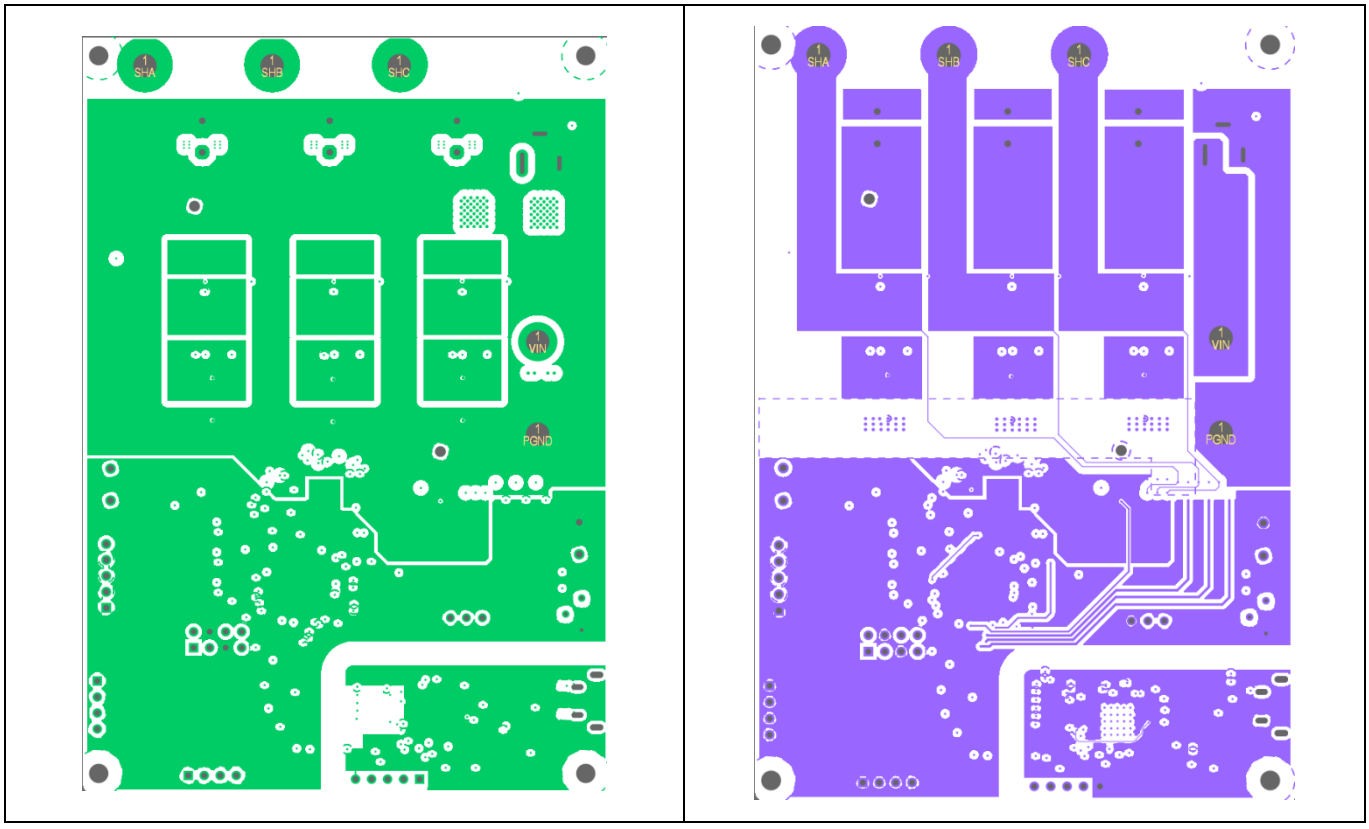

Figure 63 EVAL_6EDL7151_36V_1kW PCB internal layer 3 (left) and layer 4 (right)

PCB layout

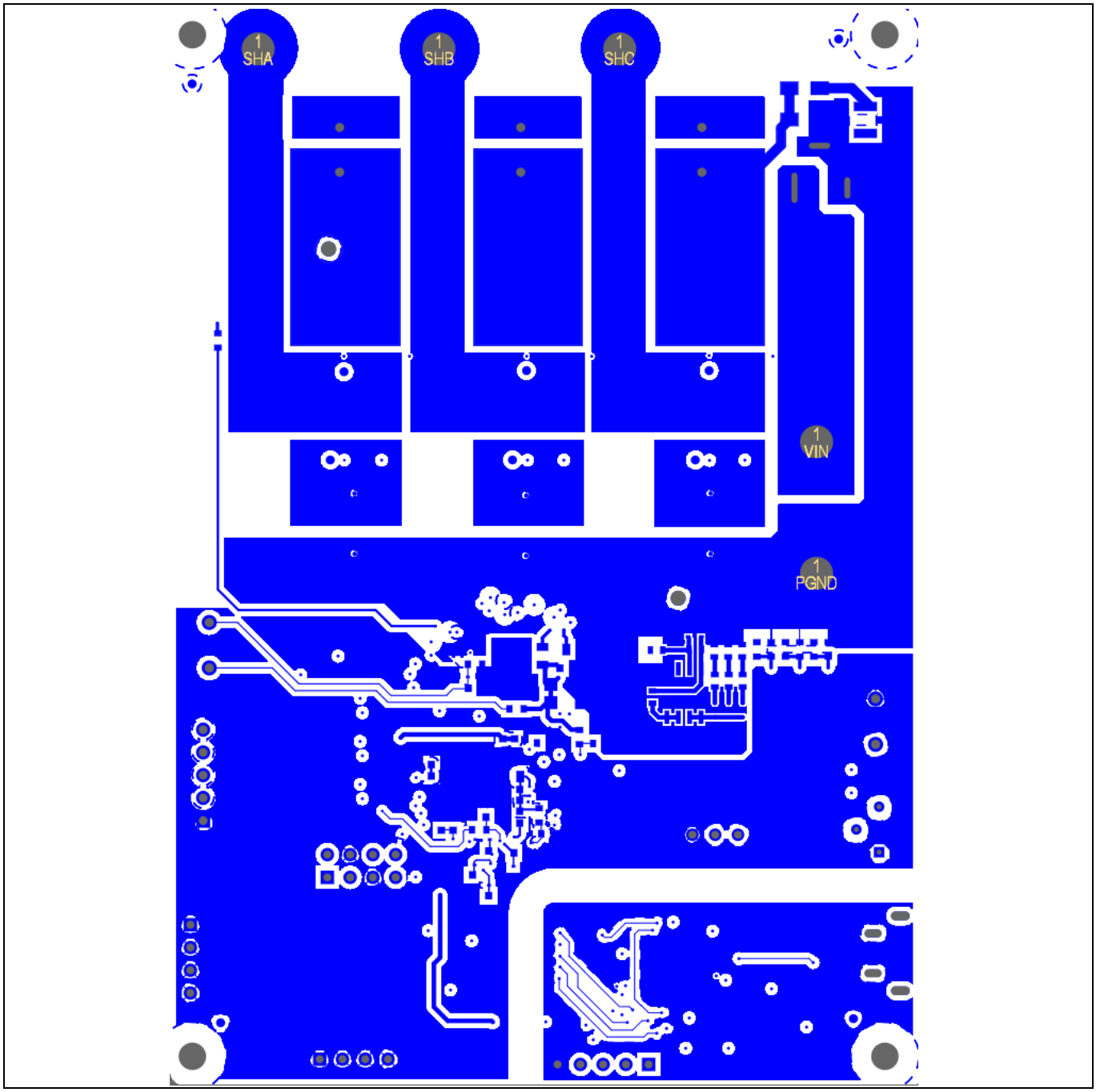

Figure 64 EVAL_6EDL7151_36V_1kW PCB bottom layer with silkscreen

The PCB layout is optimized to minimize EMI by keeping the loops carrying the switching currents as small as possible. The high frequency switching current loops are illustrated in the Figure 65. It should be noted that during the switching transition, the high-side gate drive loop current returns to the main ground rather than back to the gate driver as in a conventional high-side driver. Since this is the case, the high-side gate drive loop should also be kept as tight as possible. The top layer connects the DC bus to the topside MOSFET drains, while the first internal layer returns the MOSFET current via the current sense shunt. The switching loop for each phase begins and ends at the electrolytic capacitor and the high-frequency decoupling capacitors. The return traces on the first internal layer pass underneath the power traces, thus creating very tight high-frequency switching loops.

PCB layout

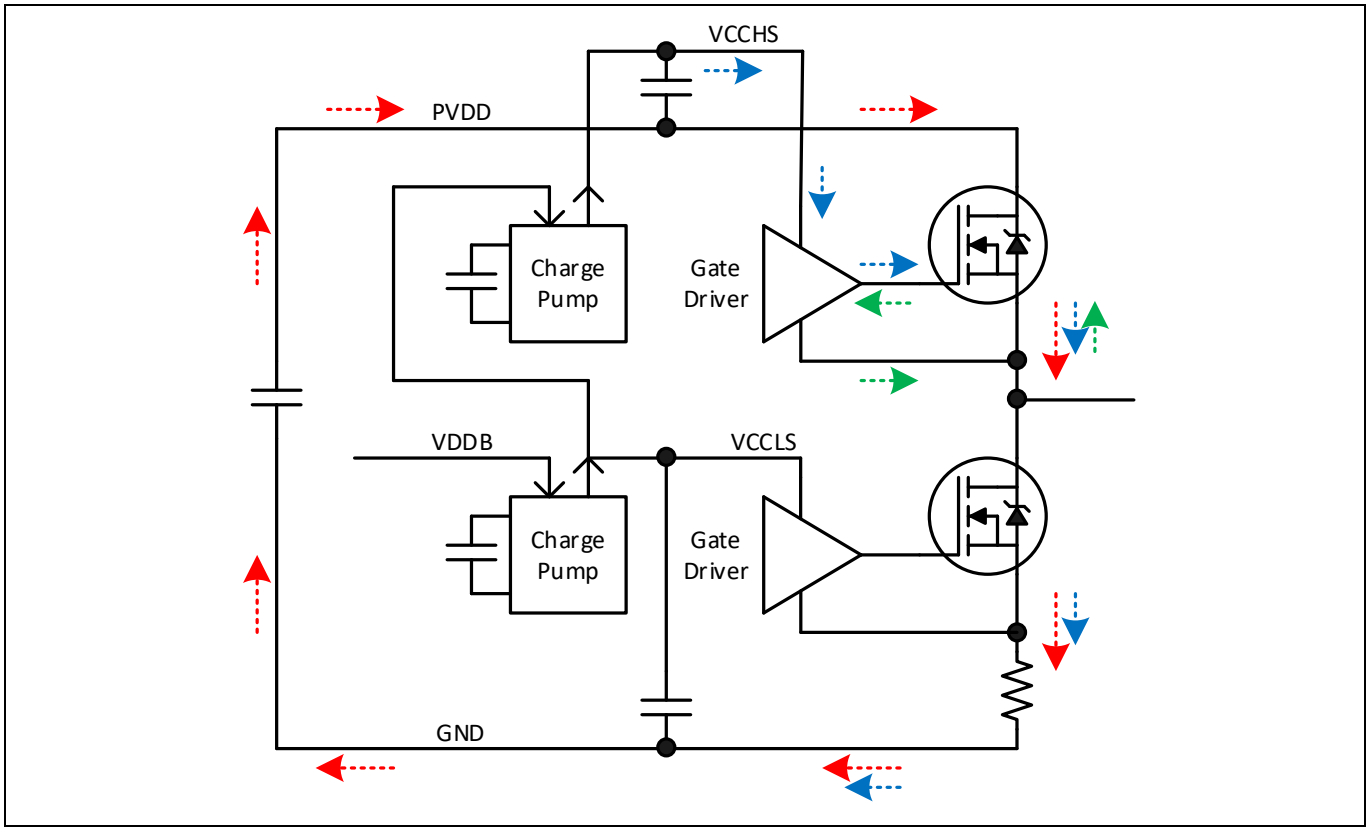

Figure 65 **High-frequency current loop for one phase**
Red: Main HF switching loop; Blue: high-side gate drive switch on current loop;
Green: High-side gate drive switch-off current loop

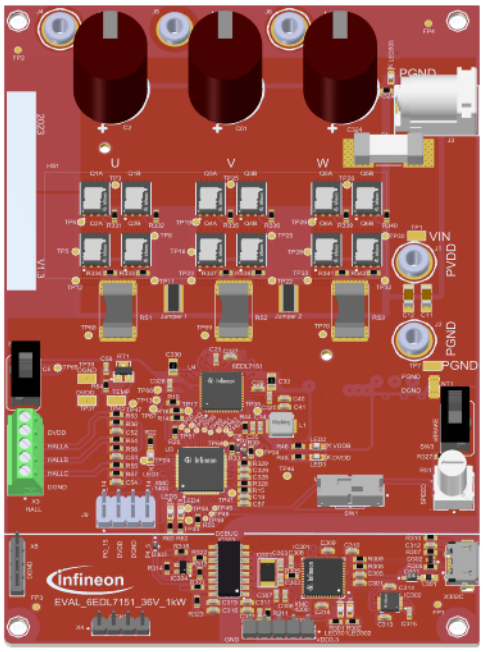

Figure 66 **Board topside view with option to attach heatsink on top of MOSFETs**

10 Test results

10.1 Operating waveforms

The following waveforms were captured with the EVAL_6EDL7151_36V_1kW board driving a motor at 1500 RPM with an input power of 1000 W at 36 V input.

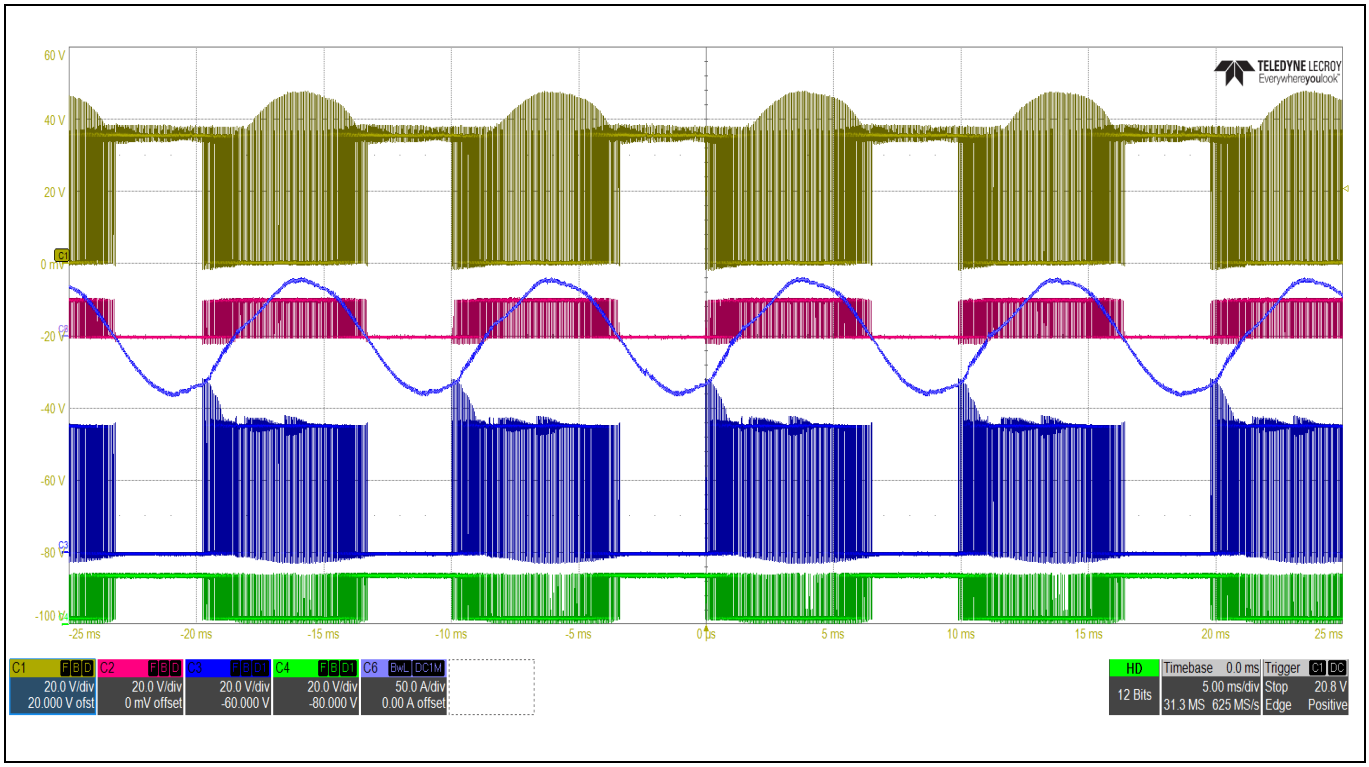

Figure 67 Phase “V” waveforms

C1-V_{DS_HS}, C2- V_{GS_HS}, C3-V_{DS_LS}, C4-V_{GS_LS}, C6-I_{PH_V}

Test results

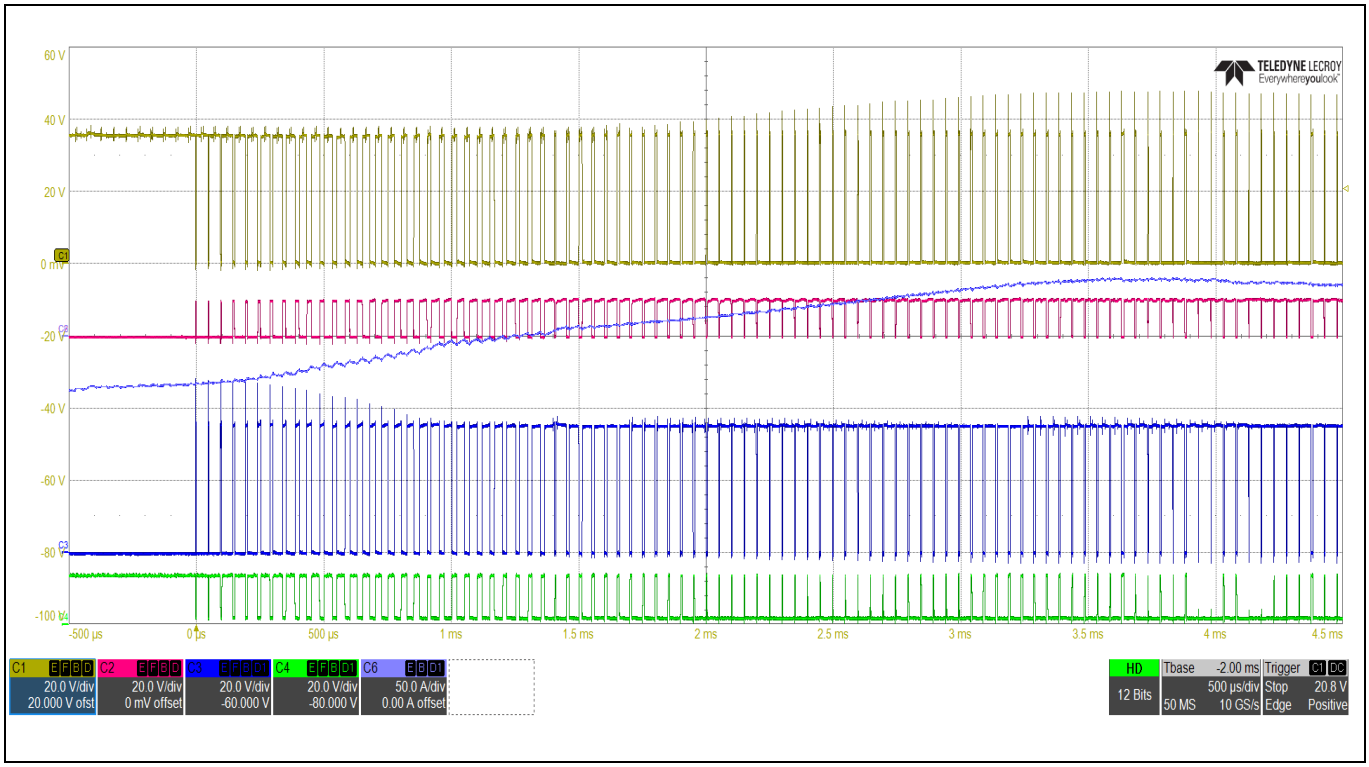

Figure 68 **Phase “V” waveforms**
C1-V_{DS_HS}, C2- V_{GS_HS}, C3-V_{DS_LS}, C4-V_{GS_LS}, C6-I_{PH_V}

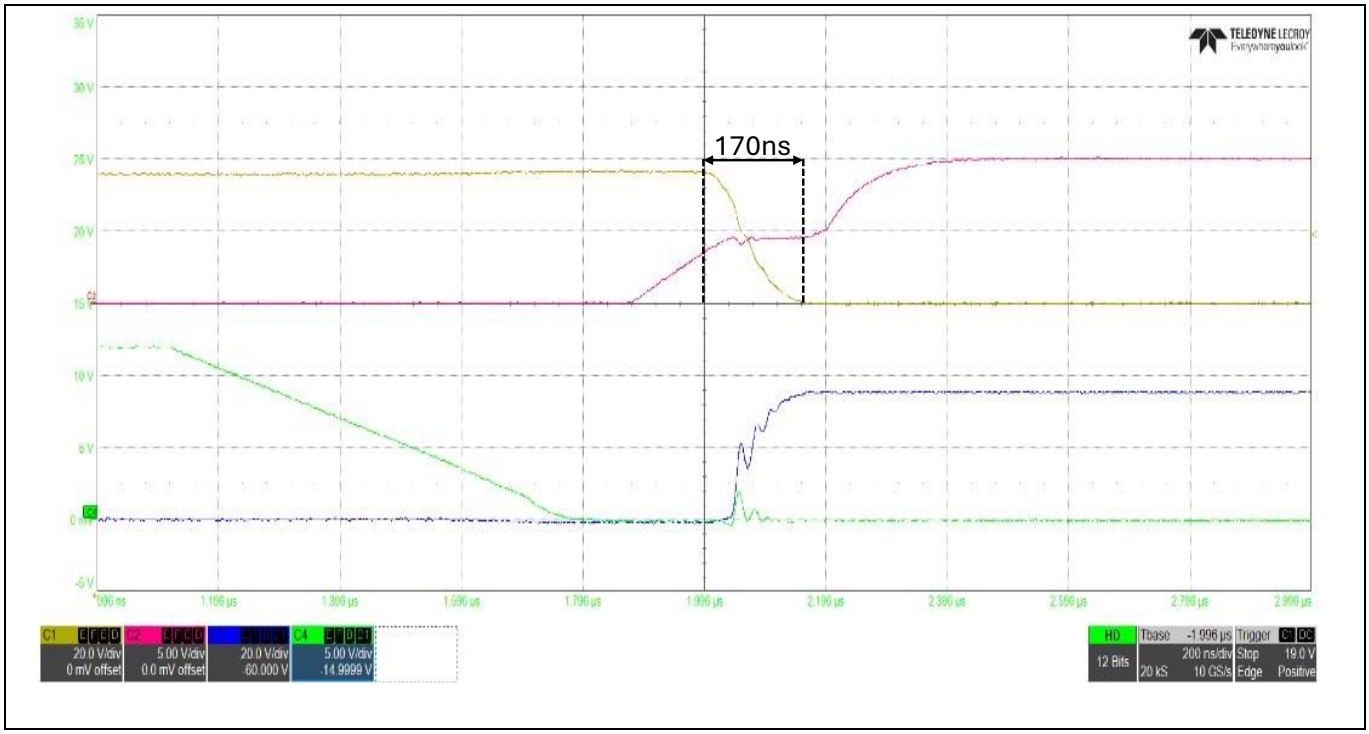

Figure 69 **Phase “V” waveforms for 36 V input at 1000 W**
C1-V_{DS_HS}, C2- V_{GS_HS}, C3-V_{DS_LS}, C4-V_{GS_LS}

Test results

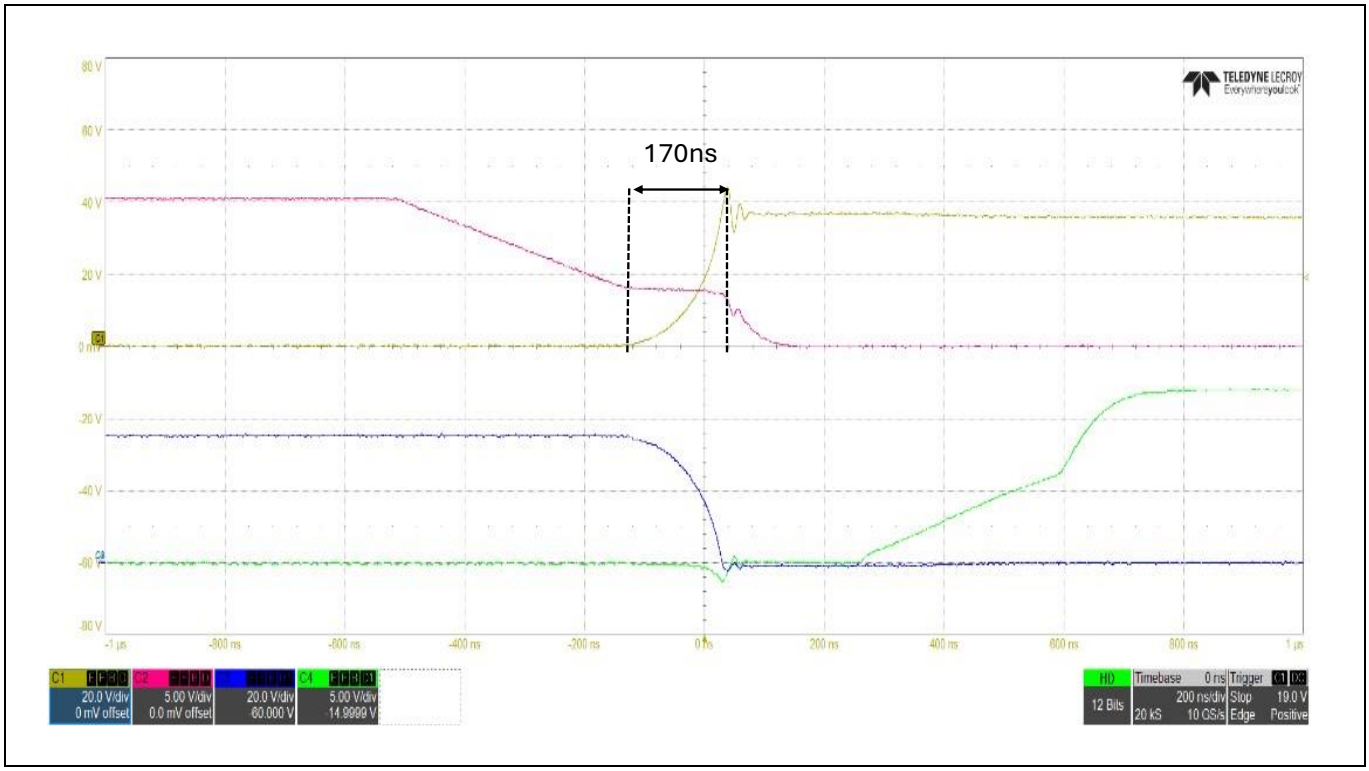

Figure 70 **Phase "V" node negative transition for 36 V input at 1000 W**
C1-V_{DS_HS}, C2- V_{GS_HS}, C3-V_{DS_LS}, C4-V_{GS_LS}

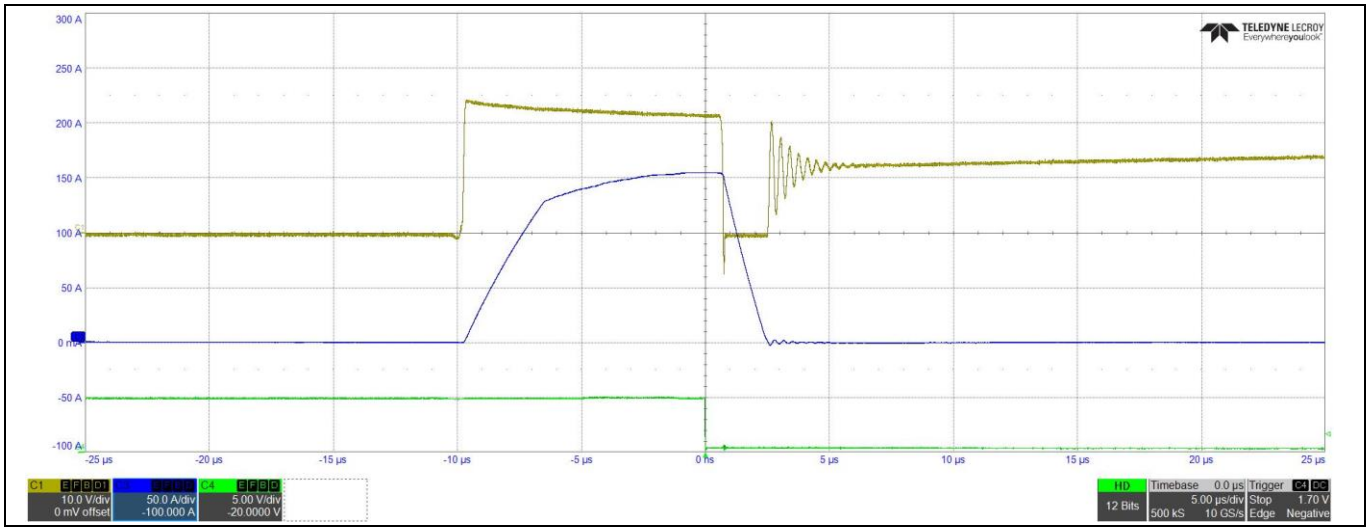

Figure 71 **On the fly short circuit between Phase "V" node and ground;**
V_{DS_HS} (yellow), I_SC (blue), nFault (Green); Highside threshold is 0.25 V, Blanking time =5 us, Filter time =5 us

10.1 Power measurements

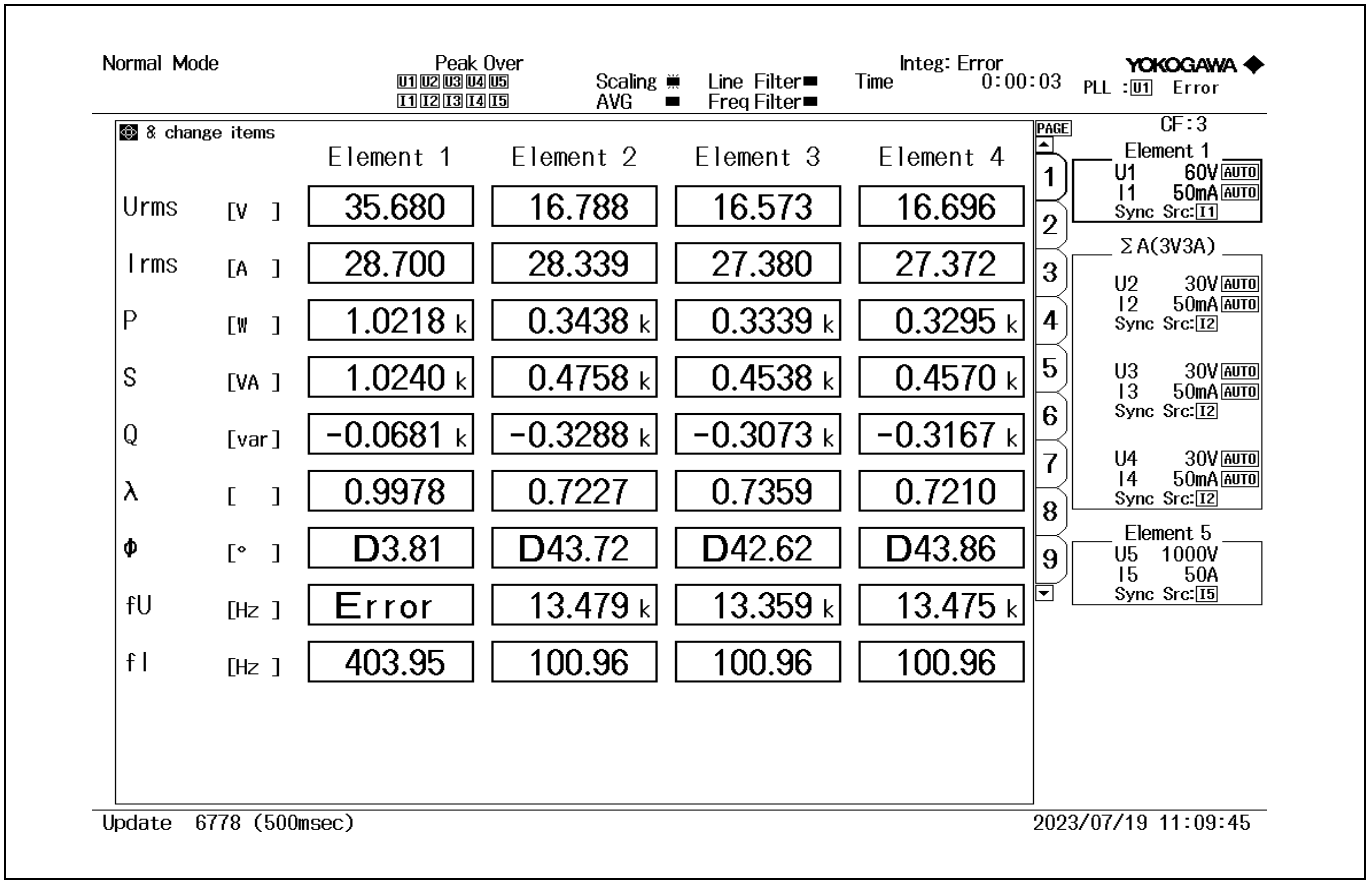

Figure 72 Input and output measurements at nominal input voltage 36 V and 1000 W input power

In the above results, element 3 represents the DC input to the inverter. Elements 4, 5 and 6 are connected to the output phases U, V, and W, respectively.

The total output power is equal to 343.8 W + 333.9 W + 329.5 W = 1007.2 W for an input power of 1022 W.

This gives an efficiency of 1007.2/1022 = 98.5% with losses of 15 W for the electrical power stage.

This is evidenced by the very moderate component temperature rise measurements in the following section.

10.2 Thermal measurements

Thermal images were taken after 30 minutes of continuous operation at an ambient temperature was 25°C, without forced air-cooling, to capture the steady-state component temperatures.

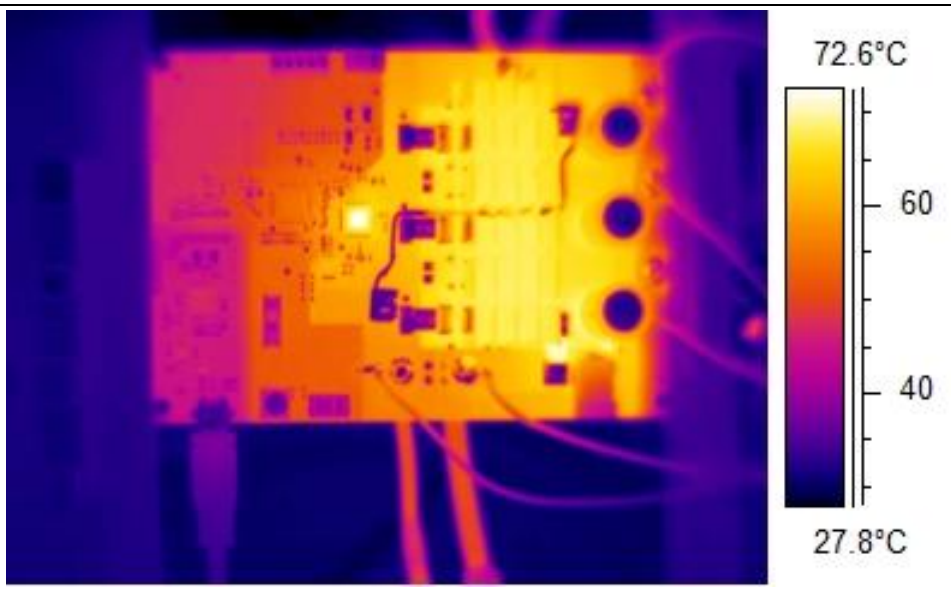

Figure 73 Thermal measurements at 36 V input and Input power are 1 kW

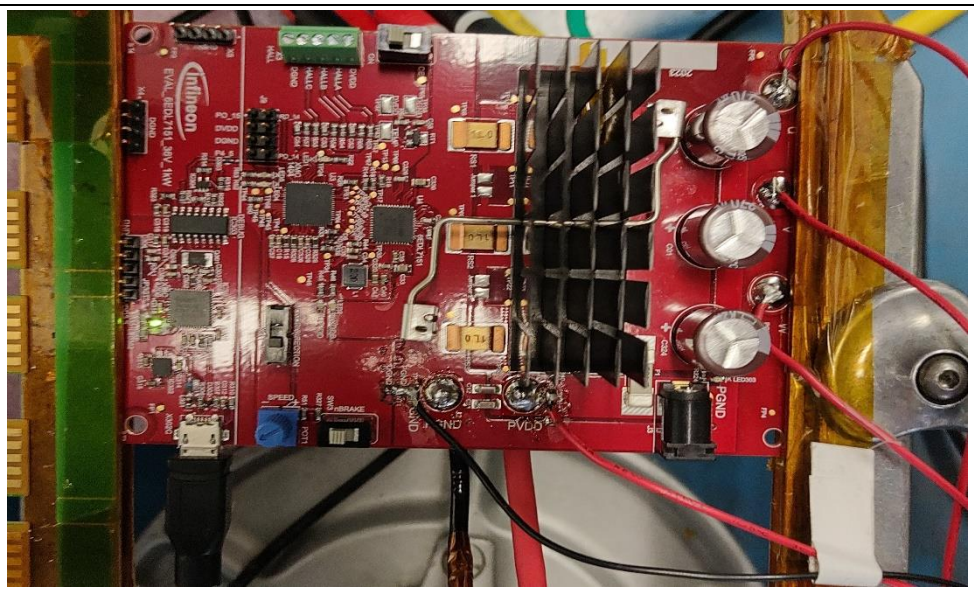

Figure 74 Image of test setup used for thermal measurement

Test results

The hot spots on the evaluation board are the heatsink at ~70°C and 6EDL7151 gate driver IC at ~72°C. The MBS setup was used to perform the above test with the motor running at 1500 rpm and a load of 54 in-lb. All the electrical waveforms obtained by driving a motor at the same test condition are presented in Section 10.1.

11 Conclusion

The EVAL_6EDL7151_36V_1kW evaluation board meets the required specifications, showcases its features, and the versatility of the 6EDL7151 in this application note. The principle of operation, design of the circuitry, control scheme, and PCB layout have been discussed. The motor speed, direction, and braking may be controlled locally with switches and a potentiometer located on the board or may be controlled by the GUI tool. The extensive capabilities of the ModusToolbox™ Motor Suite GUI have been explained. The MOSFET Tuning tool in the ModusToolbox™ Motor Suite, which is used to obtain the gate drive parameters has been shown and the results were verified through test waveforms. The ability to install customized firmware and configuration parameters to the system greatly simplifies the design process, eliminates unnecessary components and is thereby able to simplify product development and reduce time to market.

The measured slew rate of 211 V/µs and the turn-on and turn-off times are 170 ns. The measured values will be slightly different from the estimated values from MOSFET tuning tool is due to the non-linearity and expected tolerances in the gate charge and gate drive current values. Allowing for this, the benefits of the 6EDL7151 configurable gate drive outputs are clearly seen and the switching performance has been shown without the need for any gate drive resistors or diodes.

Thermal measurements show that the 3-phase inverter BSC014N06NSSC Dual-Side Cooling OptiMOS™ switches in 5x6 SuperSO8 (PG-WSON-8) packages offer excellent performance. By attaching a heatsink directly on dual side cooled MOSFETS of the board, the power handling ability of this driver could be further increased.

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