UG-2024-03 EVAL-2EP130R-PR-SiC evaluation board

User guide

EiceDRIVER™ Power EVAL-2EP130R-PR-SiC

Full-bridge transformer driver for isolated gate driver power supply for SiC MOSFETs

About this document

Scope and purpose

This user guide is intended to provide information about the Infineon evaluation board EiceDRIVER™ Power EVAL-2EP130R-PR-SiC. It describes the start-up, measurements, and parameter adjustments of the 2EP1xxR (2EP100R, 2EP101R, 2EP110R, and 2EP130R) product family. The 2EP1xxR is a full-bridge transformer driver IC to design isolated gate driver supplies for IGBT and SiC MOSFETs.

Intended audience

This document is intended for electrical engineers who are knowledgeable about isolated gate driver supply with open loop architecture.

Evaluation board

This board is used for evaluating and measuring 2EP130R.

This user guide is intended to help adapt the evaluation board EVAL-2EP130R-PR-SiC to the supply needs of a large variety of switches. The board supports isolated supply voltages for two gate driver ICs, for example, a high-side and a low-side gate driver IC.

***Note**: The PCB and auxiliary circuits are NOT optimized for final customer design.*

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***Note**: Please note the following warnings regarding the hazards associated with development systems.*

Table 1 Safety precautions

	**Warning:** *The isolated output voltages provide a creepage/clearance of 4 mm between output 1 and output 2. Ensure proper protection and coverage in case of use for voltages above SELV level.*
	**Warning:** *The input to output isolation is built for reinforced applications. However the board has not a hipot-test and can therefore not be declared as proven reinforced isolation.*
	**Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

Table of contents

1 The board at a glance

This user guide (UG-2024-03) describes the evaluation board, EVAL-2EP130R-PR-SiC. This board has been designed as a validation board that can be used by design engineers to evaluate the family of full-bridge transformer driver ICs – 2EP1xxR.

The board includes all necessary components.

Details about the transformer driver IC is available in the datasheet of the EiceDRIVER™ Power 2EP1xxR family.

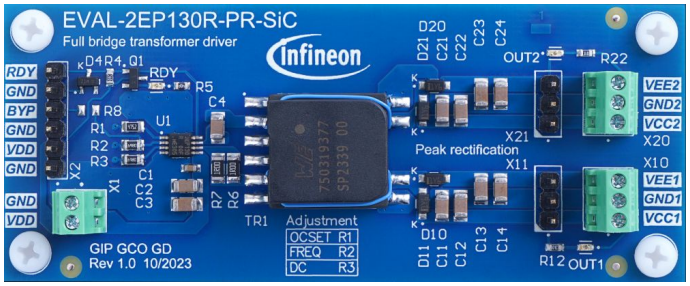

Figure 1 Evaluation board EVAL-2EP130R-PR-SiC

Delivery content

The delivery contains:

- One EVAL-2EP130R-PR-SiC, 90 × 37 mm^2 in size

Simplified schematic

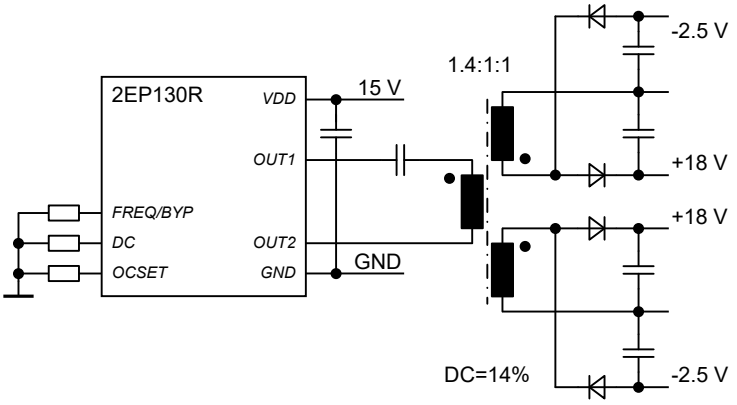

Figure 2 Peak rectifier schematic for 2EP130R

The simplified schematic shows a peak rectification for two separated rails, each with positive and negative output voltage.

Main features

The evaluation board, EVAL-2EP130R-PR-SiC, is designed for easy evaluation of the full-bridge transformer driver IC. The following table shows the product variants in the EiceDRIVER™ Power 2EP1xxR family and their differentiating features.

1 The board at a glance

Table 2 2EP1xxR product variants

Product name	Frequency	Duty cycle	Average overcurrent protection	Bypass input
2EP100R	66 kHz or 100 kHz	33% or 50%	Level 4	no
2EP101R	50 kHz or 66 kHz	12% or 17%	Level 4	no
2EP110R	50 kHz or 66 kHz	10% .. 50%	Level 4	no
2EP130R	50 kHz .. 695 kHz	10% .. 50%	Level 1-5	yes

All product variants are pin compatible and can be used with matching configuration settings in customer-specific designs. 2EP130R is pre-assembled on EVAL-2EP130R-PR-SiC for complete feature evaluation.

The evaluation board provides all the necessary supply, load, and signal connections for an application. It offers the following features:

- Wide input supply range V_{VDD} from 5 V to 20 V
- Output power of up to 5 W (depending on duty cycle)
- Dual isolated output supply rails with peak rectification topology and duty-cycle adjustable output voltage ratio
- Wide frequency operating range from 50 kHz to 695 kHz using the internal oscillator or an external pulse width modulation (PWM)
- Adjustable overcurrent threshold
- Short circuit protection of power outputs
- Overtemperature protection
- *RDY* status output indication for normal operation

Board parameters and technical data

Parameters of the evaluation board, EVAL-2EP130R-PR-SiC, must respect the absolute maximum ratings listed below and should be operated within the recommended operating range.

Table 3 Absolute maximum ratings

Parameter	Symbol	Values		Unit	Note/conditions
		Min	Max		
Supply voltage	V_{VDD}	0	22	V	Referenced to *GND*
Positive output voltage	V_{VCC1},V_{VCC2}	0	35	V	Limited by capacitor and diode voltage rating, referenced to *GND1*/*GND2*
Negative output voltage	V_{VEE1},V_{VEE2}	-35	0	V	Limited by capacitor and diode voltage rating, referenced to *GND1*/*GND2*
Input to output/between output rails	V_{ISO}	-800	800	V	Functional isolation, no HiPot test performed
Output current	I_{VCC1}, I_{VCC2}, I_{VEE1}, I_{VEE2}	2	400	mA	Depending on configuration, limited by IC
RDY sink current	I_{RDY}	0	10	mA	Referenced to *GND*
RDY voltage	V_{RDY}	0	6.5	V	Referenced to *GND*

1 The board at a glance

Table 4 Recommended operating range

Parameter	Symbol	Values		Unit	Note/conditions
		Min	Max		
Supply voltage	V_{VDD}	5	20	V	Referenced to *GND*, depending on configuration
Positive output voltage	V_{VCC1},V_{VCC2}	0	35	V	Limited by capacitor and diode voltage rating, referenced to *GND1*/*GND2*
Negative output voltage	V_{VEE1},V_{VEE2}	-35	0	V	Limited by capacitor and diode voltage rating, referenced to *GND1*/*GND2*
Bypass signal voltage	V_{BYP}	0	5.5	V	Referenced to *GND*
Bypass signal frequency	f_{BYP}	50	695	kHz	Transformer and duty-cycle dependent
Output current	I_{VCC1}, I_{VCC2}, I_{VEE1}, I_{VEE2}	2 [1)]	150	mA	Depending on configuration, limited by IC
RDY sink current	I_{RDY}	0	10	mA	Referenced to *GND*

1) minimal load for stable operation

2 System and functional description

2.1 Theory of 2EP1xxR using peak rectification topology

This section describes the theory behind the full-bridge power stage of 2EP1xxR and the peak rectification topology to provide two isolated output voltages. Each transformer output winding supports a positive and negative output voltage. The ratio between the positive voltage and negative voltage is defined by the duty cycle.

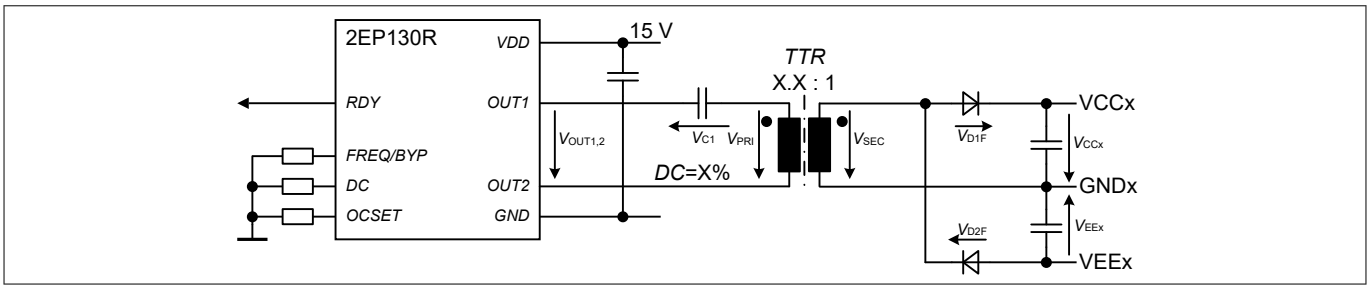

Figure 3 Simplified schematic of 2EP130R using peak rectification topology

The voltage arrows indicate the polarity of the corresponding symbol for use in the equations provided later. V_{PRI} and V_{SEC} represent the transformer voltages, V_{DxF} the individual diode forward voltages, V_{C1} the voltage across the primary DC blocking capacitor, and V_{CCx}/V_{EEx} the output voltage.

The following sections describe how to determine the output voltages of a peak rectification according to:

- the applied input voltage to 2EP
- the applied duty cycle by chopping the input voltage
- the level-shift (offset) of the serial capacitor
- the transformer turn ratio
- the peak current rectification

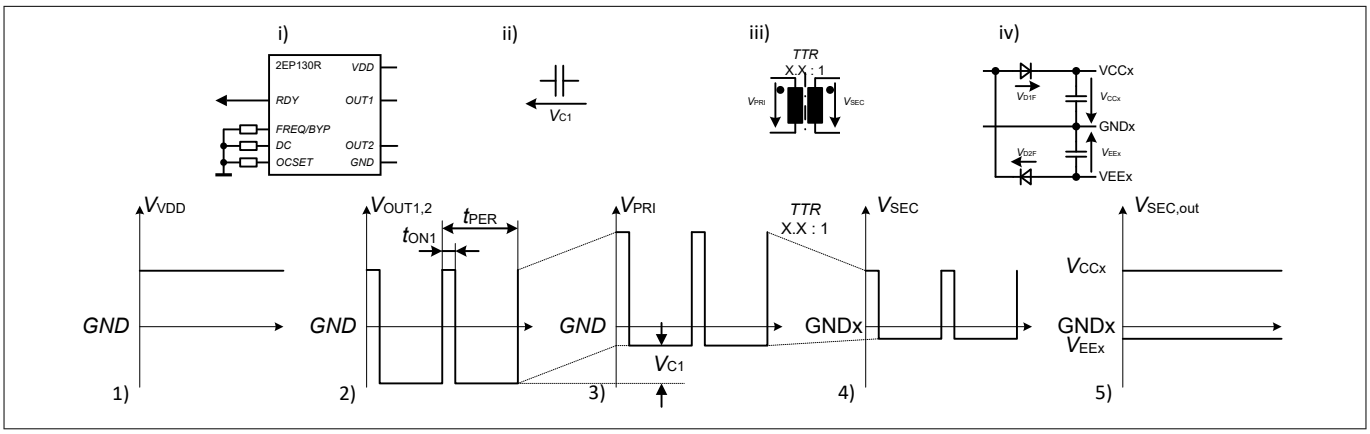

Figure 4 DC offset voltage and influence of transformer turn ratio output voltage

The figure visualizes the idealized voltage wave forms at each step (1-5) and the involved components at the intermediate step (i-iv). The input supply voltage V_{VDD} (1) is applied to 2EP130R (i). It provides the output voltage $V_{OUT1,2}$ (2) to the serial capacitor (ii). This results in the shifted input voltage V_{PRI} (3) for the transformer (iii). The transformer scales the input voltage to the secondary side as V_{SEC} (4). The last step is peak current rectification (iv) and its output voltages (5).

Full-bridge transformer driver 2EP130R

2EP130R chops the applied supply voltage, V_{VDD}, according to the configured switching frequency and duty cycle (*DC*). The output of *OUT1* is switched between *VDD* and *GND*. The same is valid for *OUT2*. However, its

switching pattern is inverted. This results in twice the amplitude of V_{VDD} across the outputs $V_{OUT1,2}$ or with a *GND* reference:

$$V_{OUT1,2} = \pm V_{VDD}$$

The duty cycle is calculated as: $DC = \frac{t_{ON1}}{t_{PER}}$ with the on duration of output 1, t_{ON1}, and the period time, t_{PER}, of the switching frequency. The duty cycle for *OUT2* always complements that of *OUT1*. The duty cycle always refers to *OUT1*.

Serial capacitor *C1*

The serial capacitor creates an offset derived from the duty cycle. The DC offset voltage, V_{C1}, is therefore an integral component for calculating output voltages. The capacitor voltage level during steady state operation is calculated as:

$$V_{C1} = V_{VDD}\left(1 - \frac{2 \cdot DC}{100\,\%}\right)$$

The offset voltage V_{C1} varies between 80% of V_{VDD} at 10% and 0% of V_{VDD} at 50% duty cycle. Since 2EP130R only allows duty cycles between 10% to 50%, the resulting offset voltage is positive according to its indicated polarity. Any waveform with a duty cycle not equal to 50% has a DC offset voltage component. The serial capacitor basically removes the direct component from the chopped supply voltage. Due to this, the asymmetric duty cycle converts the symmetric peak, $V_{OUT1,2}$, into asymmetric peak voltages:

$$V_{RPI} = \pm V_{VDD} + V_{C1}$$

The primary transformer voltage alternates between (+V_{VDD}+V_{C1}) and (-V_{VDD}+V_{C1}) due to the full-bridge output stage of 2EP130R and the aforementioned offset voltage stored within V_{C1}.

Transformer, transformer turn ratio (*TTR*), and transformer saturation

The transformer transforms the primary input voltage, V_{PRI}, according to the transformer turn ratio (*TTR*) to the secondary side. The secondary transformer voltage, V_{SEC}, is calculated as:

$$V_{SEC} = \frac{V_{PRI}}{TTR} = \pm \frac{V_{DD}}{TTR} + \frac{V_{C1}}{TTR}$$

The aforementioned V_{C1} offset voltage ensures an equal voltage * time product below and above ground potential for the primary winding. This equal voltage * time product prevents the transformer from saturating, even when driven with asymmetric peak voltages.

Peak current rectification

Due to the diodes in the peak rectification circuit, individual current paths must be considered separately. The matching voltage polarity of the secondary transformer voltage should be taken into account when calculating the expected output capacitor voltages.

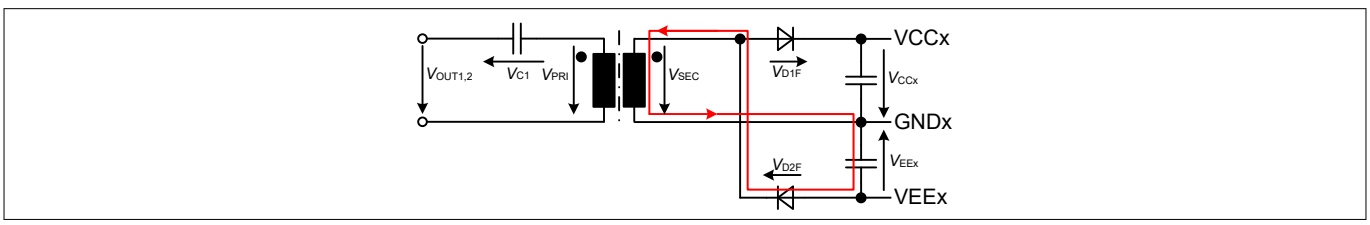

Figure 5 Current path of negative voltage rail

The current path to charge the negative voltage rail requires V_{SEC} to be in reverse polarity. The current charges the negative output voltage capacitor and closes the circuit via the diode, D2, in forward direction resulting in the V_{D2F} voltage drop.

The negative output voltage then results in: $V_{EEx} = V_{SEC(neg)} + V_{D2F}$

As the secondary transformer voltage is negative at that half-wave, the resulting output voltage is also negative, but reduced by the diode forward voltage.

The positive output voltage behaves similar to the negative output voltage.

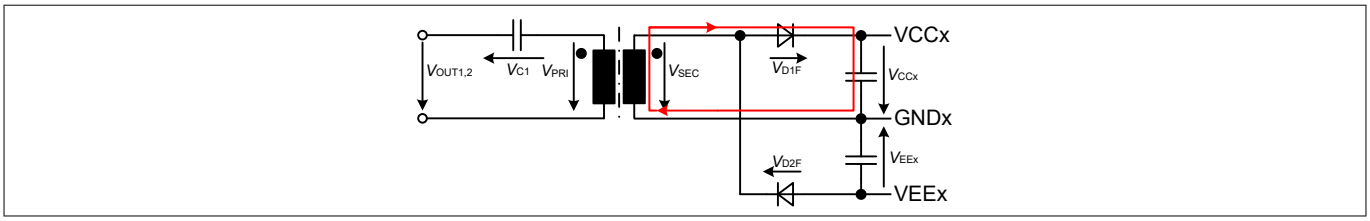

Figure 6 Current path of positive voltage rail

The current path to charge the positive voltage rail requires V_{SEC} to be in the indicated polarity (positive half-wave). The current charges the positive output voltage capacitor and closes the circuit via the diode, D1, in forward direction resulting in the V_{D1F} voltage drop.

The positive output voltage then results in: $V_{CCx} = V_{SEC(pos)} - V_{D1F}$

Both output voltages can be written as:

Assumption 1: All forward voltages are equal:

$$V_F = V_{D1F} = V_{D2F}$$

Assumption 2: Amplitudes of both the positive and negative half-waves experience the same offset:

$$V_{SEC} = \pm \frac{V_{DD}}{TTR} + \frac{V_{C1}}{TTR}$$

Positive output voltage:

$$V_{CCx} = \left(\frac{V_{DD}}{TRR} + \frac{V_{C1}}{TRR} - V_F \right)$$

Negative output voltage:

$$V_{EEx} = -\left(\frac{V_{DD}}{TRR} - \frac{V_{C1}}{TRR} - V_F \right)$$

(1)

***Note**: Equal load at positive and negative voltage rails result in asymmetric currents for positive and negative half-waves. This can result in output voltages different from the ones calculated using the equations given in this section. When designing a peak rectifier circuit with dual output rails, use the same winding polarity for both rails to ensure that the offset gets applied in the same manner.*

Inserting the V_{CI} equation into the output voltage equations results in:

Positive output voltage:

$$V_{CCx} = \frac{2 \cdot V_{VDD}}{TRR}(1 - DC) - V_F$$

Negative output voltage:

$$V_{EEx} = \frac{2 \cdot V_{VDD}}{TRR}(- DC) + V_F$$

(2)

2.2 Getting started

This section describes the default board configuration and its power up.

Default configuration for 15 V input voltage

- Dual output voltage of +18 V/-2.6 V at 120 mA maximum output current
- Transformer turn ratio (*TTR*) 1.4:1:1
- OCset level 5 (output current limit at 350 mA on equally loaded output rails)
- Switching frequency 65 kHz, duty cycle 14%, internally generated

Steps to power upEVAL-2EP130R-PR-SiC with its default configuration

1. Connect a load to the isolated transformer output terminals of *X10*/*X11* and *X20*/*X21* connectors.
   - Consider the polarities of *VCC1*/*GND1*/*VEE1* and *VCC2*/*GND2*/*VEE2*
   - The LEDs OUT1 and OUT2 also act as a minimal base load. Without external load, the output voltages will be higher than calculated in Chapter 2.5
2. Connect a 15 V positive supply voltage between *VDD* and *GND* at the corresponding terminals of the *X1*/*X2* connectors.
3. The RDY LED indicated the ready status of the 2EP130R.

After the supply voltage is applied at *VDD*, 2EP130R performs a soft start. The voltage at the isolated outputs increases and the RDY status LED lights up. If the status LED does not light up, the transformer driver is either not powered correctly, is still in start-up mode (soft-start), or is in the fault mode (overcurrent or overtemperature).

2.3 Resistor based operating parameter adjustment

2EP130R offers three input pins to configure the switching frequency, the duty cycle, and the average overcurrent protection during an operation.

- Resistor *R1* sets the overcurrent threshold at pin *OCSET*; default: *R1* = 47500 Ω, OCset level: 5
- Resistor *R2* sets the frequency at pin *FREQ/BYP*; default: *R2* = 698, switching frequency: 65 kHz
- Resistor *R3* sets the duty cycle at pin *DC*; default: *R3* = 698, duty cycle: 14%

You can use the following table to select an individual resistor value from the column **E96 series** and match it to OCSET, FREQ, and DC column values in the same row.

Table 5 Parameter adjustments of resistor value to functional value

Resistor	R1	R2	R3	Resistor	R1	R2	R3
E96 series	OCSET	FREQ	DC	E96 series	OCSET	FREQ	DC
Ω	–	kHz	%	Ω	–	kHz	%
332	1	50	10	5760	3	199	31
412	1	53	11	6980	3	213	32
499	1	57	12	8250	3	227	33
590	1	61	13	9530	4	243	34
698	1	65	14	11000	4	259	35
806	1	70	15	12700	4	277	36
931	1	74	16	14700	4	295	37
1070	1	79	17	16500	4	316	38
1210	2	85	18	18700	4	337	39
1370	2	90	19	21000	4	360	40
1540	2	97	20	23700	4	384	41
1740	2	103	21	26700	5	410	42
1960	2	110	22	30100	5	438	43
2210	2	118	23	34000	5	468	44
2490	2	126	24	38300	5	500	45
2800	2	134	25	42200	5	534	46

(table continues...)

Table 5 (continued) Parameter adjustments of resistor value to functional value

Resistor	R1	R2	R3	Resistor	R1	R2	R3
E96 series	OCSET	FREQ	DC	E96 series	OCSET	FREQ	DC
3160	3	143	26	47500	5	570	47
3480	3	153	27	52300	5	609	48
3920	3	163	28	57600	5	651	49
4320	3	175	29	63400	5	695	50
4750	3	186	30				

2.4 Bypass mode operation

2EP130R supports bypass mode operation. In this mode, 2EP130R follows an externally applied pulse width modulation (PWM) signal at *FREQ/BYP* pin for frequency and duty cycle during operation.

During start-up, the IC follows the internal soft start sequence. Therefore, the frequency and individual pulse length deviate from the externally applied PWM signal during the soft start. The applied switching frequency should be kept constant during start-up. The transformer driver syncs up with that frequency in the final moments of the start-up sequence. For further information, see EiceDRIVER™ 2EP1xxR family datasheet.

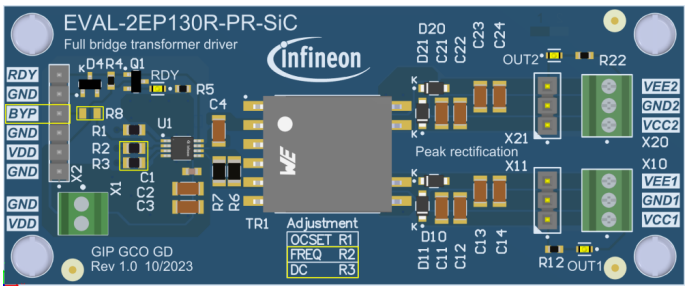

Figure 7 Modification for bypass mode operation

Modify the default assembly to operate the evaluation board in bypass mode:

- Resistor *R3* at *DC* pin: change to 0 Ω to enable bypass mode
- Resistor *R2* at *FREQ/BYP* pin: remove resistor
- Resistor *R8*: assemble 0 Ω resistor to connect the *X2.BYP* pin to the *FREQ/BYP* pin

Ensure that the external frequency stays within the 2EP130R frequency an duty cycle range.

2.5 Use case: SiC MOSFET supply example

The calculations in this section are based on the equations from Chapter 2.1. They have been re-arranged to calculate the duty cycle and transformer turn ratio (*TTR*) from the requested voltages. The purpose for this example is to get an output voltage suitable for SiC MOSFETs.

Application parameters (input)

- Input supply voltage for 2EP130R: V_{DD} = 15 V
- Nominal target positive output voltage after peak rectification: V_{CCx} = 18 V
- Nominal target negative output voltage after peak rectification: V_{EEx} = *-2.5 V*
- Expected diode forward voltage: V_F = 0.4 V

The output voltages provided here are considered nominal when increase in light load output voltage and drop in load-dependent output voltage are negligible. For the transformer suggested in this example, the nominal load is approximately 15 mA. To consider the impact of the diode forward voltage on the output voltages a more accurate calculation of parameters is required.

Calculating and selecting the duty cycle

To calculate the duty cycle (*DC*) for 2EPxxR, the positive output voltage V_{CCx} should be put relative to the total output voltage. The voltage at the transformer should be one forward voltage drop higher then each of the expected output voltages. The whole value then needs to be subtracted from 1 to get the duty cycle for *OUT1*:

$$DC = 1 - \frac{V_{CCx} + V_F}{2 \cdot V_F + V_{CCx} - V_{EEx}}$$

$$DC = 1 - \frac{18\,V + 0.4\,V}{2 \cdot 0.4\,V + 18\,V - (-2.5\,V)}$$

$$DC = 0.136 \Rightarrow DC_{selected} = 14\,\%$$

The percentage value needs to be a whole number to be compatible with 2EP. The selected duty cycle, in this example, is rounded to 14%. According to the resistor selection table given in the 2EP1xxR datasheet, this duty cycle setting requires a resistor value of 698 Ω at the *DC* pin. It introduces a slight offset in the actual output voltage compared to the target value.

***Note**: 2EP1xxR supports duty cycles in the range of 10% and 50%.*

Calculating and selecting the transformer turn ratio

To calculate the transformer turn ratio (*TTR*), the total primary transformer voltage needs to be put relative to the total output voltage of the transformer on the secondary side as required by the application. As 2EP1xxR is a full-bridge transformer driver, the total voltage at the primary transformer winding is twice the input supply voltage of 2EP1xxR. The serial capacitor between 2EP1xxR and the transformer does not influence the total input voltage of the transformer. Its offset is applied to both polarities so that the absolute voltage remains constant:

$$TTR = \frac{2 \cdot V_{DD}}{2 \cdot V_F + V_{CCx} - V_{EEx}}$$

$$TRR = \frac{2 \cdot 15\,V}{2 \cdot 0.4\,V + 18\,V - (-2.5\,V)}$$

$$TTR = 1.41 \Rightarrow TTR_{selected} = 1.4$$

In this example, the calculated transformer turn ratio is very close to that of the Würth Elektronik transformer (part number 750319377) that has a transformer turn ratio of 1.4:1. The calculation and selection of a matching transformer again introduces an offset from the target values. It is therefore, recommended that the selection be verified as the last step.

Verifying the selection

After all required parameters are identified and matched to their components, the resulting output voltage can be calculated and compared to the target voltages:

$$V_{CC} = \frac{2 \cdot V_{DD} \cdot (1 - DC_{selected})}{TRR_{selected}} - V_F \Rightarrow V_{CC} = 18.03\,V$$

$$V_{EE} = \frac{2 \cdot V_{DD} \cdot (-DC_{selected})}{TRR_{selected}} + V_F \Rightarrow V_{EE} = -2.60\,V$$

In this example, the output voltages match with the target values quite well and only deviate by 0.2% for the positive and 4% for the negative output voltage. Considering that 2EP1xxR is an open loop transformer driver, the actual output voltages also depend on the stability of the input voltages and the load condition of these output voltages.

3 System design

3.1 Schematics

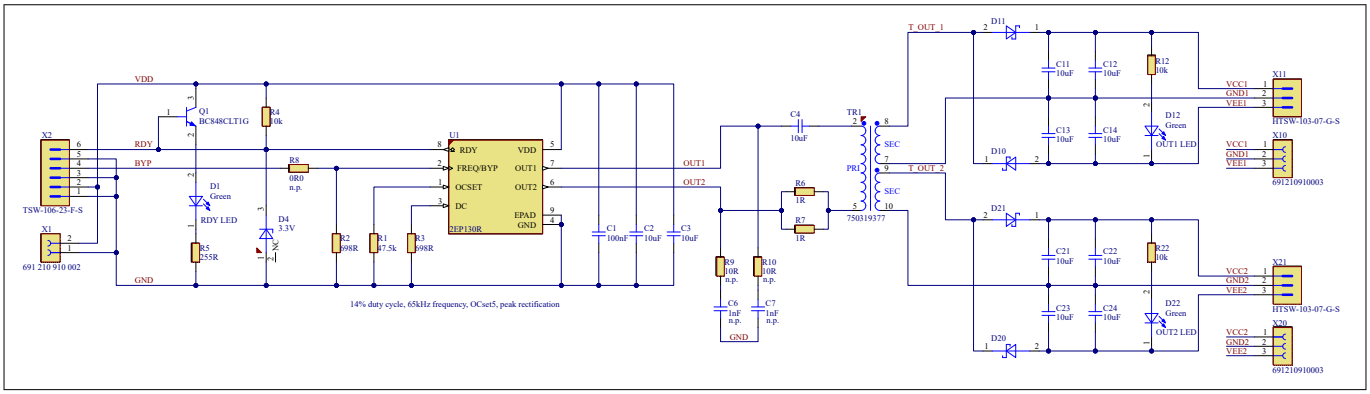

Figure 8 Schematic

The schematic uses default resistor values for average overcurrent setting level 5 and a target switching frequency of 65 kHz. With the transformer turn ratio of 1.4:1 and a duty cycle of 14%, an input voltage of 15 V will result in a positive output voltage of approximately 18 V and a negative output voltage of -2.6 V.

3.2 Layout

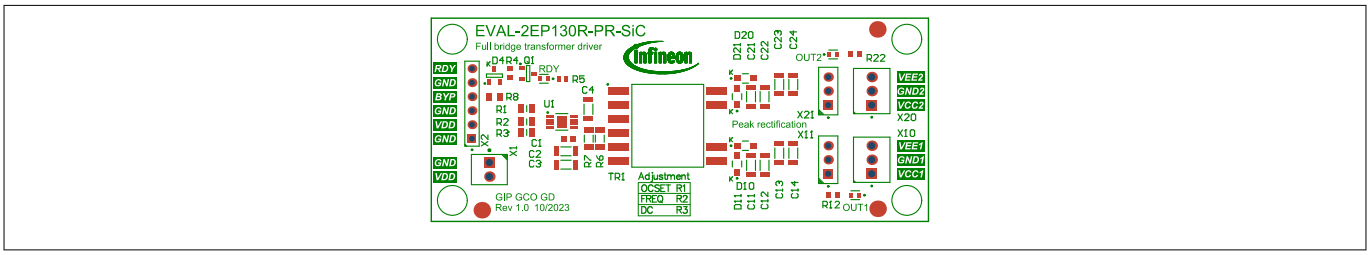

Figure 9 Component side assembly

The EVAL-2EP130R-PR-SiC evaluation board has an approximate size of 91 × 37 mm^2. The two-layer PCB uses a standard copper thickness of 1 oz. The top layer is used for routing, the bottom layer mainly consists of three GND planes. A single layer design is possible.

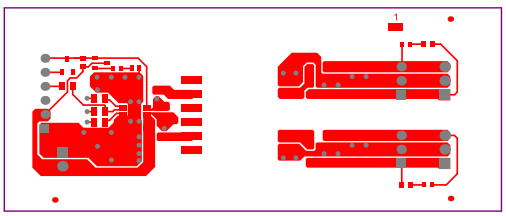

Figure 10 Top layer

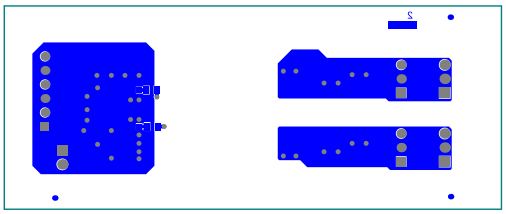

Figure 11 Bottom layer

Figure 12 Solder side assembly

3.3 Bill of material

The complete bill of material is available in the download section of Infineon's homepage. Login credentials are required to download this material.

Table 6 BOM of the most important parts of the evaluation board

S. No.	Ref Designator	Description	Manufacturer	Manufacturer P/N	Populated
1	R1	RES SMD 47.5 kΩ 125mW 1% 0805	Vishay	CRCW080547K5FK	Yes
1	R2	RES SMD 698Ω 125mW 1% 0805	Vishay	CRCW0805698RFK	Yes
1	R3	RES SMD 698Ω 125mW 1% 0805	Vishay	CRCW0805698RFK	Yes
1	TR1	Transformer, 1mH, Turn Ratio 1.4:1	Wurth Elektronik	750319377 r00	Yes
1	U1	Full-bridge transformer driver for IGBT and SiC MOSFET gate driver supply	Infineon	2EP130R	Yes

3.4 Connector details

Table 7 Connector X1 - Input supply (alternate connector)

PIN	Label	Function
X1.1	GND	Primary input ground reference
X1.2	VDD	Input supply voltage for transformer driver 2EP130R

Table 8 Connector X2 - Input side signals and supply

PIN	Label	Function
X2.1	GND	Primary input ground reference
X2.2	VDD	Input supply voltage for transformer driver 2EP130R
X2.3	GND	Primary input ground reference
X2.4	BYP	External PWM input pin for bypass operation mode
X2.5	GND	Primary input ground reference
X2.6	RDY	Ready status output pin, open drain

Table 9 Connectors X10 and X11 - Output supply rail 1

PIN	Label	Function
X10.1, *X11.1*	VCC1	Positive supply voltage output rail 1
X10.2, *X11.2*	GND1	Ground reference output rail 1
X10.3, *X11.3*	VEE1	Negative supply voltage output rail 1

Table 10 Connectors X20 and X21 - Output supply rail 2

PIN	Label	Function
X20.1, *X21.1*	VCC2	Positive supply voltage output rail 2
X20.2, *X21.2*	GND2	Ground reference output rail 2
X20.3, *X21.3*	VEE2	Negative supply voltage output rail 2

4 System performance

This section shows measurement results of the EVAL-2EP130R-PR-SiC evaluation board on efficiency, switching wave forms, start-up behavior of output voltages, and output voltage ripple.

Efficiency

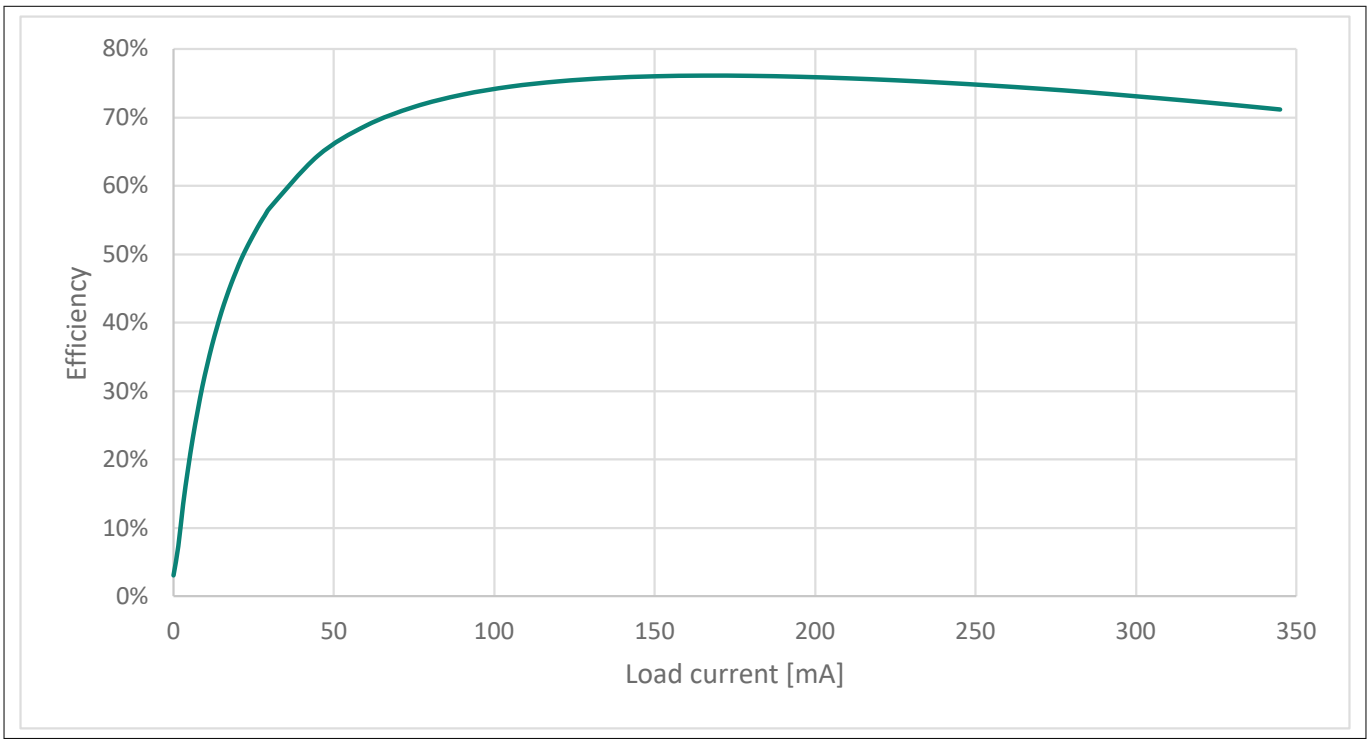

Figure 13 Measuring efficiency using 15 V input voltage and the WE 750319377 transformer

The efficiency measurement records the output voltages and currents and puts them relative to the 2EP input voltage and current during a steady state operation. This measurement was repeated for each individual load current point and drawn on this graph. The efficiency curve varies under different operating conditions such as input voltage, switching frequency, duty cycle and component selection of the transformer. This measurement was performed at 15 V, 80 kHz, 12% duty cycle, and using Würth Elektronik's transformer 750319377.

Switching waveform at start-up

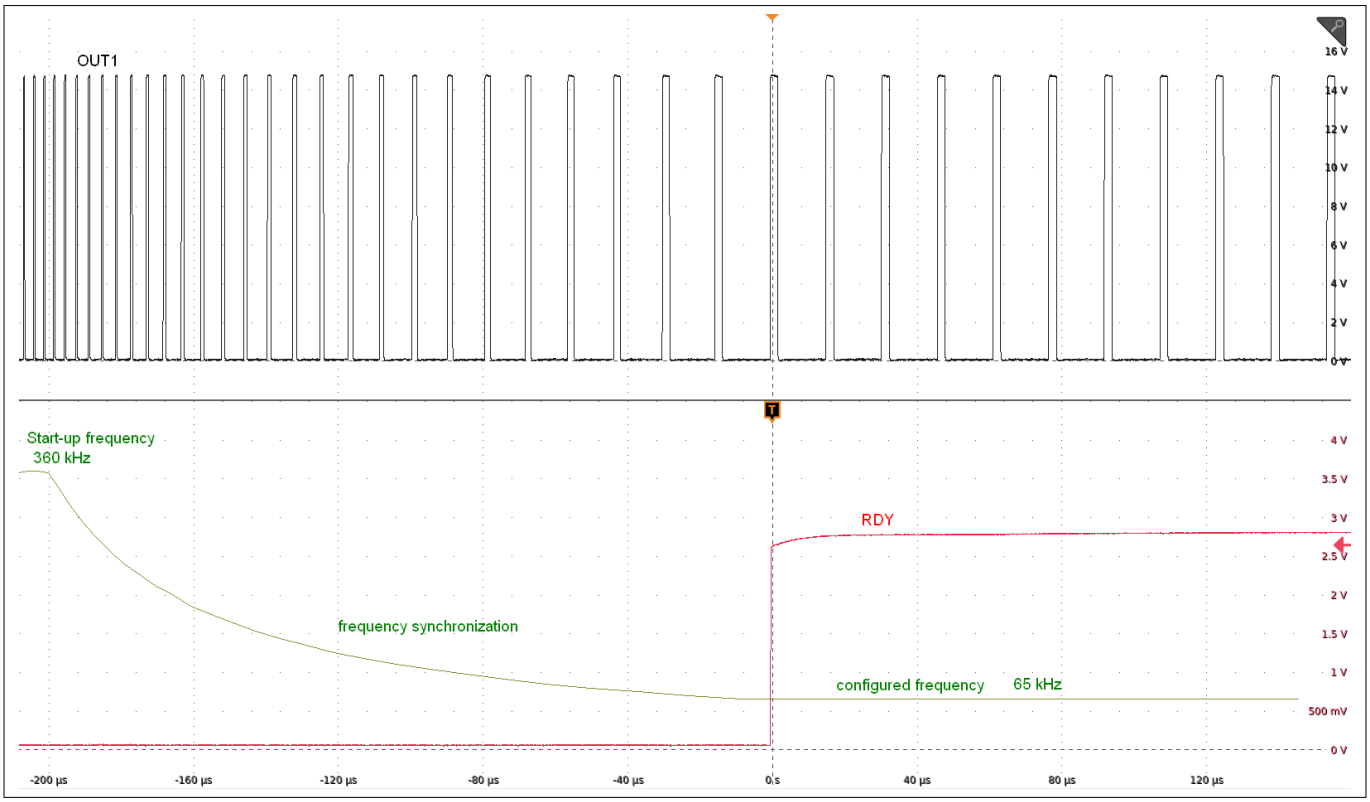

Figure 14 *OUT1* switching waveform

The upper diagram shows the *OUT1* switching waveform. From left to right, 2EP1xxR is operating in the start-up peak current mode. When it reaches the target duty cycle without triggering the peak current limits, it synchronizes the switching frequency with the configured frequency. On reaching the target frequency, 2EP1xxR releases the *RDY* pin to indicate a successful start-up.

Start-up behavior of the output voltages

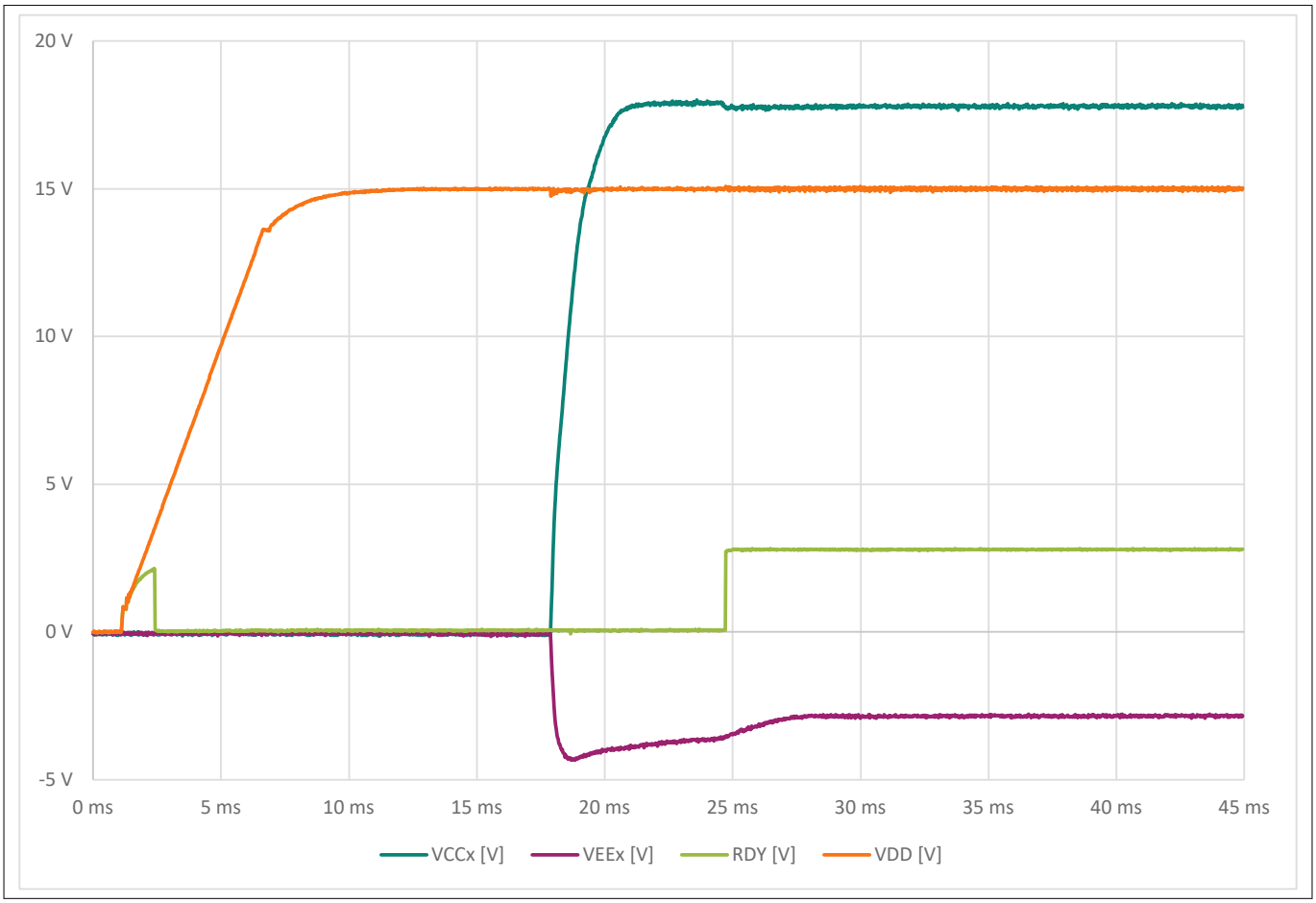

Figure 15 Start-up behavior

This diagram shows the input voltage ramp up at *VDD* together with the generated output voltages, *VCCX* and *VEEX*, and the *RDY* signal of the evaluation board.

The *RDY* signal briefly follows the input supply voltage, *VDD,* until the internal under voltage lockout (UVLO) circuit activates and pulls the *RDY* signal down to *GND* level. 2EP1xxR releases the *RDY* signal after the internal start-up phase.

4 System performance

Output voltage ripple

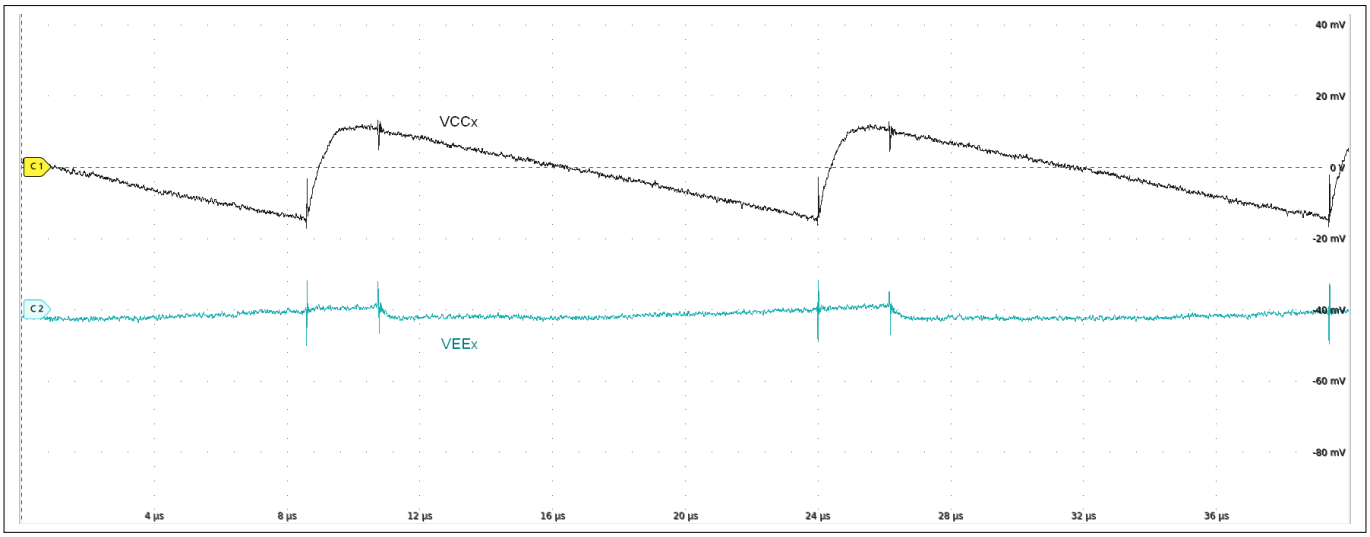

Figure 16 *VCCx* and *VEEx* output voltage ripple

The output voltage ripple of *VCCx* has a higher amplitude due to the selected duty cycle. At a constant load on both output levels, 2EP1xxR needs to recharge the output capacitor for *VCCx* within a shorter period of time compared to the output capacitor for *VEEx*. This measurement shows the output ripple for a load current of approximately 30 mA.

5 Additional information

Table 11 Orderable part numbers

Evaluation board	OPN	Description
EVAL-2EP130R-PR	EVAL2EP130RPRTOBO1	2EP130R board with peak rectification and 3 transformers
EVAL-2EP130R-PR-SiC	EVAL2EP130RPRSICTOBO1	2EP130R board with peak rectification for SiC MOSFETs
EVAL-2EP130R-VD	EVAL2EP130RVDTOBO1	2EP130R board with voltage doubler for IGBTs

Table 12 Compatible gate driver evaluation boards

Evaluation board	OPN	Description
EVAL-1ED3121MX12H	EVAL1ED3121MX12HTOBO1	1ED3121MX12H board - 2300 V, 5.5 A, 5.7 kV (rms) with separate output
EVAL-1ED3122MX12H	EVAL1ED3122MX12HTOBO1	1ED3122MX12H board - 2300 V, 10 A, 5.7 kV (rms) with active Miller clamp
EVAL-1ED3124MX12H	EVAL1ED3124MX12HTOBO1	1ED3124MX12H board - 2300 V, 14 A, 5.7 kV (rms) with separate output
EVAL-1ED3142MU12F-SIC	EVAL1ED3142MU12FSICTOBO1	1ED3142MU12F board - 2300 V, 6.5 A, 3 kV (rms) with separate output
EVAL-1ED3241MC12H	EVAL1ED3241MC12HTOBO1	1ED3241MC12H board - 2300 V, 18 A, 5.7 kV (rms) with two-level slew-rate control
EVAL-1ED3251MC12H	EVAL1ED3251MC12HTOBO1	1ED3251MC12H board - 2300 V, 18 A, 5.7 kV (rms) with slew-rate control and clamp
EVAL-1ED3321MC12N	EVAL1ED3321MC12NTOBO1	1ED3321MC12N board - 2300 V, 8.5 A, 5.7 kV (rms) with DESAT and Soft-off
EVAL-1ED3491MX12M	EVAL1ED3491MX12MTOBO1	1ED3491MX12M board - 2300 V, 9 A, 5.7 kV (rms) with adjustable DESAT and Soft-off
EVAL-1ED3890MX12M	EVAL1ED3890MX12MTOBO1	1ED3890MX12M board - 2300 V, 9 A, 5.7 kV (rms) with I2C configurable behavior

Revision history

Document version	Date of release	Description of changes
v1.00	2024-02-26	• initial version
		•

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