

**PROFET™ +2 12V**  
**Smart high-side power switch**

**Features**

- High-side switch with diagnosis and embedded protection
- Part of PROFET™+2 12V family
- Switch ON capability while inverse current condition (InverseON)
- Capacitive load switching mode
- Green product (RoHS compliant)

**Potential applications**

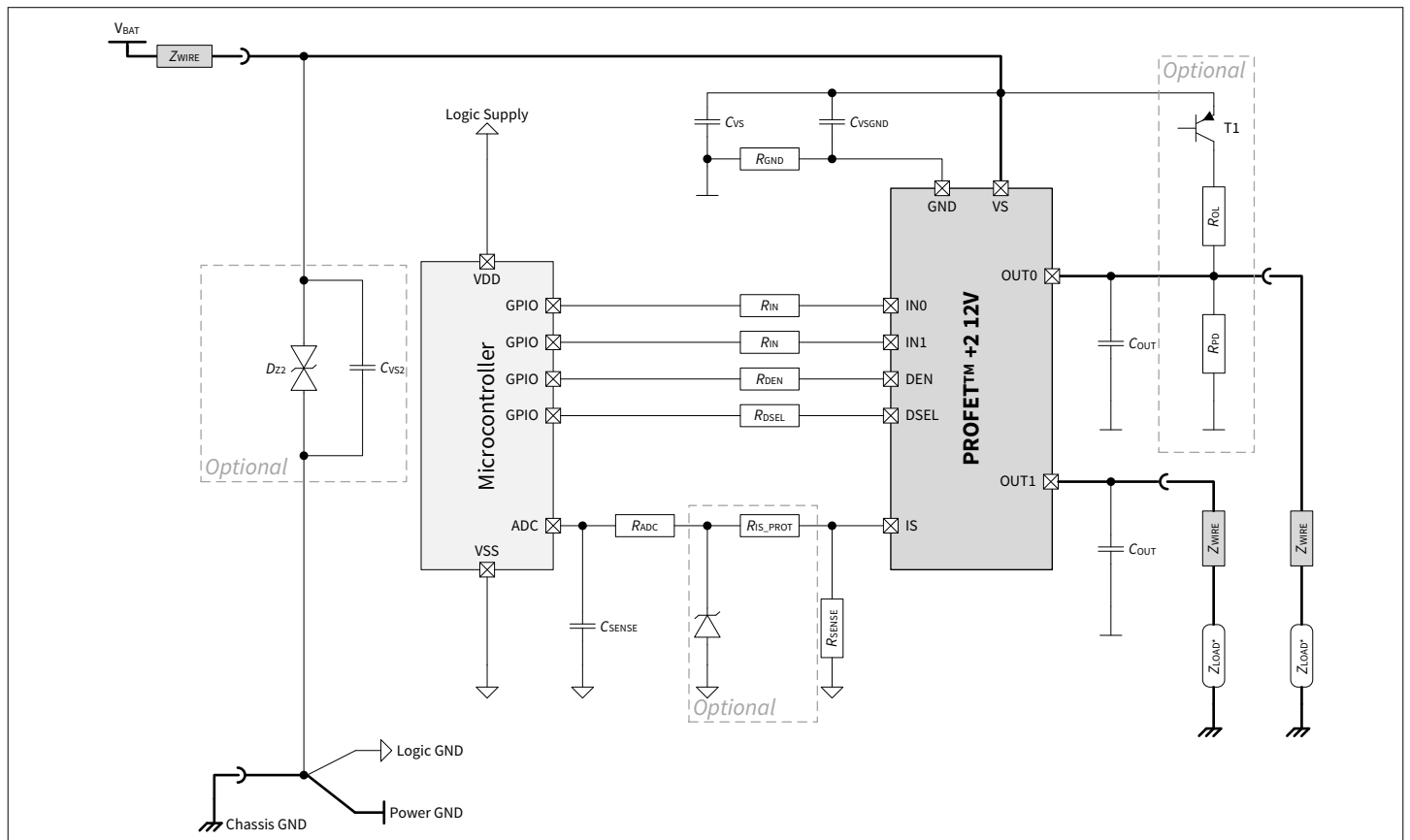
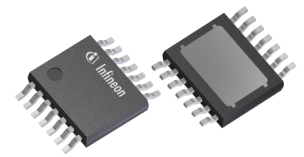
- Replaces electromechanical relays, fuses and discrete circuits
- Protection of system supply
- Main switch for ECU power supply
- Suitable for driving resistive, inductive and capacitive loads
- Suitable for driving heating elements

**Product validation**

Qualified for automotive applications.  
 Product validation according to AEC-Q100, Grade 1.

**Description**

The BTS7090-2EPL is a Smart High Side Switch, providing protection functions and diagnosis capabilities. The device offers current limitation and has a capacitive load switching mode implemented to charge capacitors. It is integrated in SMART7 technology.



Further information in [Chapter 9](#)

**Description**

<b>Parameter</b>	<b>Symbol</b>	<b>Values</b>
Minimum operating voltage	$V_{S(OP)}$	3 V
Minimum operating voltage (cranking)	$V_{S(UV)}$	2.7 V
Maximum operating voltage	$V_S$	28 V
Minimum overvoltage protection ( $T_J \geq 25^\circ\text{C}$ )	$V_{DS(CLAMP)_25}$	35 V
Maximum current in sleep mode ( $T_J \leq 85^\circ\text{C}$ )	$I_{VS(SLEEP)_85}$	0.5 $\mu\text{A}$
Maximum operative current	$I_{GND(ACTIVE)}$	4.5 mA
Typical ON-state resistance ( $T_J = 25^\circ\text{C}$ )	$R_{DS(ON)_25}$	90 m $\Omega$
Maximum ON-state resistance ( $T_J = 150^\circ\text{C}$ )	$R_{DS(ON)_150}$	180 m $\Omega$
Nominal load current ( $T_A = 85^\circ\text{C}$ )	$I_{L(NOM)}$	2 A
Typical current sense ratio at $I_L = I_{L(NOM)}$	$k_{ILIS}$	1000
Overcurrent limitation	$I_{LIM}$	4.7 A

**Diagnostic features**

- Proportional load current sense
- Open load in ON and OFF state
- Short circuit to ground and battery

**Protection features**

- Absolute and dynamic temperature protection with restart control
- Overcurrent limitation
- Overvoltage protection

<b>Type</b>	<b>Package</b>	<b>Marking</b>
BTS7090-2EPL	PG-TSDSO-14	7090-2AL

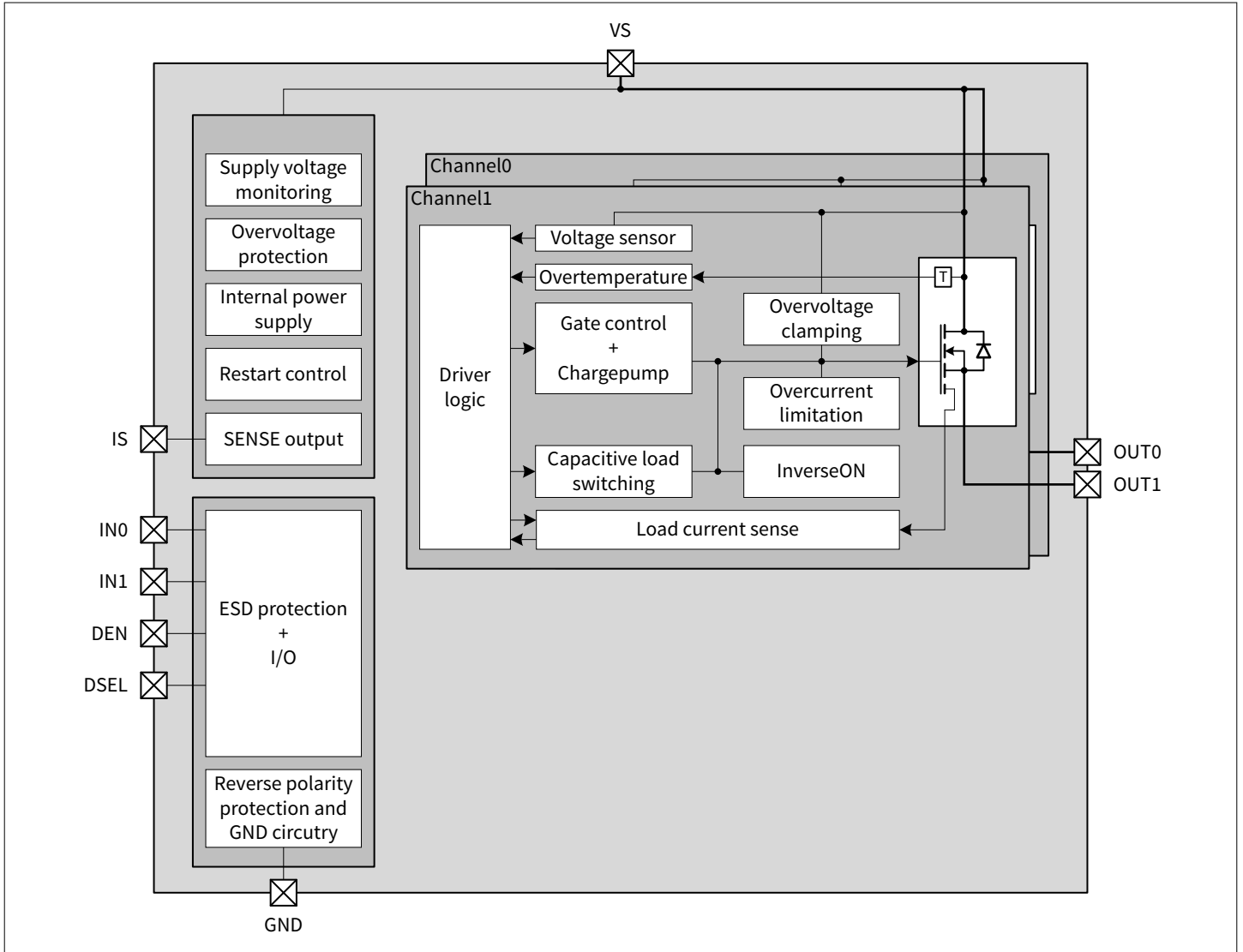
## Table of contents

	<b>Table of contents</b> .....	3
<b>1</b>	<b>Block diagram and terms</b> .....	5
1.1	Block diagram .....	5
1.2	Terms .....	6
<b>2</b>	<b>Pin configuration</b> .....	7
2.1	Pin assignment .....	7
2.2	Pin definitions and functions .....	7
<b>3</b>	<b>General product characteristics</b> .....	8
3.1	Absolute maximum ratings .....	8
3.2	Functional range .....	10
3.3	Thermal resistance .....	10
3.3.1	PCB setup .....	11
3.3.2	Thermal impedance .....	12
<b>4</b>	<b>I/O pins</b> .....	14
4.1	Digital I/O pins .....	14
4.1.1	Input pins .....	14
4.1.2	Diagnosis pins .....	15
4.2	Electrical characteristics I/O pins .....	15
<b>5</b>	<b>Power Supply</b> .....	16
5.1	Operation modes and transitions .....	16
5.1.1	Operation modes .....	16
5.1.1.1	Unsupplied .....	17
5.1.1.2	Power-up .....	17
5.1.1.3	Sleep .....	17
5.1.1.4	Inactive with diagnosis .....	17
5.1.1.5	Active with diagnosis .....	17
5.1.1.6	Active without diagnosis .....	17
5.1.1.7	Capacitive load switching mode with diagnosis .....	17
5.1.1.8	Capacitive load switching mode without diagnosis .....	18
5.2	Undervoltage on VS .....	18
5.3	Electrical characteristics power supply .....	18
<b>6</b>	<b>Power Stage</b> .....	20
6.1	Output ON-state resistance .....	20
6.2	Switching loads .....	20
6.2.1	Switching resistive loads .....	20
6.2.2	Switching inductive loads .....	21
6.2.3	Switching capacitive loads .....	22
6.3	Advanced switching characteristics .....	23

6.3.1	Inverse current behavior .....	23
6.4	Electrical characteristics power stage .....	24
<b>7</b>	<b>Protection</b> .....	<b>28</b>
7.1	Overcurrent protection .....	28
7.1.1	Overcurrent threshold .....	28
7.2	Overtemperature protection .....	28
7.3	Protection and diagnosis in case of fault .....	29
7.3.1	Retry strategy .....	29
7.4	Additional protection .....	31
7.4.1	Reverse polarity protection .....	31
7.4.2	Overvoltage protection .....	31
7.4.3	Loss of battery and loss of load .....	31
7.4.4	Loss of ground .....	32
7.5	Electrical characteristics protection .....	32
<b>8</b>	<b>Diagnosis</b> .....	<b>34</b>
8.1	Overview .....	34
8.1.1	SENSE signal truth table .....	35
8.2	Diagnosis in ON state .....	36
8.2.1	Current sense (KILIS) .....	36
8.2.2	Fault current (IIS(FAULT)) .....	36
8.3	Diagnosis in OFF State .....	38
8.3.1	Open load current .....	38
8.4	SENSE timings .....	39
8.5	Electrical characteristics diagnosis .....	40
<b>9</b>	<b>Application information</b> .....	<b>44</b>
<b>10</b>	<b>Package outlines</b> .....	<b>46</b>
<b>11</b>	<b>Revision history</b> .....	<b>47</b>
	<b>Disclaimer</b> .....	<b>48</b>

# 1 Block diagram and terms

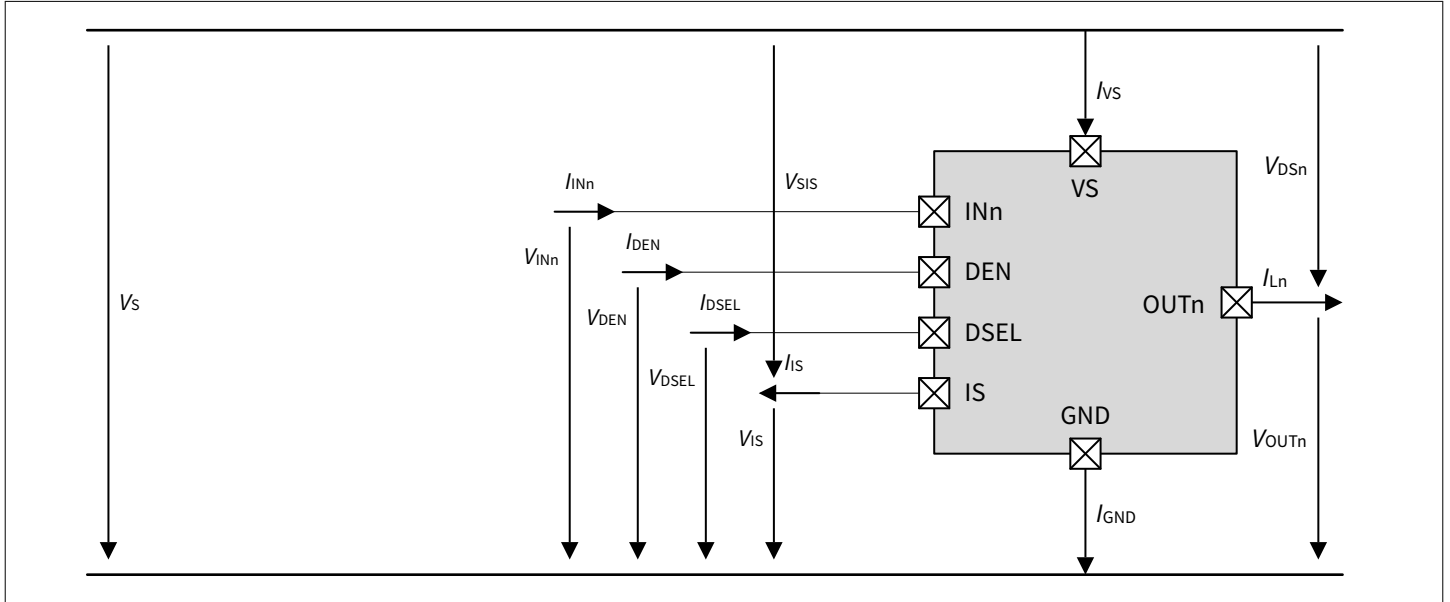
## 1.1 Block diagram



**Figure 2** Block diagram of BTS7090-2EPL

## 1.2 Terms

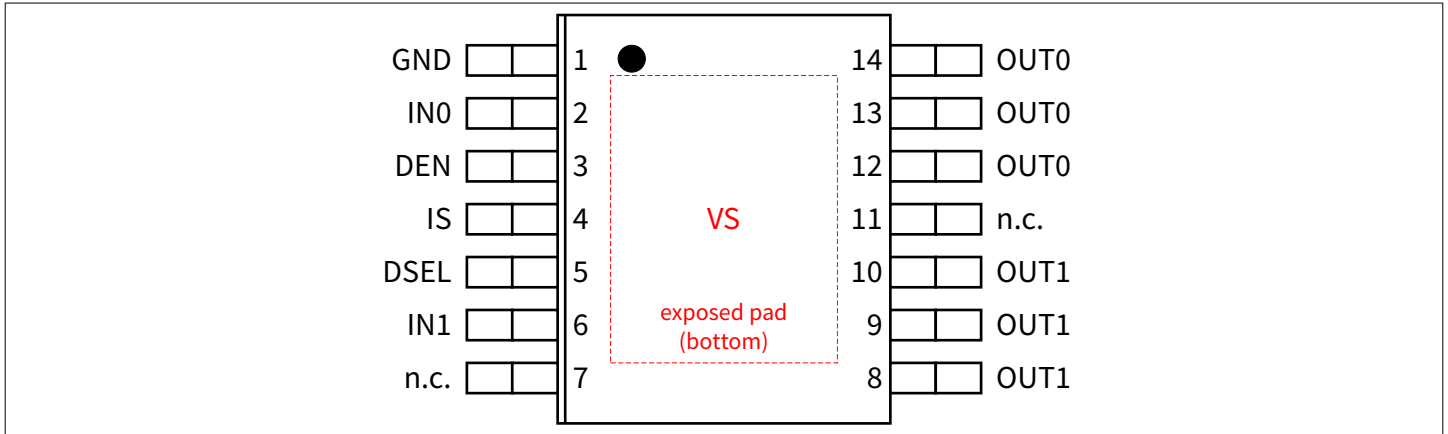
Figure 3 shows all terms used in this data sheet, with associated convention for positive values.



**Figure 3** Voltage and current convention

## 2 Pin configuration

### 2.1 Pin assignment



**Figure 4** Pin configuration

### 2.2 Pin definitions and functions

**Table 1** Pin definition

Pin	Symbol	Function
EP	VS (exposed pad)	<b>Supply Voltage</b> Battery voltage
1	GND	<b>Ground</b> Ground connection for the internal logic
2, 6	INn	<b>Input Channel n</b> Digital signal to switch ON channel n ("high" active) If not used: Connect with a 10kΩ resistor either to GND pin or to module ground
3	DEN	<b>Diagnostic Enable</b> Digital signal to enable device diagnosis ("high" active) and to clear the protection counter of channel selected with DSEL pin. If not used: Connect with a 10kΩ resistor either to GND pin or to module ground
4	IS	<b>SENSE current output</b> Analog/digital signal for diagnosis If not used: Left open
5	DSEL	<b>Diagnosis Selection</b> Digital signal to toggle between the channels. If not used: Connect with a 10kΩ resistor either to GND pin or to module ground
7, 11	n.c.	Not connected, internally not bonded
8-10, 12-14	OUTn	<b>Output n</b> Protected high-side power output channel n <sup>1)</sup>

1) All output pins of the channel must be connected together on the PCB. All pins of the output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

### 3 General product characteristics

#### 3.1 Absolute maximum ratings

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

**Table 2 Absolute maximum ratings**

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
<b>Supply pins</b>							
Power supply voltage	$V_S$	-0.3	-	28	V	2) -	PRQ-34
Load dump voltage	$V_{\text{BAT(LD)}}$	-	-	35	V	2) suppressed load dump acc. to ISO16750-2 (2010). $R_i = 2 \Omega$	PRQ-36
Supply voltage for short circuit protection	$V_{\text{BAT(SC)}}$	0	-	24	V	2) Setup acc. to AEC-Q100-012	PRQ-38
Reverse polarity voltage	$-V_{\text{BAT(REV)}}$	-	-	16	V	2) $t \leq 2 \text{ min}$ $T_A = +25^\circ\text{C}$ Setup as described in <a href="#">Chapter 9</a>	PRQ-40
Current through GND pin	$I_{\text{GND}}$	-50	-	50	mA	2) $R_{\text{GND}}$ according to <a href="#">Chapter 9</a>	PRQ-44

#### Logic & control pins (Digital Input = DI)

##### DI = INN, DEN, DSEL

Current through DI pin	$I_{\text{DI}}$	-1	-	2	mA	2) 1)	PRQ-47
Current through DI pin - Reverse battery condition	$I_{\text{DI(REV)}}$	-1	-	10	mA	2) 1) $t \leq 2 \text{ min}$	PRQ-48

##### IS pin

Voltage at IS pin	$V_{\text{IS}}$	-1.5	-	$V_S$	V	2) $I_{\text{IS}} = 10 \mu\text{A}$	PRQ-50
Current through IS Pin	$I_{\text{IS}}$	-25	-	$I_{\text{IS(SAT),M AX}}$	mA	2) -	PRQ-52

#### Temperatures

Junction temperature	$T_J$	-40	-	+150	$^\circ\text{C}$	2) -	PRQ-53
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(table continues...)



**Table 2** (continued) **Absolute maximum ratings**

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Storage temperature	$T_{STG}$	-55	-	+150	°C	2) -	PRQ-54
<b>ESD susceptibility</b>							
ESD Susceptibility all pins (HBM)	$V_{ESD(HBM)}$	-2	-	2	kV	2) HBM <sup>3)</sup>	PRQ-55
ESD Susceptibility OUTn vs GND and VS connected (HBM)	$V_{ESD(HBM)_OUT}$	-4	-	4	kV	2) HBM <sup>3)</sup>	PRQ-56
ESD Susceptibility all pins (CDM)	$V_{ESD(CDM)}$	-500	-	500	V	2) CDM <sup>4)</sup>	PRQ-57
ESD Susceptibility corner pins (CDM) - (pins 1, 7, 8, 14)	$V_{ESD(CDM)_CRN}$	-750	-	750	V	2) CDM <sup>4)</sup>	PRQ-58
<b>Power stage</b>							
Maximum energy dissipation - single pulse	$E_{AS}$	-	-	6.5	mJ	2) $I_L = 2 \cdot I_{L(NOM)}$ $T_{J(0)} = 150^\circ\text{C}$ $V_S = 28\text{ V}$	PRQ-63
Maximum energy dissipation - repetitive pulse	$E_{AR}$	-	-	1.5	mJ	2) $I_L = I_{L(NOM)}$ $T_{J(0)} = 85^\circ\text{C}$ $V_S = 13.5\text{ V}$ 1M cycles	PRQ-64
Load current	$ I_L $	-	-	$I_{LIM,MAX}$	A	2) -	PRQ-65

- 1) Maximum  $V_{DI}$  to be considered for Latch-Up tests: 5.5 V
- 2) Not subject to production test - specified by design
- 3) ESD susceptibility, Human Body Model "HBM", according to AEC Q100-002
- 4) ESD susceptibility, Charged Device Model "CDM", according to AEC Q100-011

**Notes**

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

## 3.2 Functional range

**Table 3** Functional range

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply voltage range for normal operation	$V_{S(NOR)}$	4	13.5	20	V	1) –	PRQ-66
Lower extended supply voltage range for operation (normal)	$V_{S(EXT,LOW)}$	2.7	–	4	V	1) 2) 3) (parameter deviations possible)	PRQ-67
Upper extended supply voltage range for operation	$V_{S(EXT,UP)}$	20	–	28	V	1) 3) (parameter deviations possible)	PRQ-68
Junction temperature	$T_J$	-40	–	+150	°C	1) –	PRQ-69

1) Not subject to production test - specified by design

2) In case of  $V_S$  voltage decreasing refer to the maximum voltage of  $V_{S(UV)}$ , in case of  $V_S$  voltage increasing refer to the maximum voltage of  $V_{S(OP)}$

3) Protection functions still operative

### Note

Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified by the conditions given in the Electrical Characteristics tables.

## 3.3 Thermal resistance

**Table 4** Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal characterization parameter junction-top	$\Psi_{JTOP}$	–	7	11.8	K/W	1) 2)	PRQ-74
Thermal resistance junction-to-case	$R_{thJC}$	–	7.6	12.9	K/W	1) 2) simulated at exposed pad	PRQ-71
Thermal resistance junction-to-ambient	$R_{thJA}$	–	38	–	K/W	1) 2)	PRQ-72

1) Not subject to production test - specified by design

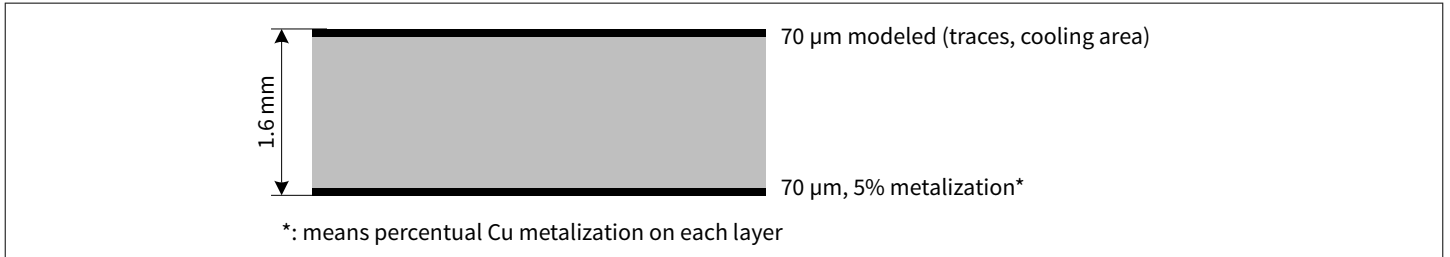
**3 General product characteristics**

- 2) According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Simulation done at  $T_A = 105^\circ\text{C}$ ,  $P_{\text{DISSIPATION}} = 1 \text{ W}$

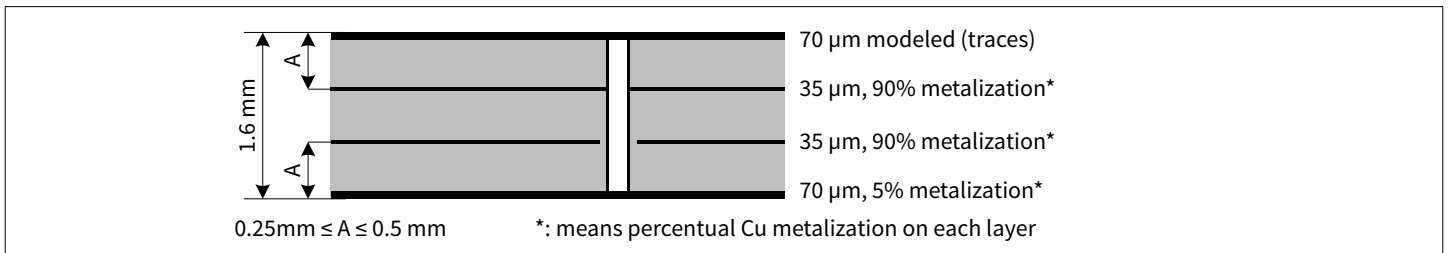
**Note**

This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

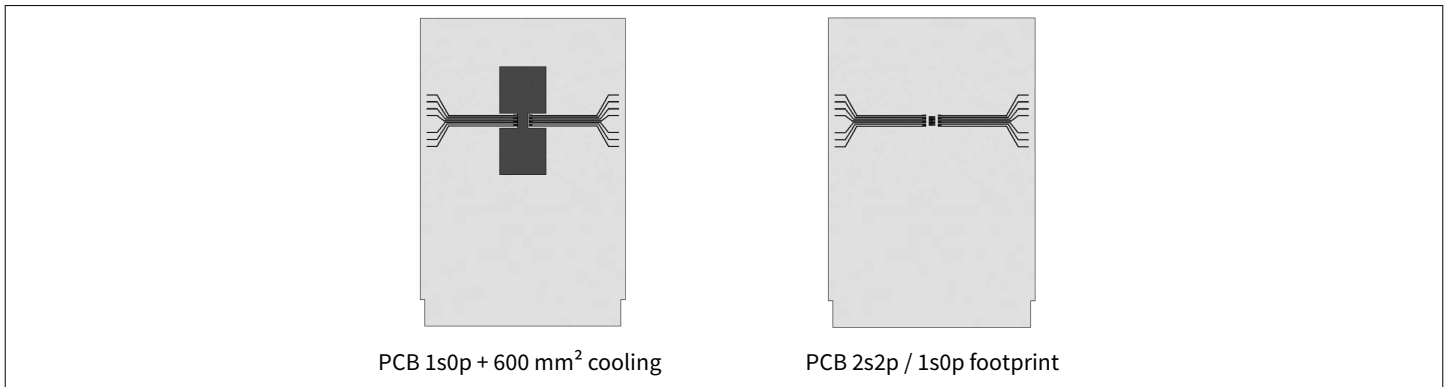
**3.3.1 PCB setup**



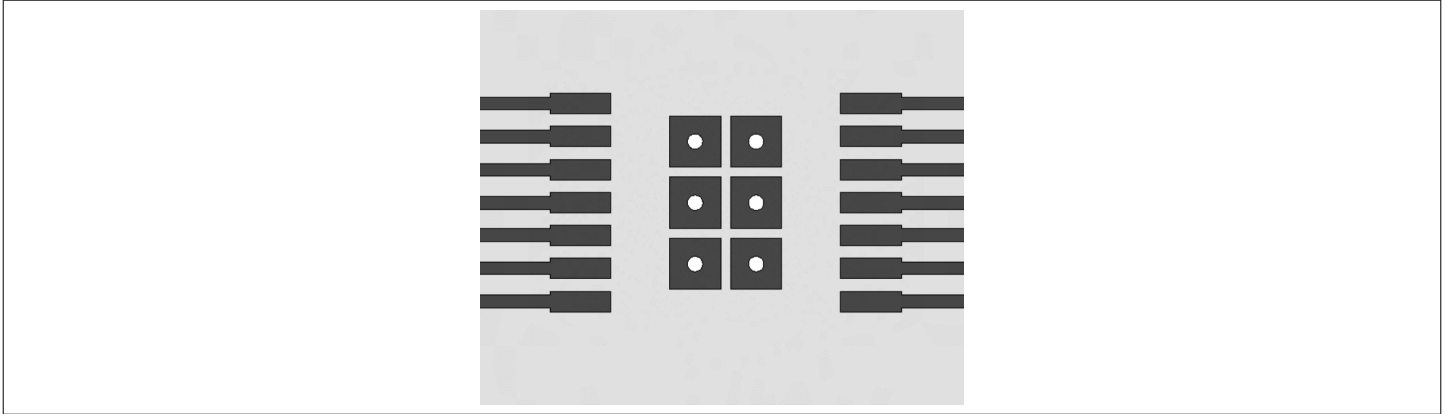
**Figure 5 1s0p PCB cross section**



**Figure 6 2s2p PCB cross section**

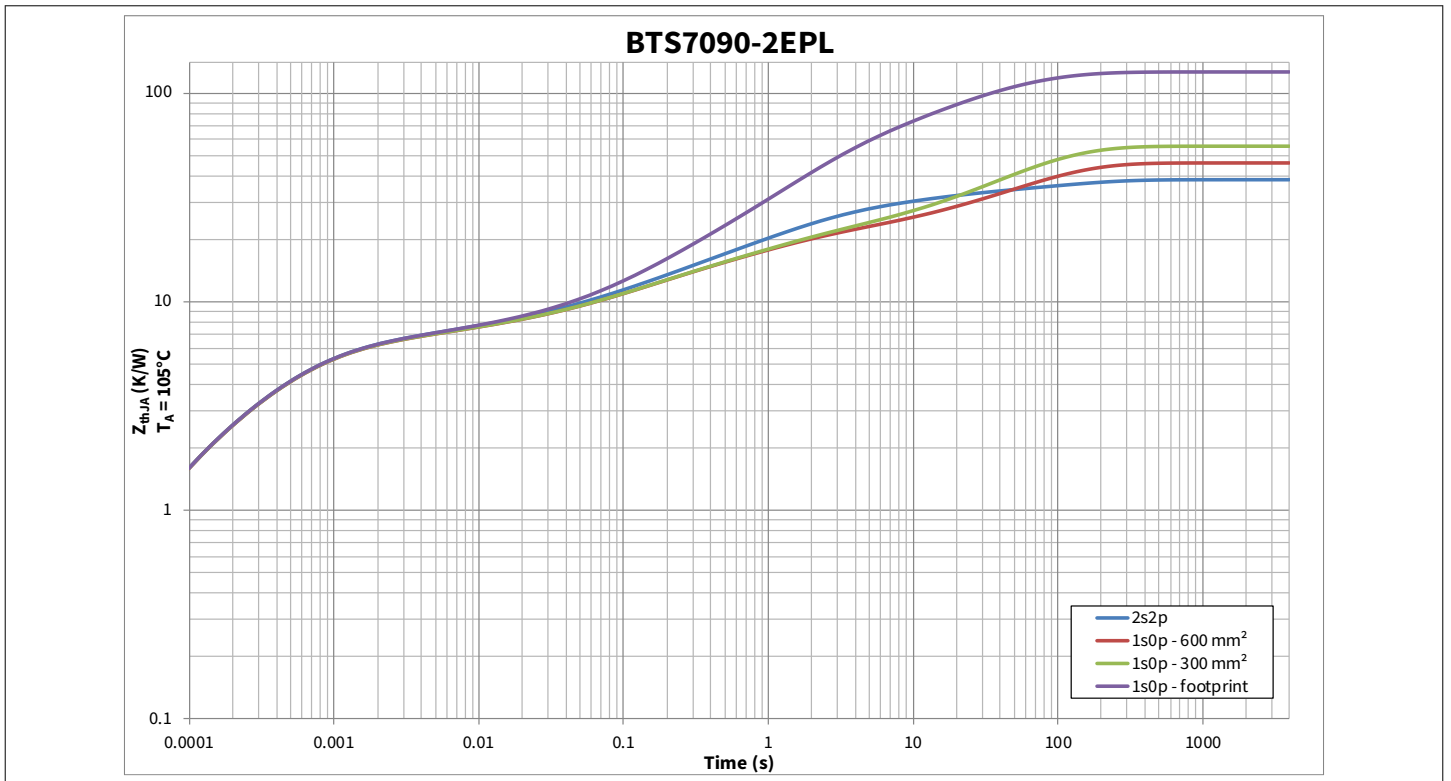


**Figure 7 PCB setup for thermal simulations**

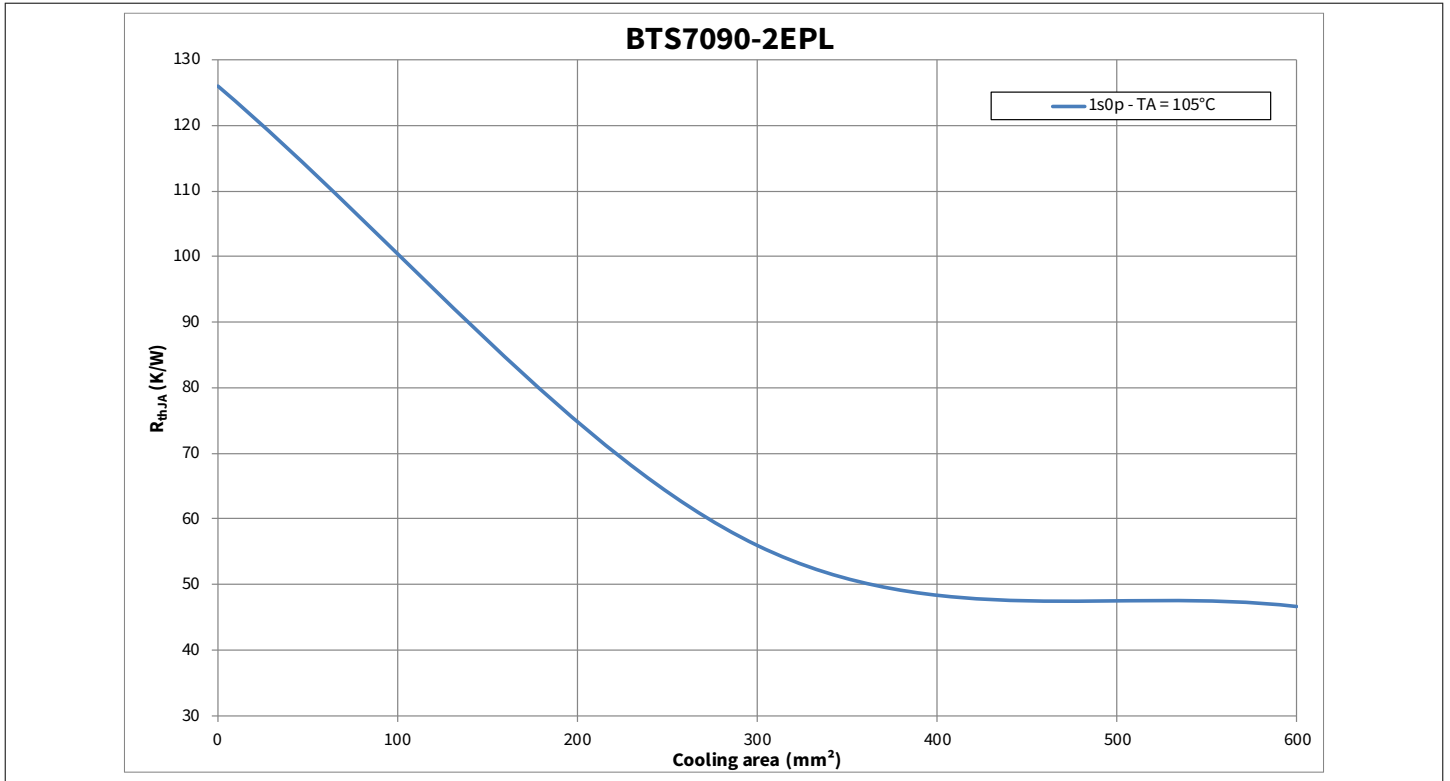


**Figure 8** Thermal vias on PCB for 2s2p PCB setup

### 3.3.2 Thermal impedance



**Figure 9** Typical thermal impedance. PCB setup according to PCB setup



**Figure 10** Thermal resistance on 1s0p PCB with various cooling surfaces

## 4 I/O pins

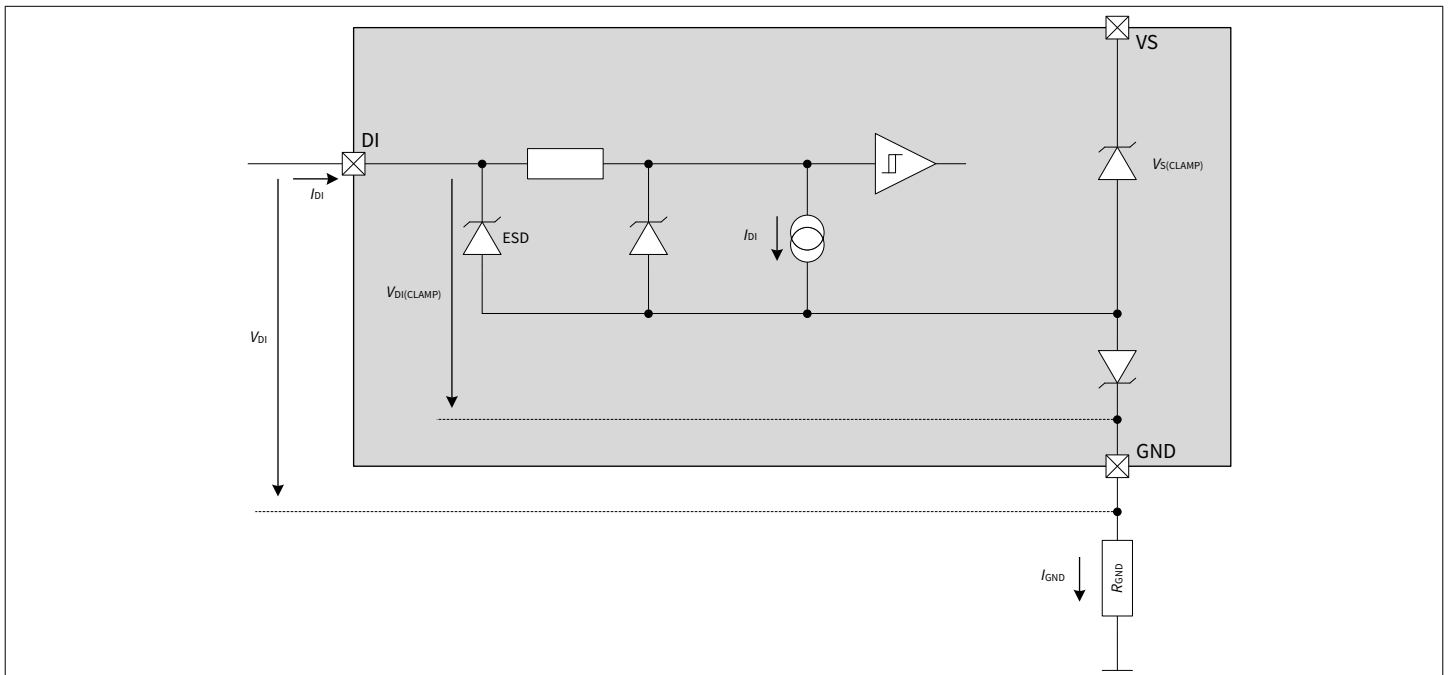
The device has four digital pins for direct control.

### 4.1 Digital I/O pins

Digital input (DI) pins = INn, DEN, DSEL

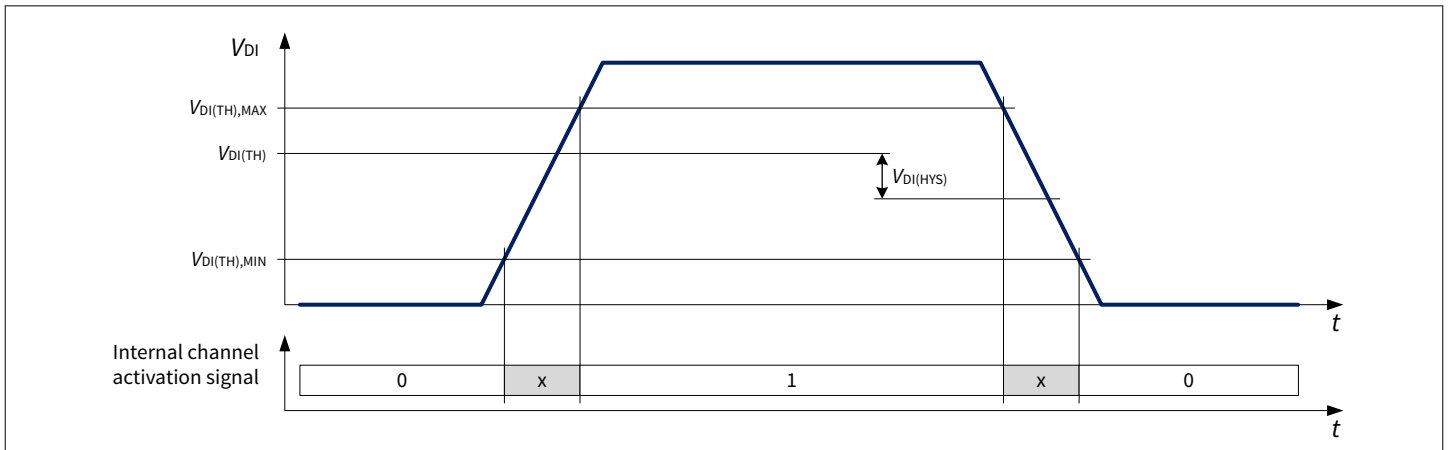
#### 4.1.1 Input pins

The input pins IN0 and IN1 activate the corresponding output channel. The input circuitry is compatible with 3.3 V and 5 V microcontroller. The electrical equivalent of the input circuitry is shown in [Figure 11](#). In case a pin is not used, it must be connected by a 10 kΩ resistor either to GND pin or to module ground.



**Figure 11** Input circuitry

The logic thresholds for “low” and “high” states are defined by parameters  $V_{DI(TH)}$  and  $V_{DI(HYS)}$ . The relationship between these two values is shown in [Figure 12](#).



**Figure 12** Input threshold voltages and hysteresis

### 4.1.2 Diagnosis pins

The Diagnosis Enable (DEN) pin controls the diagnosis circuitry and the protection circuitry. When DEN pin is set to “high”, the diagnosis is enabled (see [Chapter 8.2](#) for more details). When it is set to “low”, the diagnosis is disabled (IS pin is set to high impedance). The Diagnosis Selection (DSEL) pin selects the channel where the diagnosis is performed (see [Table 12](#)). See [Figure 12](#) for more details.

The transition from “high” to “low” of DEN pin clears the protection latch of the channel selected with DSEL pin depending on the logic state of IN pin and DEN pulse length (see [Chapter 7.3](#) for more details).

## 4.2 Electrical characteristics I/O pins

$V_S = 4\text{ V to }20\text{ V}$ ,  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$

Unless otherwise specified typical values:  $V_S = 13.5\text{ V}$ ,  $T_J = 25^\circ\text{C}$

Digital input (DI) pins = INn, DEN, DSEL

**Table 5 Electrical characteristics I/O pins**

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
<b>DI pins</b>							
Digital input voltage threshold	$V_{DI(TH)}$	0.8	1.3	2	V	See <a href="#">Figure 11</a> and <a href="#">Figure 12</a>	PRQ-76
Digital input clamping voltage	$V_{DI(CLAMP1)}$	–	7	–	V	<sup>1)</sup> $I_{DI} = 1\text{ mA}$ See <a href="#">Figure 11</a> and <a href="#">Figure 12</a>	PRQ-77
Digital input clamping voltage	$V_{DI(CLAMP2)}$	6.5	7.5	8.5	V	$I_{DI} = 2\text{ mA}$ See <a href="#">Figure 11</a> and <a href="#">Figure 12</a>	PRQ-78
Digital input hysteresis	$V_{DI(HYS)}$	–	0.25	–	V	<sup>1)</sup> See <a href="#">Figure 11</a> and <a href="#">Figure 12</a>	PRQ-80
Digital input current ("high")	$I_{DI(H)}$	2	10	25	$\mu\text{A}$	$V_{DI} = 2\text{ V}$ See <a href="#">Figure 11</a> and <a href="#">Figure 12</a>	PRQ-81
Digital input current ("low")	$I_{DI(L)}$	2	10	25	$\mu\text{A}$	$V_{DI} = 0.8\text{ V}$ See <a href="#">Figure 11</a> and <a href="#">Figure 12</a>	PRQ-82

<sup>1)</sup> Not subject to production test - specified by design

## 5 Power Supply

The device is supplied by  $V_S$ , which is used to supply the internal logic as well as to supply the power output stages. In case of an undervoltage condition, the device has a detection circuit, which prevents the activation of the power output stage as well as the diagnosis.

### 5.1 Operation modes and transitions

#### 5.1.1 Operation modes

The device has the following operation modes:

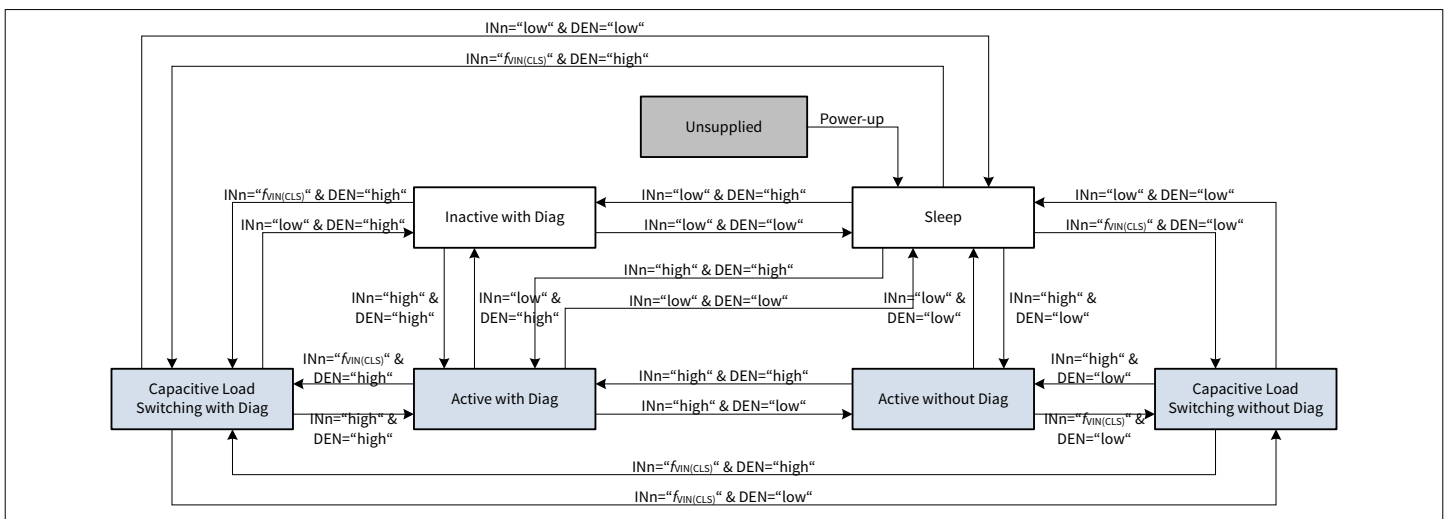
- Sleep
- Inactive with diagnosis
- Active with diagnosis
- Active without diagnosis
- Capacitive load switching mode with diagnosis
- Capacitive load switching mode without diagnosis

The transition between operation modes is determined according to these variables:

- Logic level at INn pins
- PWM signal at INn pins
- Logic level at DEN pin

The state diagram including the possible transitions is shown in Figure 13. The behavior of the device as well as some parameters may change independent from the operation mode of the device. Furthermore, due to the undervoltage detection circuitry which monitors  $V_S$  supply voltage, some changes within the same operation mode can be seen accordingly.

Table 6 shows the correlation between operation modes,  $V_S$  supply voltage, and the state of the most important functions (channel status).



**Figure 13** Operation mode state diagram

**Table 6** Operation mode, device function and  $V_S$  voltage

Operation mode	Function	$V_S > V_{S(OP)}$	$V_S < V_{S(OP)}$
Sleep	Channels	OFF	OFF
	Diagnosis	OFF	OFF

(table continues...)



**Table 6 (continued) Operation mode, device function and  $V_S$  voltage**

Operation mode	Function	$V_S > V_{S(OP)}$	$V_S < V_{S(OP)}$
Inactive with diagnosis	Channels	OFF	OFF
	Diagnosis	ON	OFF
Active with diagnosis	Channels	ON	OFF
	Diagnosis	ON	OFF
Active without diagnosis	Channels	ON	OFF
	Diagnosis	OFF	OFF
Capacitive load switching mode with diagnosis	Channels	ON	OFF
	Diagnosis	ON	OFF
Capacitive load switching mode without diagnosis	Channels	ON	OFF
	Diagnosis	OFF	OFF

### 5.1.1.1 Unsupplied

In this state the device supply voltage is below the undervoltage threshold  $V_{S(UV)}$ .

### 5.1.1.2 Power-up

The power-up transition is entered when the supply voltage ( $V_S$ ) is applied to the device. The supply rises until it exceeds the undervoltage threshold  $V_{S(OP)}$ .

### 5.1.1.3 Sleep

The device is in sleep mode when digital input (DI) pins are set to "low". While in sleep mode the current consumption is at  $I_{S(SLEEP)}$ . Overtemperature, overload protection and undervoltage mechanism are disabled. The device can go in sleep mode only if the protection is not active ( $n_{RESTART(CR)} = 0$ ,  $T_J < T_{J(ABS)}$  and  $(T_J - T_{J(REF)}) < T_{J(DYN)}$  (including hysteresis)), see [Chapter 7.3](#).

### 5.1.1.4 Inactive with diagnosis

The device is in inactive with diagnosis mode while DEN pin is set to "high" and input pins are set to "low". The channels are OFF, therefore open load in OFF diagnosis is possible. Depending on the load condition, either a fault current  $I_{S(FAULT)}$  or an open load in OFF current  $I_{S(OLOFF)}$  may be present at IS pin. During such condition, the current consumption of the device is increased.

### 5.1.1.5 Active with diagnosis

Active with diagnosis mode is the normal operation mode of the device. The device enters active with diagnosis mode for the related channel when  $INn = \text{"high"}$  and  $DEN = \text{"high"}$ , in this condition one or more outputs are switched ON with diagnosis. Device current consumption is specified by parameter  $I_{GND(ACTIVE)}$ .

### 5.1.1.6 Active without diagnosis

The device is in active without diagnosis mode when  $INn = \text{"high"}$  and  $DEN = \text{"low"}$ , in this condition, one or more outputs are switched ON without diagnosis.

### 5.1.1.7 Capacitive load switching mode with diagnosis

The device has a capacitive load switching mode implemented to drive capacitive loads. The capacitive load switching mode with diagnosis can be activated with  $INn = f_{VIN(CLS)}$  and  $DEN = \text{"high"}$ , in this condition one or more outputs are switched ON with diagnosis. Device current consumption is specified by parameter  $I_{GND(ACTIVE)}$ .

### 5.1.1.8 Capacitive load switching mode without diagnosis

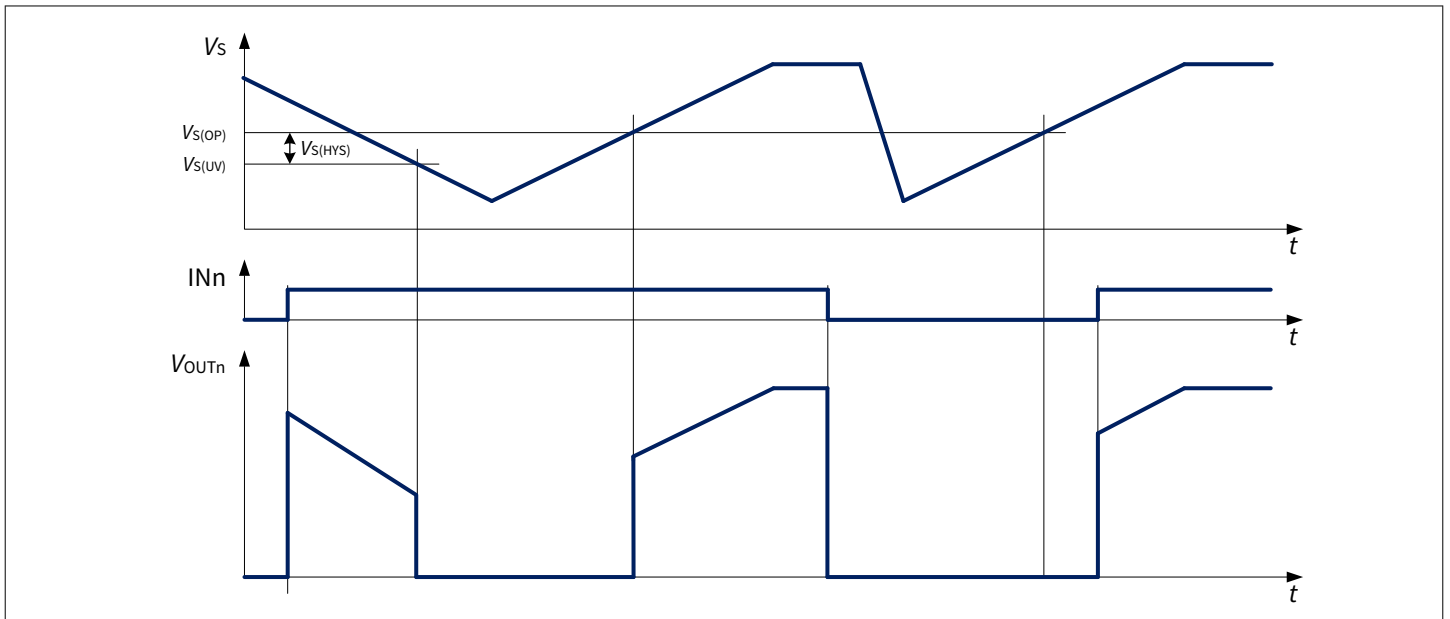
The device is in capacitive load switching mode without diagnosis when  $INn = "f_{VIN(CLS)}"$  and  $DEN = "low"$ , in this condition, one or more outputs are switched ON without diagnosis.

## 5.2 Undervoltage on VS

Between  $V_{S(OP)}$  and  $V_{S(UV)}$  the undervoltage mechanism is triggered.

The power output stage follows the input logic as long as  $V_S > V_{S(OP)}$ .

If the device is Active or in Capacitive Load Switching Mode, with or without Diagnosis and the supply voltage  $V_S$  drops below the undervoltage threshold  $V_{S(UV)}$ , the internal logic switches OFF the output channel.



**Figure 14**  $V_S$  undervoltage behavior

## 5.3 Electrical characteristics power supply

$V_S = 4\text{ V to }20\text{ V}$ ,  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$

Unless otherwise specified typical values:  $V_S = 13.5\text{ V}$ ,  $T_J = 25^\circ\text{C}$

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

BTS7090-2EPL:  $R_L = 6.8\ \Omega$

**Table 7** Electrical characteristics power supply

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
<b>VS pin</b>							
Power supply undervoltage shutdown	$V_{S(UV)}$	1.8	2.2	2.7	V	$V_S$ decreasing $INn = "high"$ From $0 \leq V_{DS} \leq 0.5\text{ V}$ to $V_{DS} \sim V_S$ See <a href="#">Figure 14</a>	PRQ-98

(table continues...)

**Table 7 (continued) Electrical characteristics power supply**

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power supply minimum operating voltage	$V_{S(OP)}$	2.1	2.5	3	V	$V_S$ increasing INn = "high" From $V_{DS} \sim V_S$ to $0 \leq V_{DS} \leq 0.5$ V See <a href="#">Figure 14</a>	PRQ-99
Power supply undervoltage shutdown hysteresis	$V_{S(HYS)}$	–	0.3	–	V	1) $V_{S(OP)} - V_{S(UV)}$ See <a href="#">Figure 14</a>	PRQ-100
Breakdown voltage between GND and VS pins in reverse battery	$-V_{S(REV)}$	16	–	30	V	1) $I_{GND(REV)} = 7$ mA $T_J = 150^\circ\text{C}$	PRQ-101
Power supply current consumption in sleep mode with Loads at $T_J \leq 85^\circ\text{C}$	$I_{VS(SLEEP)_85}$	–	0.01	0.5	$\mu\text{A}$	1) $V_S = 20$ V $V_{OUT} = 0$ V INn = DEN = DSEL = "low" $T_J \leq 85^\circ\text{C}$	PRQ-821
Power supply current consumption in sleep mode with loads at $T_J = 150^\circ\text{C}$	$I_{VS(SLEEP)_150}$	–	1	8	$\mu\text{A}$	$V_S = 20$ V $V_{OUT} = 0$ V INn = DEN = DSEL = "low" $T_J = 150^\circ\text{C}$	PRQ-822
Operating current in active with diagnosis mode	$I_{GND(ACTIVE)}$	–	3.7	4.5	mA	$V_S = 20$ V INn = DEN = DSEL = "high"	PRQ-823
Operating current in inactive with diagnosis mode	$I_{GND(INACTIVE)}$	–	1.8	2.2	mA	$V_S = 20$ V INn = "low" DEN = DSEL = "high"	PRQ-824

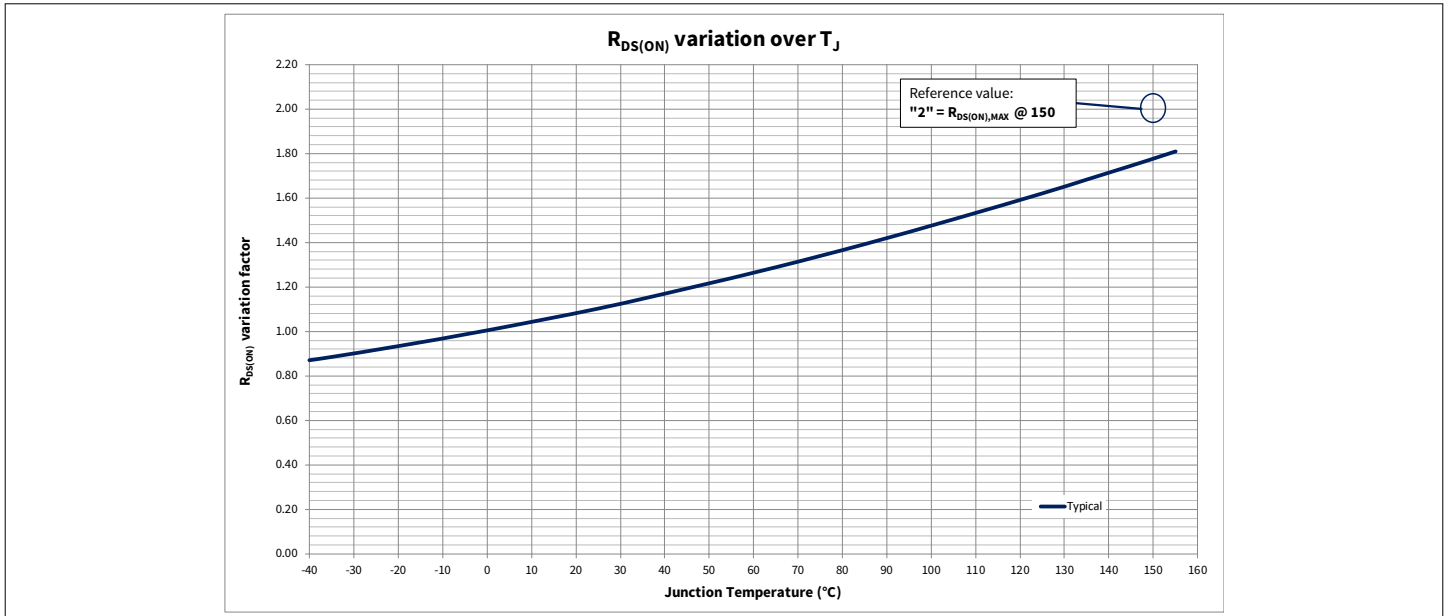
1) Not subject to production test - specified by design

## 6 Power Stage

The high-side power stages are built using a N-channel vertical power MOSFET with charge pump.

### 6.1 Output ON-state resistance

The ON-state resistance  $R_{DS(ON)}$  depends mainly on junction temperature  $T_J$ . Figure 15, shows the variation of  $R_{DS(ON)}$  across the whole  $T_J$  range. The value “2” on the y-axis corresponds to the maximum  $R_{DS(ON)}$  measured at  $T_J = 150^\circ\text{C}$ .



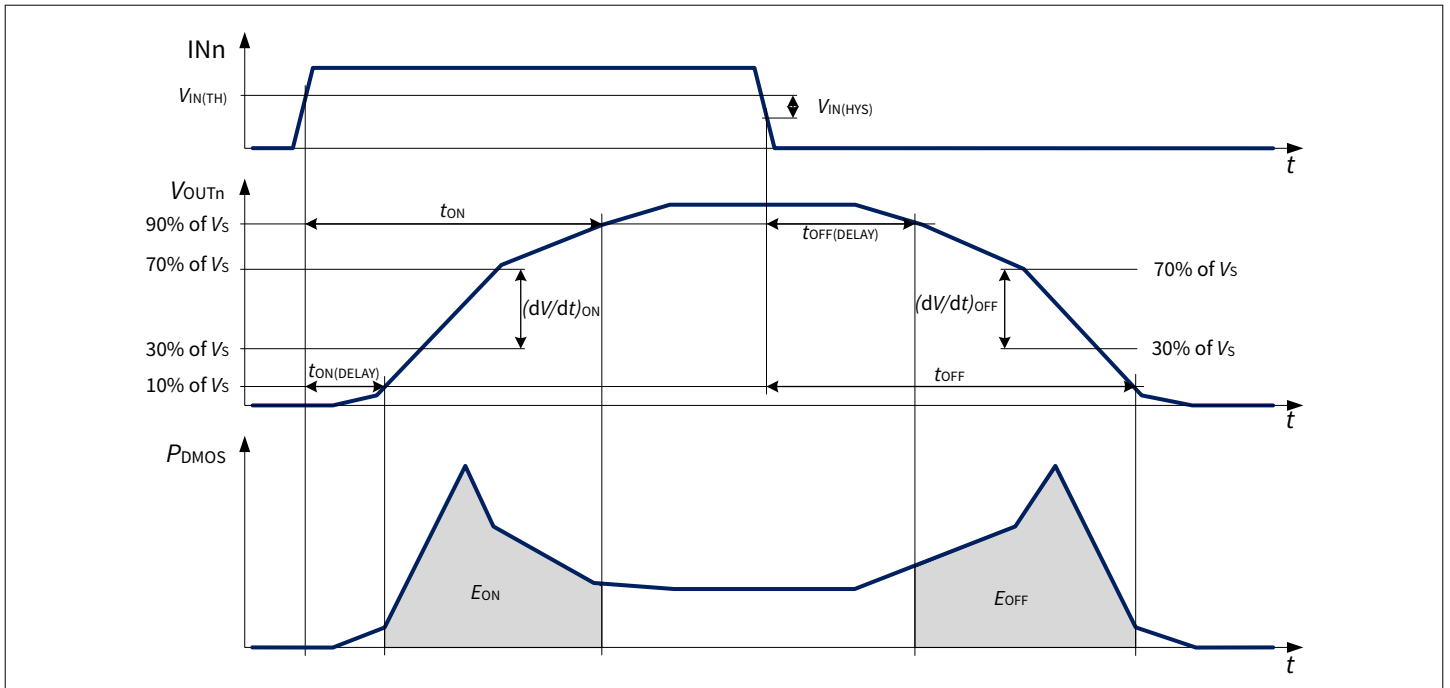
**Figure 15**  $R_{DS(ON)}$  variation factor

The behavior in reverse polarity is described in [Chapter 7.4.1](#).

## 6.2 Switching loads

### 6.2.1 Switching resistive loads

When switching resistive loads, the switching times and slew rates shown in [Figure 16](#) can be considered. The switching energy values  $E_{ON}$  and  $E_{OFF}$  are proportional to load resistance and times  $t_{ON}$  and  $t_{OFF}$ .

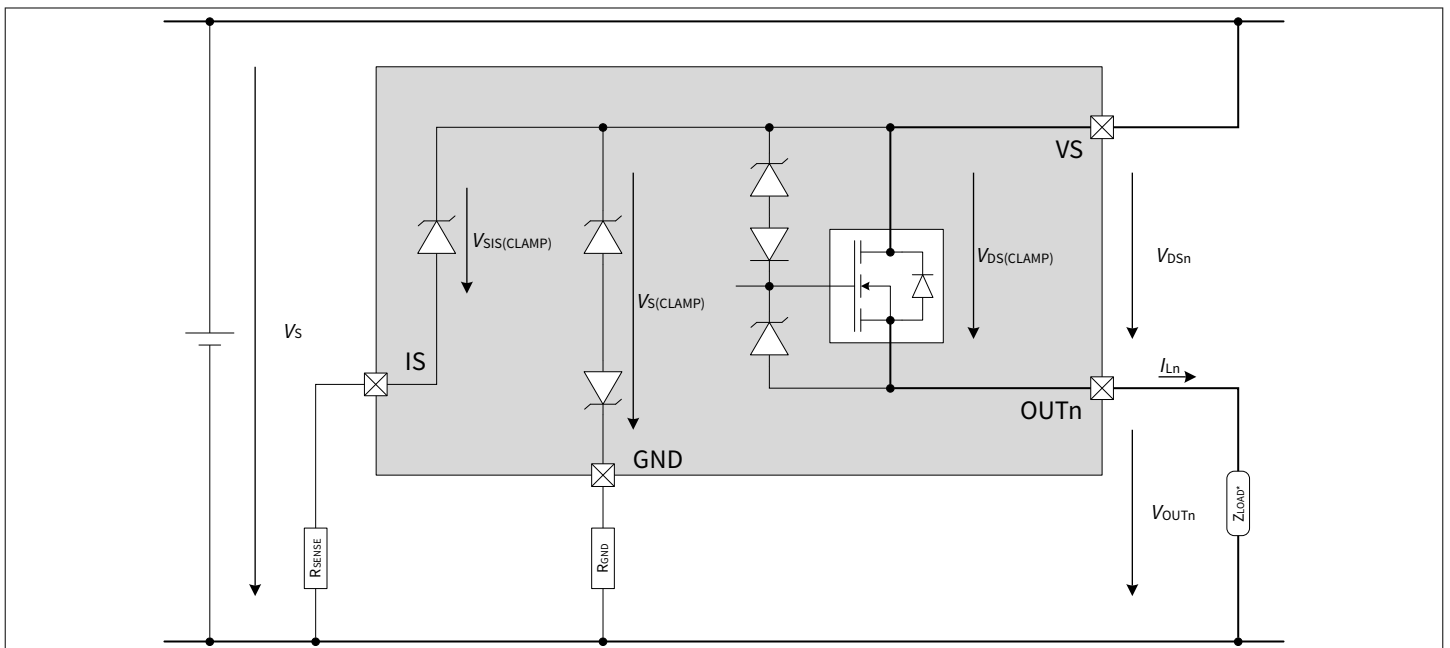


**Figure 16** Switching a resistive load

### 6.2.2 Switching inductive loads

When switching OFF inductive loads with high-side switches, the voltage  $V_{OUT}$  drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to overvoltage, a voltage clamp mechanism is implemented. The clamping structure limits the output voltage so that  $V_{DS} \leq V_{DS(CLAMP)}$ . Chapter 6.2.2 shows a concept drawing of the implementation.

The clamping structure is active in all operation modes listed in Chapter 5.1.



**Figure 17** Output clamping concept

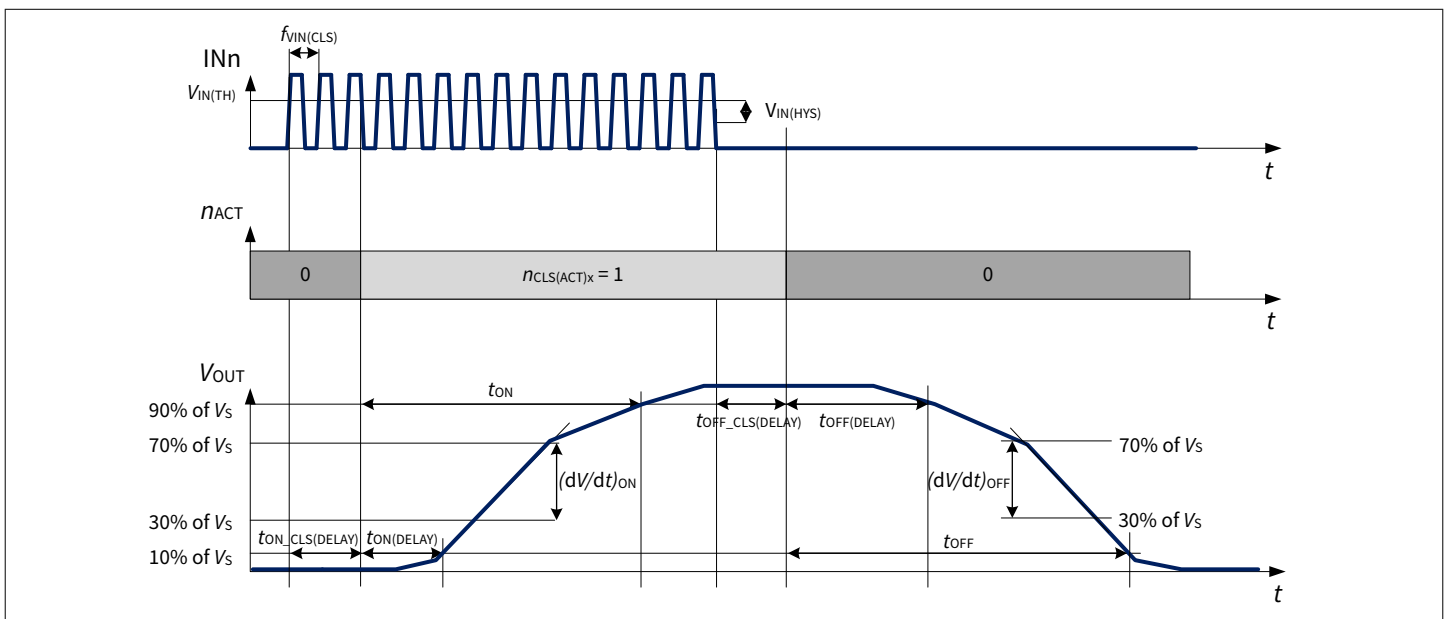
During demagnetization of inductive loads, energy has to be dissipated in the device. The energy can be calculated with:

$$E = V_{DS(CLAMP)} \cdot \left[ \frac{V_S - V_{DS(CLAMP)}}{R_L} \cdot \ln \left( 1 - \frac{R_L \cdot I_L}{V_S - V_{DS(CLAMP)}} \right) + I_L \right] \cdot \frac{L}{R_L} \quad (1)$$

The maximum energy the device can sustain is limited by the thermal design. Please refer to [Table 2](#) for the maximum allowed values of  $E_{AS}$  (single pulse energy) and  $E_{AR}$  (repetitive energy).

### 6.2.3 Switching capacitive loads

When  $f_{VIN(CLS)}$  is applied the device enters CLS mode after  $t_{ON\_CLS(DELAY)}$  as shown in [Figure 18](#). A pumping mode is applied to charge the capacitor while the overcurrent limitation is active, as shown in [Figure 19](#). During CLS mode, protection and diagnosis functions are active.



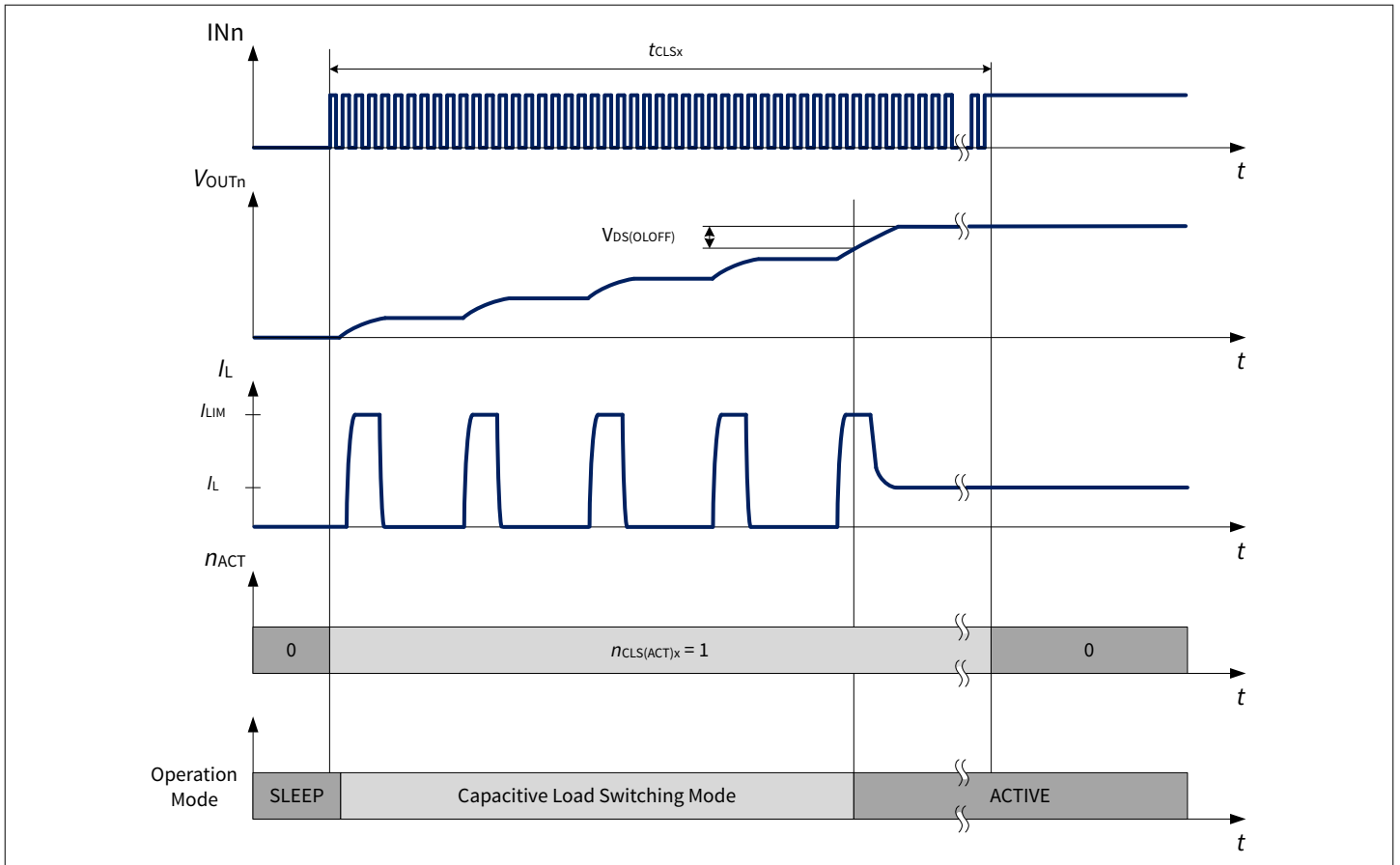
**Figure 18** Switching a capacitive load

When the device is in CLS mode, the dynamic overtemperature protection is reduced to  $T_{J(DYN)\_CLS}$  with continuous restart.

A transition from CLS mode to Active mode is performed automatically when  $V_{DS} \leq V_{DS(OLOFF)}$ .

On the contrary, when  $V_{DS} > V_{DS(OLOFF)}$ , the CLS mode has to be left after a maximum time of  $t_{CLSx}$  by setting input to "low" or "high".

A transition from capacitive load switching mode to active mode shall be performed only if there is no short circuit at the output. To distinguish between short circuit and normal load, a current sense measurement must be performed before leaving. If the current measurement delivers an expected value, the transition from CLS mode to active mode may be performed. If the current measurement delivers an open load value (no output current), it has to be assumed that there is either an open load or a short circuit at the output. Additionally, a short circuit condition could be excluded by an external voltage measurement at the output.



**Figure 19** Capacitive load switching activations

## 6.3 Advanced switching characteristics

### 6.3.1 Inverse current behavior

When  $V_{OUT} > V_S$ , a current  $I_{L(INV)}$  flows into the power output transistor (see [Figure 20](#)). This condition is known as “Inverse Current”.

If the channel is in OFF state, the current flows through the intrinsic body diode generating high power losses, therefore, an increase of overall device temperature. This may lead to a switch OFF of unaffected channels due to overtemperature. If the channel is in ON state,  $R_{DS(INV)}$  can be expected and power dissipation in the output stage is comparable to normal operation in  $R_{DS(ON)}$ .

During inverse current condition, the channel remains in ON or OFF state as long as  $|-I_L| < |-I_{L(INV)}|$ .

The feature of InverseON allows to switch ON the channel during Inverse Current condition as long as  $|-I_L| < |-I_{L(INV)}|$ , see [Figure 21](#).

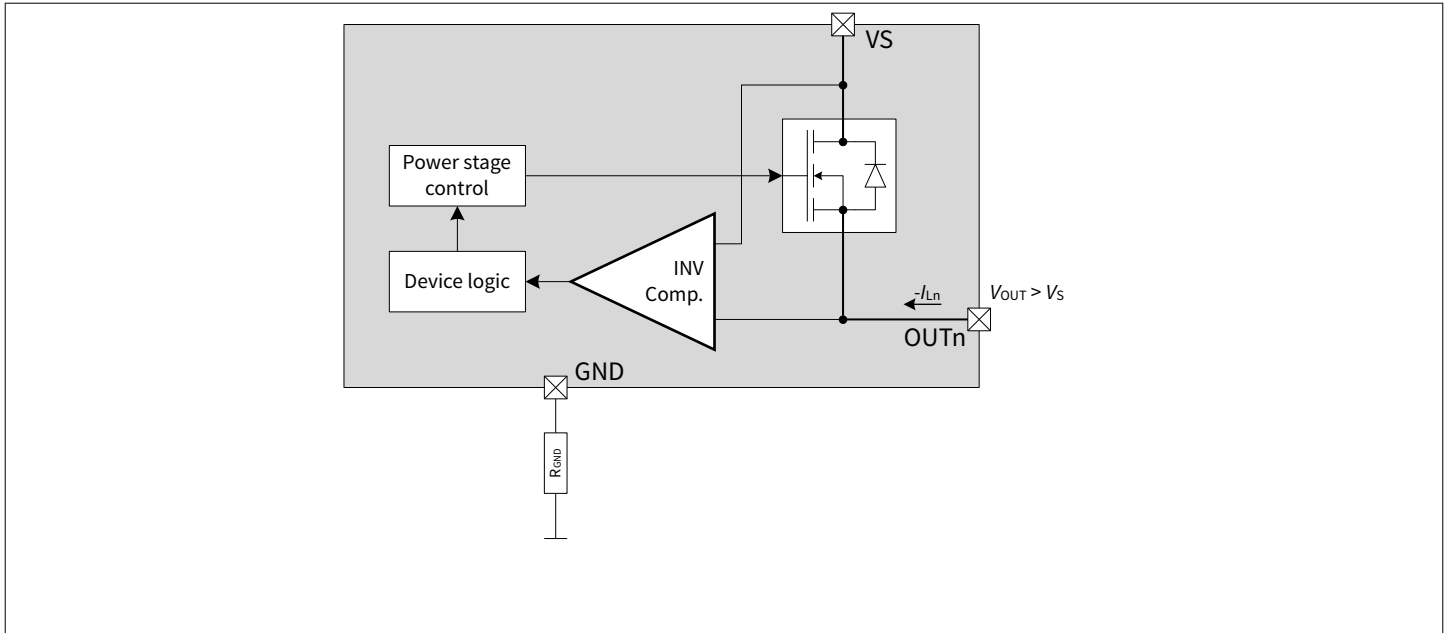


Figure 20 Inverse current circuitry

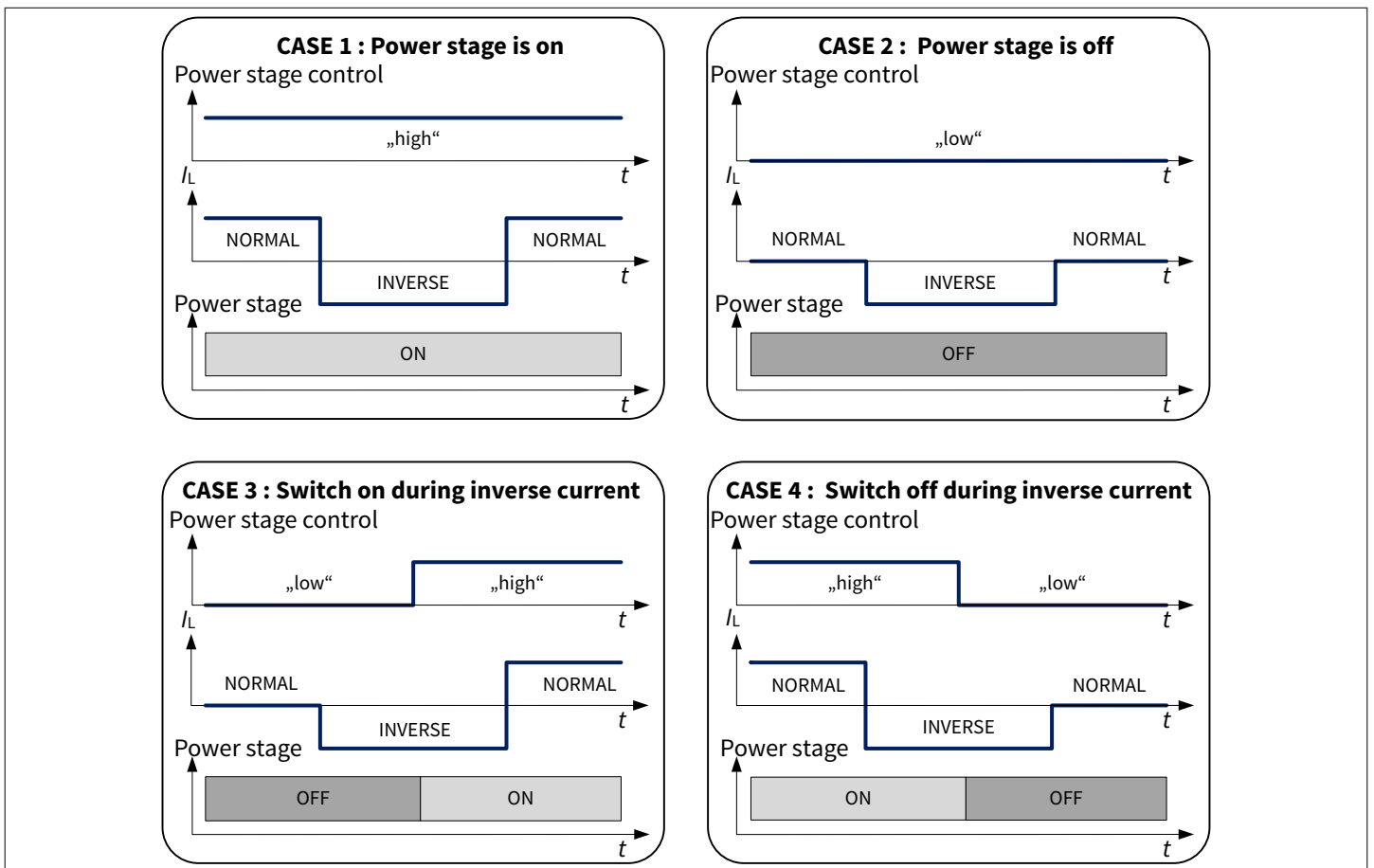


Figure 21 InverseON - Channel behavior in case of applied inverse current

### 6.4 Electrical characteristics power stage

$V_S = 4\text{ V to } 20\text{ V}$ ,  $T_J = -40^\circ\text{C to } +150^\circ\text{C}$

Unless otherwise specified typical values:  $V_S = 13.5\text{ V}$ ,  $T_J = 25^\circ\text{C}$



Typical resistive loads connected to the outputs for testing (unless otherwise specified):

BTS7090-2EPL:  $R_L = 6.8 \Omega$

**Table 8 Electrical characteristics power stage**

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
<b>Voltages</b>							
Drain to source clamping voltage at $T_J = -40^\circ\text{C}$	$V_{DS(\text{CLAMP})_{-40}}$	33	36.5	42	V	$I_L = 5 \text{ mA}$ $T_J = -40^\circ\text{C}$ See <a href="#">Chapter 6.2.2</a>	PRQ-110
Drain to source clamping voltage at $T_J \geq 25^\circ\text{C}$	$V_{DS(\text{CLAMP})_{25}}$	35	38	44	V	<sup>1)</sup> $I_L = 5 \text{ mA}$ $T_J \geq 25^\circ\text{C}$ See <a href="#">Chapter 6.2.2</a>	PRQ-111
<b>Timings</b>							
Switch-ON delay	$t_{\text{ON}(\text{DELAY})}$	10	70	130	$\mu\text{s}$	$V_S = 13.5 \text{ V}$ $V_{\text{OUT}} = 10\% V_S$ See <a href="#">Figure 16</a>	PRQ-834
Switch-OFF delay	$t_{\text{OFF}(\text{DELAY})}$	10	50	160	$\mu\text{s}$	$V_S = 13.5 \text{ V}$ $V_{\text{OUT}} = 90\% V_S$ See <a href="#">Figure 16</a>	PRQ-835
Switch-ON time	$t_{\text{ON}}$	50	130	210	$\mu\text{s}$	$V_S = 13.5 \text{ V}$ $V_{\text{OUT}} = 90\% V_S$ See <a href="#">Figure 16</a>	PRQ-836
Switch-OFF time	$t_{\text{OFF}}$	30	100	220	$\mu\text{s}$	$V_S = 13.5 \text{ V}$ $V_{\text{OUT}} = 10\% V_S$ See <a href="#">Figure 16</a>	PRQ-837
CLS activation delay	$t_{\text{ON\_CLS}(\text{DELAY})}$	10	70	200	$\mu\text{s}$	$V_S = 13.5 \text{ V}$ See <a href="#">Figure 18</a>	PRQ-838
CLS de-activation delay	$t_{\text{OFF\_CLS}(\text{DELAY})}$	20	40	90	$\mu\text{s}$	$V_S = 13.5 \text{ V}$ See <a href="#">Figure 18</a>	PRQ-839
Switch-ON/OFF Matching - $t_{\text{ON}} - t_{\text{OFF}}$	$\Delta t_{\text{SW}}$	-60	25	90	$\mu\text{s}$	$V_S = 13.5 \text{ V}$	PRQ-840
<b>Voltage slope</b>							
Switch-ON slew rate	$(dV/dt)_{\text{ON}}$	0.16	0.27	0.39	$\text{V}/\mu\text{s}$	$V_S = 13.5 \text{ V}$ $V_{\text{OUT}} = 30\% \text{ to } 70\% \text{ of } V_S$	PRQ-841
Switch-OFF slew rate	$(dV/dt)_{\text{OFF}}$	-0.39	-0.27	-0.16	$\text{V}/\mu\text{s}$	$V_S = 13.5 \text{ V}$ $V_{\text{OUT}} = 70\% \text{ to } 30\% \text{ of } V_S$	PRQ-842
Slew rate matching - $(dV/dt)_{\text{ON}} + (dV/dt)_{\text{OFF}}$	$\Delta(dV/dt)_{\text{SW}}$	-0.15	0	0.15	$\text{V}/\mu\text{s}$	$V_S = 13.5 \text{ V}$	PRQ-843

**(table continues...)**

**Table 8 (continued) Electrical characteristics power stage**

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
<b>CLS mode</b>							
Input frequency for capacitive load switching mode activation	$f_{VIN(CLS)}$	22	30	38	kHz	<sup>2)</sup> $DC_{VIN(CLS)} = 50\%$	PRQ-353
Duty cycle for capacitive load switching mode activation	$DC_{VIN(CLS)}$	30%	50%	70%	–	<sup>2)</sup> $f_{VIN(CLS)} = 30 \text{ kHz}$	PRQ-354
Maximum time in CLS mode	$t_{CLS1}$	–	–	25	ms	<sup>2)</sup> See <a href="#">Chapter 6.2.3</a>	PRQ-355
Maximum time in CLS mode	$t_{CLS2}$	–	–	90	ms	<sup>2)</sup> See <a href="#">Chapter 6.2.3</a>	PRQ-813
Maximum number of CLS mode activations	$n_{CLS\_ACT1}$	–	–	500	kcycles	<sup>2)</sup> See <a href="#">Chapter 6.2.3</a>	PRQ-812
Maximum number of CLS mode activations	$n_{CLS\_ACT2}$	–	–	50	kcycles	<sup>2)</sup> See <a href="#">Chapter 6.2.3</a>	PRQ-814
<b>Output characteristics</b>							
ON-state resistance at $T_J = 25^\circ\text{C}$	$R_{DS(ON)\_25}$	–	90	–	m $\Omega$	<sup>2)</sup> $T_J = 25^\circ\text{C}$	PRQ-121
ON-state resistance at $T_J = 150^\circ\text{C}$	$R_{DS(ON)\_150}$	–	–	180	m $\Omega$	$T_J = 150^\circ\text{C}$ $I_L = 1 \text{ A}$	PRQ-122
ON-state resistance in cranking at $T_J = 150^\circ\text{C}$	$R_{DS(ON)\_CRANK\_150}$	–	–	200	m $\Omega$	$T_J = 150^\circ\text{C}$ $V_S = 3.1 \text{ V}$ $I_L = 0.5 \text{ A}$	PRQ-124
ON-state resistance in inverse current at $T_J = 25^\circ\text{C}$	$R_{DS(INV)\_25}$	–	90	–	m $\Omega$	<sup>2)</sup> $T_J = 25^\circ\text{C}$ $V_S = 13.5 \text{ V}$ $I_L = -1 \text{ A}$ See <a href="#">Figure 20</a>	PRQ-131
ON-state resistance in inverse current at $T_J = 150^\circ\text{C}$	$R_{DS(INV)\_150}$	–	–	200	m $\Omega$	$T_J = 150^\circ\text{C}$ $V_S = 13.5 \text{ V}$ $I_L = -1 \text{ A}$ See <a href="#">Figure 20</a>	PRQ-132
Nominal load current per channel (all channels active) at $T_A = 85^\circ\text{C}$	$I_{L(NOM)\_85}$	–	2	–	A	<sup>2)</sup> $T_A = 85^\circ\text{C}$ $T_J \leq 150^\circ\text{C}$	PRQ-134

**(table continues...)**

**Table 8 (continued) Electrical characteristics power stage**

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output leakage current at $T_J \leq 85^\circ\text{C}$	$I_{L(\text{OFF})_85}$	–	0.01	0.5	$\mu\text{A}$	2) $V_{\text{OUT}} = 0\text{ V}$ $I_{\text{Nn}} = \text{"low"}$ $T_A \leq 85^\circ\text{C}$	PRQ-136
Output leakage current at $T_J = 150^\circ\text{C}$	$I_{L(\text{OFF})_150}$	–	1.2	4	$\mu\text{A}$	$V_{\text{OUT}} = 0\text{ V}$ $I_{\text{Nn}} = \text{"low"}$ $T_A = 150^\circ\text{C}$	PRQ-137
Inverse current capability	$I_{L(\text{INV})}$	–	2	–	A	2) $V_S < V_{\text{OUT}}$ $I_{\text{Nn}} = \text{"high"}$ see <a href="#">Figure 20</a>	PRQ-139

**Voltages**

Drain source diode voltage	$ V_{\text{DS}(\text{DIODE})} $	–	550	700	mV	$I_L = -190\text{ mA}$ $T_J = 150^\circ\text{C}$	PRQ-141
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**Switching energy**

Switch-ON energy	$E_{\text{ON}}$	–	0.75	–	mJ	2) $V_S = 20\text{ V}$ See <a href="#">Chapter 6.2.1</a>	PRQ-142
Switch-OFF energy	$E_{\text{OFF}}$	–	0.85	–	mJ	2) $V_S = 20\text{ V}$ See <a href="#">Chapter 6.2.1</a>	PRQ-144

1) Tested at  $T_J = 150^\circ\text{C}$

2) Not subject to production test - specified by design

## 7 Protection

The device is protected against overload, overtemperature and overvoltage.

Overtemperature and overload protection are operational in all operation modes, except when in sleep mode.

Overload protection is not active during inverse current condition.

Overtemperature and overload protection during inverse current condition is inactive on the channel which is in inverse condition.

Overvoltage protection is active in all operation modes.

### 7.1 Overcurrent protection

#### 7.1.1 Overcurrent threshold

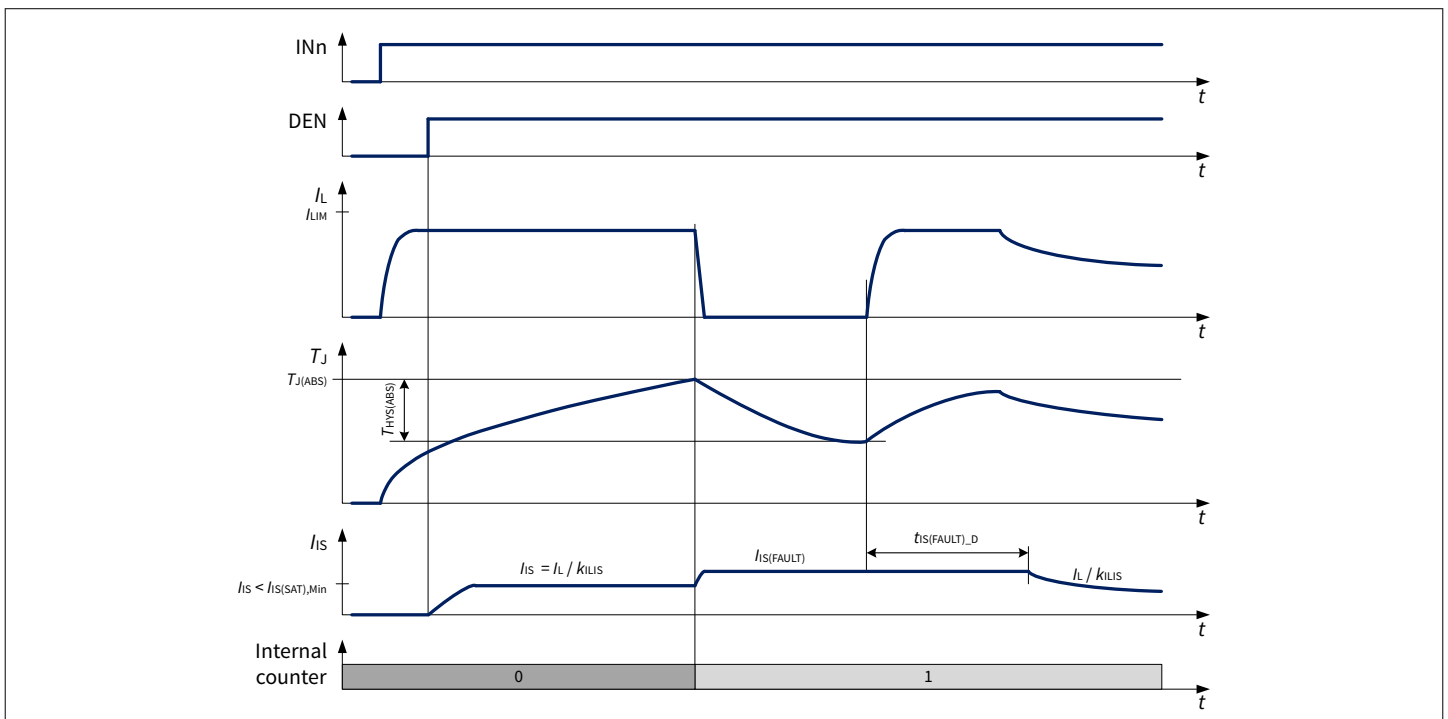
The device is protected in case of overload and short circuit to ground.

The device offers a current limitation, this feature offers protection against overstress for the power output stage. At first step, the instantaneous power in the switch is maintained at a safe value by limiting the current to the maximum current allowed in the switch ( $I_{LIM}$ ). The current limitation is independent of  $V_{DS}$  and  $T_J$ . In case of DMOS temperature increase exceeding the device safe operation environment, overtemperature and dynamic temperature protection mechanism will be triggered as shown in [Figure 22](#) and [Figure 23](#).

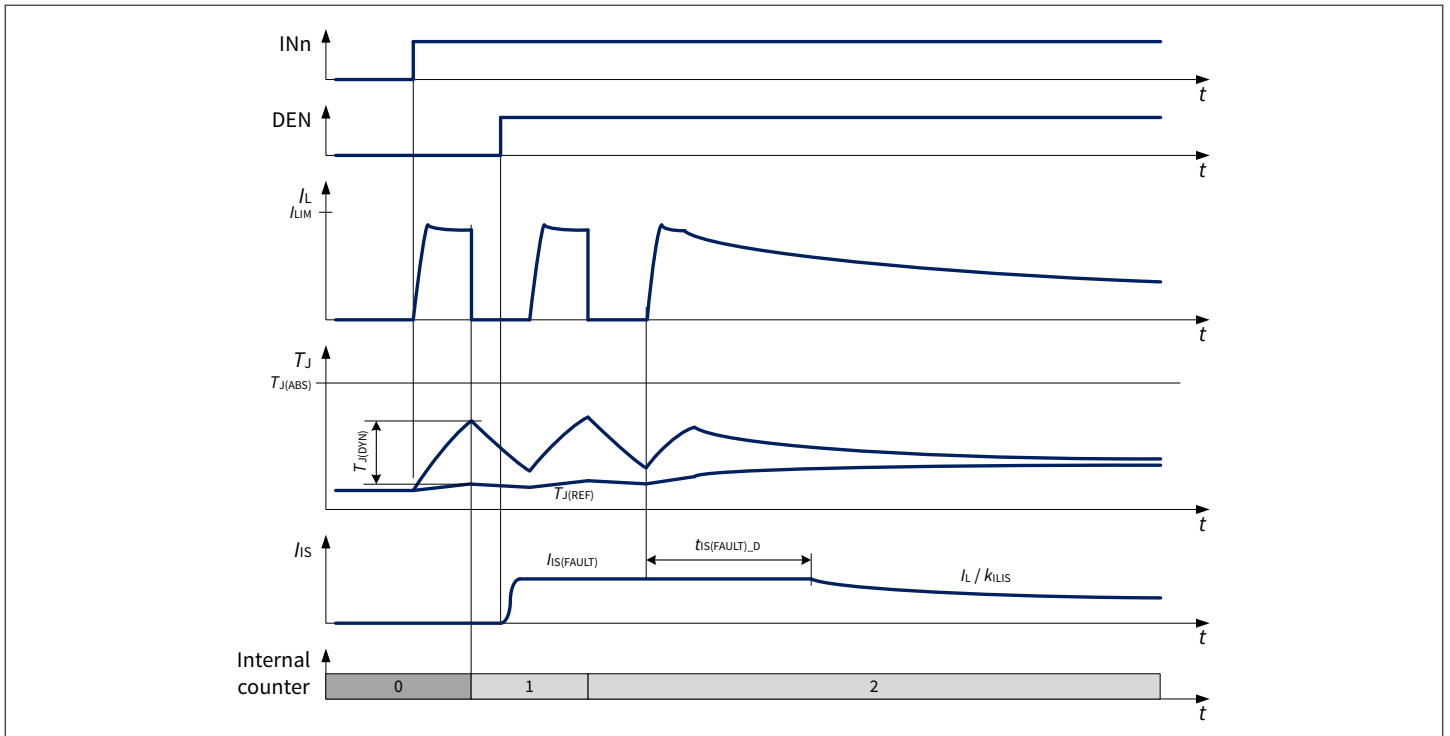
### 7.2 Overtemperature protection

The device incorporates both an absolute ( $T_{J(ABS)}$ ) and a dynamic ( $T_{J(DYN)}$ ) temperature protection circuitry for each channel.

An increase in junction temperature  $T_J$  above either one of the two thresholds ( $T_{J(ABS)}$  or  $T_{J(DYN)}$ ) switches OFF the overheated channel. The affected channel will perform automatic restart attempts. The channel remains switched OFF until the junction temperature has reached the restart condition described in [Table 9](#) according to [Chapter 7.3.1](#). If the number of automatic restart attempts exceeds  $n_{RESTART(CR),TYP}$ , the affected channel latches OFF to prevent destruction. The behavior is shown in [Figure 22](#) and [Figure 23](#).  $T_{J(REF)}$  is the reference temperature used for dynamic temperature protection.



**Figure 22** Overtemperature protection (absolute)



**Figure 23** Overtemperature protection (dynamic)

When the overtemperature protection circuitry allows the channel to be switched ON again, the retry strategy described in [Chapter 7.3](#) is followed.

### 7.3 Protection and diagnosis in case of fault

Any event that triggers overtemperature protection has two consequences:

- The affected channel switches OFF according to [Chapter 7.3.1](#).
- If the diagnosis is active for the affected channel, a current  $I_{IS(FAULT)}$  is provided by IS pin (see [Chapter 8.2.2](#) for further details).

The channel can be switched ON again if all the protection mechanisms fulfill the “restart” conditions described in [Table 9](#) and  $n_{RESTART(CR)} < n_{RESTART(CR),typ}$ .

**Table 9** Protection "restart" condition

Fault condition	Switch OFF event	"Restart" condition
Overtemperature	$T_J \geq T_{J(ABS)}$ or $(T_J - T_{J(REF)}) \geq T_{J(DYN)}$	$T_J < T_{J(ABS)}$ and $(T_J - T_{J(REF)}) < T_{J(DYN)}$ (including hysteresis)

#### 7.3.1 Retry strategy

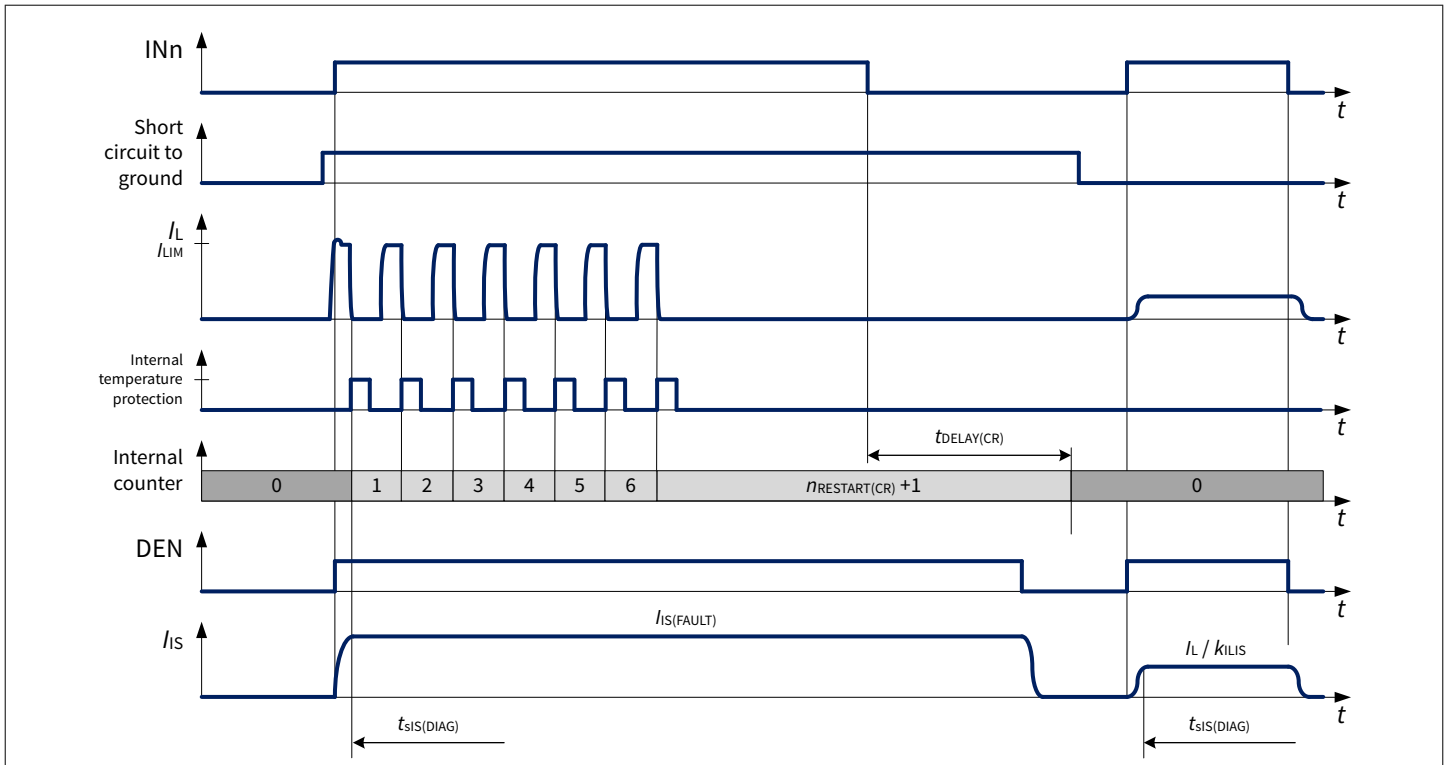
When INn is set to “high”, the related power output stage is switched ON. If a fault condition is detected the power output stage is switched OFF. The device will apply the restart strategy and return to normal operation or latches OFF if the fault remains to be present after  $n_{RESTART(CR),TYP}$ .

The device has an internal retry counter  $n_{RESTART(CR)}$  (one for each channel) to maximize the robustness in case of fault.

The channel is allowed to switch ON for  $n_{RESTART(CR)}$  times before switching OFF. After  $n_{RESTART(CR),TYP}$  consecutive “restart” cycles, the channel latches OFF. To de-latch the power output stage and reset the internal counter it is necessary to set the input pin to “low” for a time longer than  $t_{DELAY(CR)}$ .

If the fault is no longer present and  $t_{DELAY(CR)}$  is observed the device will enter normal operation. In case the fault is still present, the device will trigger again the retry strategy.

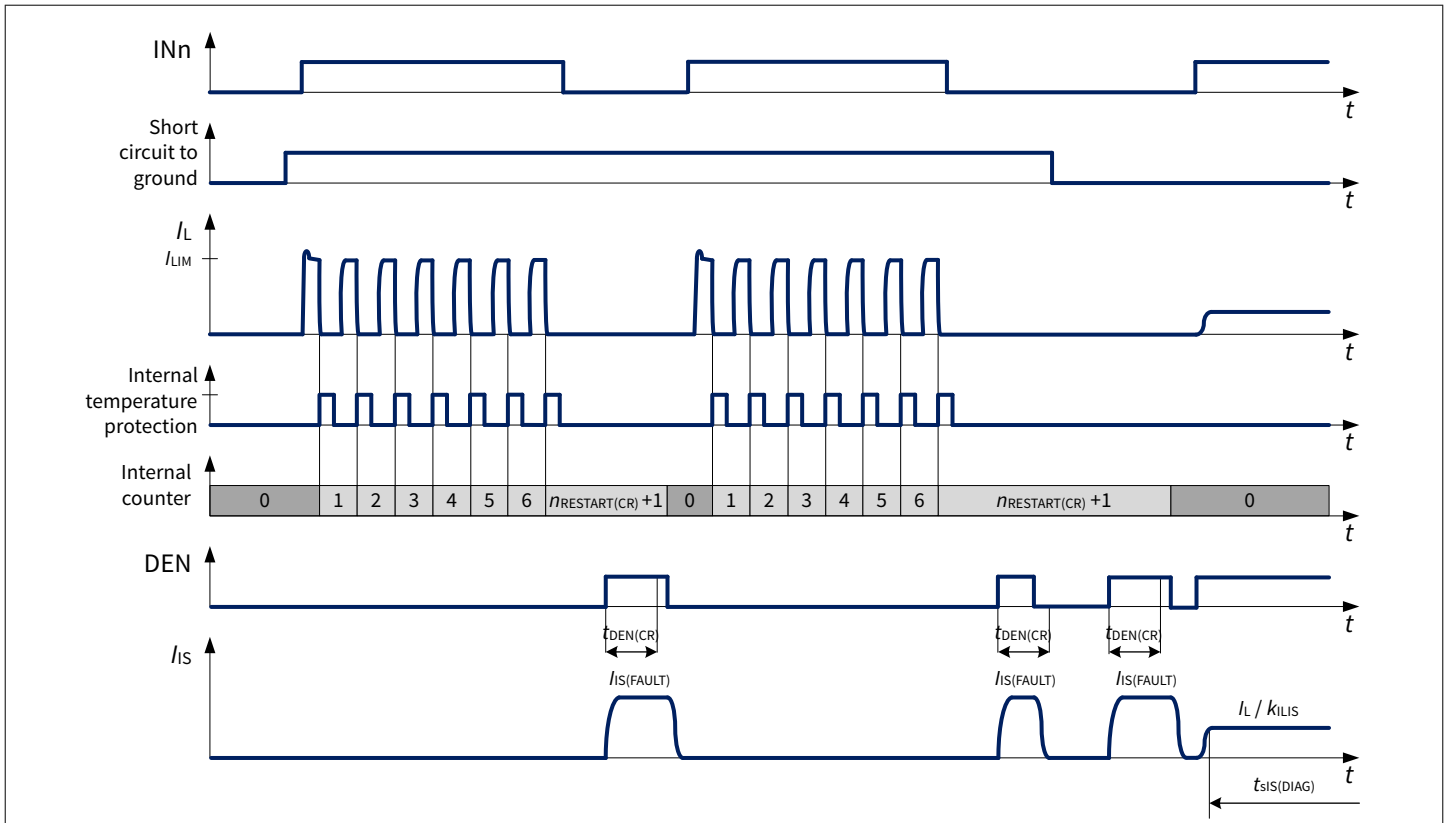
The retry strategy is shown in [Figure 24](#).



**Figure 24** Retry strategy timing diagram

It is possible to “force” a reset of the internal counter without waiting for  $t_{DELAY(CR)}$  by applying a pulse (rising edge followed by a falling edge) to the DEN pin while IN pin is “low”. The pulse applied to DEN pin must have a duration longer than  $t_{DEN(CR)}$  to ensure a reset of the internal counter. The DSEL pin must select the channel that has to be de-latched and keep the same logic value while DEN pin toggles twice (rising edge followed by a falling edge).

The timings are shown in [Figure 25](#).



**Figure 25** Retry strategy timing diagram with forced reset

## 7.4 Additional protection

### 7.4.1 Reverse polarity protection

In reverse polarity condition (also known as reverse battery), power dissipation is caused by the intrinsic body diode of the DMOS channel. Each ESD diode of the logic contributes to total power dissipation. The reverse current through the output stages must be limited by the connected loads. The current through digital input pins has to be limited by an external resistor (please refer to the absolute maximum ratings listed in [Table 2](#) and to Application Information in [Chapter 9](#)).

### 7.4.2 Overvoltage protection

In the case of supply voltages between  $V_{S(EXT,UP)}$  and  $V_{BAT(LD)}$ , the output transistors are still operational and follow the input pin.

In addition to the output clamp for inductive loads as described in [Chapter 6.2.2](#), there is a clamp mechanism available for overvoltage protection for the logic and the output channels, monitoring the voltage between  $V_S$  and GND pins ( $V_{S(CLAMP)}$ ).

### 7.4.3 Loss of battery and loss of load

The loss of connection to the battery or the load does not influence device robustness as long as load and wire harness are purely resistive. In case of driving an inductive load, the energy stored in the inductance must be handled.

The device can handle the inductivity of the wire harness up to 10  $\mu\text{H}$  with  $I_{L(NOM),85}$ .

In case of applications where currents and/or the aforementioned inductivity are exceeded, an external suppressor diode (like diode  $D_{Z2}$  shown in [Chapter 9](#)) is recommended to handle the energy and to provide a well-defined path for the load current.

### 7.4.4 Loss of ground

It is recommended to have a resistor connected between any digital input pin and the microcontroller to ensure a channel switch OFF in case of a loss of device ground event (as described in [Chapter 9](#)).

**Note**

In case any digital input pin is pulled to ground (either by a resistor or active) a parasitic ground path is present, which could keep the device operational during a loss of device ground.

### 7.5 Electrical characteristics protection

$V_S = 4\text{ V to }20\text{ V}$ ,  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$

Unless otherwise specified typical values:  $V_S = 13.5\text{ V}$ ,  $T_J = 25^\circ\text{C}$

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

BTS7090-2EPL:  $R_L = 6.8\ \Omega$

**Table 10 Electrical characteristics protection**

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal shutdown temperature (absolute)	$T_{J(ABS)}$	150	175	200	°C	<sup>1) 2)</sup> See <a href="#">Figure 22</a>	PRQ-174
Thermal shutdown hysteresis (absolute)	$T_{HYS(ABS)}$	–	30	–	K	<sup>3)</sup> See <a href="#">Figure 22</a>	PRQ-356
Thermal shutdown temperature (dynamic)	$T_{J(DYN)}$	–	80	–	K	<sup>3)</sup> See <a href="#">Figure 22</a>	PRQ-357
Thermal shutdown temperature (dynamic) in capacitive load switching mode	$T_{J(DYN)_CLS}$	–	40	–	K	<sup>3)</sup>	PRQ-177
Power supply clamping voltage at $T_J = -40^\circ\text{C}$	$V_{S(CLAMP)_{-40}}$	33	36.5	42	V	$I_{VS} = 5\text{ mA}$ $T_J = -40^\circ\text{C}$ See <a href="#">Chapter 6.2.2</a>	PRQ-179
Power supply clamping voltage at $T_J \geq 25^\circ\text{C}$	$V_{S(CLAMP)_{25}}$	35	38	44	V	<sup>2)</sup> $I_{VS} = 5\text{ mA}$ $T_J \geq 25^\circ\text{C}$ See <a href="#">Chapter 6.2.2</a>	PRQ-184
Automatic restarts in case of fault after counter reset	$n_{RESTART(CR)}$	–	6	–	–	<sup>1)</sup> See <a href="#">Figure 24</a>	PRQ-186
Counter reset delay time after fault condition	$t_{DELAY(CR)}$	40	70	100	ms	<sup>1)</sup> See <a href="#">Figure 24</a>	PRQ-188
Minimum DEN pulse duration for counter reset	$t_{DEN(CR)}$	50	100	150	µs	<sup>3)</sup> See <a href="#">Figure 25</a>	PRQ-190

(table continues...)



**Table 10** (continued) **Electrical characteristics protection**

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
<b>Overcurrent limitation</b>							
Overcurrent limitation	$I_{LIM}$	3.7	4.7	5.7	A	<sup>4)</sup> $V_{DS} = 3\text{ V}$	PRQ-831

- 1) Functional test only
- 2) Tested at  $T_J = 150^\circ\text{C}$  only
- 3) Not subject to production test - specified by design
- 4) Tested at  $T_J = -40^\circ\text{C}$  only

## 8 Diagnosis

For the purpose of diagnosis, the device provides a proportional sense current signal ( $I_{IS}$ ) at pin IS. In case of disabled diagnostic (DEN pin set to “low”), IS pin becomes high impedance.

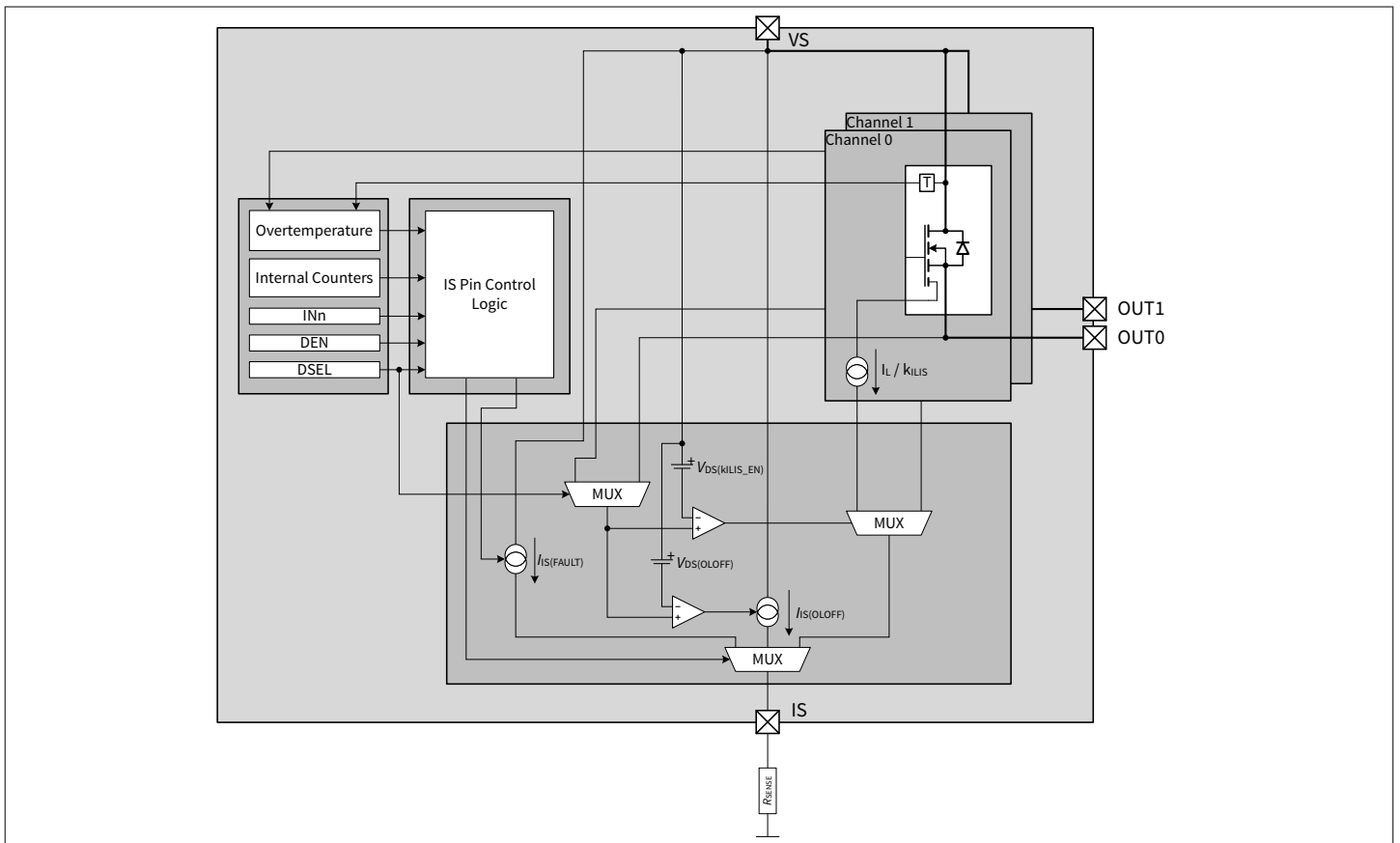
A sense resistor  $R_{SENSE}$  must be connected between IS pin and module ground if the current sense diagnosis is used.

$R_{SENSE}$  value has to be higher than 820  $\Omega$  (or 400  $\Omega$  when a central Reverse Battery protection is present on the battery feed) to limit the power losses in the sense circuitry.

A typical value is  $R_{SENSE} = 1.2 \text{ k}\Omega$ .

Due to the internal connection between IS pin and  $V_S$  supply voltage, it is not recommended to connect the IS pin to the sense current output of other devices, if they are supplied by a different battery feed.

See [Figure 26](#) for details as an overview.



**Figure 26** Diagnosis block diagram

### 8.1 Overview

[Table 11](#) gives a quick reference to the state of the IS pin during the device operation.

**Table 11** SENSE signal as a function of application condition

Operation mode	Input level	DEN level	$V_{OUT}$	Diagnostic output
Normal operation	LOW/OFF	HIGH	$\sim$ GND	Z $I_{IS(FAULT)}$ if $n_{RESTART(CR)} > 0$
Short circuit to GND			$\sim$ GND	Z $I_{IS(FAULT)}$ if $n_{RESTART(CR)} > 0$

(table continues...)

**Table 11** (continued) **SENSE signal as a function of application condition**

Operation mode	Input level	DEN level	V <sub>OUT</sub>	Diagnostic output		
Thermal shutdown temperature (absolute)			Z	I <sub>IS(FAULT)</sub>		
Thermal shutdown temperature (dynamic)			Z	I <sub>IS(FAULT)</sub>		
Short circuit to V <sub>S</sub>			= V <sub>S</sub>	I <sub>IS(OLOFF)</sub> I <sub>IS(FAULT)</sub> if n <sub>RESTART(CR)</sub> > 0		
Open load			< V <sub>S</sub> - V <sub>DS(OLOFF)</sub>	Z		
			> V <sub>S</sub> - V <sub>DS(OLOFF)</sub> <sup>1)</sup>	I <sub>IS(OLOFF)</sub> or I <sub>IS(FAULT)</sub> if n <sub>RESTART(CR)</sub> > 0 for both cases		
Inverse current			~ V <sub>INV</sub> = V <sub>OUT</sub> > V <sub>S</sub>	I <sub>IS(OLOFF)</sub> or I <sub>IS(FAULT)</sub> if n <sub>RESTART(CR)</sub> > 0		
Normal operation			HIGH/ON or CLS		< V <sub>S</sub> - V <sub>DS(kILIS_EN)</sub>	I <sub>IS</sub> = I <sub>L</sub> / k <sub>ILIS</sub>
Short circuit to GND					~ GND	I <sub>IS(FAULT)</sub>
Thermal shutdown temperature (absolute)					Z	I <sub>IS(FAULT)</sub>
Thermal shutdown temperature (dynamic)					Z	I <sub>IS(FAULT)</sub>
Short circuit to V <sub>S</sub>	= V <sub>S</sub>	I <sub>IS</sub> < I <sub>L</sub> / k <sub>ILIS</sub>				
Open load	~ V <sub>S</sub> <sup>2)</sup>	I <sub>IS</sub> = I <sub>IS(EN)</sub>				
Inverse current	~ V <sub>INV</sub> = V <sub>OUT</sub> > V <sub>S</sub>	I <sub>IS</sub> = I <sub>IS(EN)</sub>				
Current limitation	< V <sub>S</sub>	I <sub>IS(FAULT)</sub>				
Underload	~ V <sub>S</sub> <sup>3)</sup>	I <sub>IS(EN)</sub> < I <sub>IS</sub> < I <sub>L(NOM)</sub> / k <sub>ILIS</sub>				
All conditions	n.a.	LOW			n.a.	Z

1) With additional pull up resistor

2) The output current has to be smaller than I<sub>L(OL)</sub>

3) The output current has to be higher than I<sub>L(OL)</sub>

### 8.1.1 SENSE signal truth table

Diagnosis can be activated or deactivated using the DEN pin. Channel selection is done with DSEL pin according to [Table 12](#).

**Table 12** **Diagnostic truth table**

DEN	DSEL	IS
"low"	not relevant	Z
"high"	"low"	SENSE output 0
"high"	"high"	SENSE output 1

## 8.2 Diagnosis in ON state

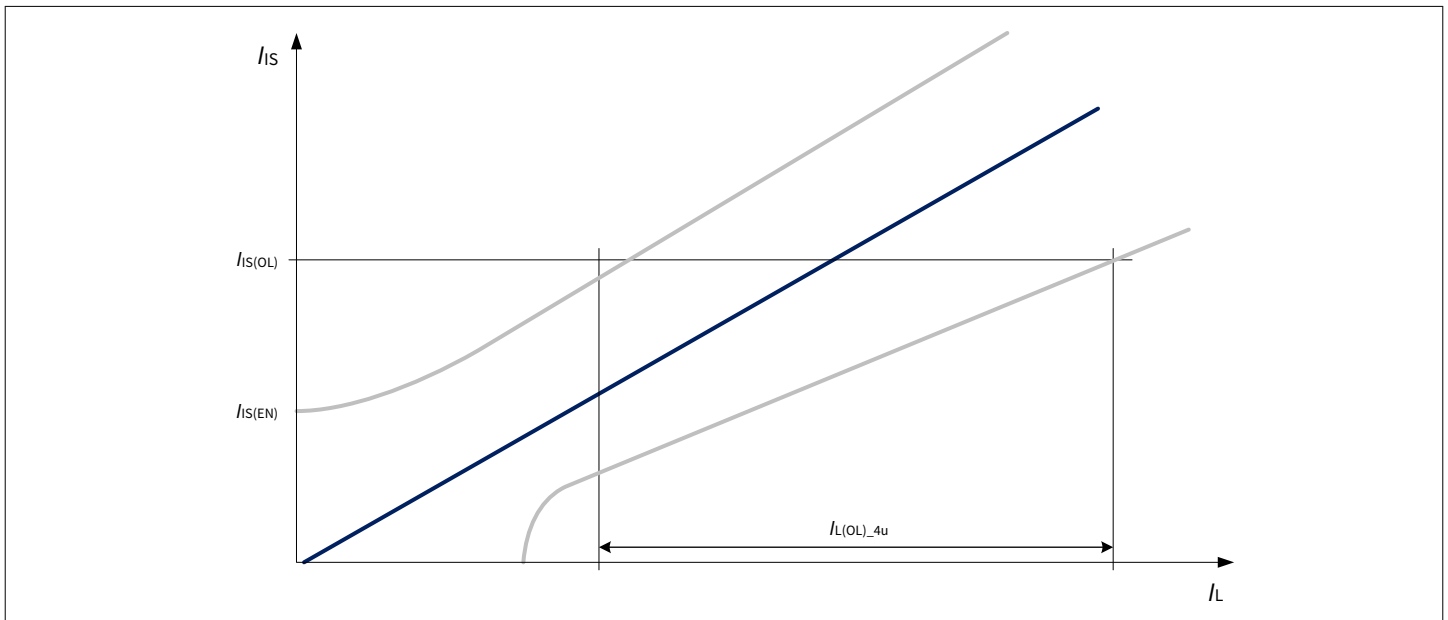
A current proportional to the load current ( $I_{IS} = I_L/k_{ILIS}$ ) is provided at pin IS when the following conditions are fulfilled:

- The power output stage is switched ON with  $V_{DS} < V_{DS(kILIS\_EN)}$
- The diagnosis is enabled for that channel
- No fault (as described in [Chapter 7.3](#)) is present or was present and not cleared yet (see [Chapter 8.2.2](#) for further details)

As long as a fault is present or was present and not cleared yet a current  $I_{IS(FAULT)}$  is provided at IS pin.

### 8.2.1 Current sense (kILIS)

$I_{IS}$  increases linearly with  $I_L$  output current until it reaches the saturation current  $I_{IS(SAT)}$ . In case of open load at the output stage ( $I_L$  close to 0 A), the maximum sense current  $I_{IS(EN)}$  (no load, diagnosis enabled) is specified. This condition is shown in [Figure 27](#). The center line represents the ideal  $k_{ILIS}$ , while the outer lines show the behavior of a typical product. An external RC filter between IS pin and microcontroller ADC input pin is recommended to reduce signal ripple and oscillations (a minimum time constant of 1  $\mu$ s for the RC filter is recommended). The  $k_{ILIS}$  factor is specified with limits that take into account effects due to temperature, supply voltage, and manufacturing process.



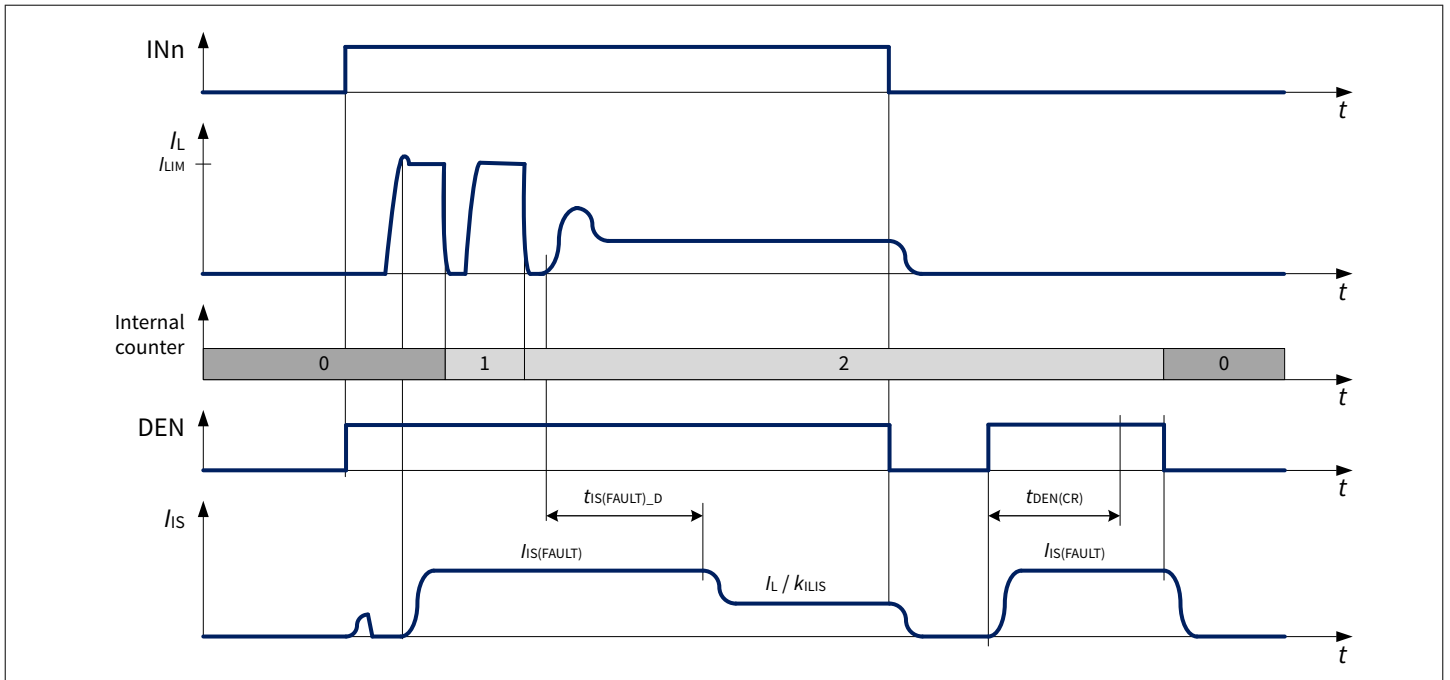
**Figure 27** Current sense ratio in open load at ON condition

### 8.2.2 Fault current (IIS(FAULT))

In case a fault is present and DEN is set to “high” and the affected channel is selected by DSEL, a current  $I_{IS(FAULT)}$  is provided.

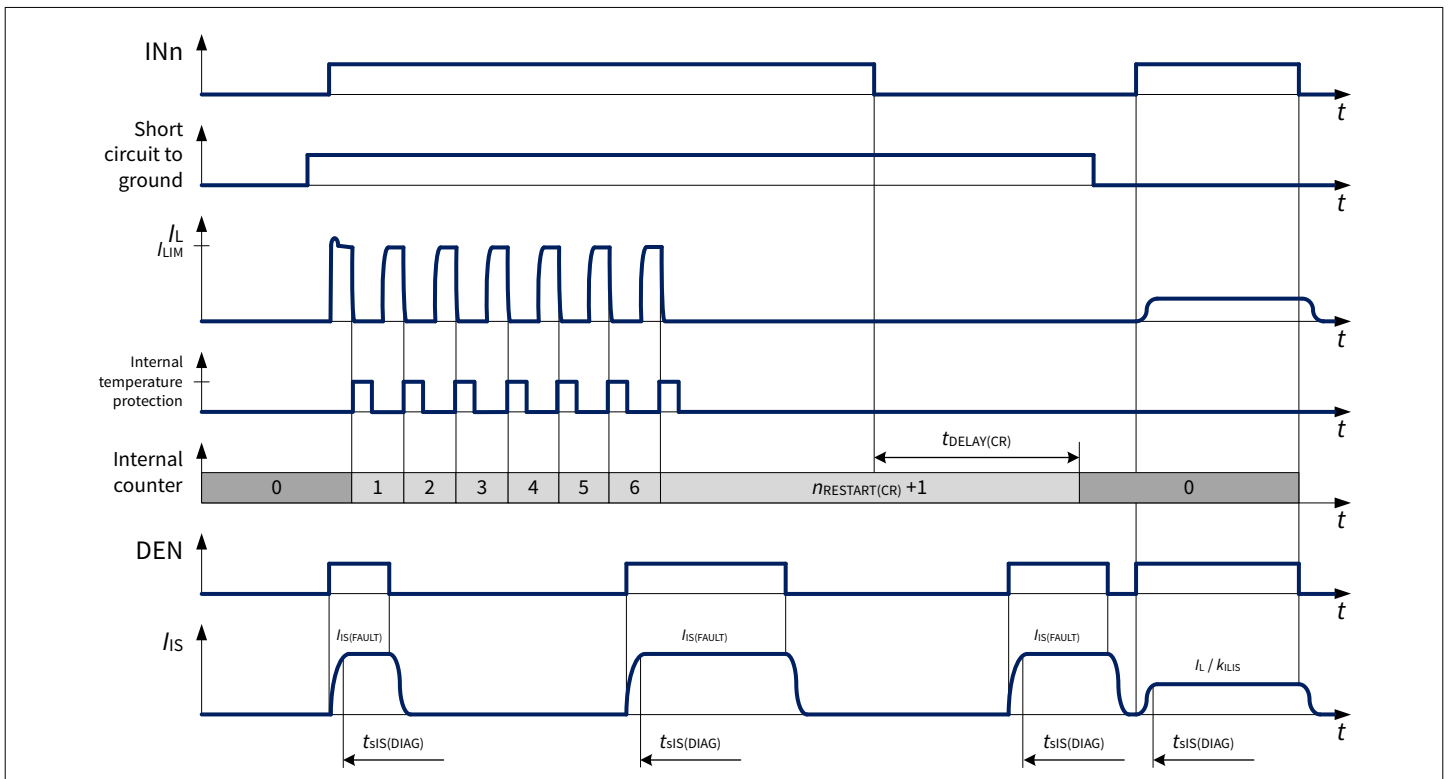
The following situations may occur:

- If the channel is ON and the number of restarts is less than “ $n_{RESTART(CR),TYP}$ ”, the current  $I_{IS(FAULT)}$  is provided for a time  $t_{IS(FAULT)\_D}$  after the channel is allowed to restart, and thereafter  $I_{IS} = I_L/k_{ILIS}$  (as shown in [Figure 28](#)). During a restart cycle the current  $I_{IS(FAULT)}$  is provided each time the channel diagnosis is checked.
- If the channel is ON and the number of restarts is equal to “ $n_{RESTART(CR),TYP}$ ”, the current  $I_{IS(FAULT)}$  is provided until the internal counter is reset. The internal counter can be cleared either by  $INn = \text{“low”}$  for  $t_{DELAY(CR)}$  or by  $INn = \text{“low”}$  and DEN pin pulse for  $t_{DEN(CR)}$ , as described in [Chapter 7.3.1](#).
- While the channel is OFF and the internal counter value is not reset, the current  $I_{IS(FAULT)}$  is provided.

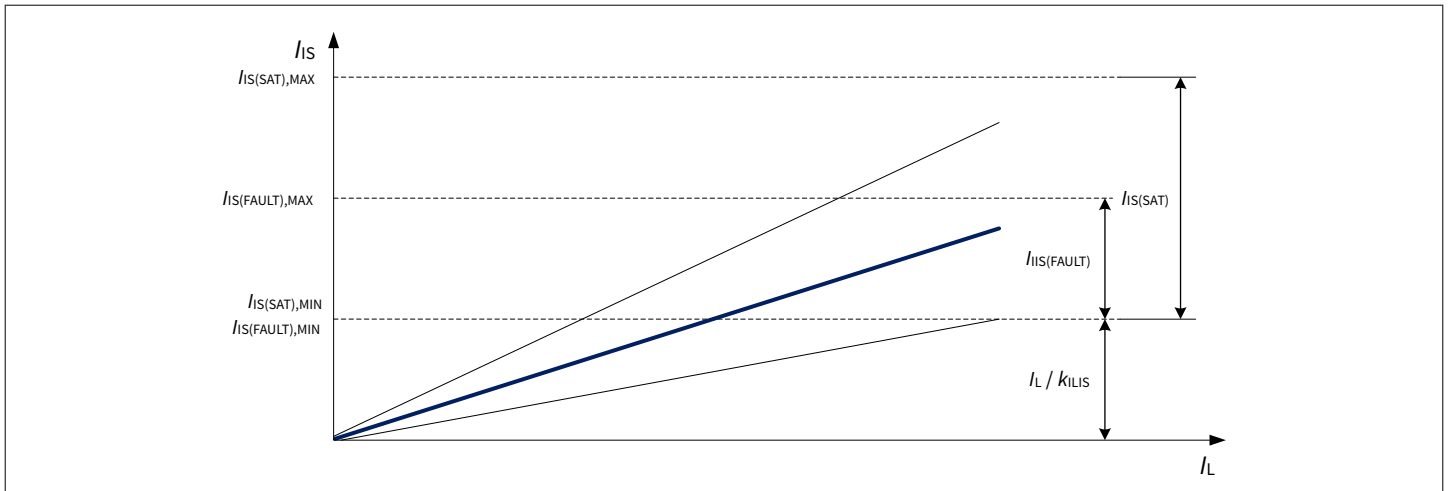


**Figure 28**  $I_{IS(FAULT)}$  at load switching

Figure 29 adds the behavior of SENSE signal to the timing diagram seen in Figure 24, while Figure 30 shows the relation between  $I_{IS} = I_L / k_{ILIS}$ ,  $I_{IS(SAT)}$  and  $I_{IS(FAULT)}$ .



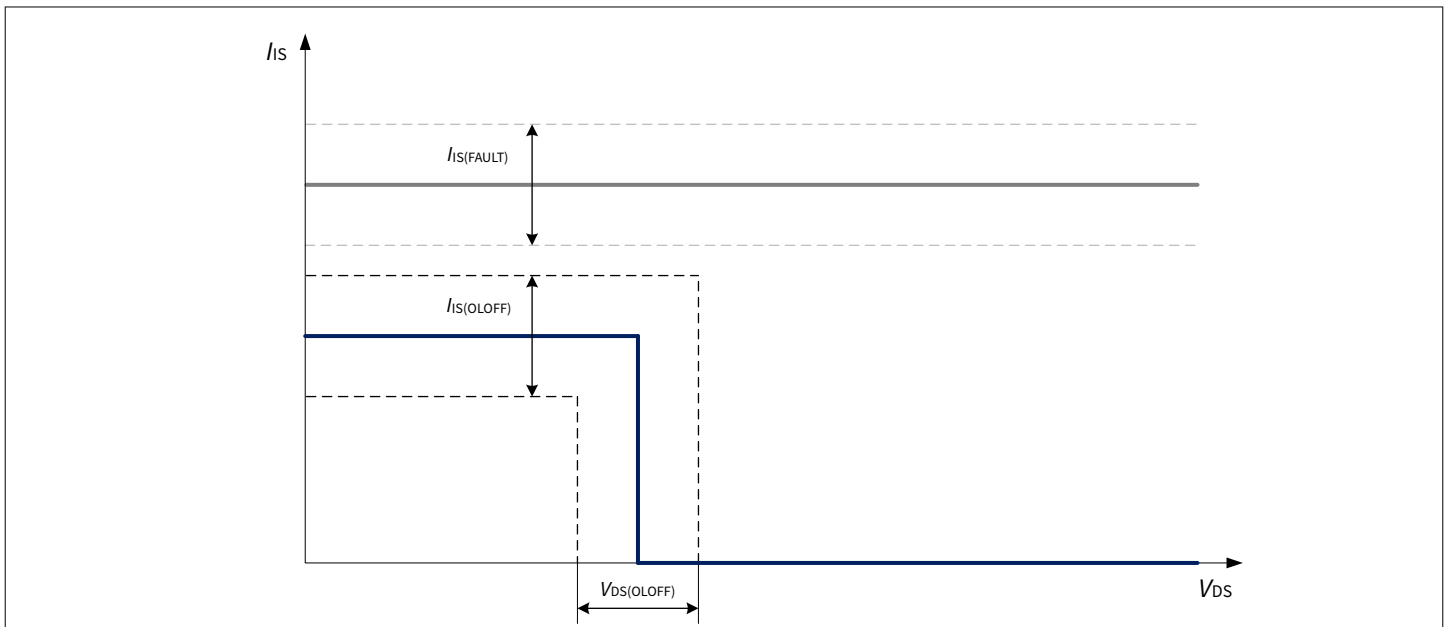
**Figure 29** SENSE behavior in fault condition



**Figure 30** SENSE behavior - overview

### 8.3 Diagnosis in OFF State

When a power output stage is in OFF state, the device can measure the output voltage and compare it with a threshold voltage. In this way, using some additional external components (a pull-down resistor and a switchable pull-up current source), it is possible to detect if the load is missing or if there is a short circuit to battery. If a fault condition was detected by the device (the internal counter has a value different from the reset value, as described in [Chapter 8.2.2](#) a current  $I_{IS(FAULT)}$  is provided by IS pin each time the channel diagnosis is checked also in OFF state. [Figure 31](#) shows the relationship between  $I_{IS(OLOFF)}$  and  $I_{IS(FAULT)}$  as functions of  $V_{DS}$ . The two currents do not overlap making it always possible to differentiate between open load in OFF and fault condition.

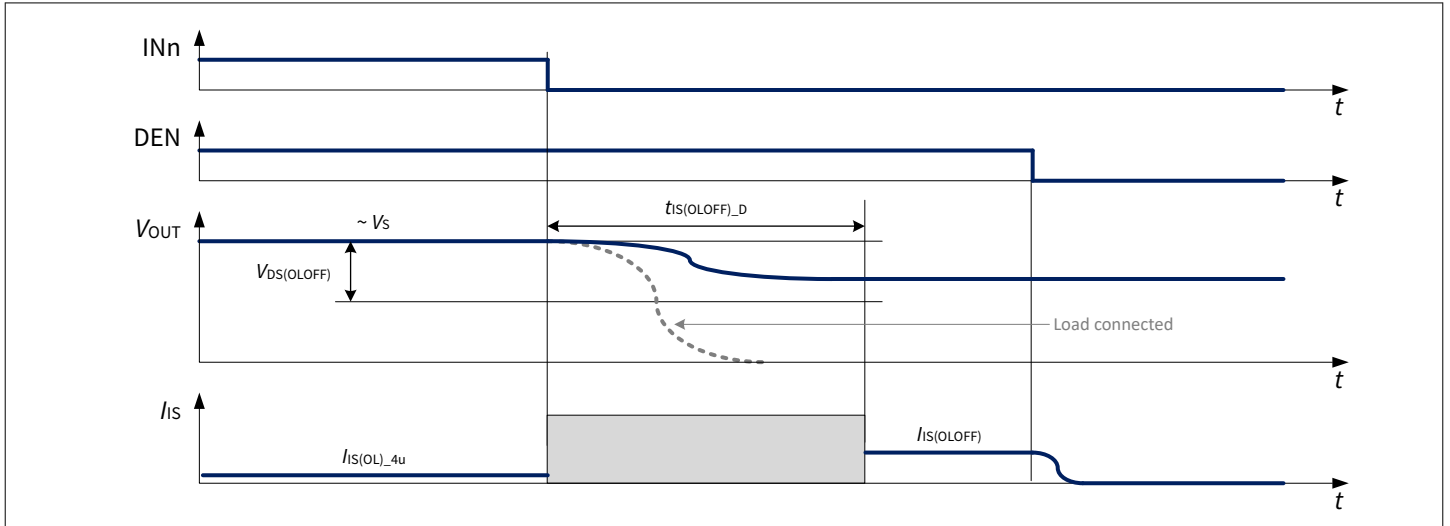


**Figure 31**  $I_{IS}$  in OFF state

#### 8.3.1 Open load current

In OFF state, while DEN pin is set to “high” and a channel is selected using DSEL pin, the  $V_{DS}$  voltage is compared with a threshold voltage  $V_{DS(OLOFF)}$ . When the diagnosis is active and  $V_{DS} \leq V_{DS(OLOFF)}$ , a current  $I_{IS(OLOFF)}$  is provided by IS pin. If the load is properly connected and there is no short circuit to battery,  $V_{DS} \sim V_S$ , therefore,  $V_{DS} > V_{DS(OLOFF)}$  the IS pin is set to high impedance.

It is necessary to wait a time  $t_{IS(OLOFF)_D}$  between the falling edge of the input pin and the sensing at pin IS for Open Load in OFF diagnosis to allow the internal comparator to settle. In Figure 32 the timings for an Open Load detection are shown - the load is always disconnected.

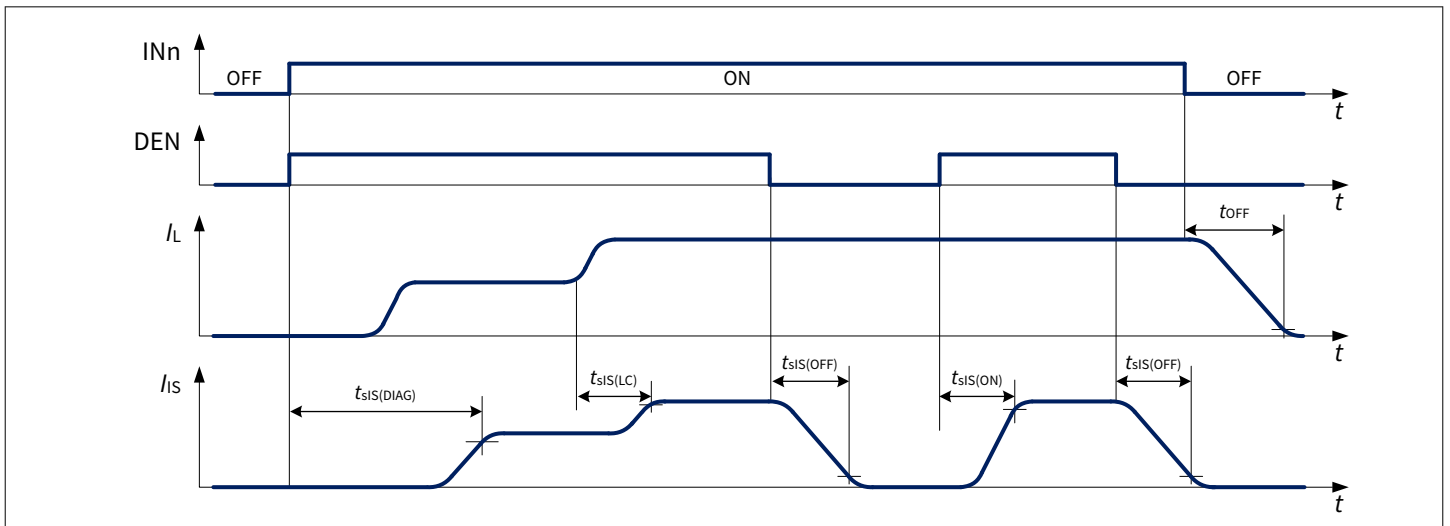


**Figure 32** Open load in OFF timings - load disconnection

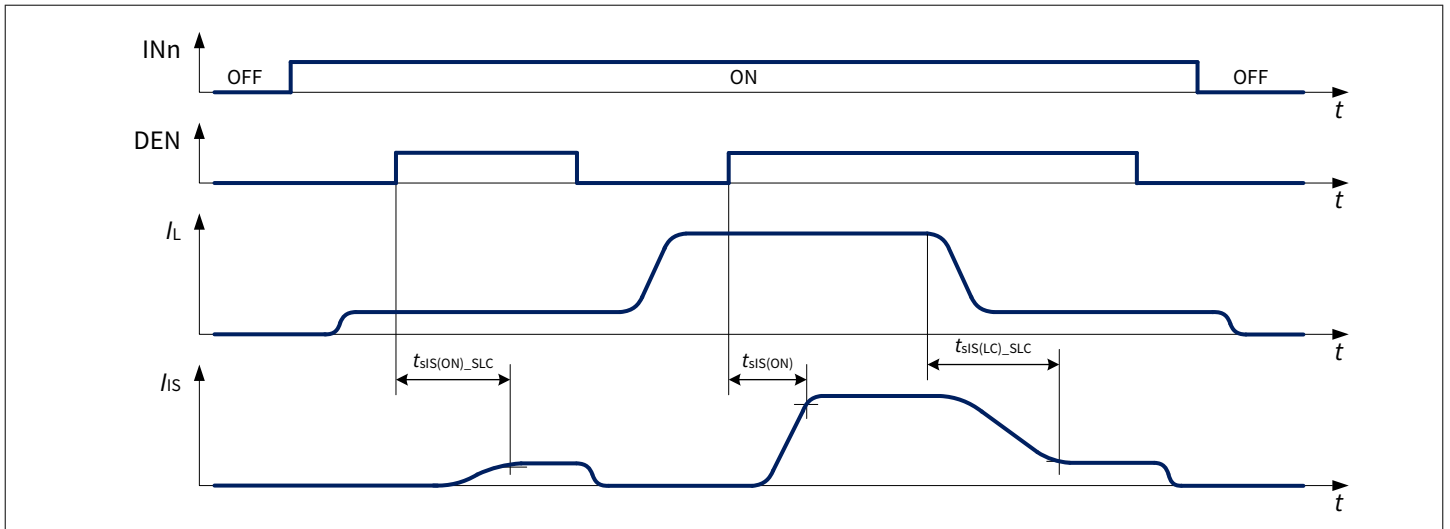
### 8.4 SENSE timings

Figure 33 and Figure 34 show the timing during settling  $t_{SIS(ON)}$  and disabling  $t_{SIS(OFF)}$  of the SENSE (including the case of load change). As a proper signal cannot be established before the load current is stable (therefore before  $t_{ON}$ ),

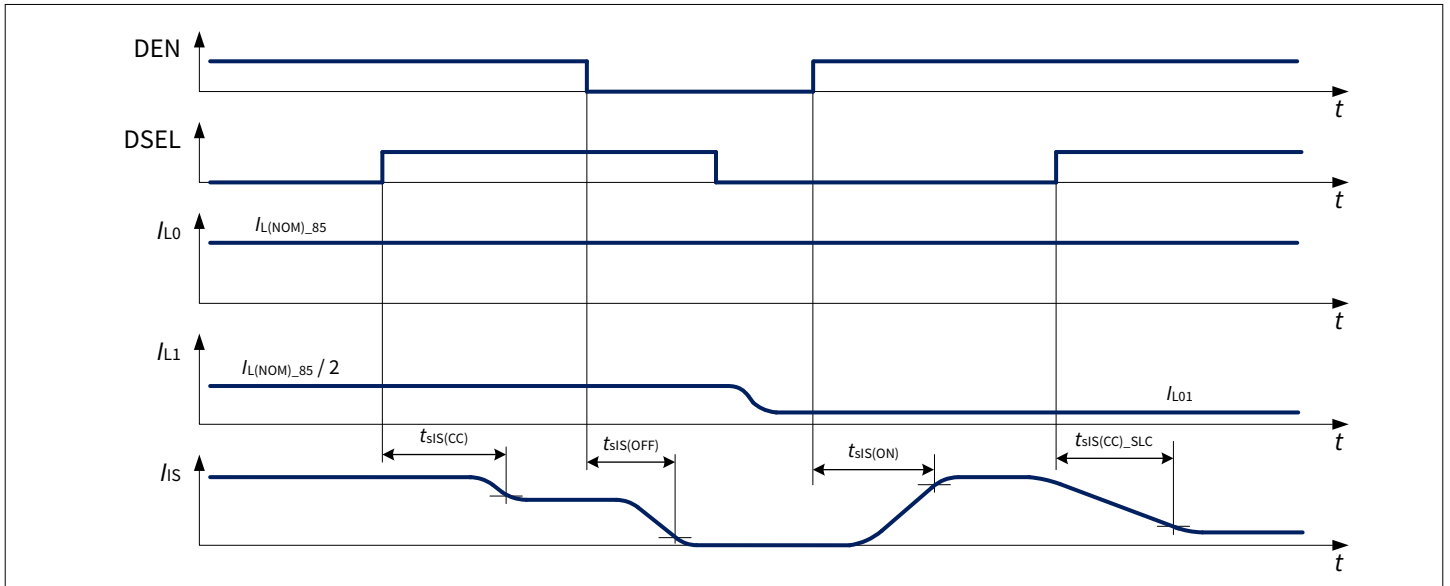
$$t_{SIS(DIAG)} = t_{SIS(ON)} + t_{ON} \quad (2)$$



**Figure 33** SENSE settling/disabling timing



**Figure 34** SENSE timing with small load current



**Figure 35** SENSE settling timing - channel change

## 8.5 Electrical characteristics diagnosis

$V_S = 4\text{ V to }20\text{ V}$ ,  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$

Unless otherwise specified typical values:  $V_S = 13.5\text{ V}$ ,  $T_J = 25^\circ\text{C}$

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

BTS7090-2EPL:  $R_L = 6.8\ \Omega$



**Table 13** Electrical characteristics diagnosis

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SENSE saturation current	$I_{IS(SAT)}$	4.4	–	15	mA	<sup>1)</sup> $V_S = 6\text{ V to }20\text{ V}$ $R_{SENSE} = 1.2\text{ k}\Omega$ See <a href="#">Figure 30</a>	PRQ-215
SENSE leakage current when disabled	$I_{IS(OFF)}$	–	0.01	0.5	$\mu\text{A}$	DEN = "low" $I_L \geq I_{L(NOM)}$ $V_{IS} = 0\text{ V}$	PRQ-219
SENSE leakage current when enabled at $T_J \leq 85^\circ\text{C}$	$I_{IS(EN)_85}$	–	0.2	2	$\mu\text{A}$	<sup>1)</sup> $T_J \leq 85^\circ\text{C}$ DEN = "high" $I_L = 0\text{ A}$ See <a href="#">Figure 27</a>	PRQ-221
SENSE leakage current when enabled at $T_J = 150^\circ\text{C}$	$I_{IS(EN)_150}$	–	0.2	2	$\mu\text{A}$	$T_J = 150^\circ\text{C}$ DEN = "high" $I_L = 0\text{ A}$ See <a href="#">Figure 27</a>	PRQ-223
Saturation voltage in kILIS operation (VS-VIS)	$V_{SIS\_k}$	–	0.5	1	V	<sup>1)</sup> $V_S = 5\text{ V}$ IN = DEN = "high"	PRQ-226
Saturation voltage in open load at OFF diagnosis (VS-VIS)	$V_{SIS\_OL}$	–	0.5	1	V	<sup>1)</sup> $V_S = 5\text{ V}$ IN = "low" DEN = "high"	PRQ-682
Saturation voltage in fault diagnosis (VS-VIS)	$V_{SIS\_F}$	–	0.5	1	V	<sup>1)</sup> $V_S = 5\text{ V}$ IN = "low" DEN = "high" counter > 0	PRQ-684
Power supply to IS pin clamping voltage at $T_J = -40^\circ\text{C}$	$V_{SIS(CLAMP)\_-40}$	33	36.5	42	V	$I_{IS} = 1\text{ mA}$ $T_J = -40^\circ\text{C}$ See <a href="#">Chapter 6.2.2</a>	PRQ-294
Power supply to IS pin clamping voltage at $T_J \geq 25^\circ\text{C}$	$V_{SIS(CLAMP)\_25}$	35	38	44	V	<sup>2)</sup> $I_{IS} = 1\text{ mA}$ $T_J \geq 25^\circ\text{C}$ See <a href="#">Chapter 6.2.2</a>	PRQ-296
SENSE fault current	$I_{IS(FAULT)}$	4.4	5.5	10	mA	See <a href="#">Chapter 8</a>	PRQ-298

**(table continues...)**

**Table 13 (continued) Electrical characteristics diagnosis**

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SENSE open load in OFF current	$I_{IS(OLOFF)}$	1.9	2.5	3.5	mA	See <a href="#">Chapter 8</a>	PRQ-306
SENSE delay time at channel switch ON after last fault condition	$t_{IS(FAULT)_D}$	–	500	–	$\mu\text{s}$	<sup>1)</sup> See <a href="#">Figure 28</a>	PRQ-308
SENSE open load in OFF delay time	$t_{IS(OLOFF)_D}$	70	185	300	$\mu\text{s}$	$V_{DS} < V_{DS(OLOFF)}$ from INn falling edge to $I_{IS} = I_{IS(OLOFF),MIN} \cdot 0.9$ DEN = "high" $n_{RESTART(CR)} = 0$ See <a href="#">Figure 32</a>	PRQ-310
VDS threshold for KILIS enable	$V_{DS(KILIS\_EN)}$	0.8	1.2	1.4	V	<sup>1)</sup>	PRQ-809
Open load VDS detection threshold in OFF state	$V_{DS(OLOFF)}$	1.3	1.8	2.3	V	See <a href="#">Chapter 8.3</a>	PRQ-313
SENSE settling time with nominal load current stable	$t_{SIS(ON)}$	–	5	20	$\mu\text{s}$	$I_L = I_{L(NOM)}$ from DEN rising edge to $I_{IS} = I_L / (k_{ILIS,MAX} @ I_L) \cdot 0.9$ See <a href="#">Figure 33</a>	PRQ-315
SENSE settling time with small load current stable	$t_{SIS(ON)_SLC}$	–	–	60	$\mu\text{s}$	<sup>1)</sup> $I_L = I_{L01}$ from DEN rising edge to $I_{IS} = I_L / (k_{ILIS,MAX} @ I_L) \cdot 0.9$ See <a href="#">Figure 34</a>	PRQ-317
SENSE disable time	$t_{SIS(OFF)}$	–	5	20	$\mu\text{s}$	<sup>1)</sup> $I_L = I_{L(NOM)}$ From DEN falling edge to $I_{IS} = I_{IS(OFF)}$ See <a href="#">Figure 33</a>	PRQ-319
SENSE settling time after load change	$t_{SIS(LC)}$	–	5	20	$\mu\text{s}$	<sup>1)</sup> from $I_L = I_{L(NOM)}/2$ to $I_L = I_{L(NOM)}$ See <a href="#">Figure 33</a>	PRQ-321
SENSE settling time after load change with small load current	$t_{SIS(LC)_SLC}$	–	250	400	$\mu\text{s}$	<sup>1)</sup> DEN = "high" from load change to $I_{IS} = I_L / (k_{ILIS} @ I_L)$ from $I_{L(NOM)}$ to $I_{L01}$ See <a href="#">Figure 34</a>	PRQ-323

**(table continues...)**

**Table 13** (continued) **Electrical characteristics diagnosis**

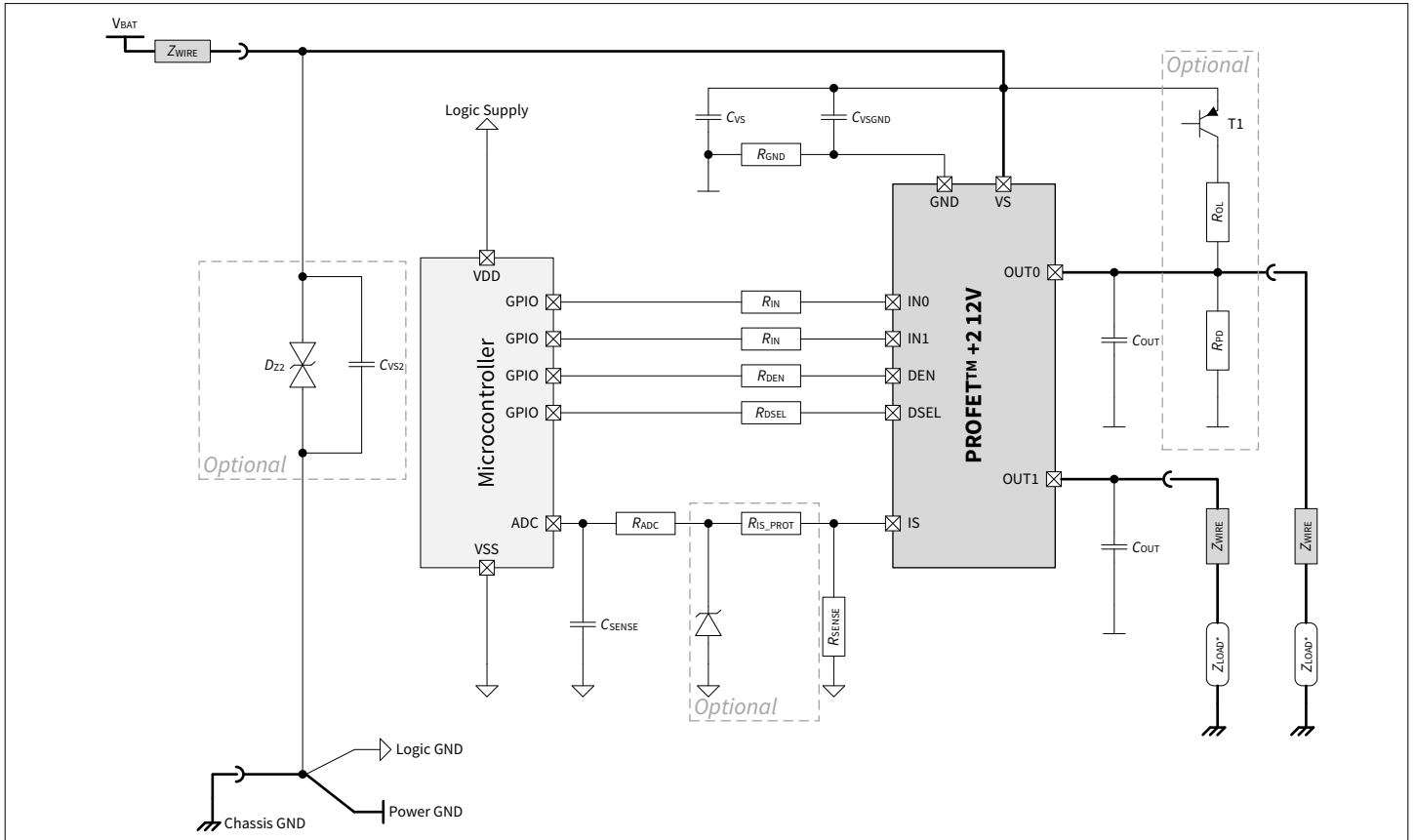
Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SENSE settling time after channel change	$t_{SIS(CC)}$	–	5	20	$\mu\text{s}$	1) Start channel: $I_L = I_{L(NOM)}$ End channel: $I_L = I_{L(NOM)}/2$ See <a href="#">Figure 35</a>	PRQ-326
SENSE settling time after channel change with small load current	$t_{SIS(CC\_SLC)}$	–	–	60	$\mu\text{s}$	1) DEN = “high” from DSEL toggling to $I_{IS} = I_L / (k_{ILIS,MIN} @ I_L) \cdot 1.1$ Start channel: $I_L = I_{L(NOM)}$ End Channel: $I_L = I_{L01}$ See <a href="#">Figure 35</a>	PRQ-327
Open load output current at $I_{IS} = 4 \mu\text{A}$	$I_{L(OL\_4u)}$	1	4	8	mA	$I_{IS} = I_{IS(OL)} = 4 \mu\text{A}$	PRQ-329
Current sense ratio at $I_L = I_{L01}$	$k_{ILIS01}$	-27%	1100	+27%	–	$I_{L01} = 10 \text{ mA}$	PRQ-333
Current sense ratio at $I_L = I_{L02}$	$k_{ILIS02}$	-25%	1000	+25%	–	$I_{L02} = 20 \text{ mA}$	PRQ-335
Current sense ratio at $I_L = I_{L04}$	$k_{ILIS04}$	-24%	1000	+24%	–	$I_{L04} = 50 \text{ mA}$	PRQ-337
Current sense ratio at $I_L = I_{L08}$	$k_{ILIS08}$	-10%	1000	+10%	–	$I_{L08} = 250 \text{ mA}$	PRQ-341
Current sense ratio at $I_L = I_{L09}$	$k_{ILIS09}$	-8.8%	1000	+8.8%	–	$I_{L09} = 450 \text{ mA}$	PRQ-342
Current sense ratio at $I_L = I_{L11}$	$k_{ILIS11}$	-6%	1000	+6%	–	$I_{L11} = 1 \text{ A}$	PRQ-344
Current sense ratio at $I_L = I_{L13}$	$k_{ILIS13}$	-5%	1000	+5%	–	$I_{L13} = 2 \text{ A}$	PRQ-346

1) Not subject to production test - specified by design

2) Tested at  $T_J = 150^\circ\text{C}$

## 9 Application information

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*



**Figure 36** Application diagram

**Table 14** Suggested component values

Reference	Value	Purpose
$R_{IN}$	4.7 k $\Omega$	Protection of the microcontroller during overvoltage and reverse polarity. Necessary to switch OFF the output during loss of ground
$R_{DEN}$	4.7 k $\Omega$	Protection of the microcontroller during overvoltage and reverse polarity. Necessary to switch OFF the output during loss of ground
$R_{DSEL}$	4.7 k $\Omega$	Protection of the microcontroller during overvoltage and reverse polarity. Necessary to switch OFF the output during loss of ground
$R_{PD}$	47 k $\Omega$	Output polarization (pull-down). Ensures polarization of the outputs to distinguish between open load and short to VS in OFF diagnosis
$R_{OL}$	1.5 k $\Omega$	Output polarization (pull-up). Ensure polarization of the output during open load in OFF diagnosis
$C_{OUT}$	10 nF	Protection of the output during ESD events and BCI
$T_1$	BC 807	Switch the battery voltage for open load in OFF diagnosis
$C_{VS}$	100 nF	Filtering of voltage spikes on the battery line
$C_{VSGND}$	47 nF	Buffer capacitor for fast transient

(table continues...)  
 Datasheet

**Table 14** (continued) **Suggested component values**

Reference	Value	Purpose
$D_{Z2}$	33V TVS Diode	Transient voltage suppressor diode. Protection during overvoltage and in case of loss of battery while driving an inductive load
$C_{VS2}$	–	Filtering/buffer capacitor located at VBAT connector
$R_{SENSE}$	1.2 k $\Omega$	SENSE resistor
$R_{IS\_PROT}$	4.7 k $\Omega$	Protection during overvoltage, reverse polarity, loss of ground. Value to be tuned according to microcontroller specifications
$D_{Z1}$	7V Z-Diode	Protection of microcontroller during overvoltage
$R_{ADC}$	4.7 k $\Omega$	Protection of microcontroller ADC input during overvoltage, reverse polarity, loss of ground. Value to be tuned according to microcontroller specifications
$C_{SENSE}$	220 pF	Sense signal filtering. A time constant ( $R_{ADC} \cdot C_{SENSE}$ ) longer than 1 $\mu$ s is recommended
$R_{GND}$	47 $\Omega$	Protection in case of overvoltage and loss of battery while driving inductive loads

- Please contact us for information regarding the pin behavior assessment
- For further information you may contact <http://www.infineon.com>

10 Package outlines

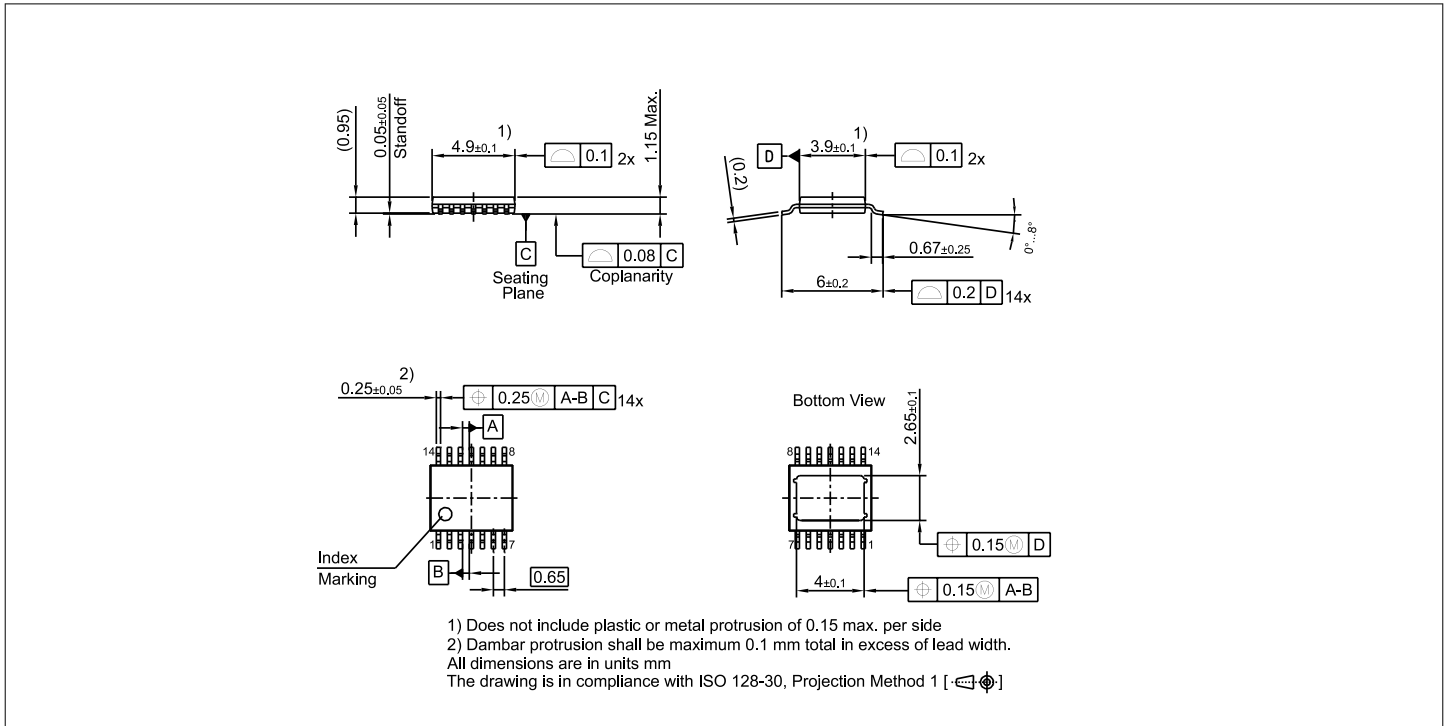


Figure 37 PG-TSDSO-14 dual small outline package dimensions

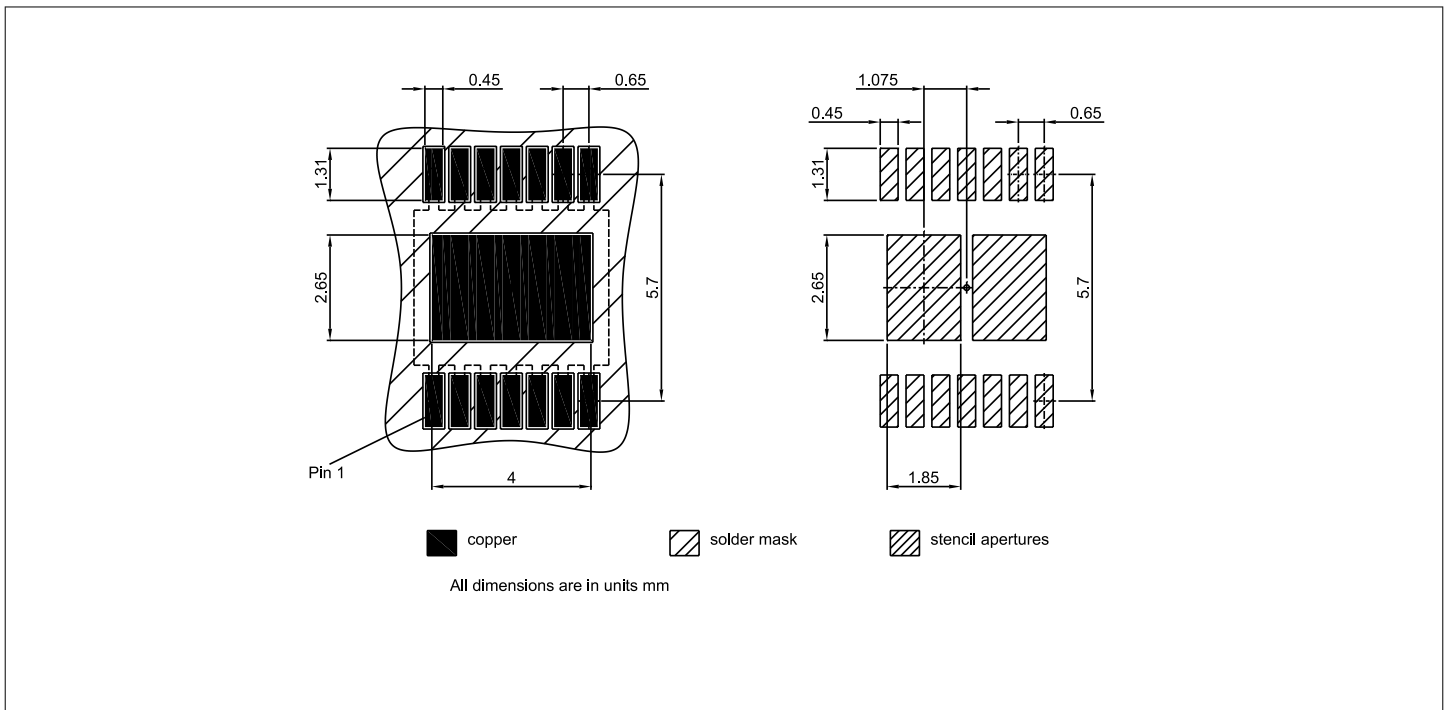


Figure 38 PG-TSDSO-14 dual small outline footprint dimensions

Note: To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages <https://www.infineon.com/packages>

## **11**            **Revision history**

**Table 15**            **Revision history**

<b>Document version</b>	<b>Date of release</b>	<b>Description of changes</b>
Rev.1.00	2022-09-20	Initial Datasheet

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**Edition 2022-09-20**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**

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