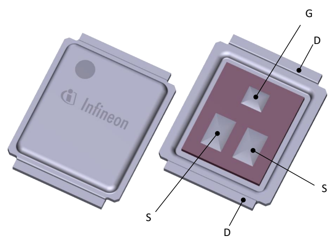
MOSFET

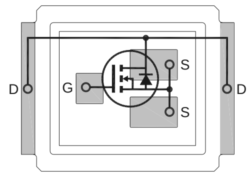
OptiMOS™3 Power-MOSFET, 60 V

DirectFET™



Features

- Optimized technology for DC/DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Superior thermal resistance
- Dual sided cooling
- low parasitic inductance
- Low profile (<0.7mm)
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant



Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	2.8	mΩ
I_D	90	A

Type / Ordering code	Package	Marking	Related links
BSB028N06NN3 G	MG-WDSON-5	0106	-

Table of contents

1 Maximum ratings

at T_j=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	90 85 22	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=58 K/W [1)
Pulsed drain current [2)	$I_{D,pulse}$	-	-	360	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	590	mJ	I_D=30 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	78 2.2	W -	T_C=25 °C T_A=25 °C, R_{thJA}=58 K/W [1)
Operating and storage temperature	T_j, T_{stg}	-40	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

1) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

2) See figure 3 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	1.0	-	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	1.6	K/W	
Device on PCB, 6 cm^2 cooling area [3)]	R_{thJA}	-	-	58	K/W	

3) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2	3	4	V	V_{DS}=V_{GS}, I_D=102 µA
Zero gate voltage drain current	I_{DSS}	-	0.1 10	10 100	µA	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	2.2	2.8	m	V_{GS}=10 V, I_D=30 A
Gate resistance	R_G	-	0.5	-	Ω	-
Transconductance	g_{fs}	42	83	-	S	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=30 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [4)]	C_{iss}	-	8800	12000	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Output capacitance [4)]	C_{oss}	-	2100	2800	pF	
Reverse transfer capacitance [4)]	C_{rss}	-	64	-	pF	
Turn-on delay time	$t_{d(on)}$	-	21	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	9	-	ns	
Turn-off delay time	$t_{d(off)}$	-	38	-	ns	
Fall time	t_f	-	6	-	ns	

4) See figure 13 for more detailed information

Table 6 Gate charge characteristics [5)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	41	-	nC	V_{DD}=30 V, I_D=30 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	8	-	nC	
Switching charge	Q_{sw}	-	23	-	nC	
Gate charge total	Q_g	-	108	143	nC	
Gate plateau voltage	$V_{plateau}$	-	4.6	-	V	
Output charge	Q_{oss}	-	87	116	-	V_{DD}=30 V, V_{GS}=0 V

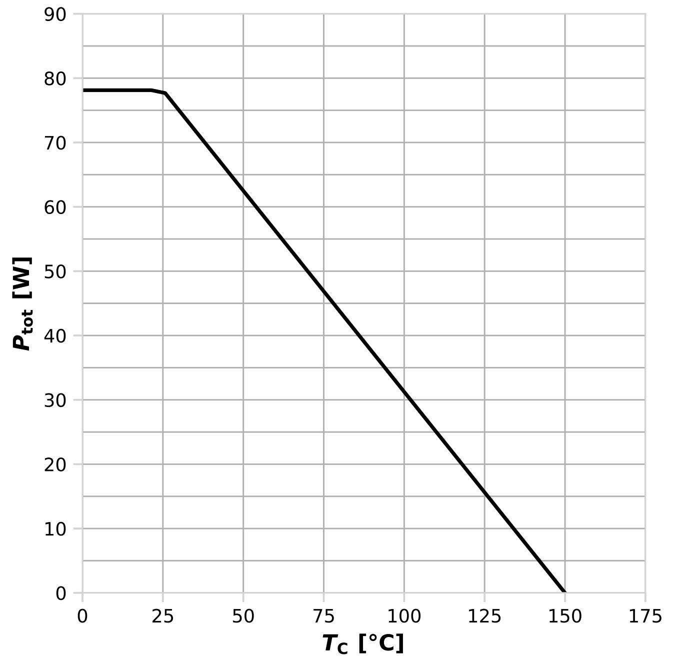
5) See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	30	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	120	A	
Diode forward voltage	V_{SD}	-	0.8	1.2	V	V_{GS}=0 V, I_F=30 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	60	-	ns	V_R=30 V, I_F=I_S, di_F/dt=100 A/µs
Reverse recovery charge	Q_{rr}	-	87	-	nC	

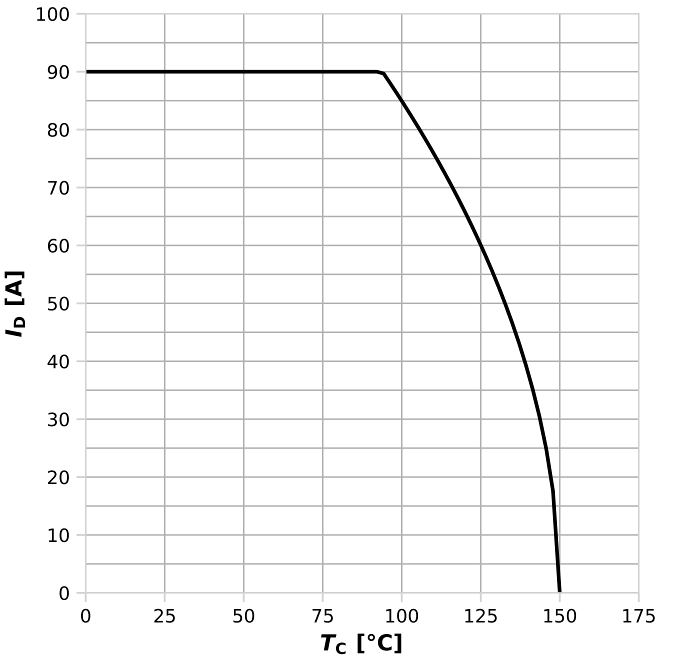
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



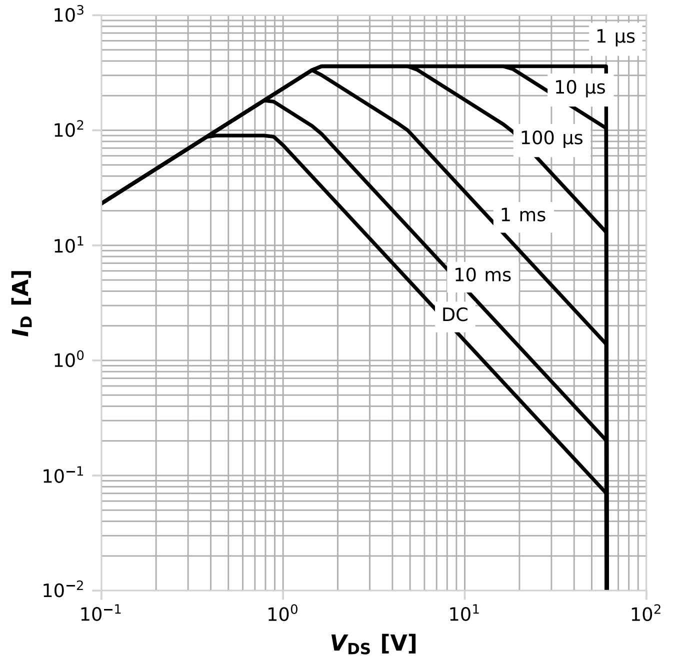
P_{tot}=f(T_C)

Diagram 2: Drain current



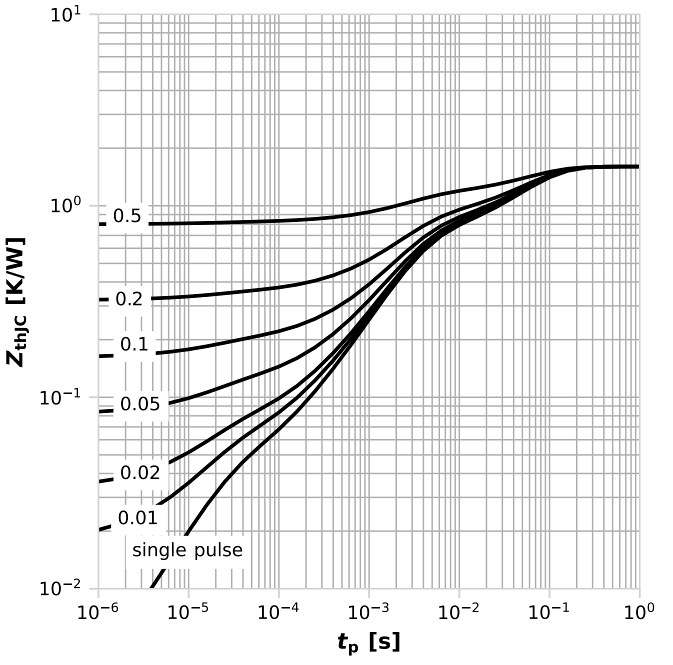
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



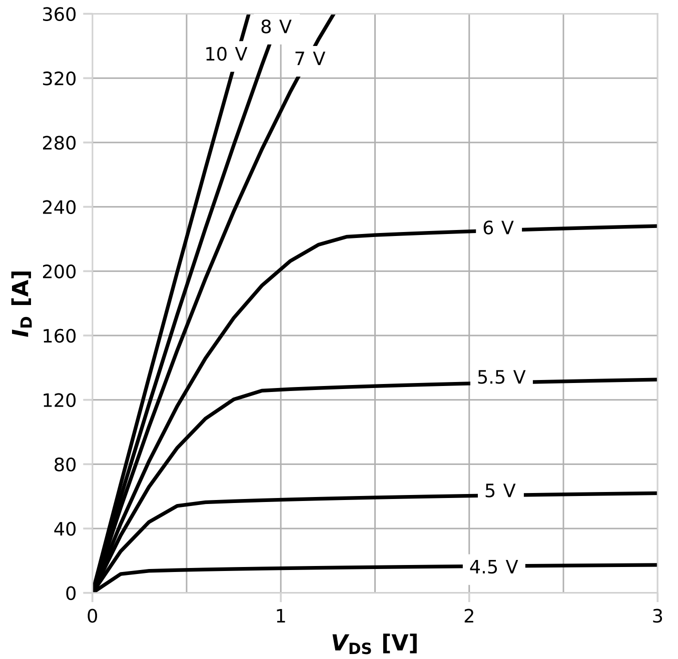
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



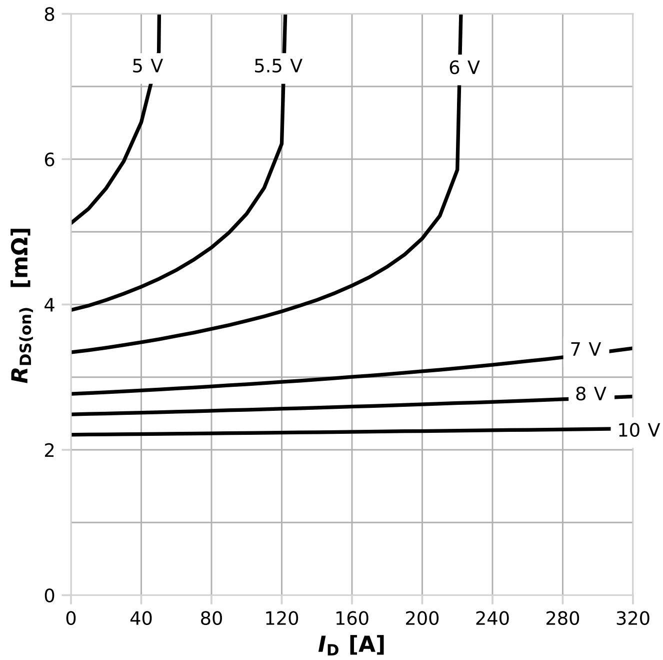
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



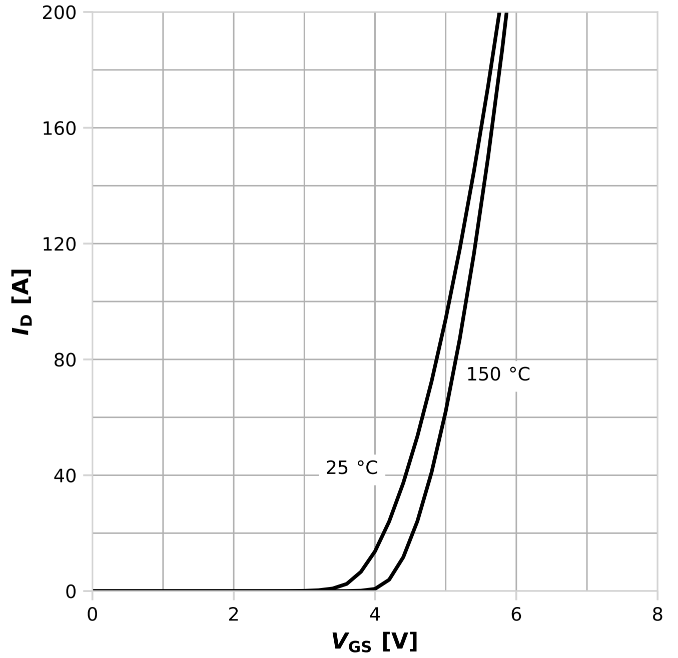
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



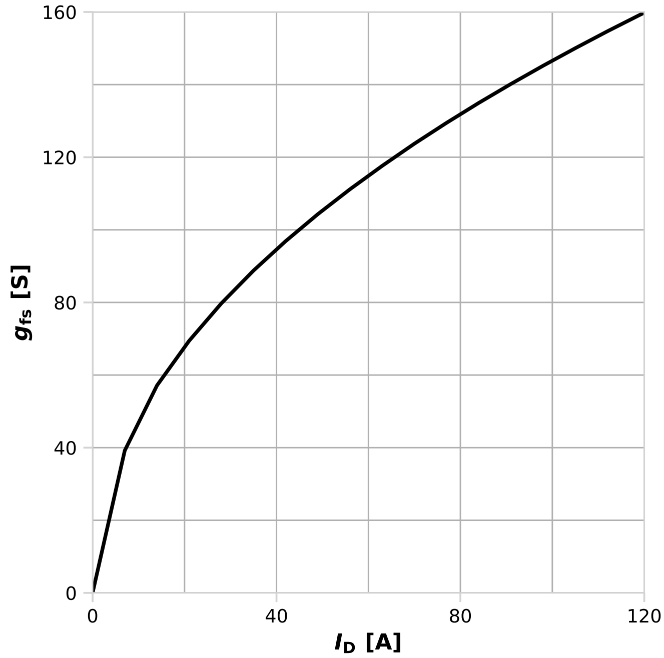
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



I_D=f(V_{GS}); $|V_{DS}|$>2$|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



g_{fs}=f(I_D); T_j=25 °C

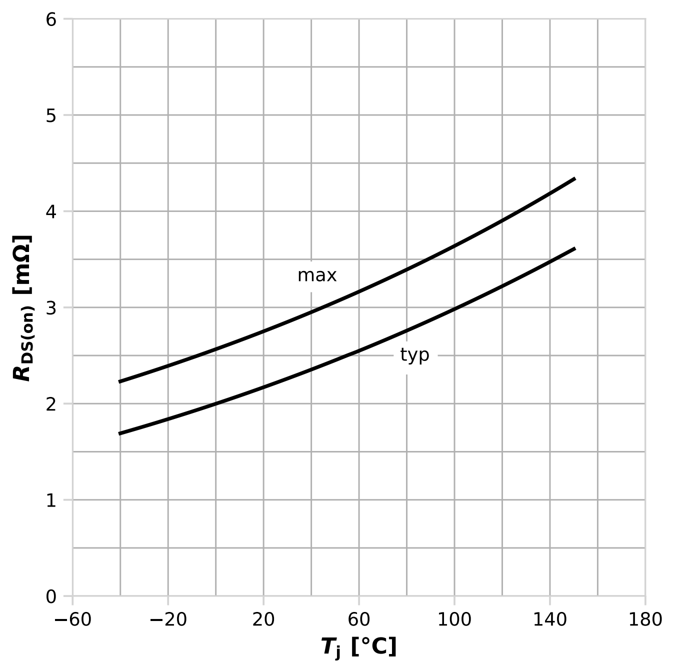
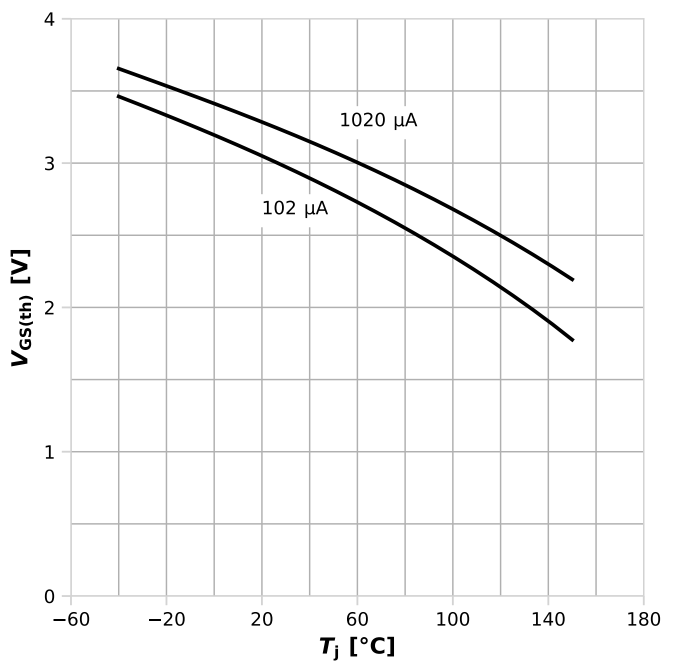
Diagram 9: Drain-source on-state resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j); I_D=30 A; V_{GS}=10 V	$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}

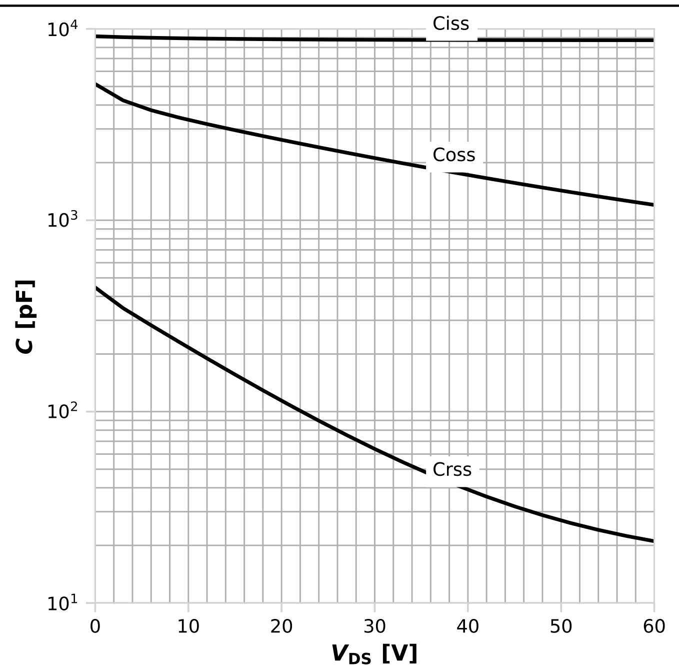
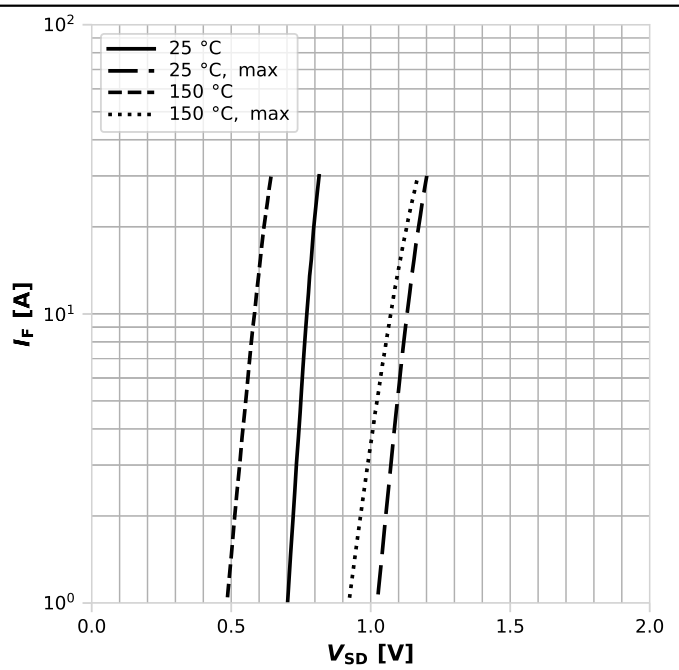
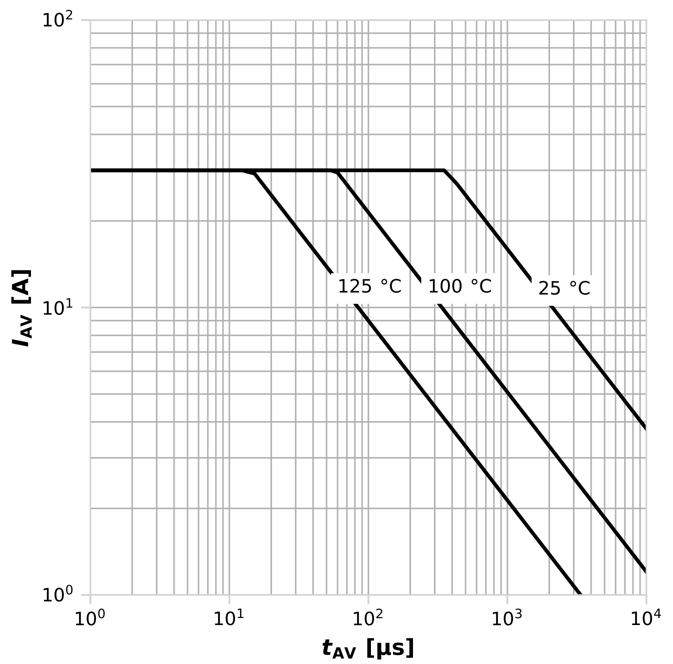
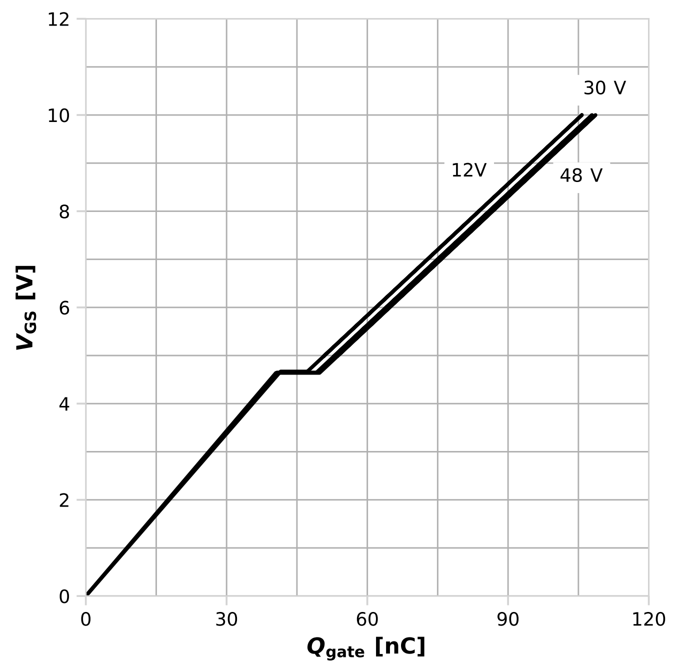
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



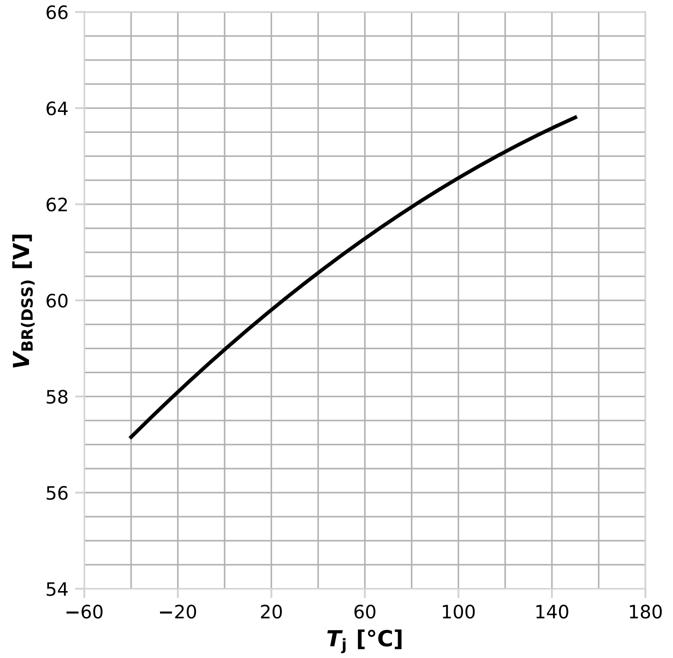
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



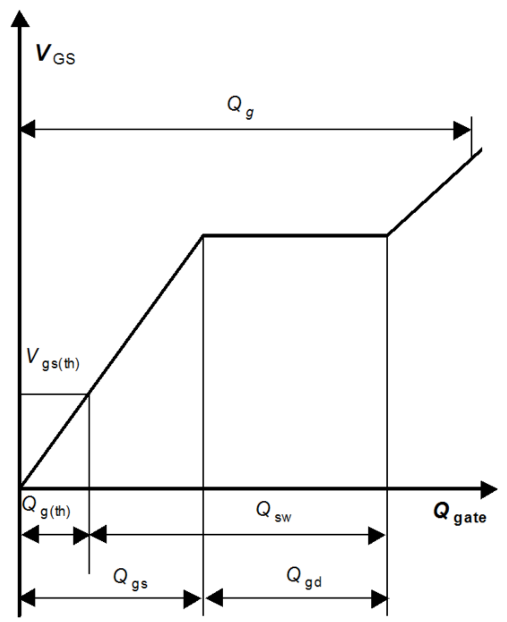
V_{GS}=f(Q_{gate}); I_D=30 A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Gate charge waveforms



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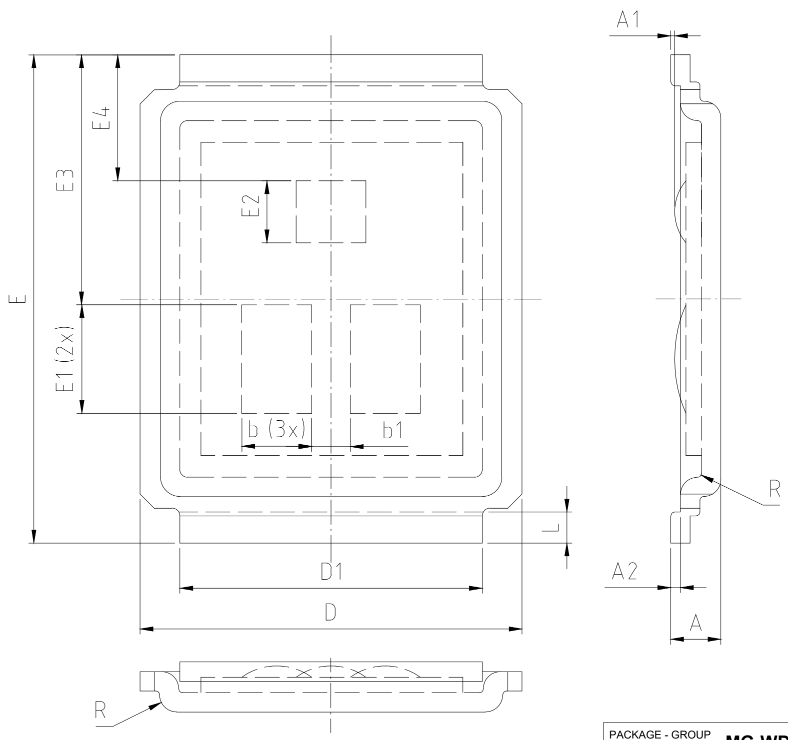
5 Package outlines



PACKAGE - GROUP NUMBER:	MG-WDSON-5-U02	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.59	0.70
A1	0.00	0.10
A2	0.08	0.17
b	0.88	0.92
b1	0.48	0.52
D	4.80	5.05
D1	3.85	3.95
E	6.25	6.35
E1	1.38	1.42
E2	0.78	0.82
E3	3.125	3.33
E4	1.525	1.73
L	0.35	0.45
R	---	0.10
N	5	

Figure 1 Outline MG-WDSON-5, dimensions in mm

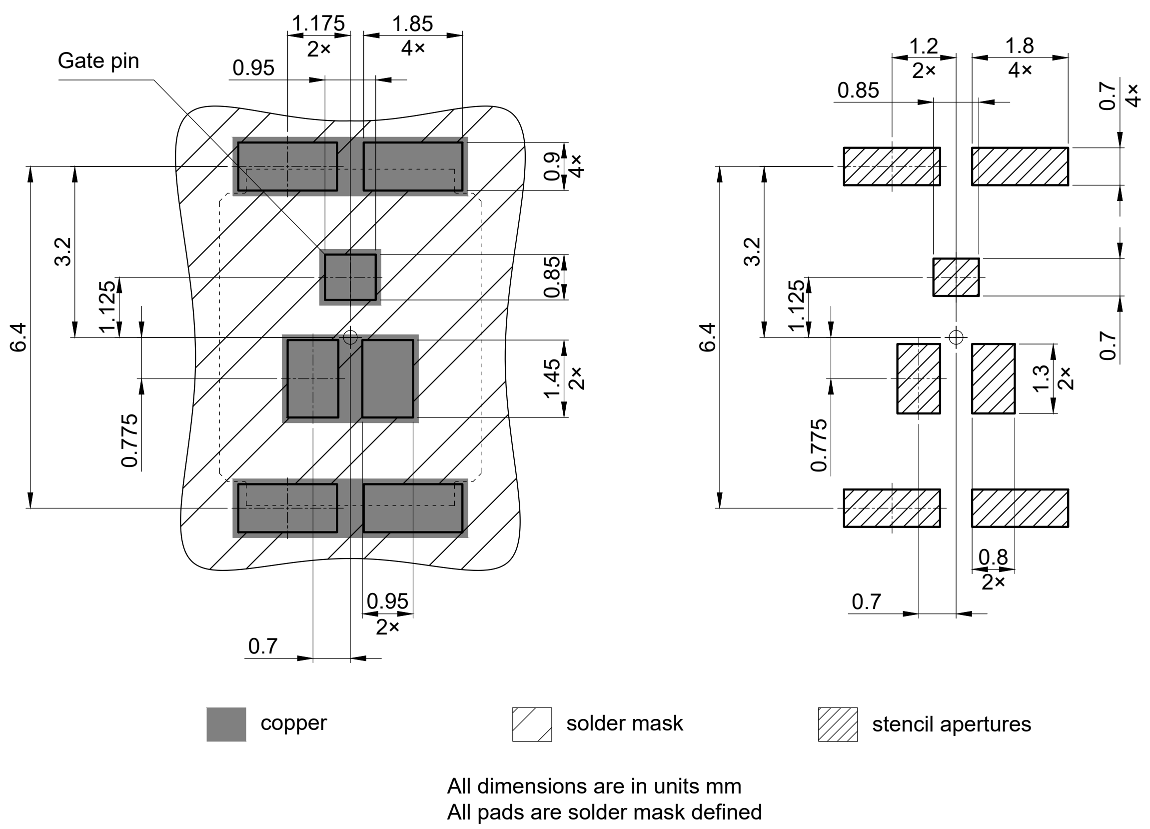
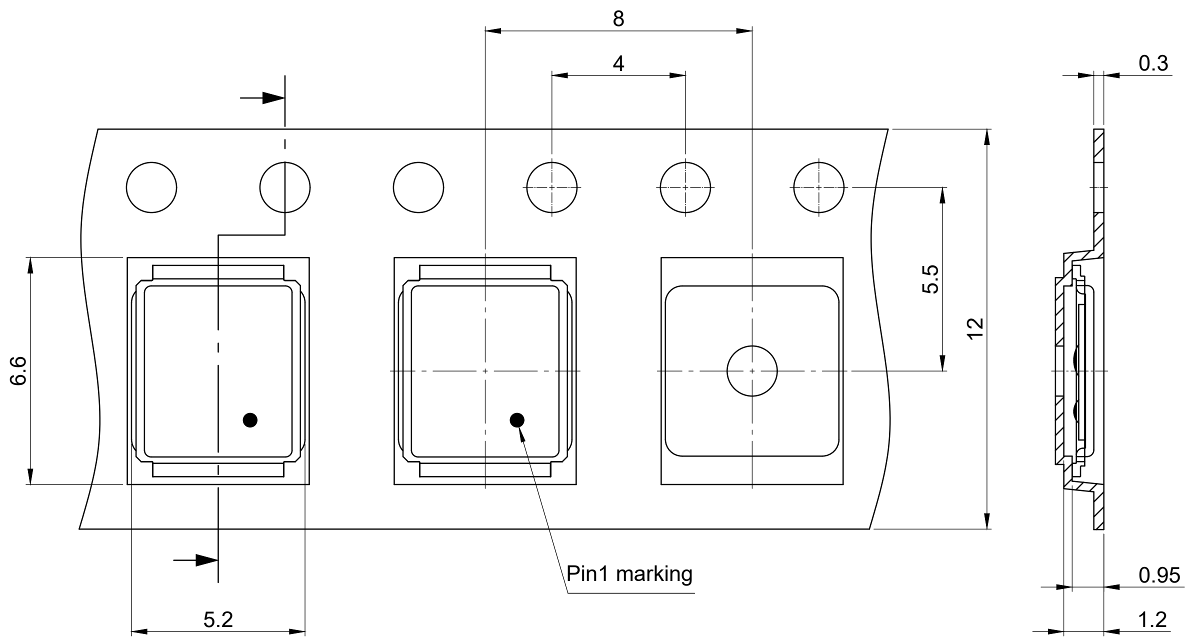


Figure 2 Footprint drawing MG-WDSON-5, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 3 **Packaging variant MG-WDSON-5, dimensions in mm**

Revision history

BSB028N06NN3 G

Revision 2024-11-09, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2024-11-09	New (Rev. 1.0) number is assigned due to datasheet tool change / improvement Updated POD from "MG-WDSON-2" to "MG-WDSON-5" page 11

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