EVB BGA9H1MN9 User Guide

Evaluation Board BGA9H1MN9

About this document

Scope and purpose

This measurement report provides an overview of the evaluation board (EVB) of the BGA9H1MN9 Mid- and High-Band Low Noise Amplifier with Gain Steps and MIPI Control. In this document, the BGA9H1MN9 circuit schematic, PCB layout and measurement results are summarized.

Table of contents

1 BGA9H1MN9 Description

The BGA9H1MN9 is a low noise amplifier for LTE and 5G which covers a wide frequency range from 1.4 GHz to 2.7 GHz. The LNA provides up to 20.2 dB gain and 0.6 dB noise figure at a current consumption of 5.8 mA. With the Gain Step feature, the gain and linearity can be adjusted to increase the system dynamic range and to accommodate to changing interference scenarios. The BGA9H1MN9 supports ultra-low bypass current of 2 µA and 1.2 V operating voltage to reduce power consumption. It operates from 1.1 V to 2.0 V supply voltage over temperature. The compact 9 pin TSNP-9 package with the dimension of 1.1 x 1.1 mm helps to save space on the PCB.

[In order to get the EVB BGA9H1MN9, place your order in either the Distribution Integrated Solution (IDIS) tool, Infineon Sample Request (ISaR) tool or contact your business partner using the reference number: SP005427061].

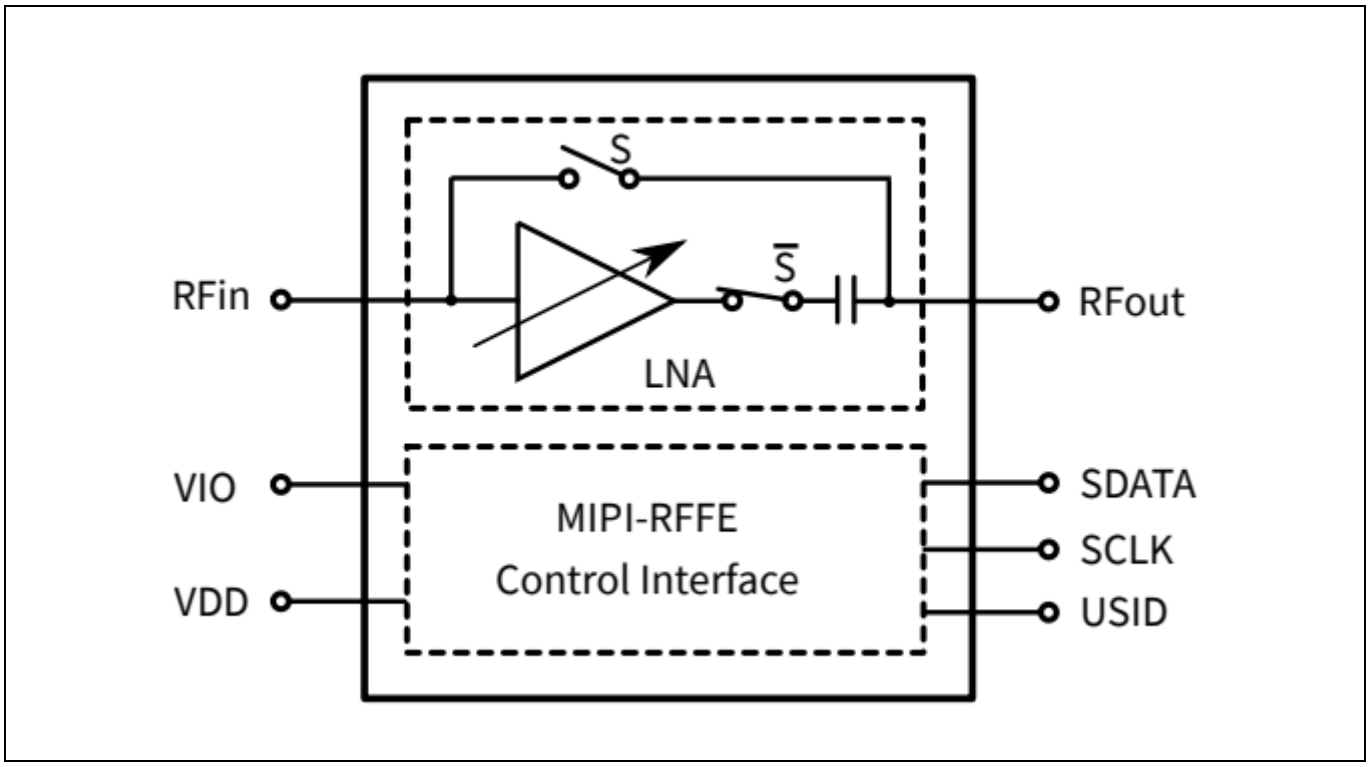


Figure 1 BGA9H1MN9 Block Diagram

1.1 MIPI Control Specification

The device complies with MIPI RFFE specification. A MIPI Stick is necessary in order to operate the device. The 10-pin connector on the EVB is used to connect it to the MIPI Stick (See image below). The following pins have to be connected for proper operation:

- SDATA (Data Line)
- SCKL (Clock Line)
- GND (Ground)
- VIO (Voltage Input-Output)
- VDD (Power Supply)
- USID (Unique Slave Identifier)

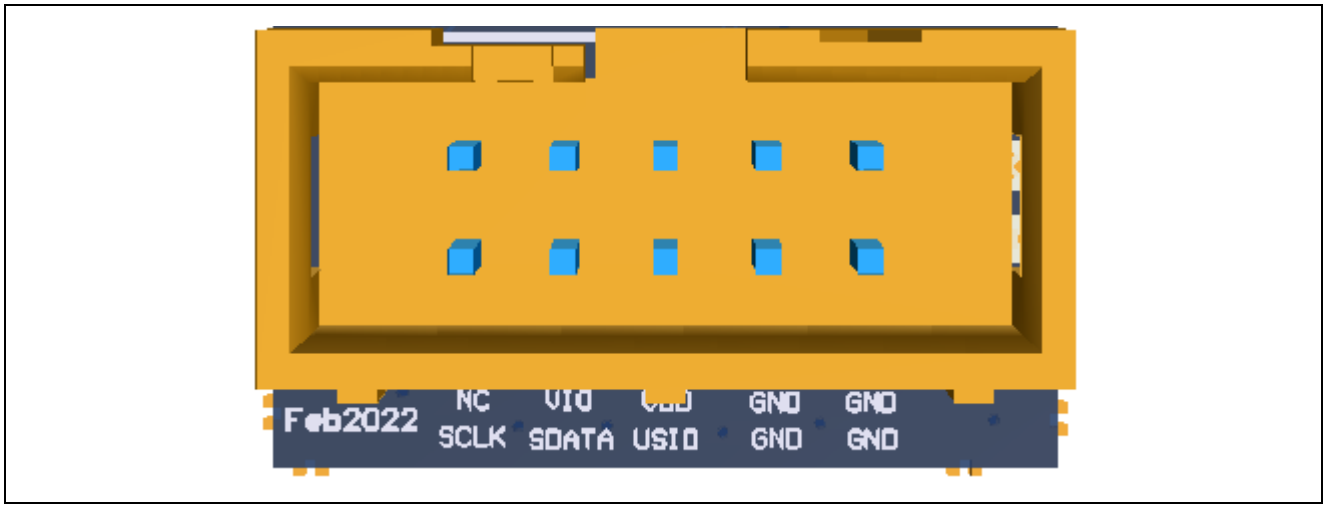


Figure 2 Control Connector

For further information about the MIPI Stick please refer to the published guide on Infineon's website: **"MIPI Stick Basic User Guide"** (See link at the bottom of this document). [In order to get the MIPI Stick, place your order on either the Integrated Distribution Solution (IDIS) tool, Infineon Sample Request (ISaR) tool or contact your business partner using the reference number: SP001160002].

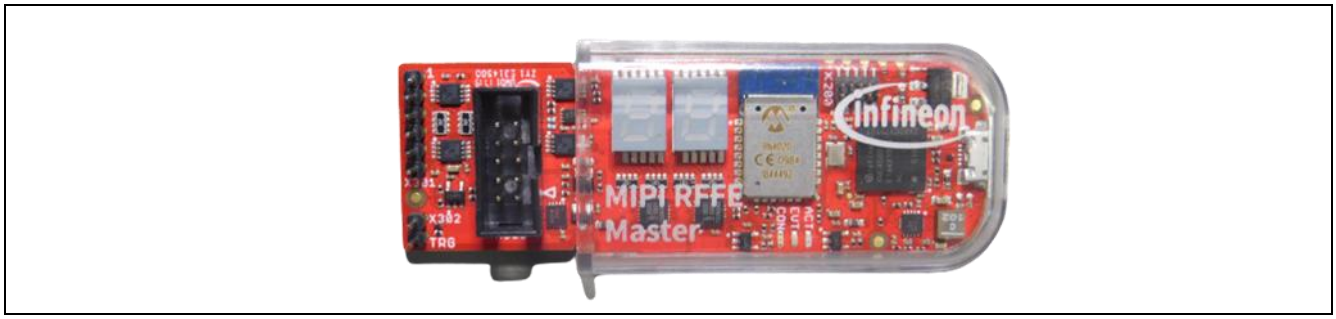


Figure 3 Infineon MIPI Stick

2 Evaluation Board

PIN	DESCRIPTION
IN	RFIn Port
OUT	RFOut Port
VDD	Supply Voltage
VIO	Voltage Input-Output
SCLK	Clock Line
SDATA	Data Line
GND	Pins used as Ground

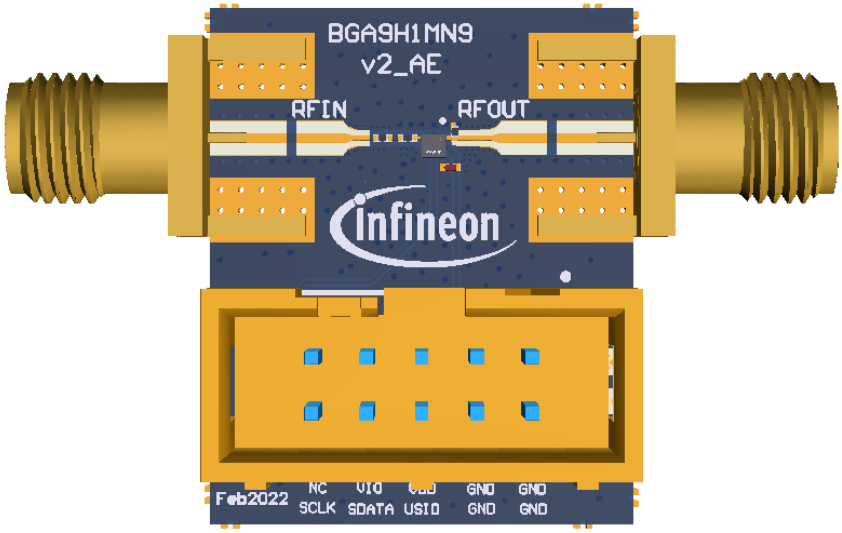


Figure 4 Evaluation Board

2.1 PCB Layout

The total thickness of the board is ~1mm and its layers' composition is presented in the image below.

Layer	Material	Via / DK-Bohr.	Dicke
LS-Lack			20
T	Cu-Folie		35
	1 x 106 (Prepreg - Panasonic R-5670 Typ 3313)		106
L2			35
	1 x 100 (Kern - Panasonic Megtron6 R-5775)		100
L3			35
	1 x 106 (Prepreg - Panasonic R-5670 Typ 3313)		106
	1 x 100 (Kern - Panasonic Megtron6 R-5775)		200
	1 x 106 (Prepreg - Panasonic R-5670 Typ 3313)		106
	1 x 100 (Kern - Panasonic Megtron6 R-5775)		100
	1 x 106 (Prepreg - Panasonic R-5670 Typ 3313)		106
B	Cu-Folie		35
LS-Lack			20
		Gesamtdicke:	1004 µm

Figure 5 PCB Layout

2.2 Schematic

2.2.1 Configuration for 1400 – 1500 MHz

Figure 6 shows the schematic of the Evaluation Board and includes the matching components.

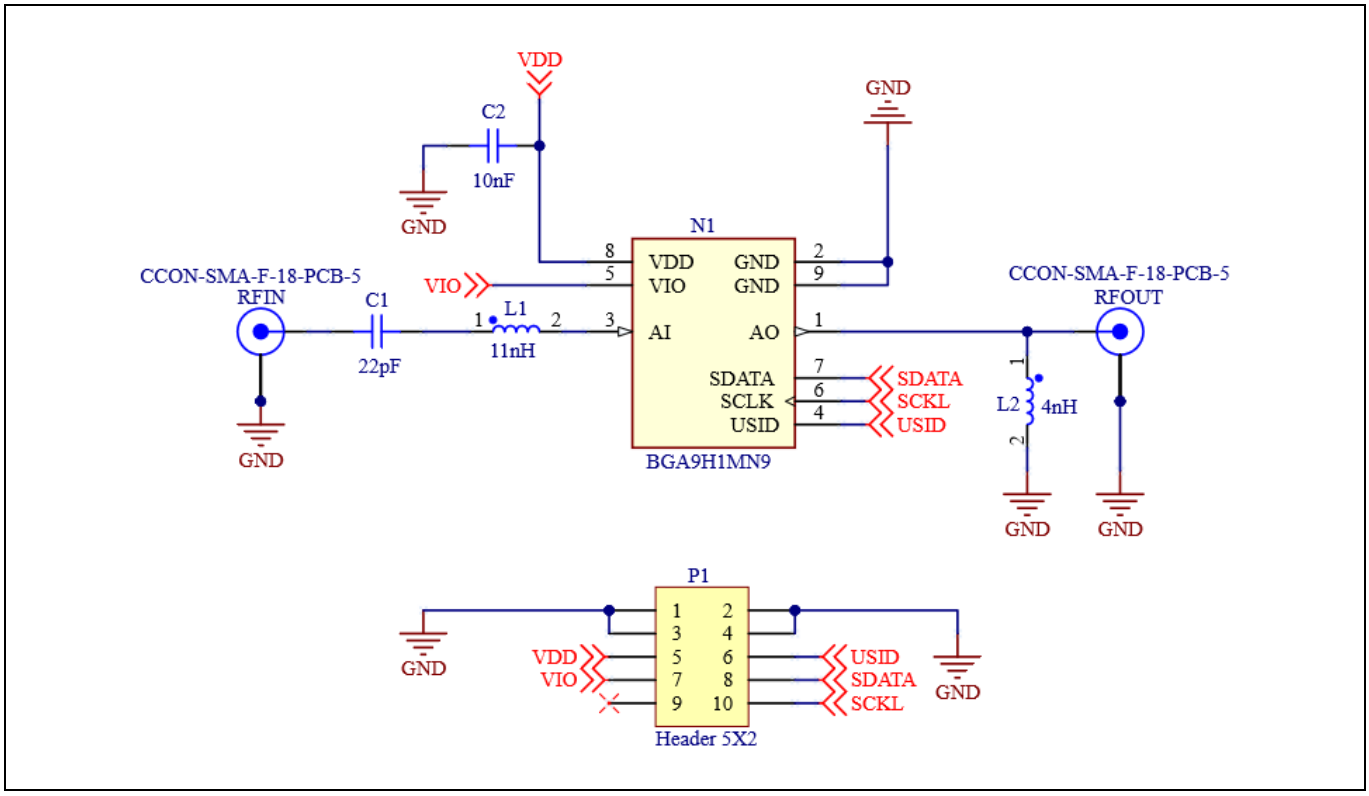


Figure 6 BGA9H1MN9 EVB Schematic

2.2.1.1 Bill of Materials

Designator	Value	Description
RFIN, RFOUT	-	SMA connectors
P1	-	10-Pin header
N1	-	BGA9H1MN9
L1	11 nH	Input matching
C1	22 pF	RF bypass
C2 (optional)	10 nF	RF bypass
PCB	v2_AE	BGAV1A10 Evaluation Board

2.2.2 Configuration for 1800 – 2200 MHz

Figure 7 shows the schematic of the Evaluation Board and includes the matching components.

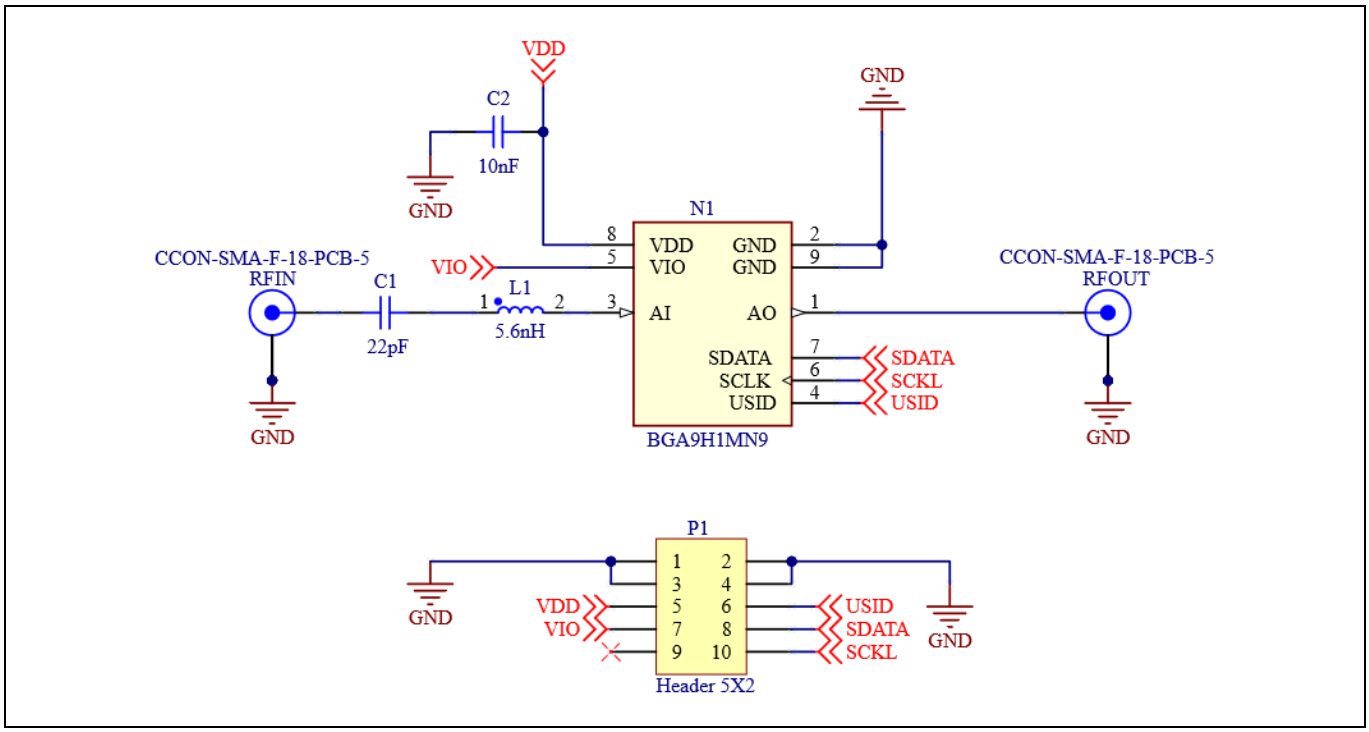


Figure 7 BGA9H1MN9 EVB Schematic

2.2.2.1 Bill of Materials

Designator	Value	Description
RFIN, RFOUT	-	SMA connectors
P1	-	10-Pin header
N1	-	BGA9H1MN9
L1	5.6 nH	Input matching
C1	22 pF	RF bypass
C2 (optional)	10 nF	RF bypass
PCB	v2_AE	BGAV1A10 Evaluation Board

2.2.3 Configuration for 2300 – 2700 MHz

Figure 8 shows the schematic of the Evaluation Board and includes the matching components.

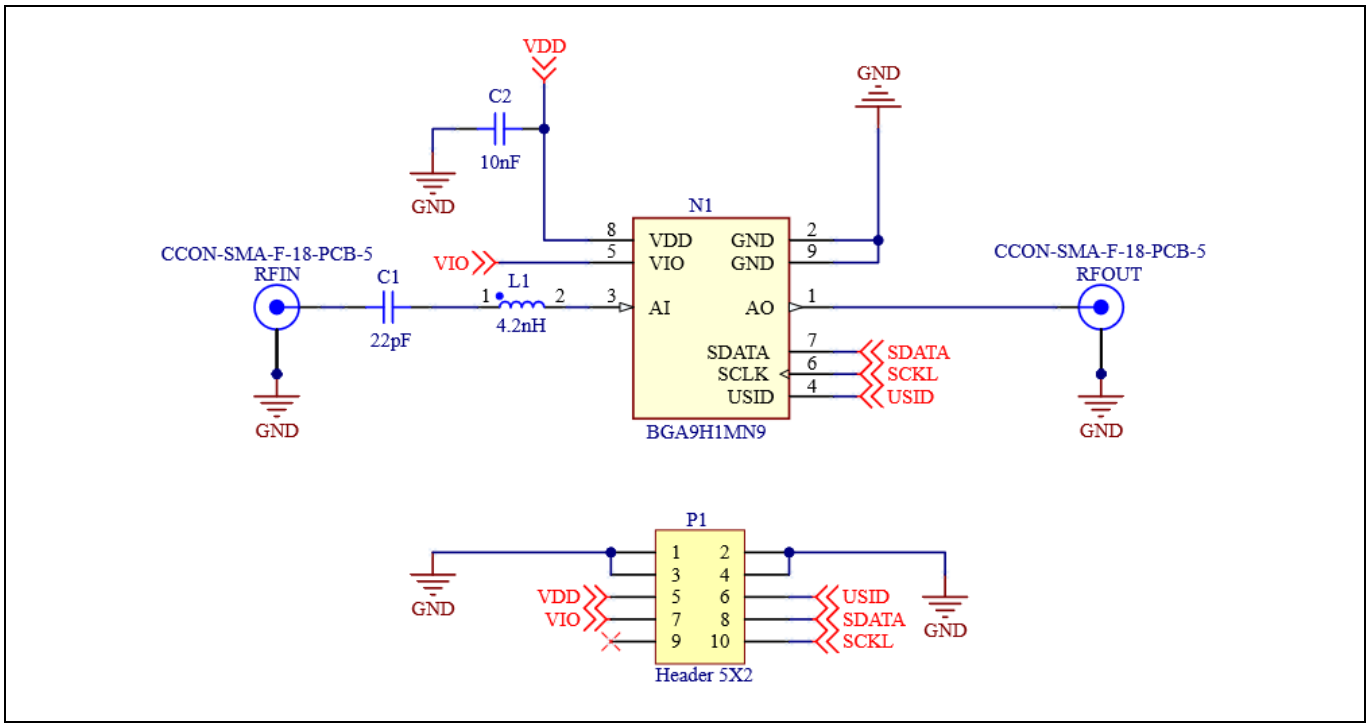


Figure 8 BGA9H1MN9 EVB Schematic

2.2.3.1 Bill of Materials

Designator	Value	Description
RFIN, RFOUT	-	SMA connectors
P1	-	10-Pin header
N1	-	BGA9H1MN9
L1	4.2 nH	Input matching
C1	22 pF	RF bypass
C2 (optional)	10 nF	RF bypass
PCB	v2_AE	BGAV1A10 Evaluation Board

2.3 Evaluation Board Hardware

The BGA9H1MN9 allows the user to connect an RF signal to the device via an SMA connector. The user controls the BGA9H1MN9 using the MIPI Stick and sets the desired state through a software interface.

3 Measurement Setups

3.1 S-Parameter

The image below shows the typical S-Parameter Measurement Setup where the input and output of the device are connected to a Network Analyzer.

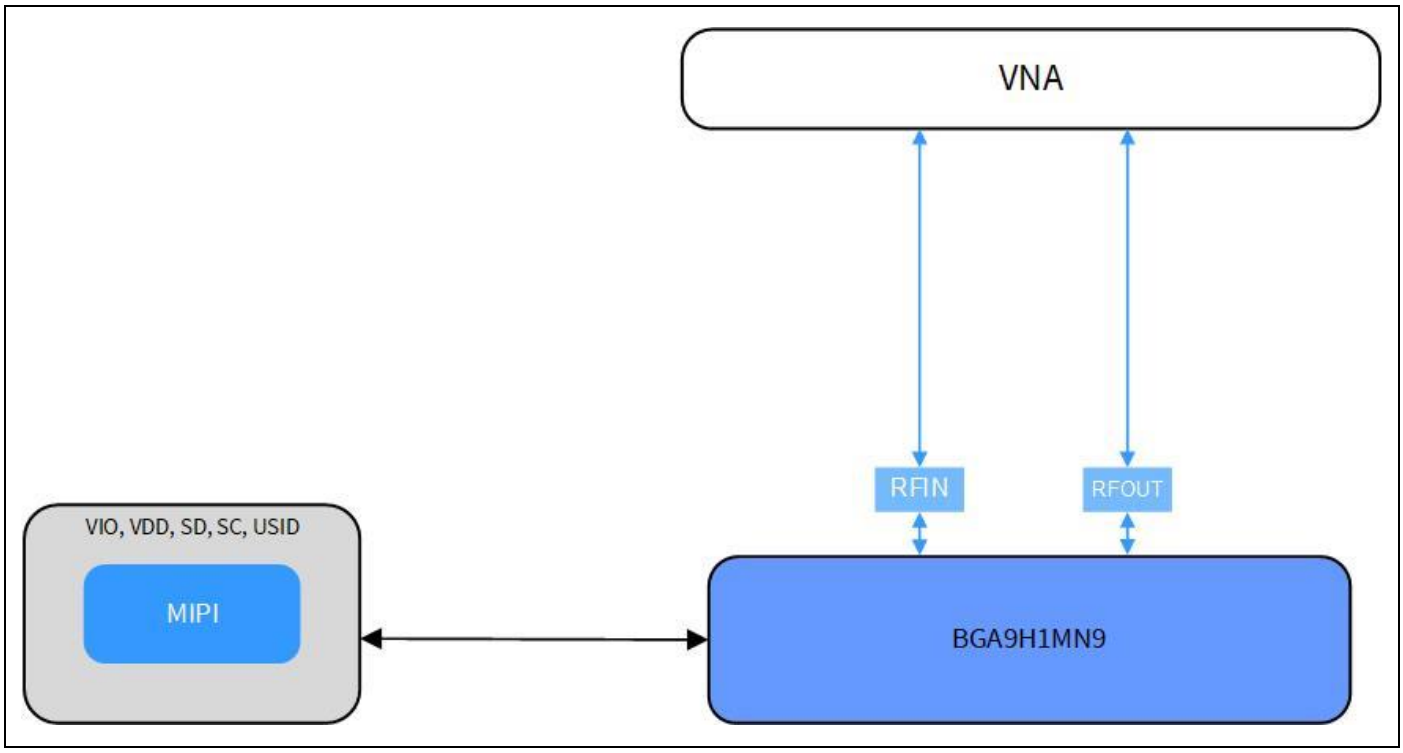


Figure 9 S-Parameter Measurement Setup

3.2 Noise Figure

The image below shows the typical Noise Figure Measurement Setup including a shielding box in which the device is contained in order to reduce noise interference.

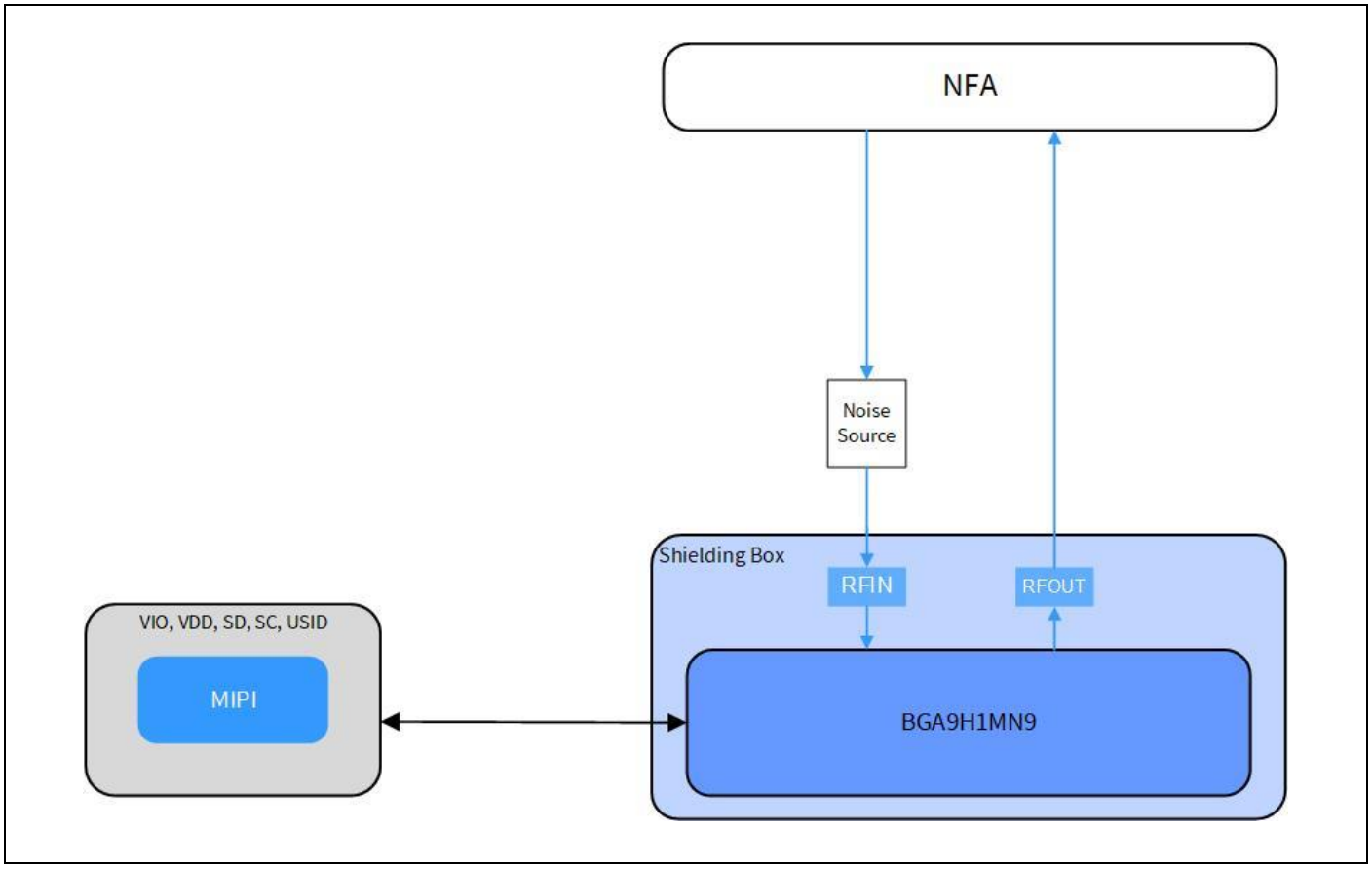
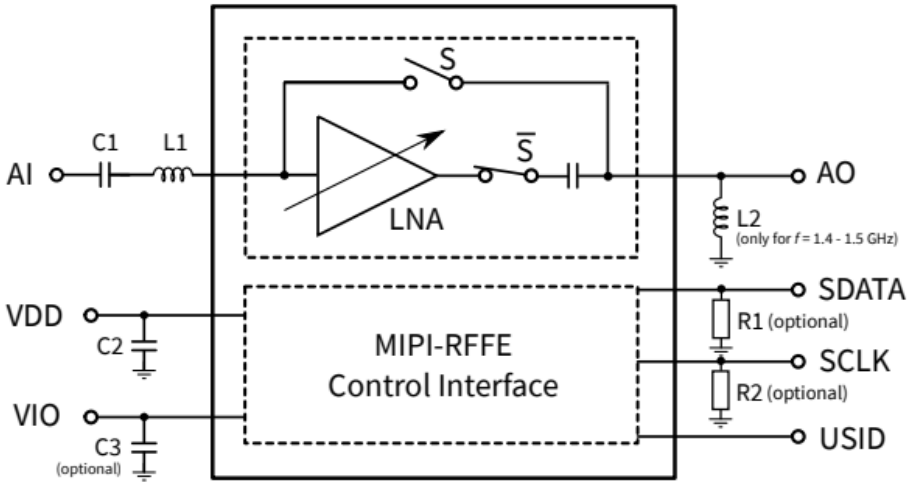


Figure 10 Noise Figure Measurement Setup

4 Results

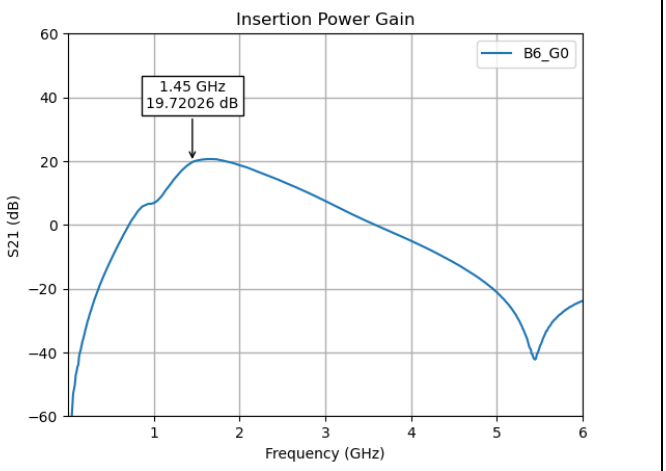
Performance plots are shown in the images below. The files can be found on Infineon's product website.

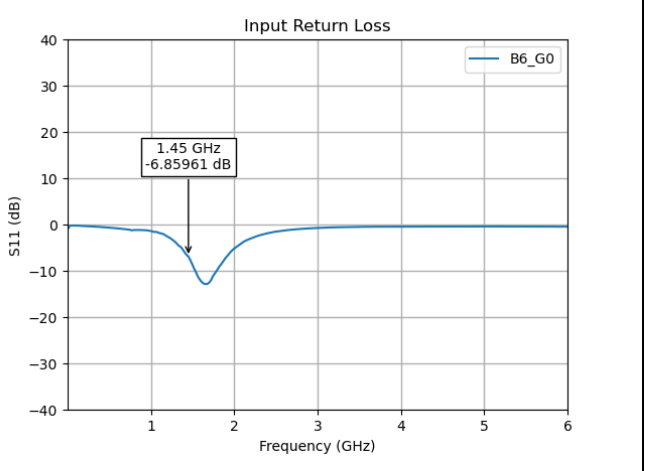
4.1 Configuration for 1400 – 1500 MHz



S-Parameter measurements are done from SMA connector to SMA connector at T = 25 ◦C, $Power_{RF}$ = -30 dBm and V_{cc} = 1.8V for Gain modes 2 through 5 using Bias mode 6 and Gain modes 0 and 1 using Bias mode 2.

4.1.1 S-Parameters





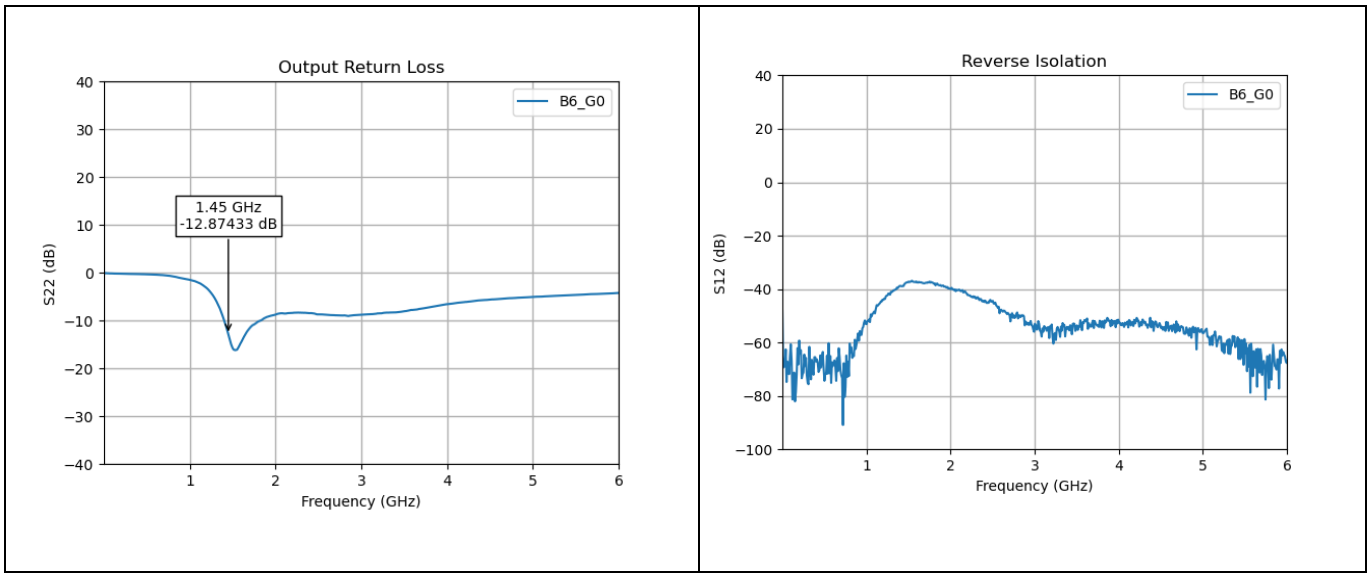


Figure 11 S-Parameters @ 1.8V in Gain 0 Bias 6 Mode

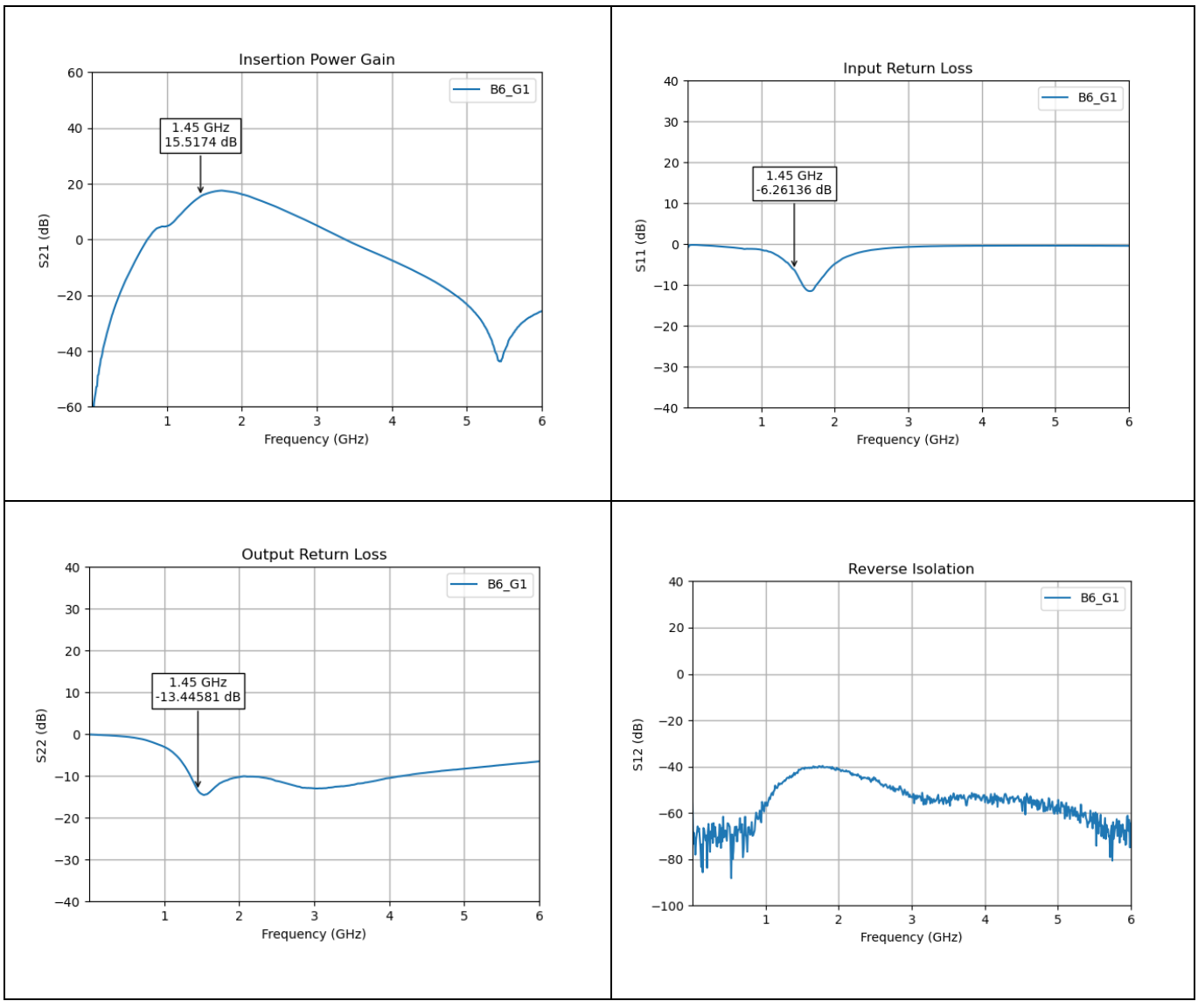


Figure 12 S-Parameters @ 1.8V in Gain 1 Bias 6 Mode

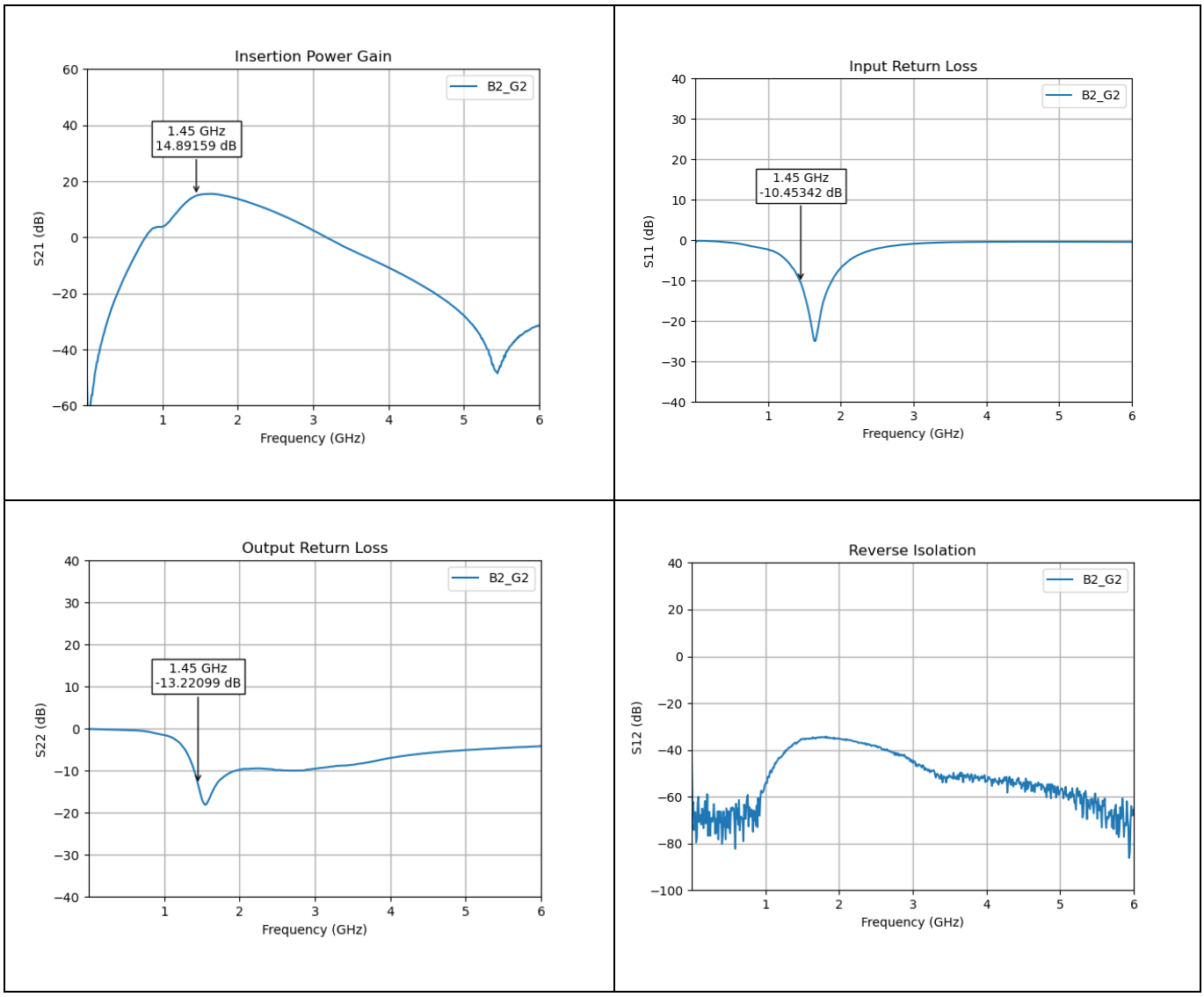
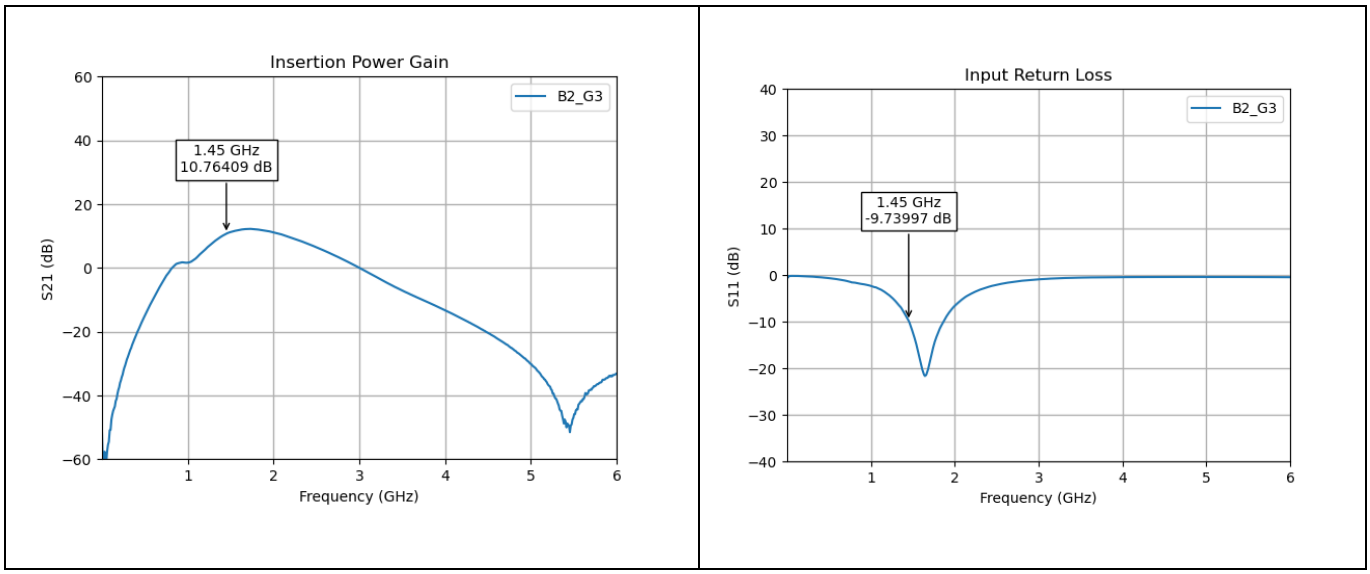


Figure 13 S-Parameters @ 1.8V in Gain 2 Bias 2 Mode



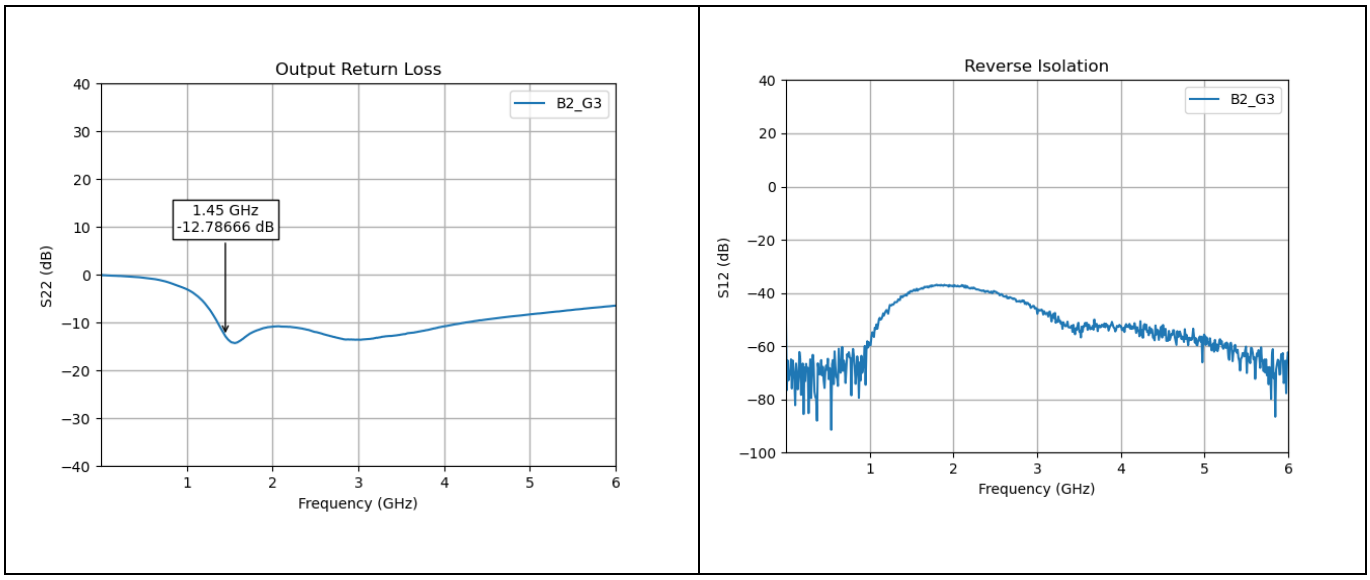


Figure 14 S-Parameters @ 1.8V in Gain 3 Bias 2 Mode

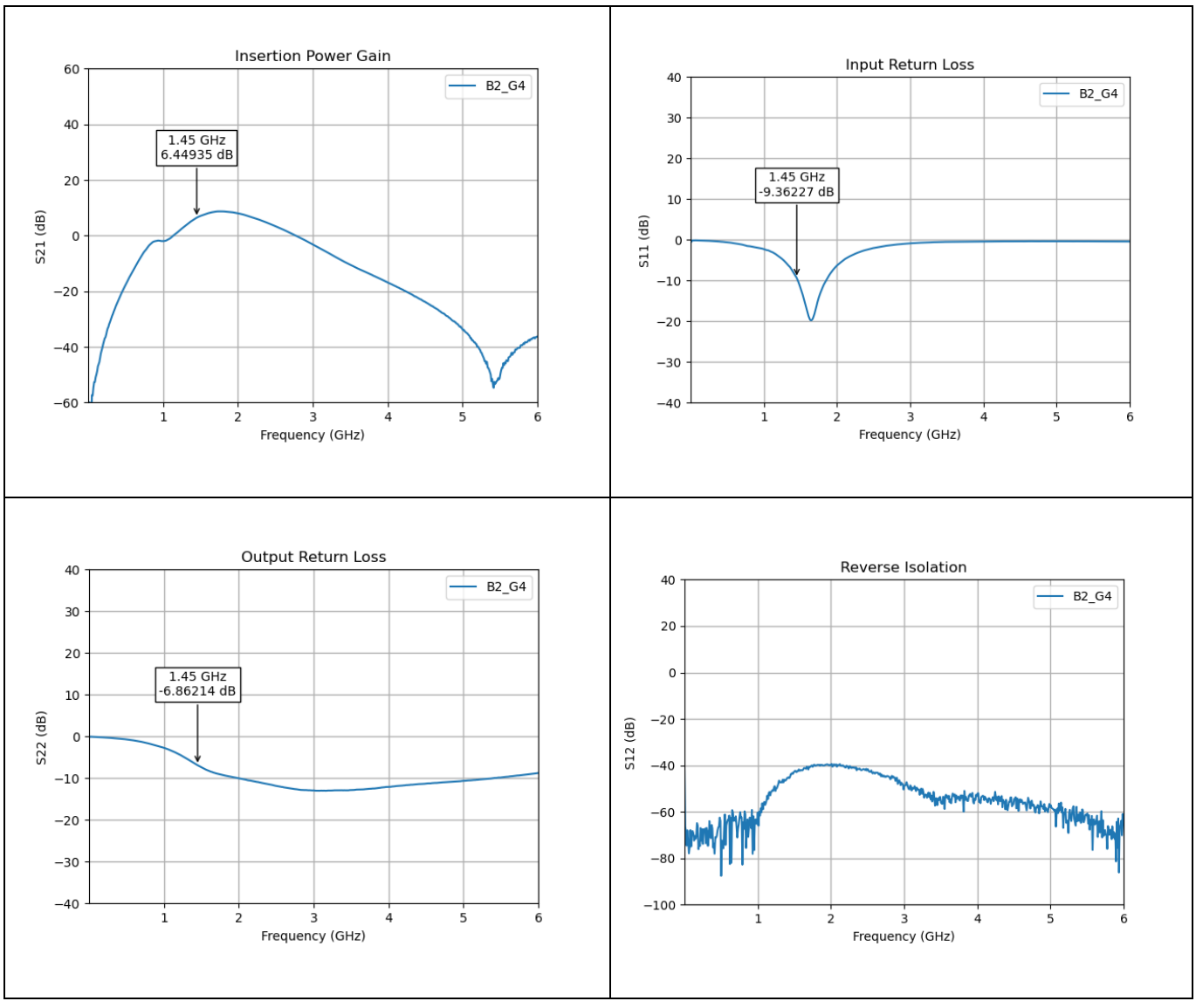


Figure 15 S-Parameters @ 1.8V in Gain 4 Bias 2 Mode

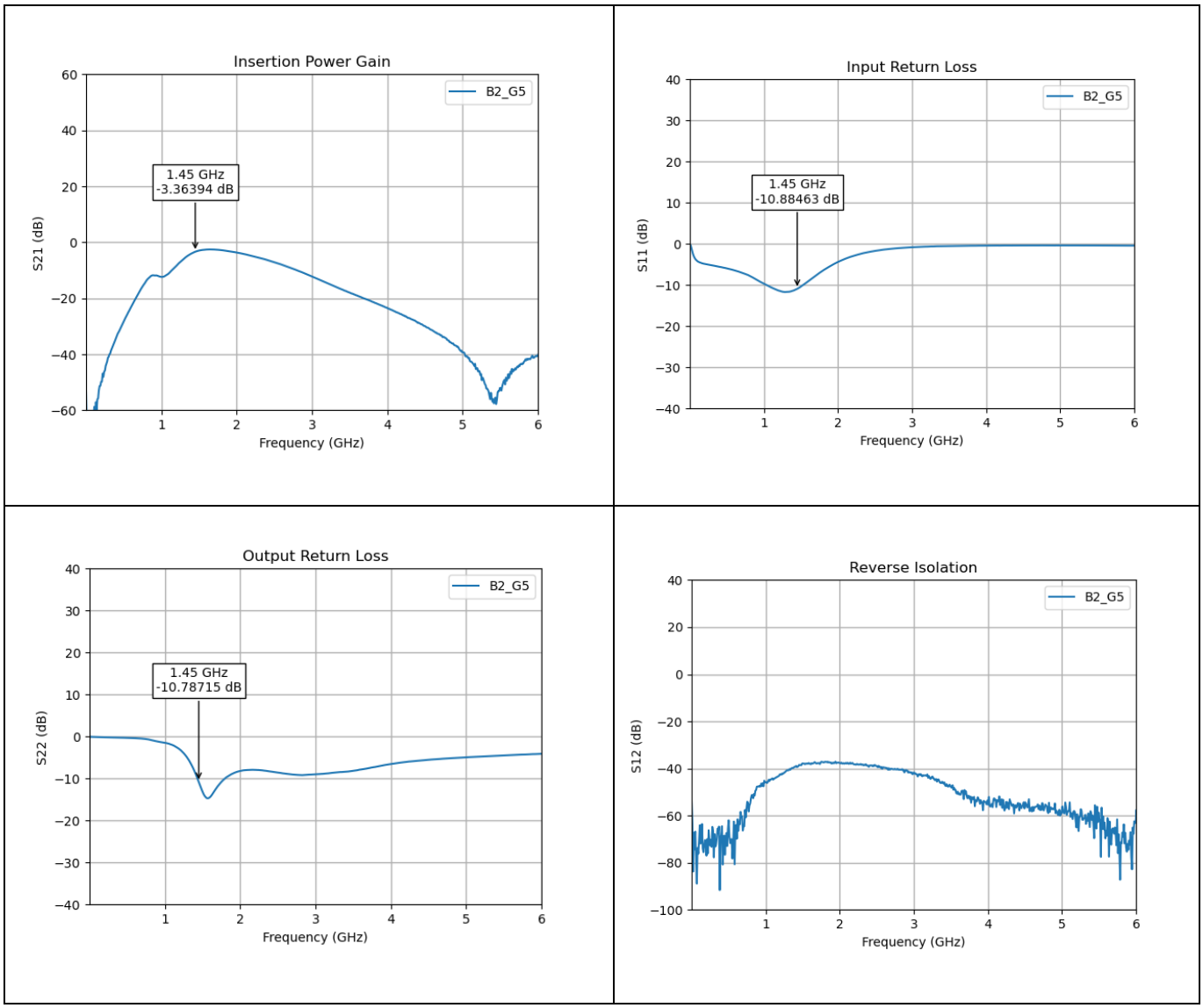
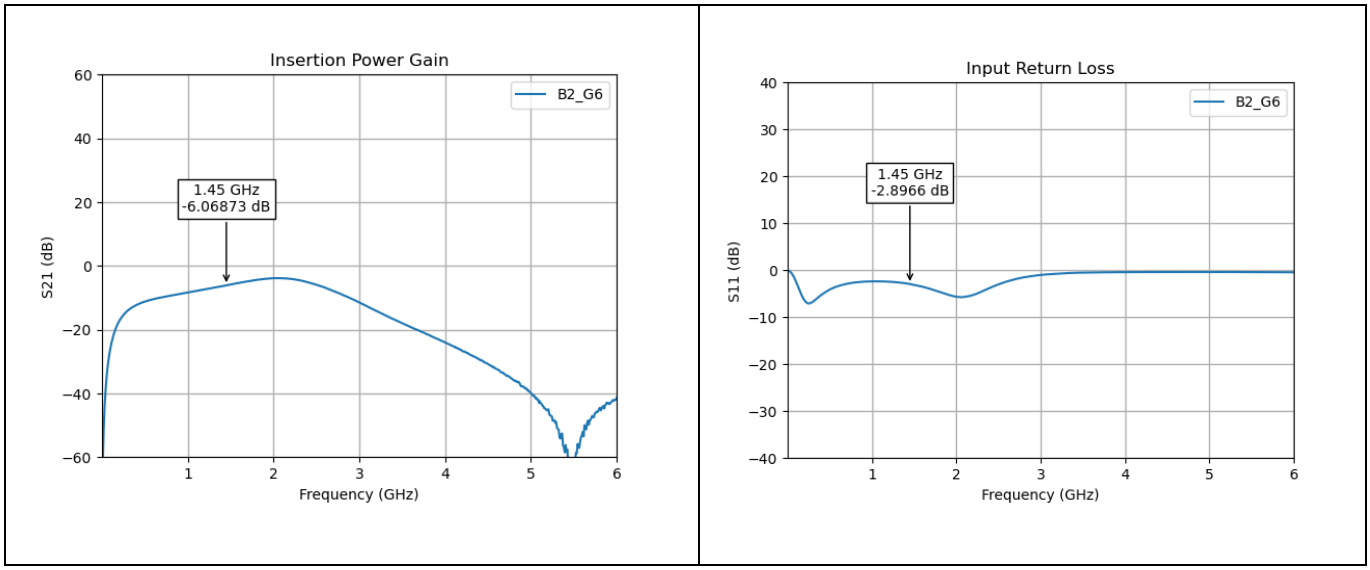


Figure 16 S-Parameters @ 1.8V in Gain 5 Bias 2 Mode



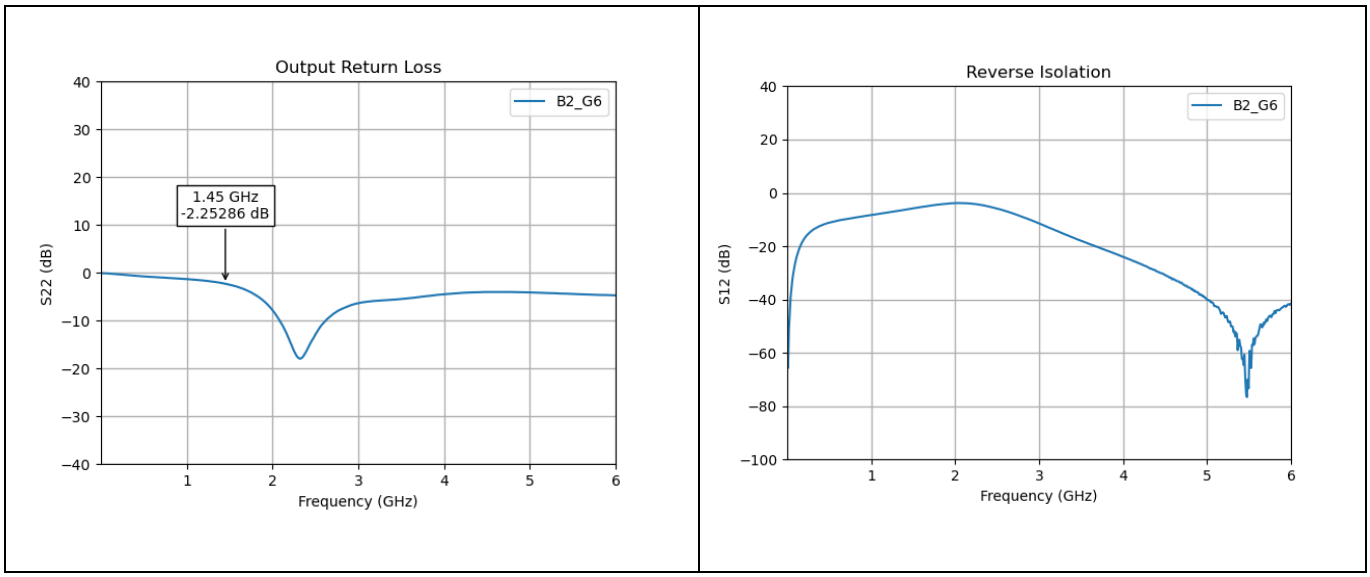


Figure 17 S-Parameters @ 1.8V in Gain 6 Bypass

4.1.1 Noise Figure Results

All NF measurements show the chip performance (de-embedded NF) at T = 25 ◦C, $Power_{RF}$ = -30 dBm and V_{cc} = 1.8V for Gain modes 2 through 5 using Bias mode 6 and Gain modes 0 and 1 using Bias mode 2.

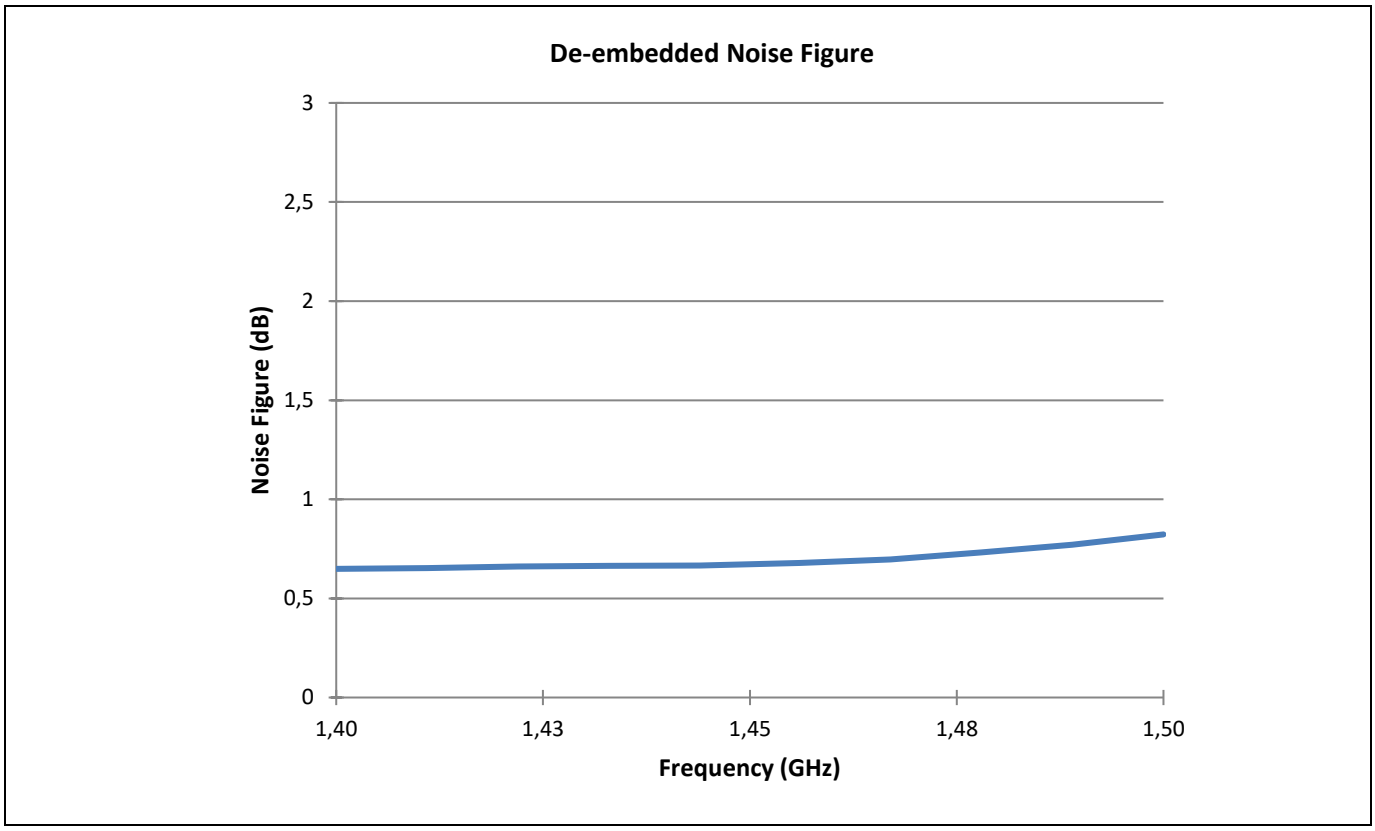


Figure 18 Noise Figure @ 1.8V in Gain 0 Bias 6 Mode

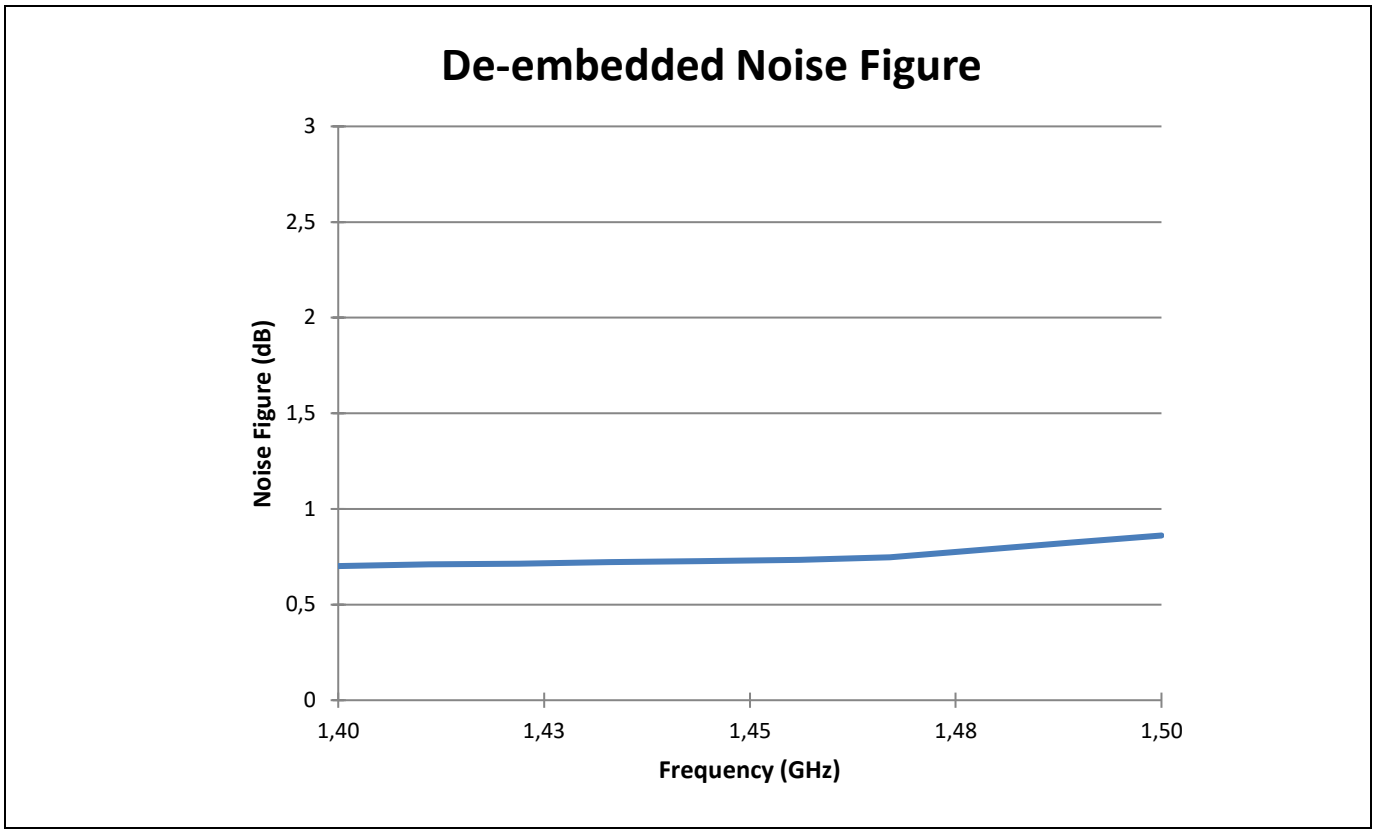


Figure 19 Noise Figure @ 1.8V in Gain 1 Bias 6 Mode

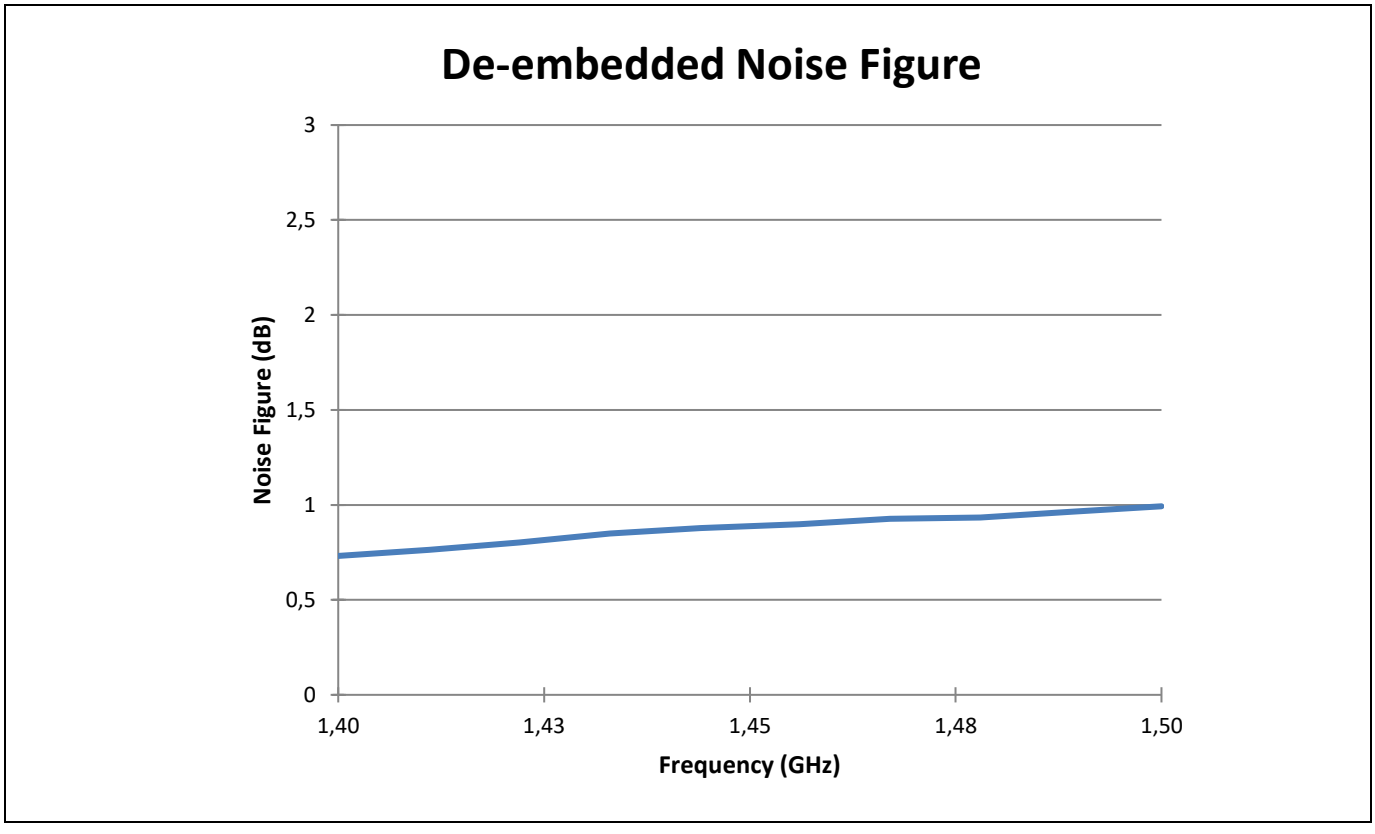


Figure 20 Noise Figure @ 1.8V in Gain 2 Bias 2 Mode

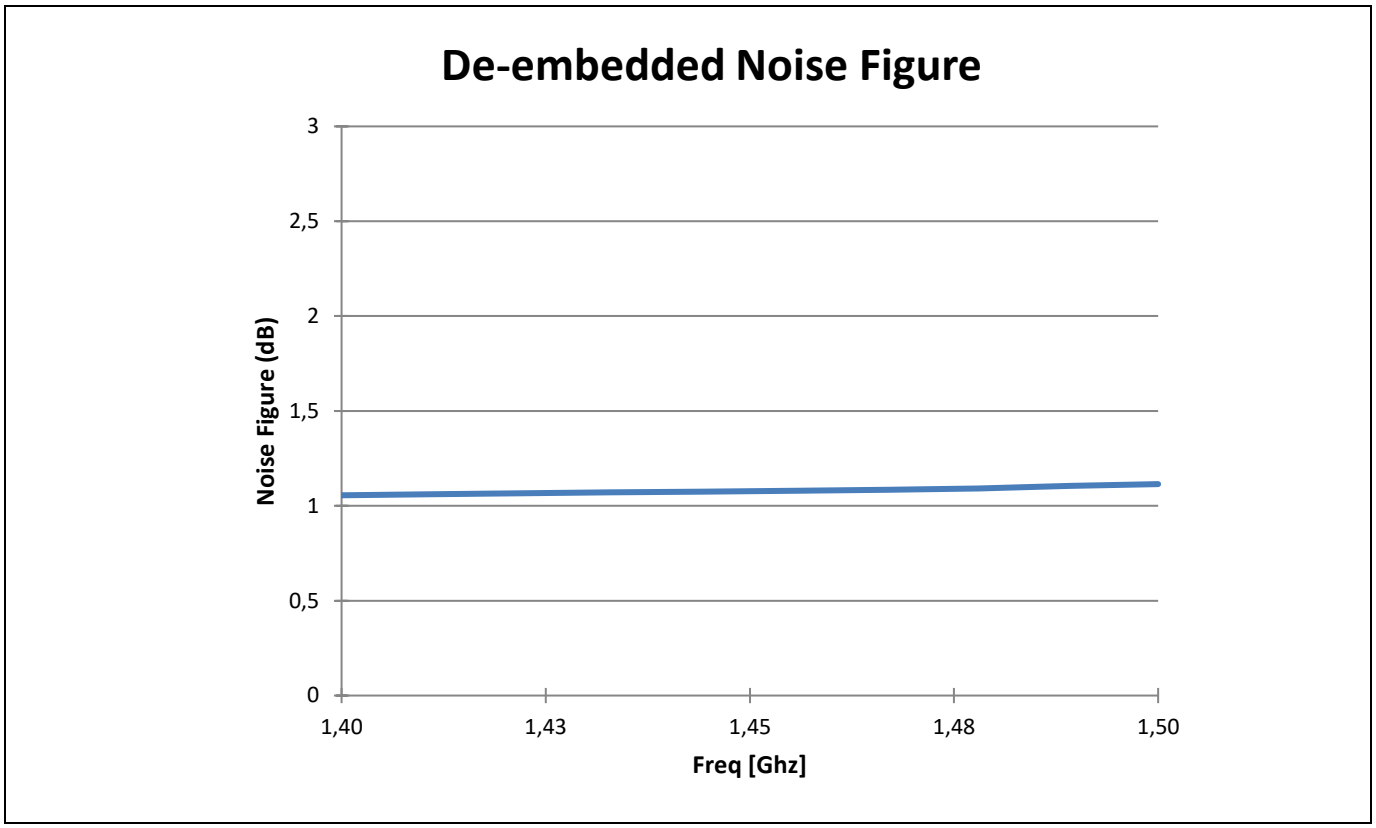


Figure 21 Noise Figure @ 1.8V in Gain 3 Bias 2 Mode

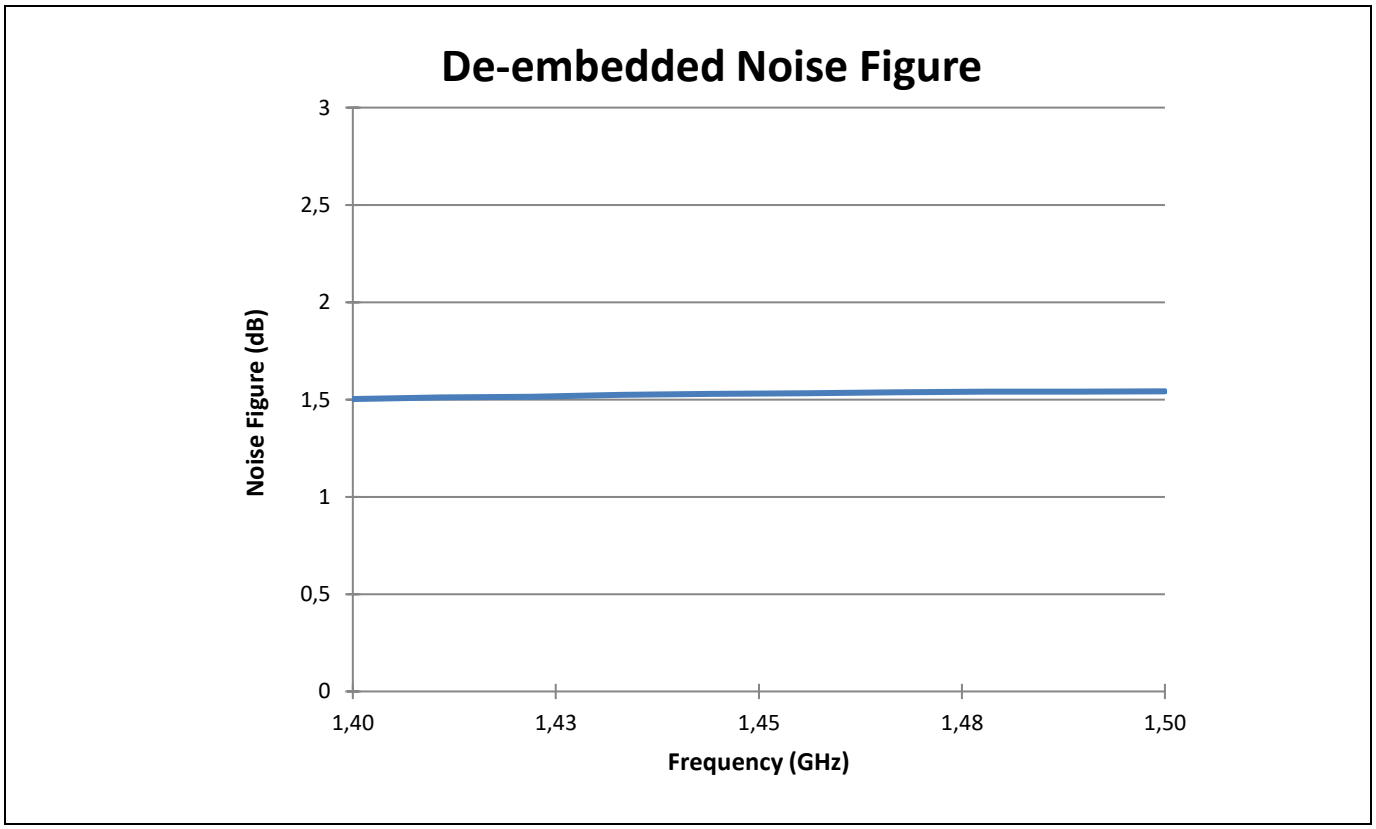


Figure 22 Noise Figure @ 1.8V in Gain 4 Bias 2 Mode

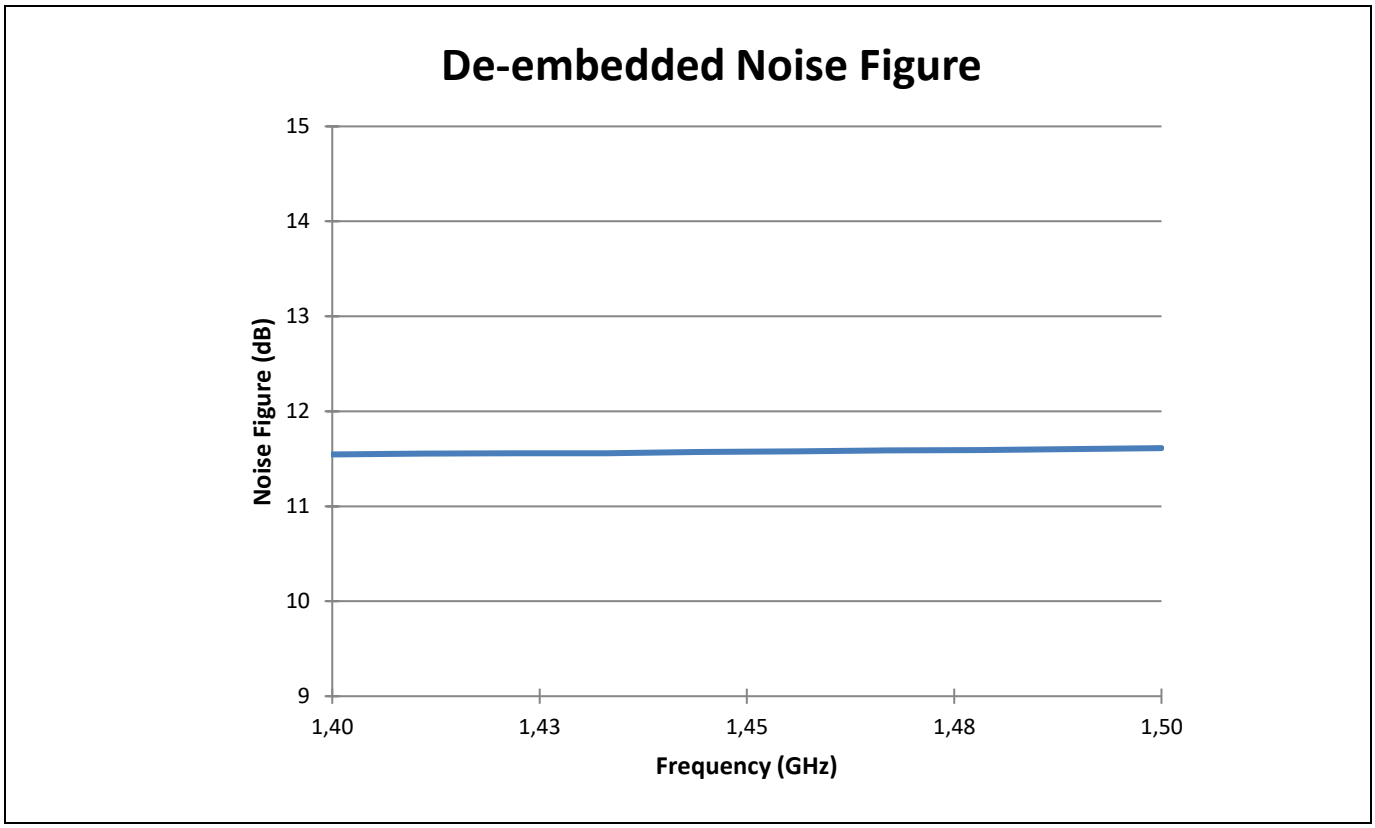


Figure 23 Noise Figure @ 1.8V in Gain 5 Bias 2 Mode

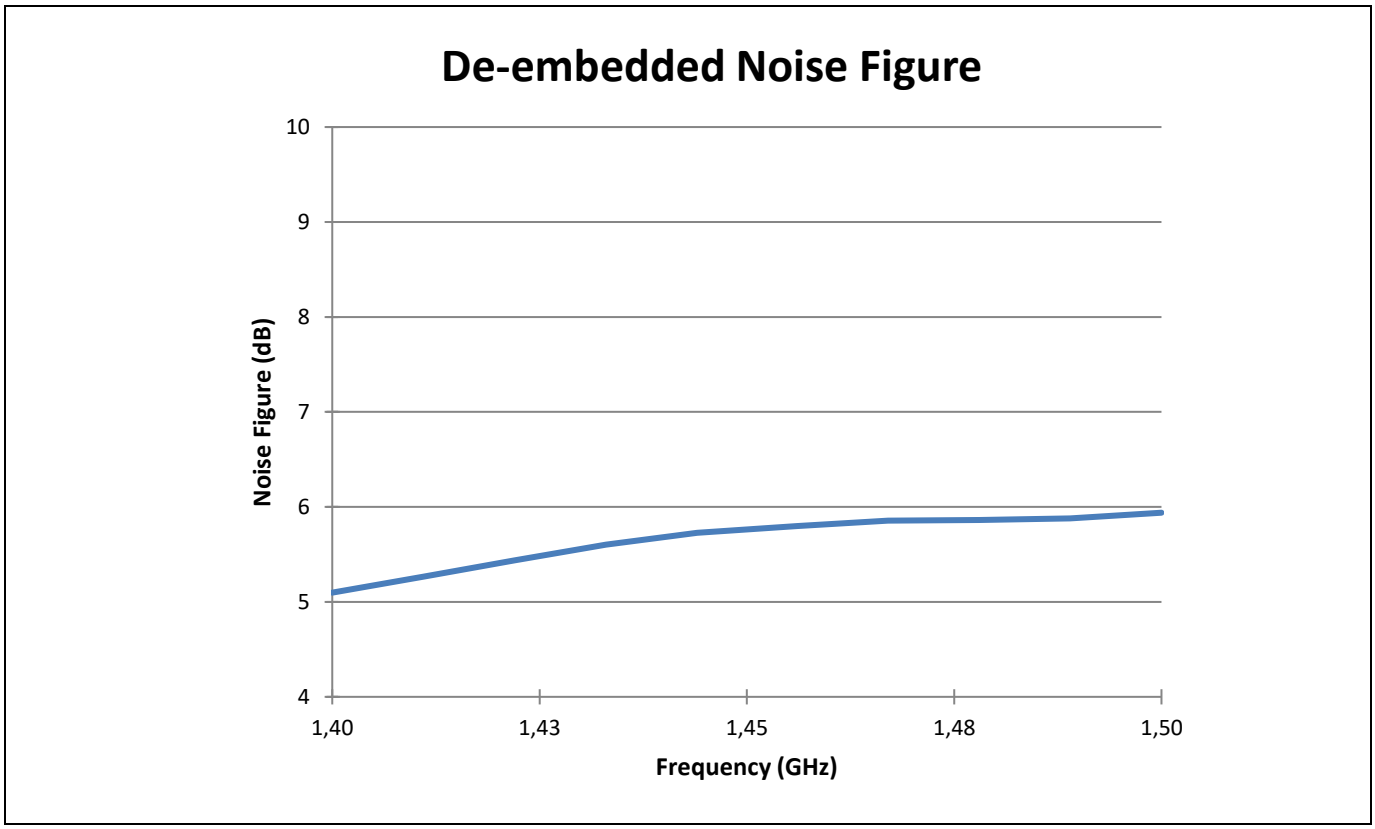
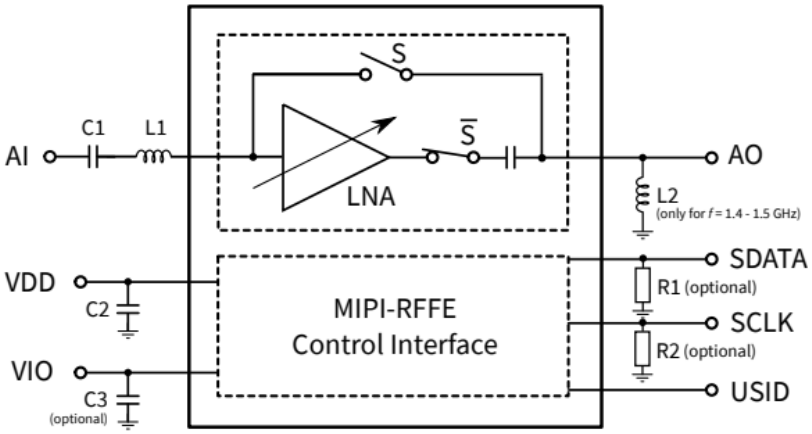


Figure 24 Noise Figure @ 1.8V in Gain 6 Bypass

4.2 Configuration for 1800 – 2200 MHz



S-Parameter measurements are done from SMA connector to SMA connector at T = 25 ◦C, $Power_{RF}$ = -30 dBm and V_{cc} = 1.8V for Gain modes 2 through 5 using Bias mode 6 and Gain modes 0 and 1 using Bias mode 2.

4.2.1 S-Parameters

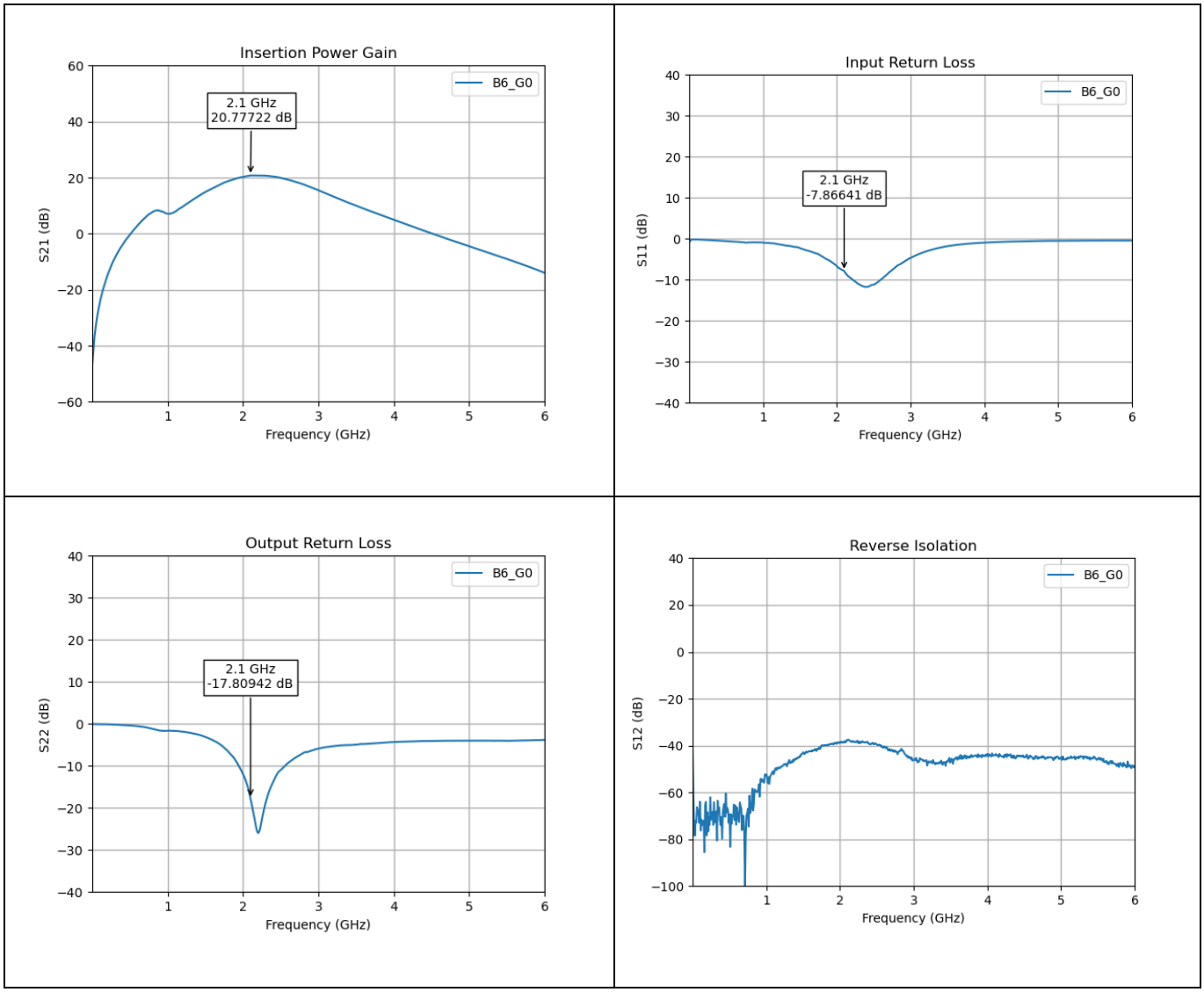


Figure 25 S-Parameters @ 1.8V in Gain 0 Bias 6 Mode

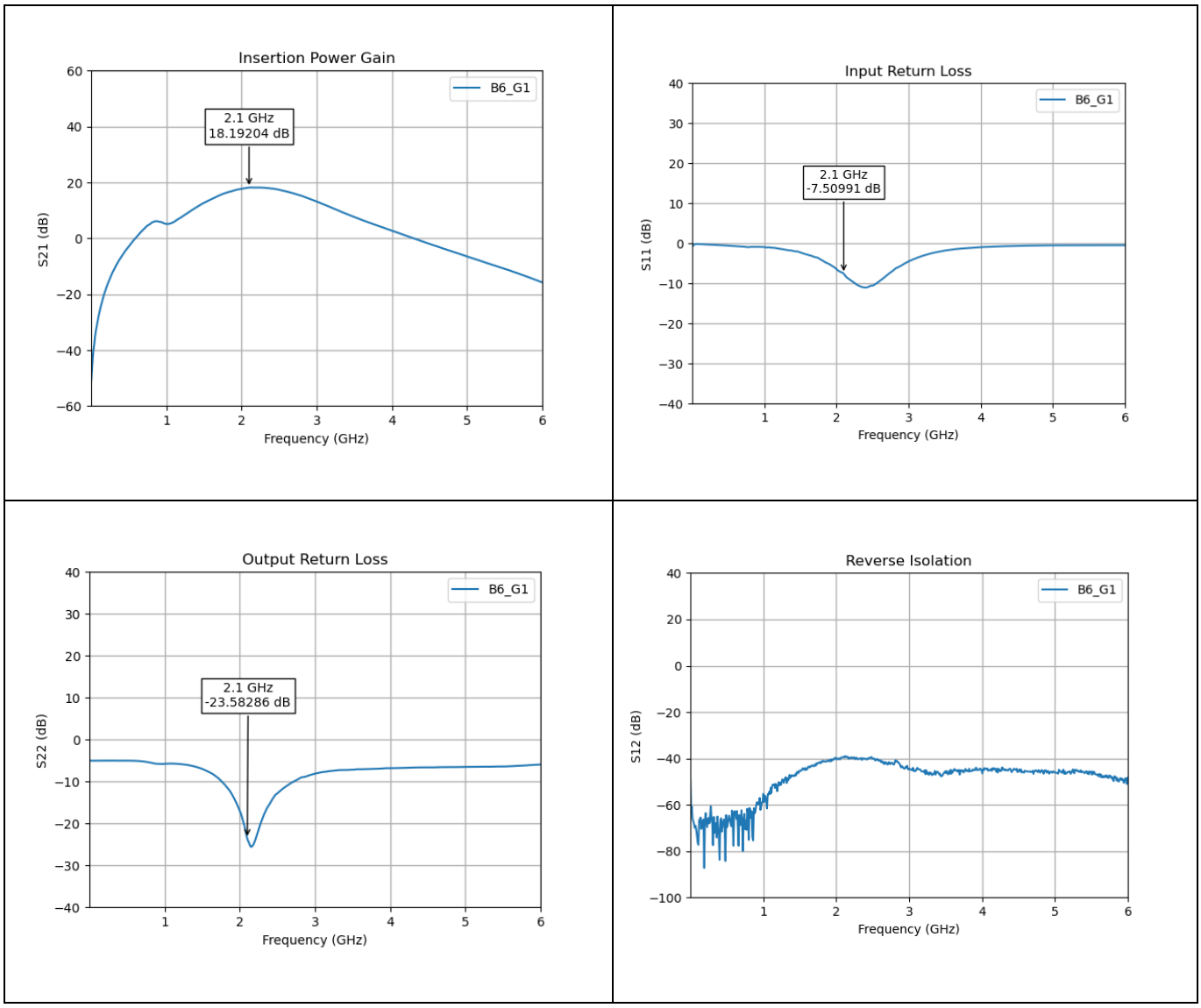
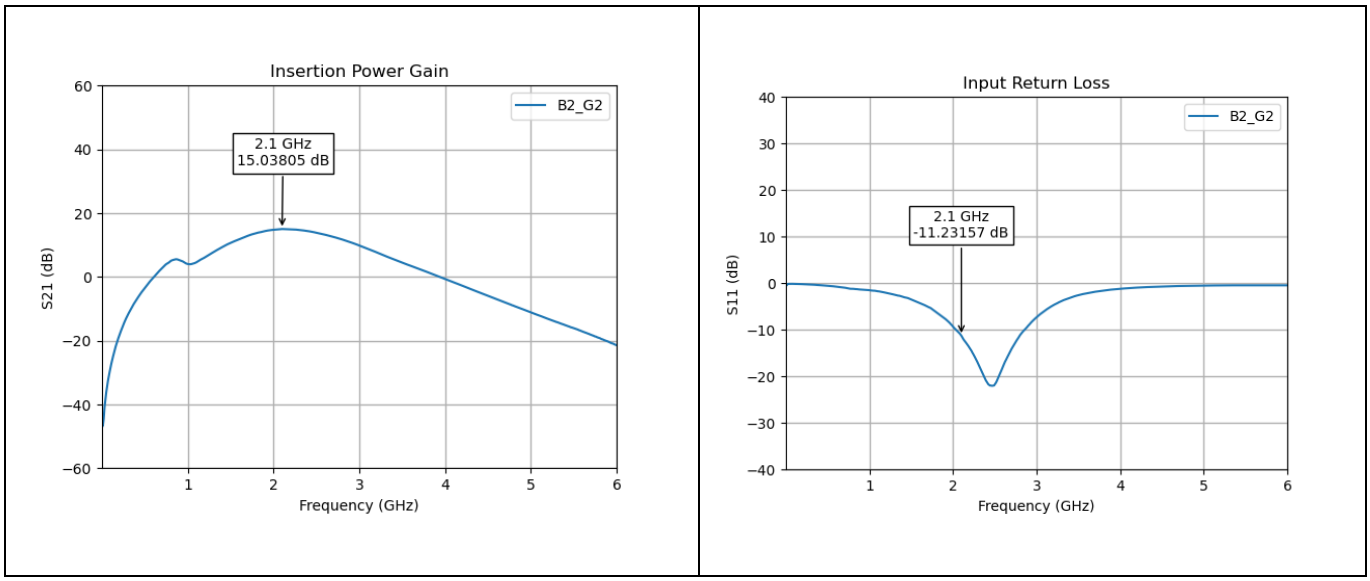


Figure 26 S-Parameters @ 1.8V in Gain 1 Bias 6 Mode



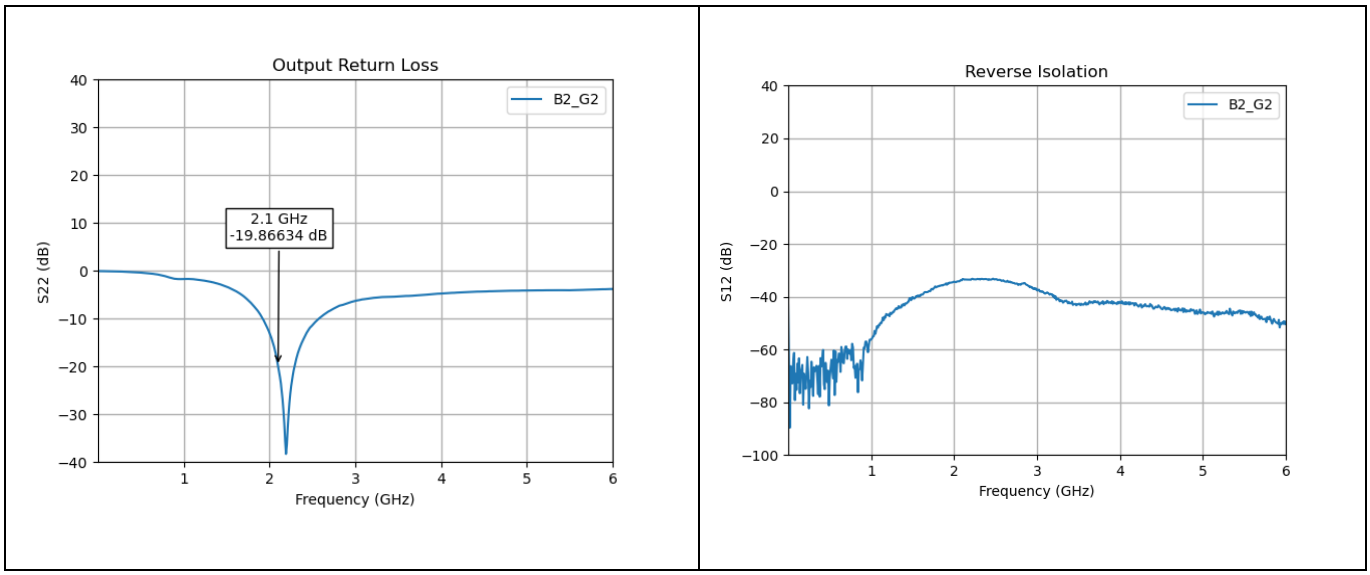


Figure 27 S-Parameters @ 1.8V in Gain 2 Bias 2 Mode

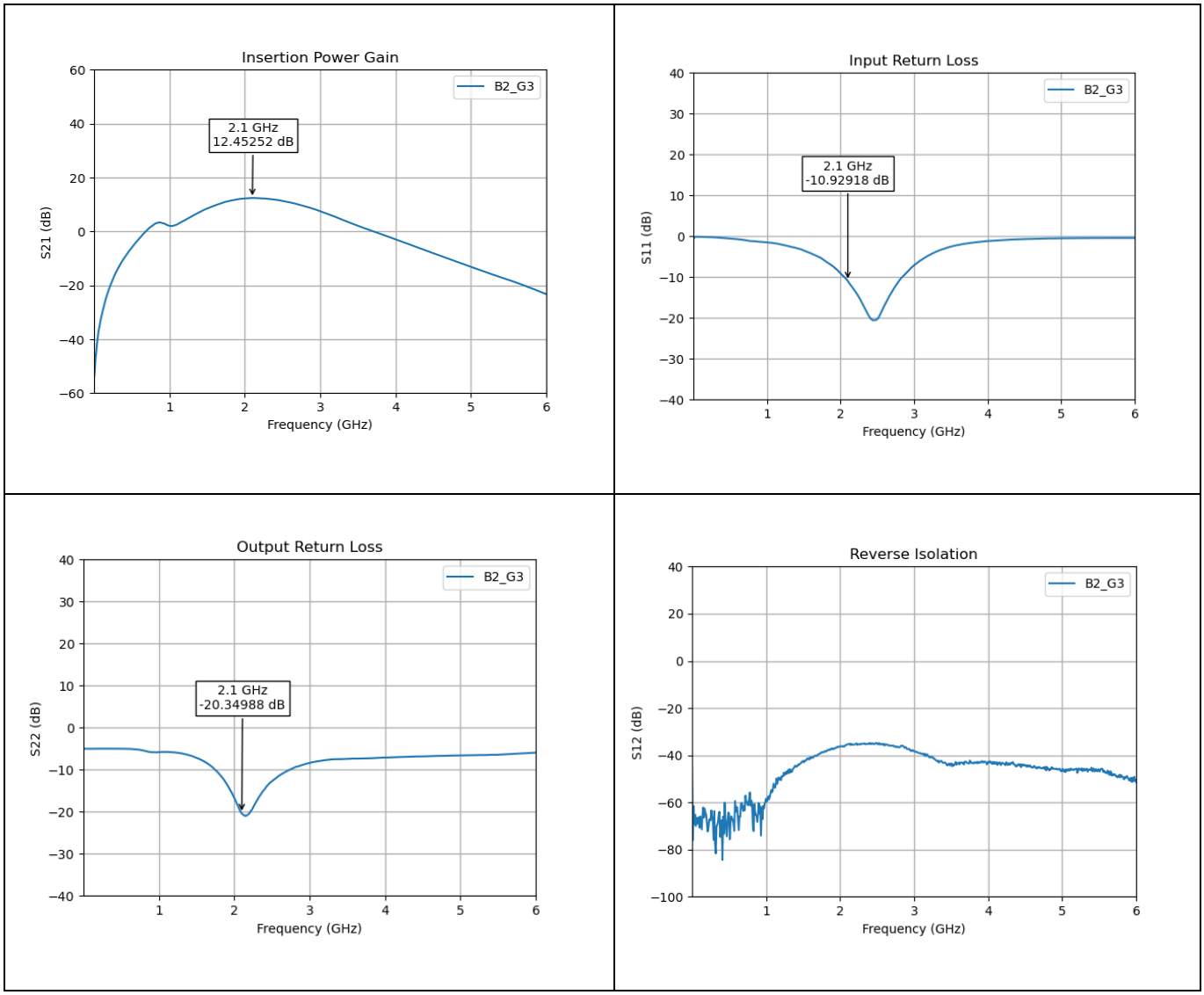


Figure 28 S-Parameters @ 1.8V in Gain 3 Bias 2 Mode

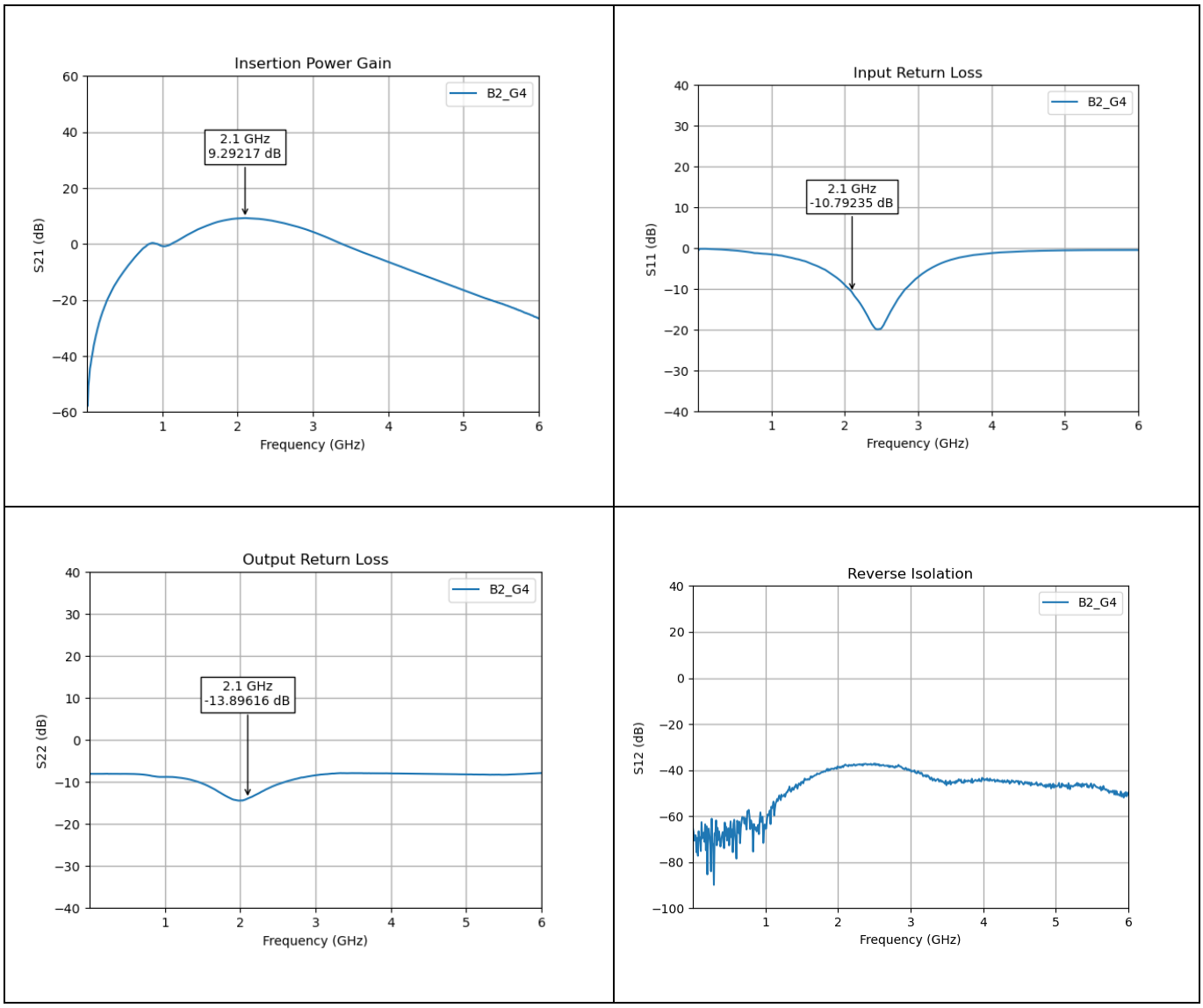
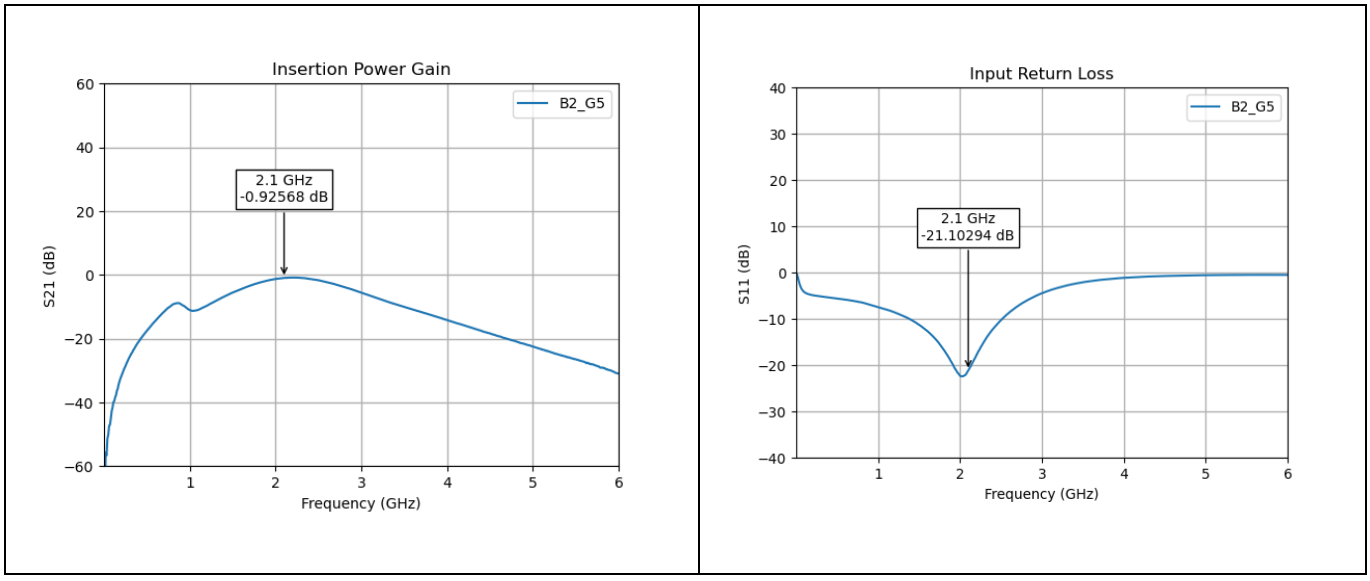


Figure 29 S-Parameters @ 1.8V in Gain 4 Bias 2 Mode



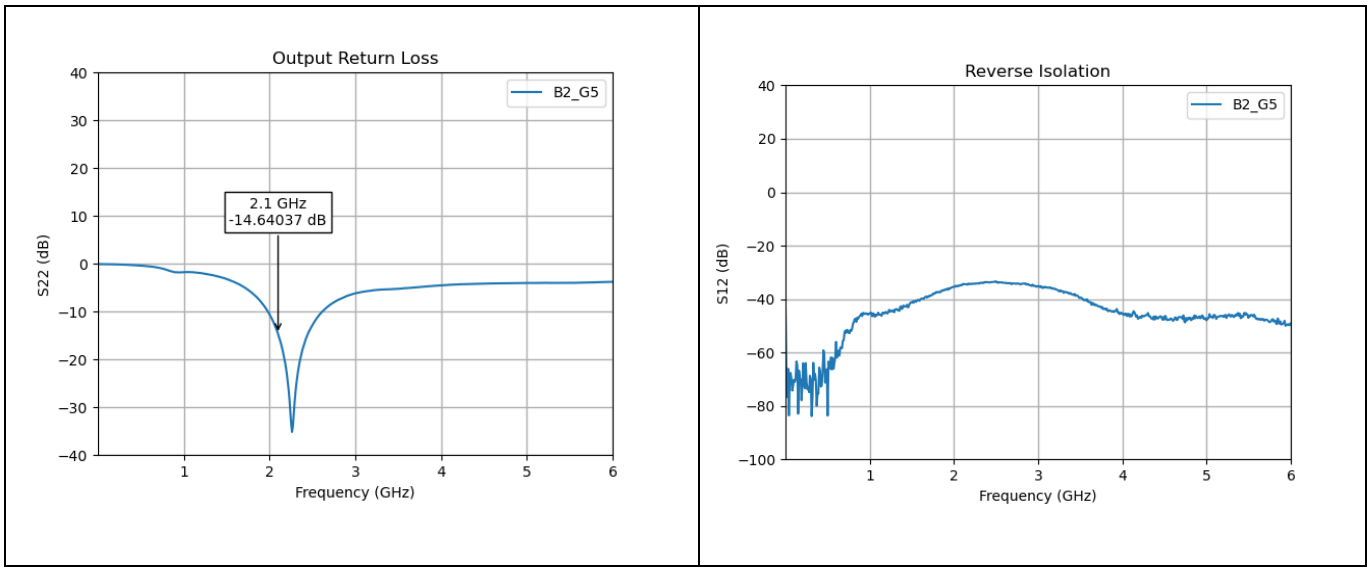


Figure 30 S-Parameters @ 1.8V in Gain 5 Bias 2 Mode

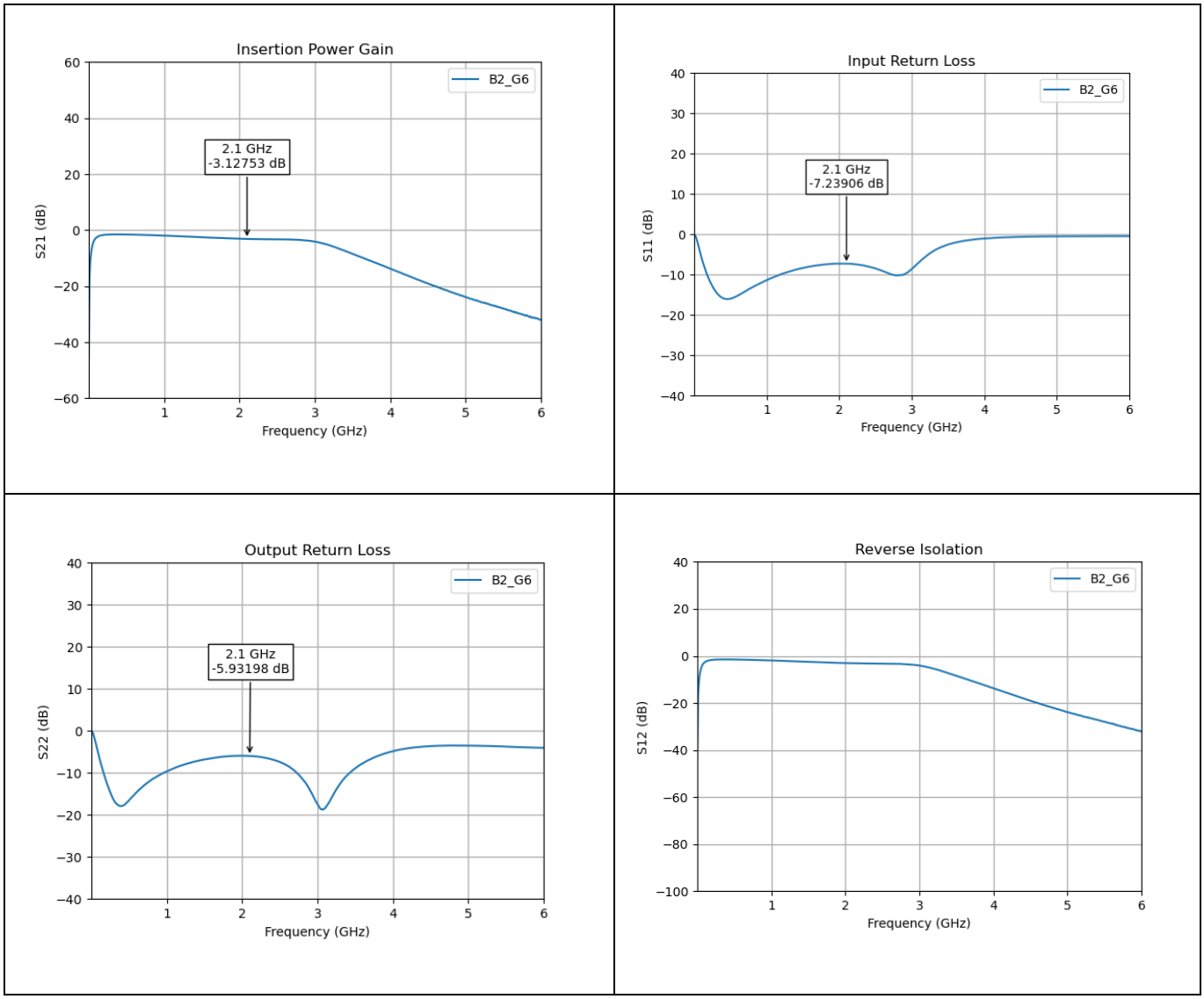


Figure 31 S-Parameters @ 1.8V in Gain 6 Bypass

4.2.2 Noise Figure Results

All NF measurements show the chip performance (de-embedded NF) at T = 25 ◦C, $Power_{RF}$ = -30 dBm and V_{cc} = 1.8V for Gain modes 2 through 5 using Bias mode 6 and Gain modes 0 and 1 using Bias mode 2.

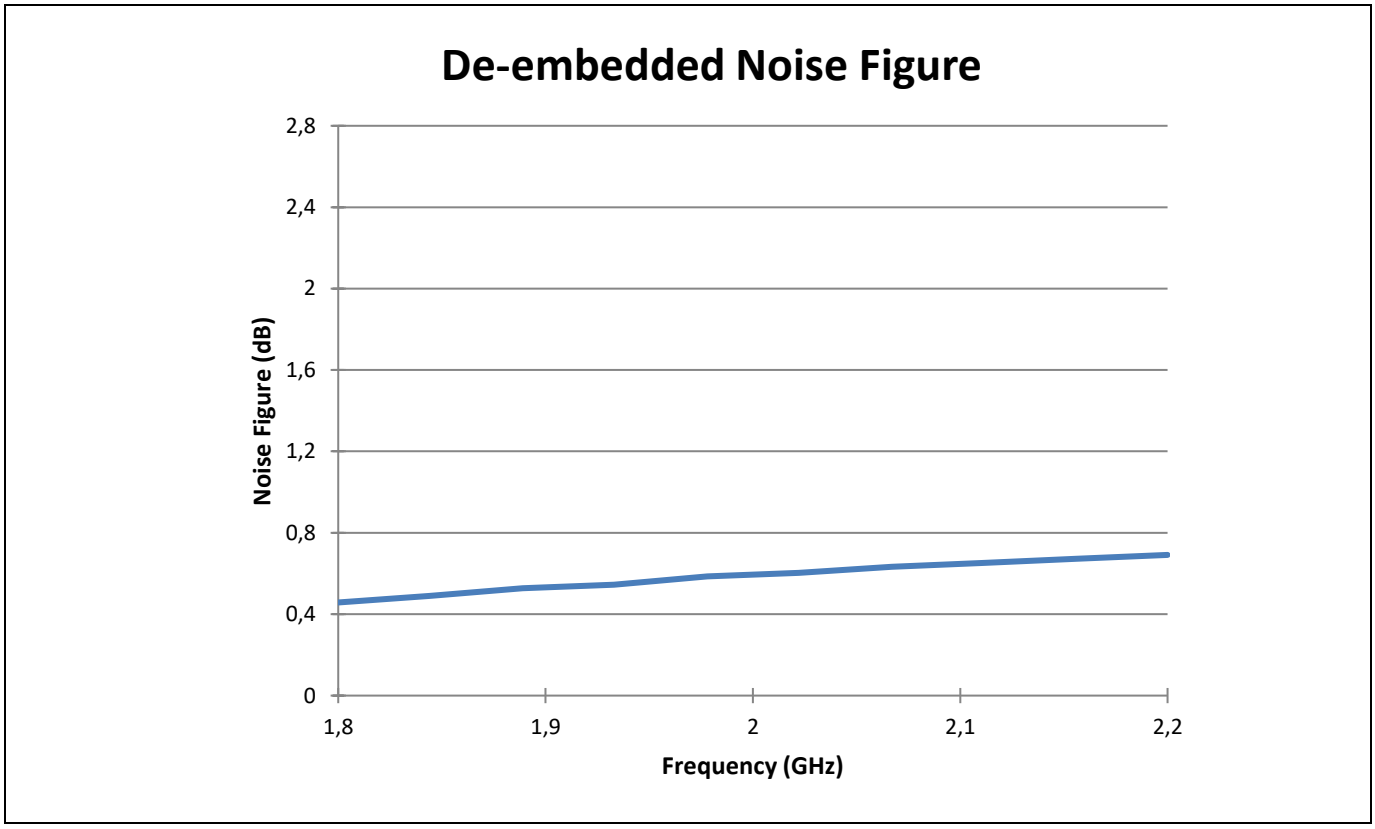


Figure 32 Noise Figure @ 1.8V in Gain 0 Bias 6 Mode

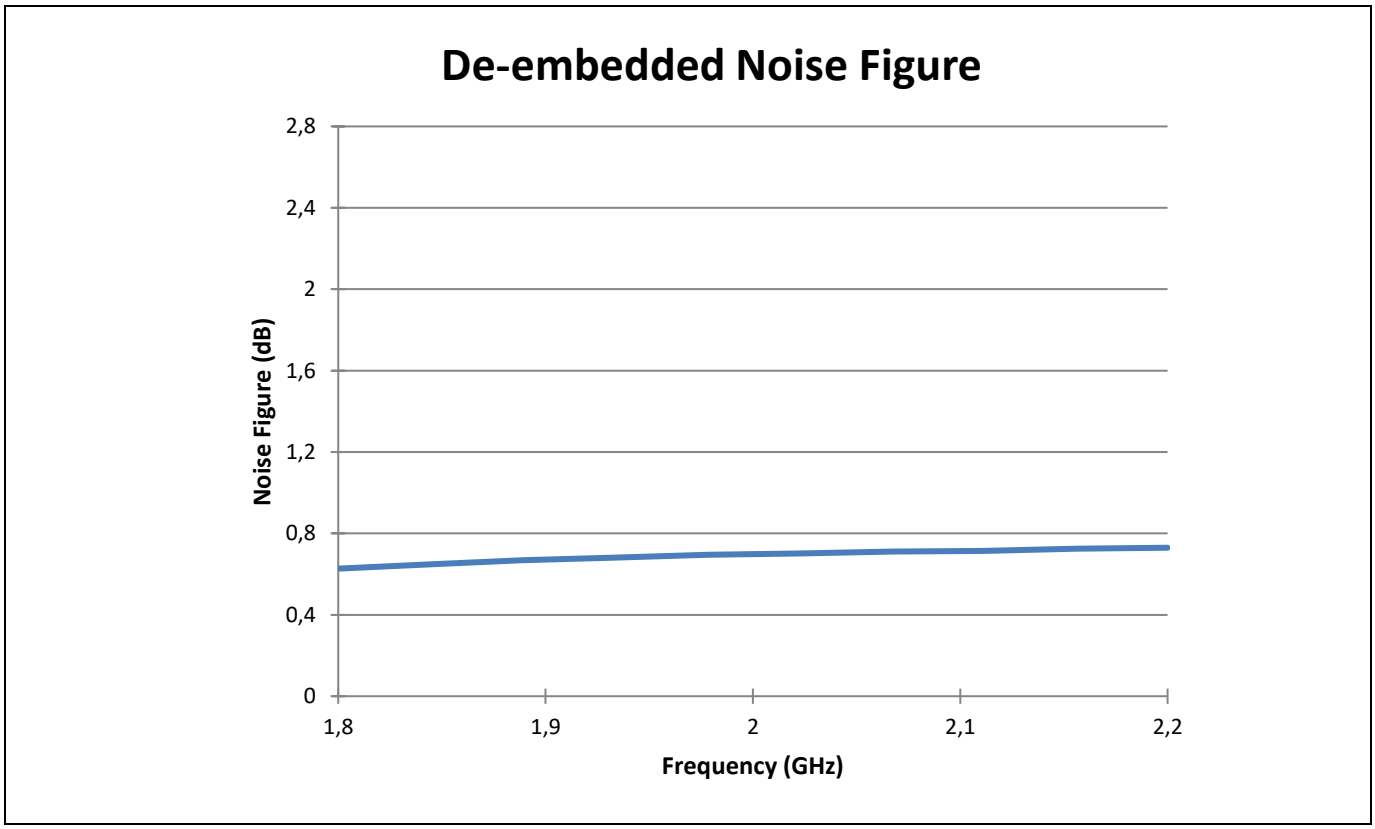


Figure 33 Noise Figure @ 1.8V in Gain 1 Bias 6 Mode

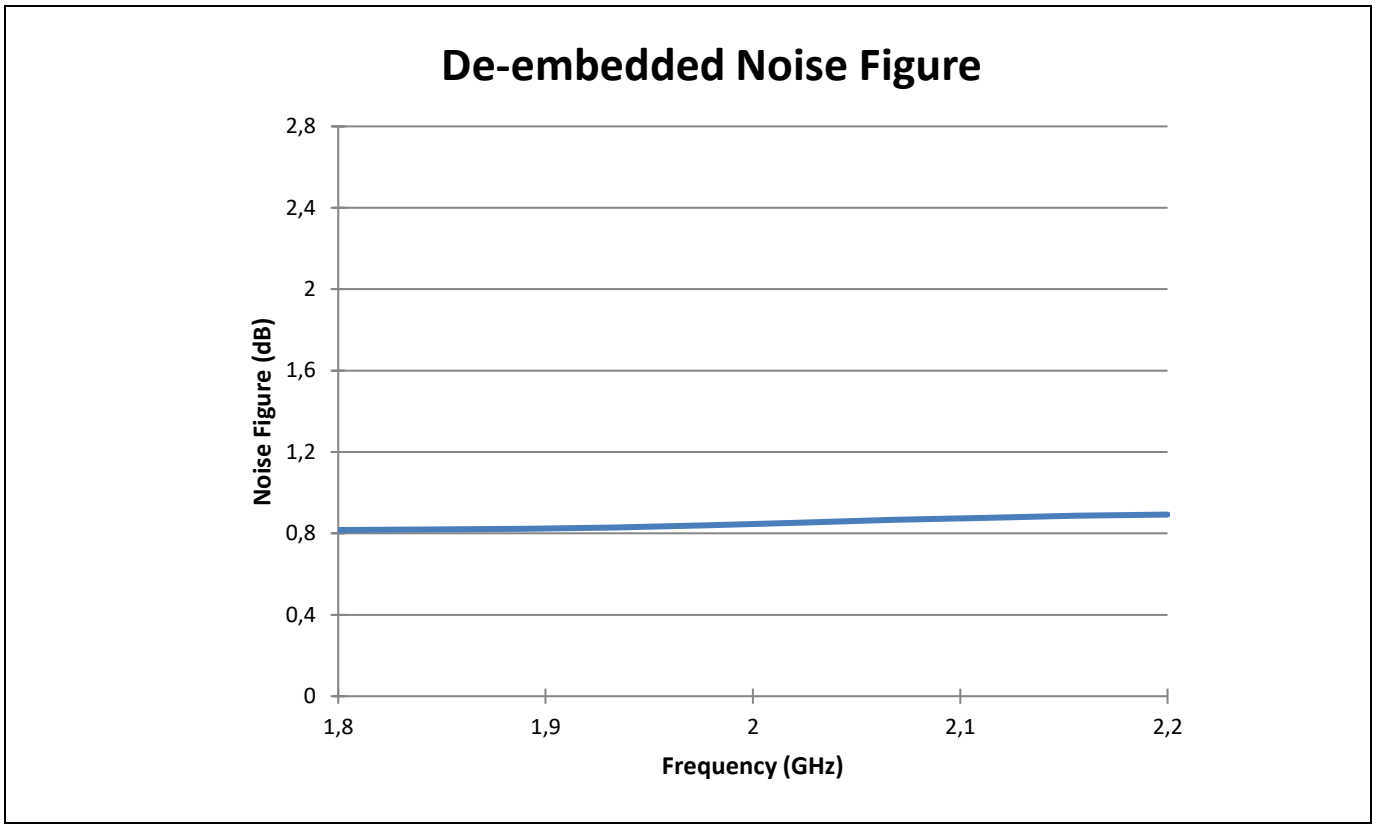


Figure 34 Noise Figure @ 1.8V in Gain 2 Bias 2 Mode

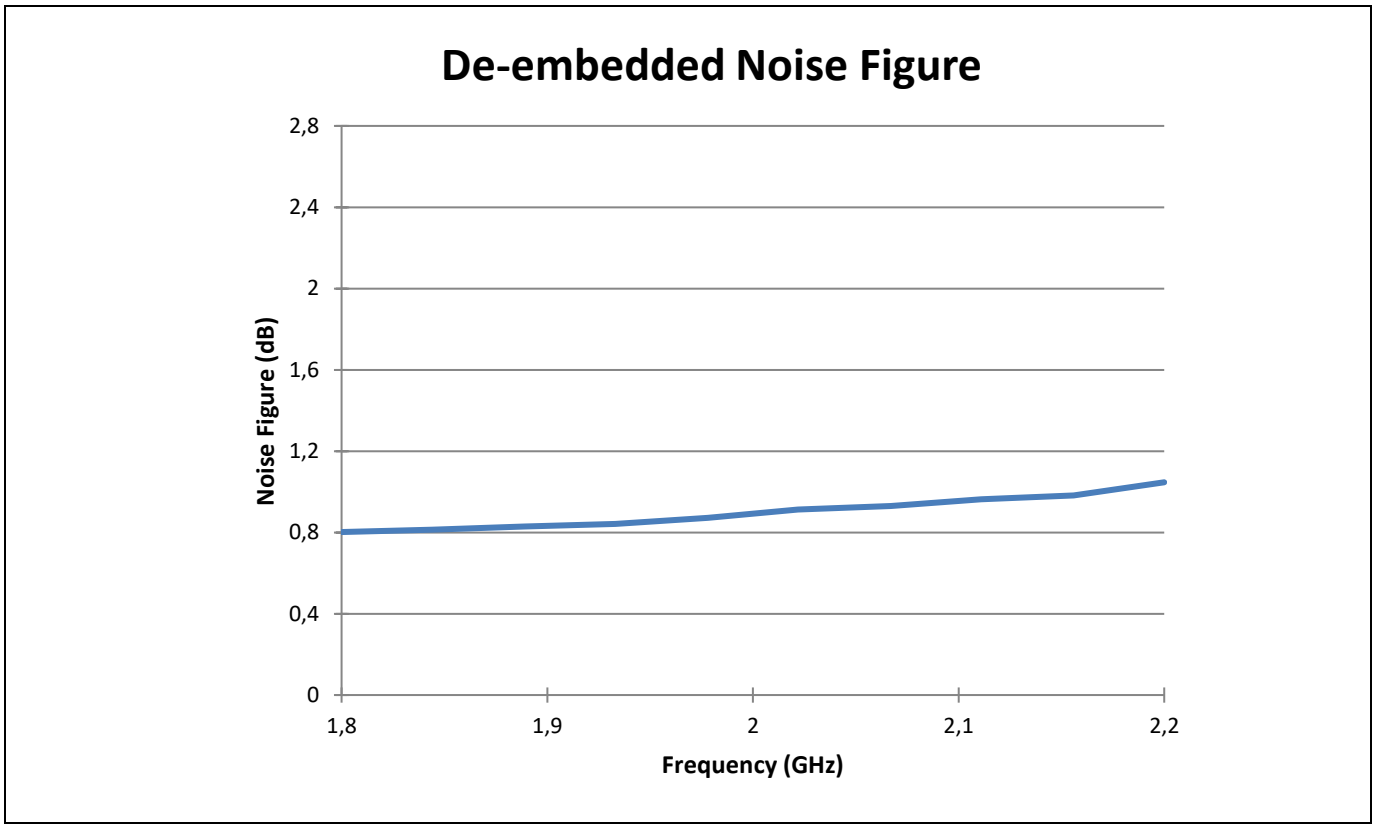


Figure 35 Noise Figure @ 1.8V in Gain 3 Bias 2 Mode

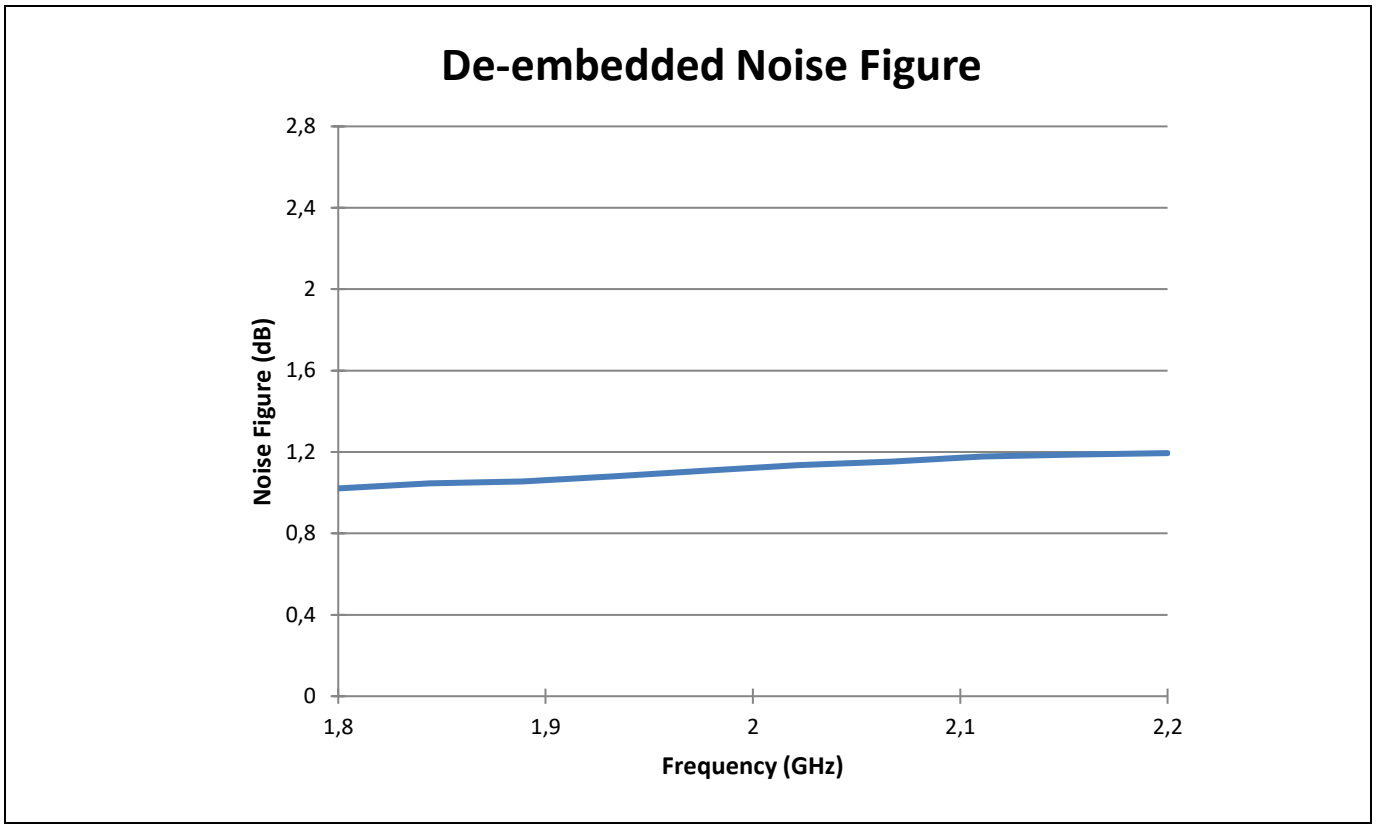


Figure 36 Noise Figure @ 1.8V in Gain 4 Bias 2 Mode

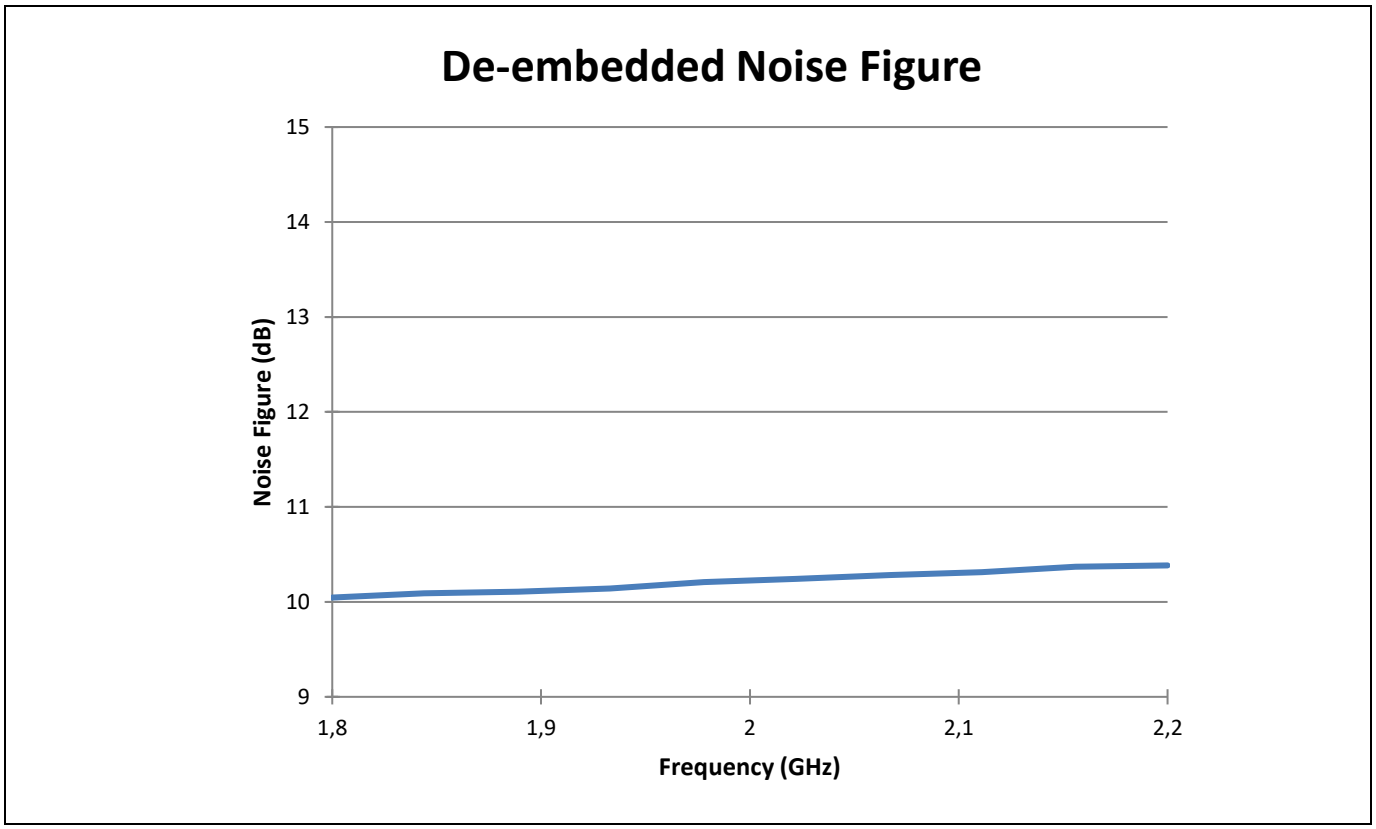


Figure 37 Noise Figure @ 1.8V in Gain 5 Bias 2 Mode

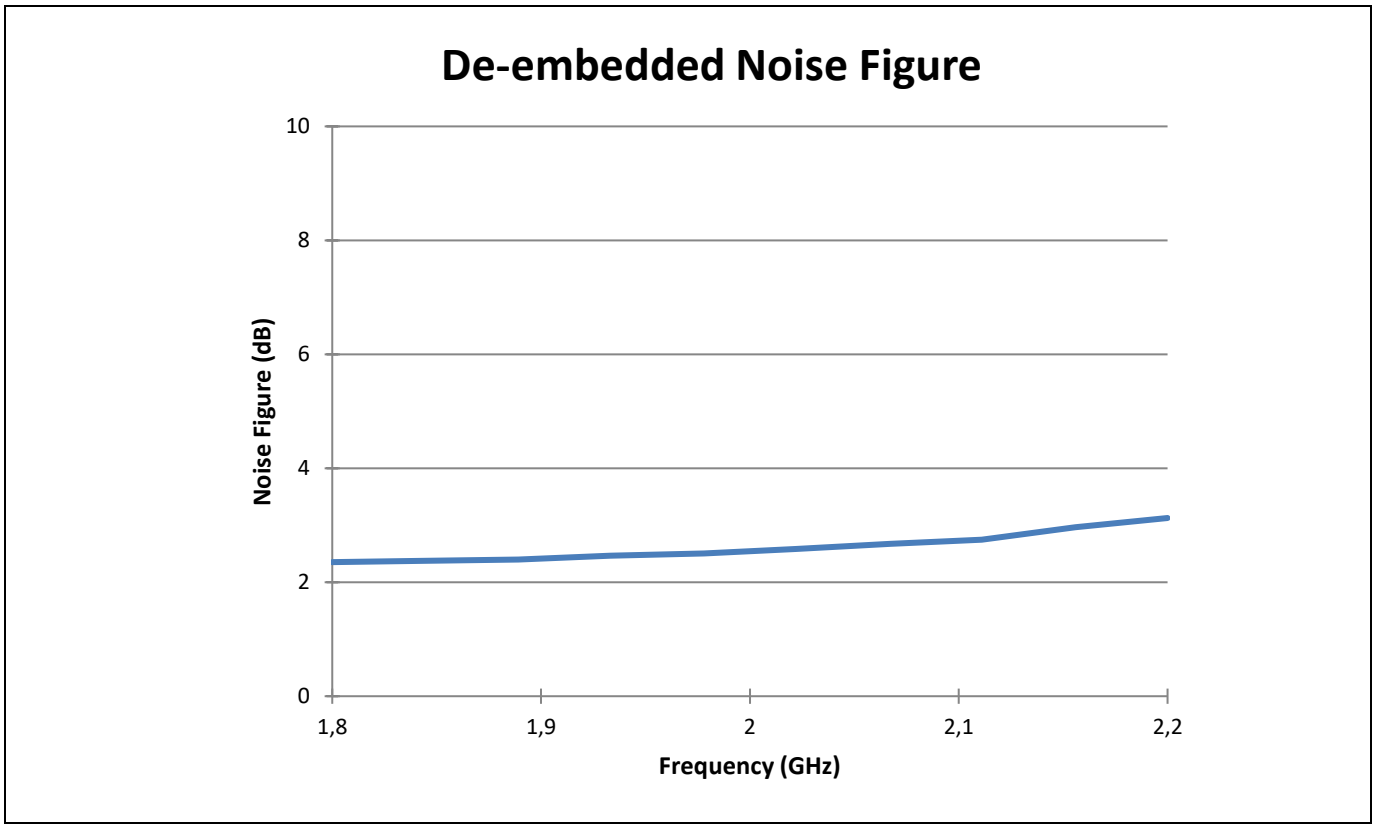
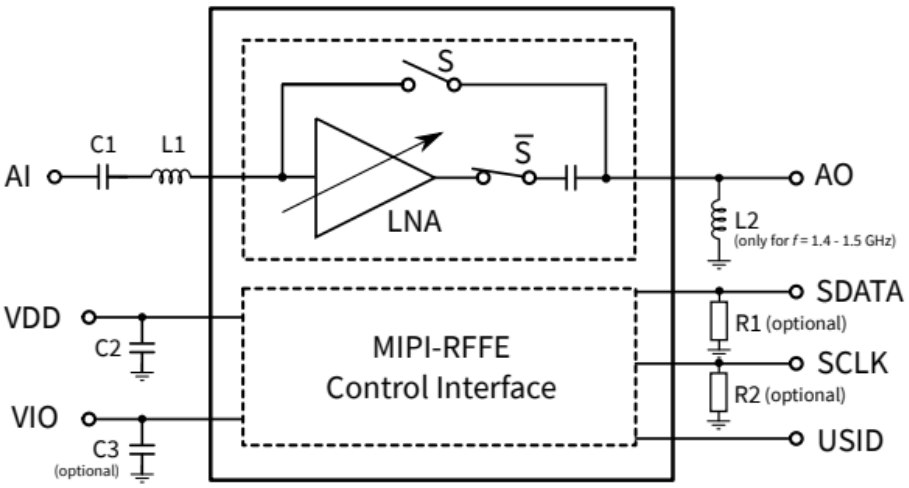


Figure 38 Noise Figure @ 1.8V in Gain 6 Bypass

4.3 Configuration for 2300 – 2700 MHz



S-Parameter measurements are done from SMA connector to SMA connector at T = 25 ◦C, $Power_{RF}$ = -30 dBm and V_{cc} = 1.8V for Gain modes 2 through 5 using Bias mode 6 and Gain modes 0 and 1 using Bias mode 2.

4.3.1 S-Parameters

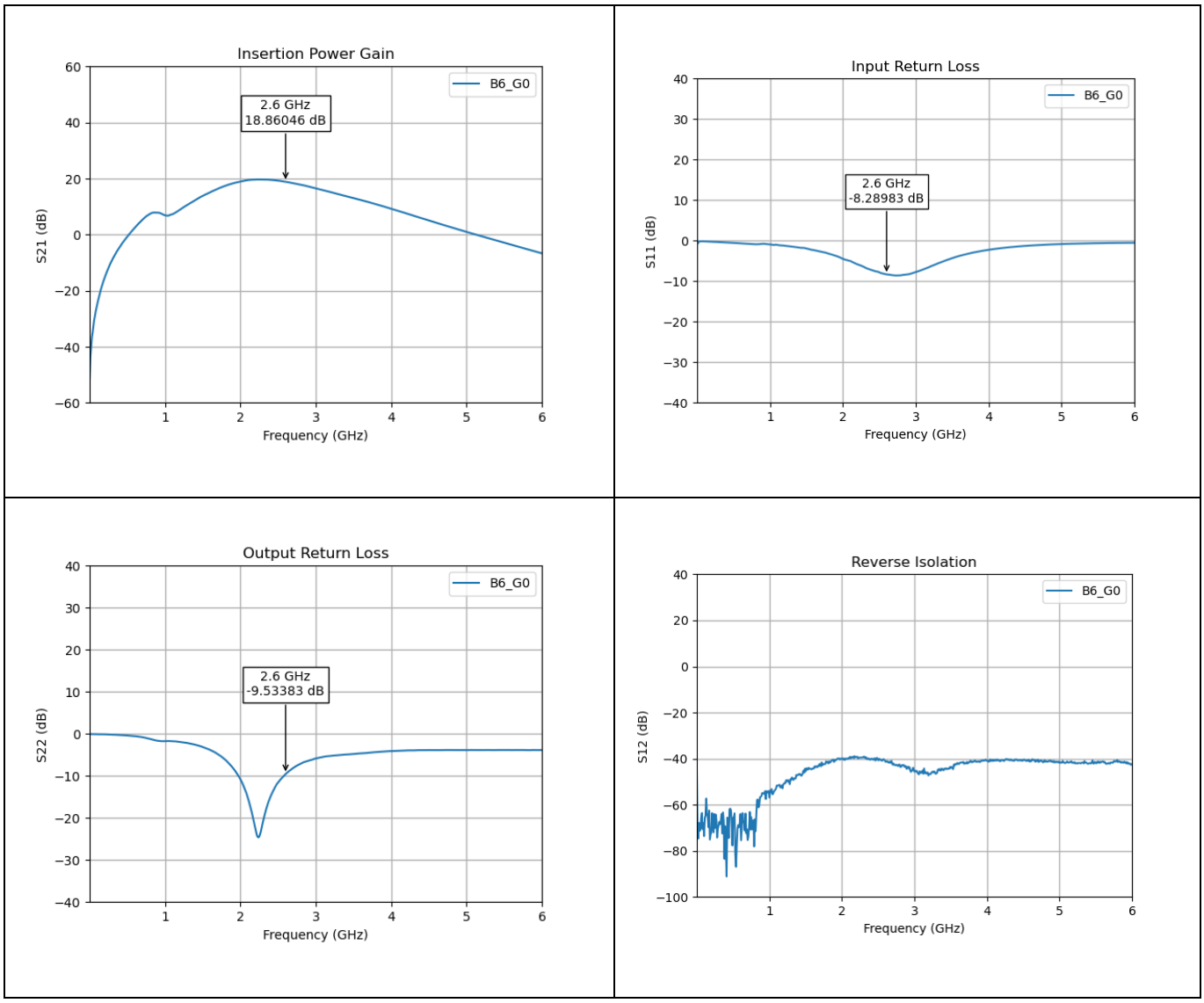
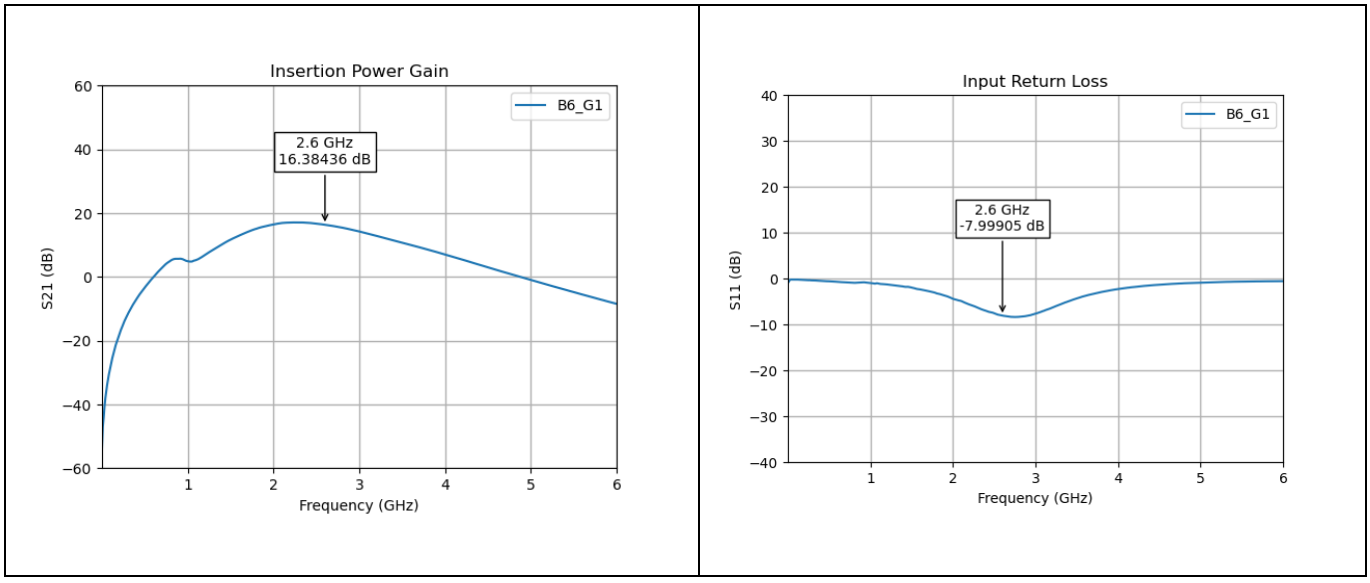


Figure 39 S-Parameters @ 1.8V in Gain 0 Bias 6 Mode



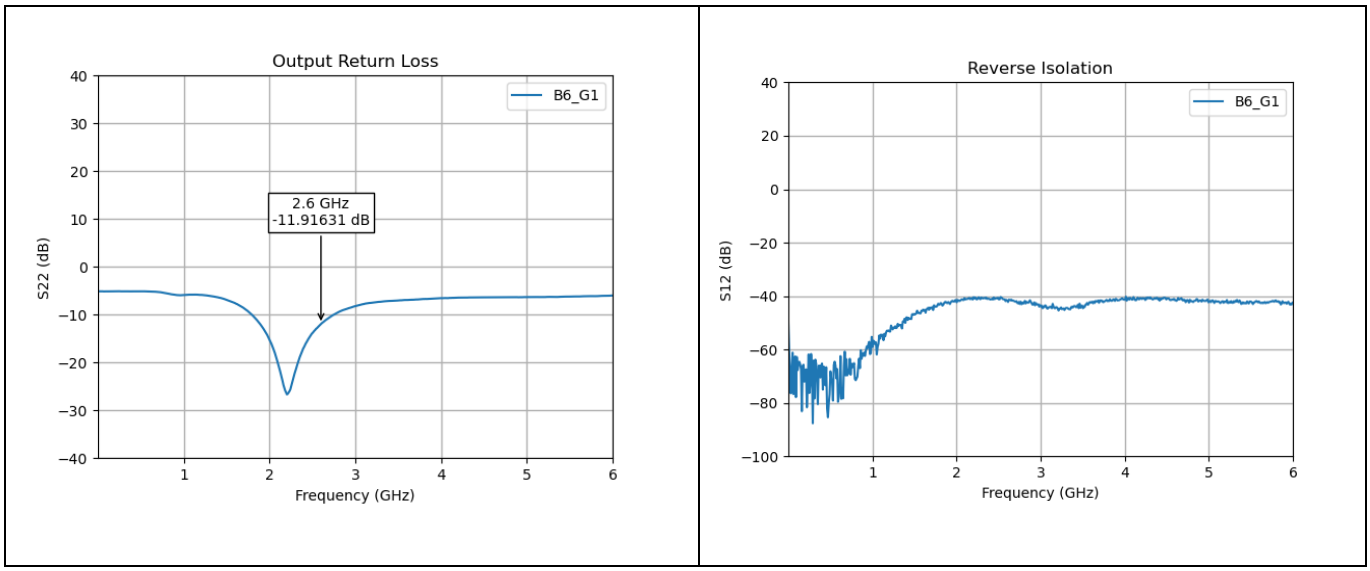


Figure 40 S-Parameters @ 1.8V in Gain 1 Bias 6 Mode

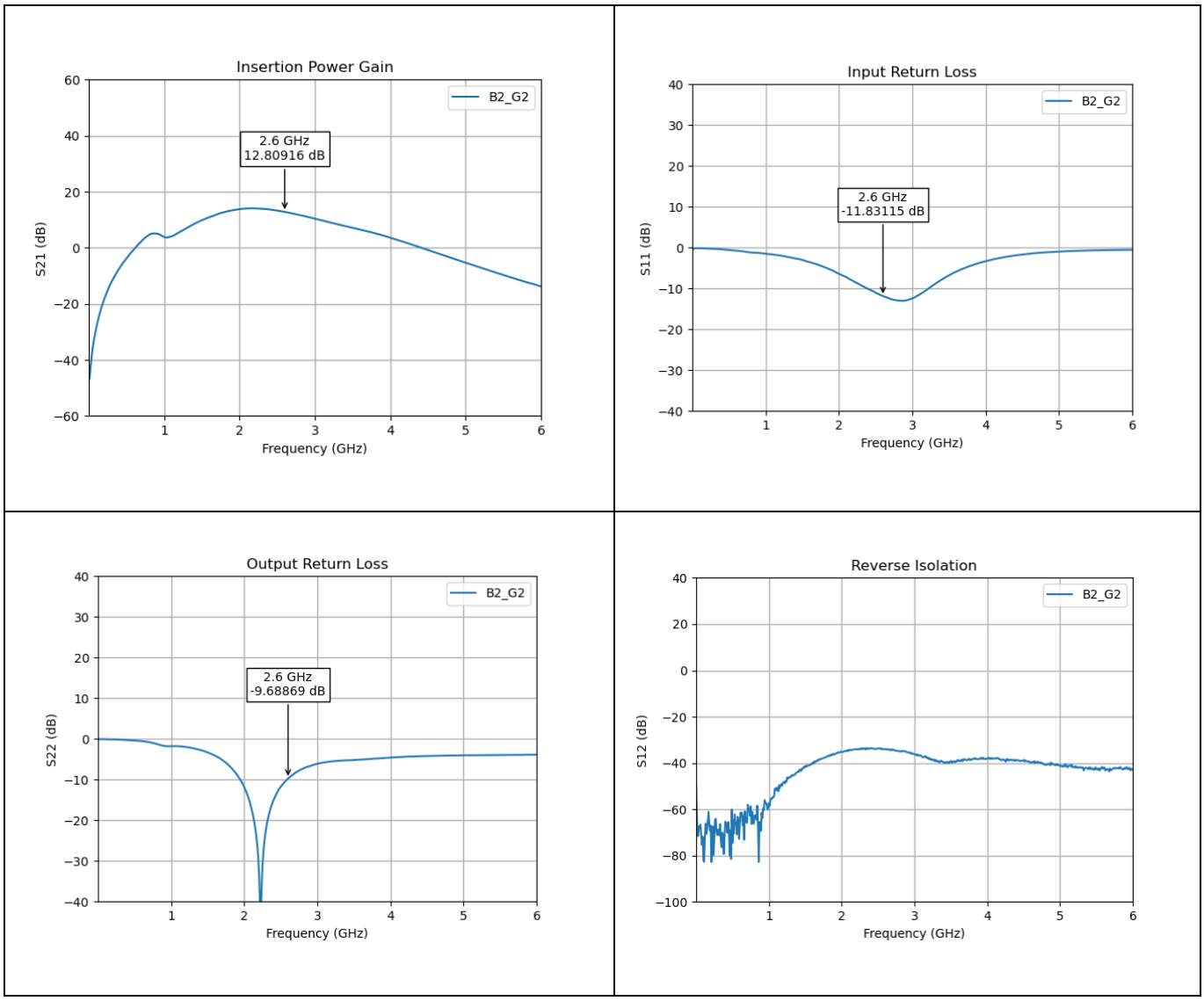


Figure 41 S-Parameters @ 1.8V in Gain 2 Bias 2 Mode

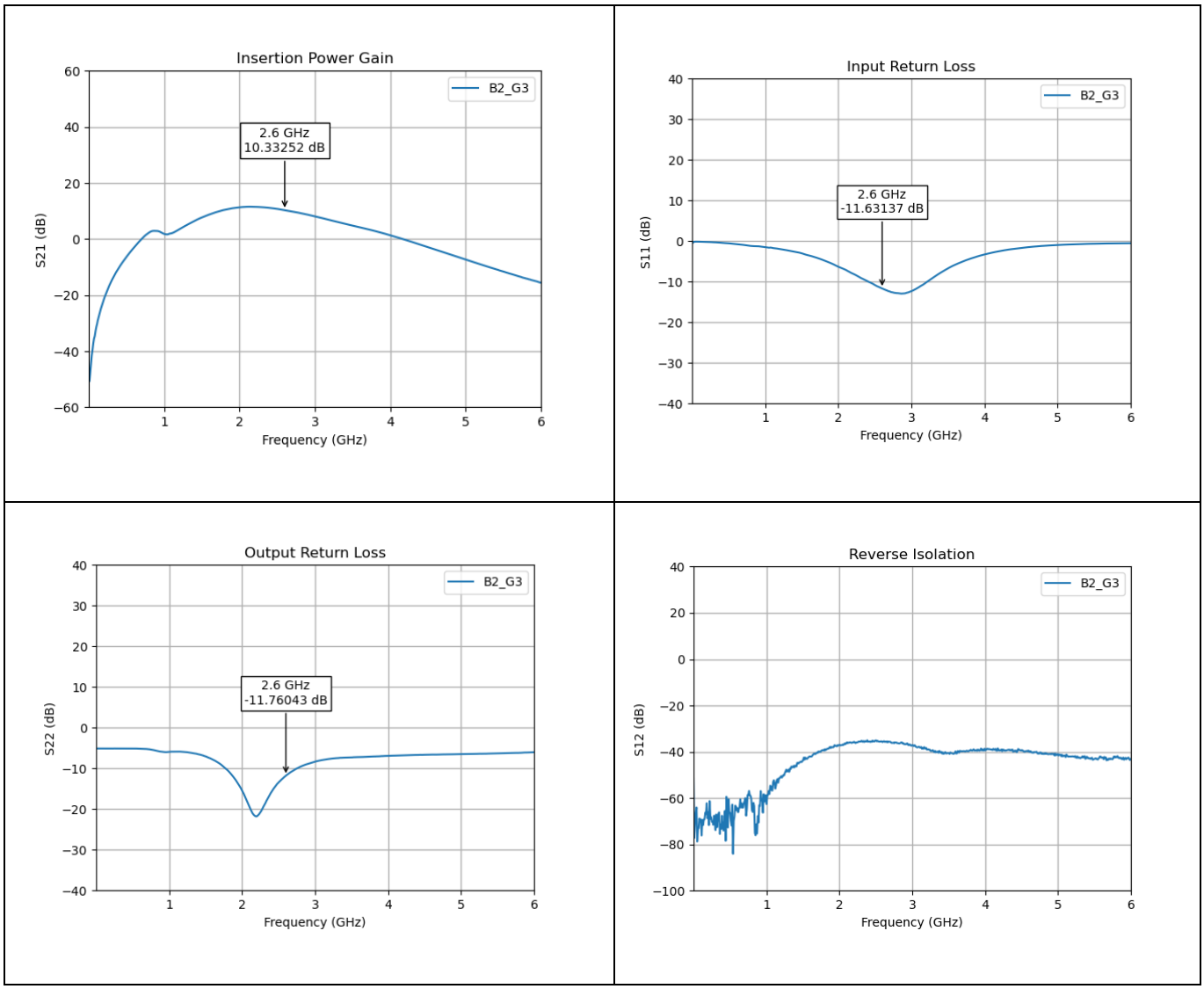
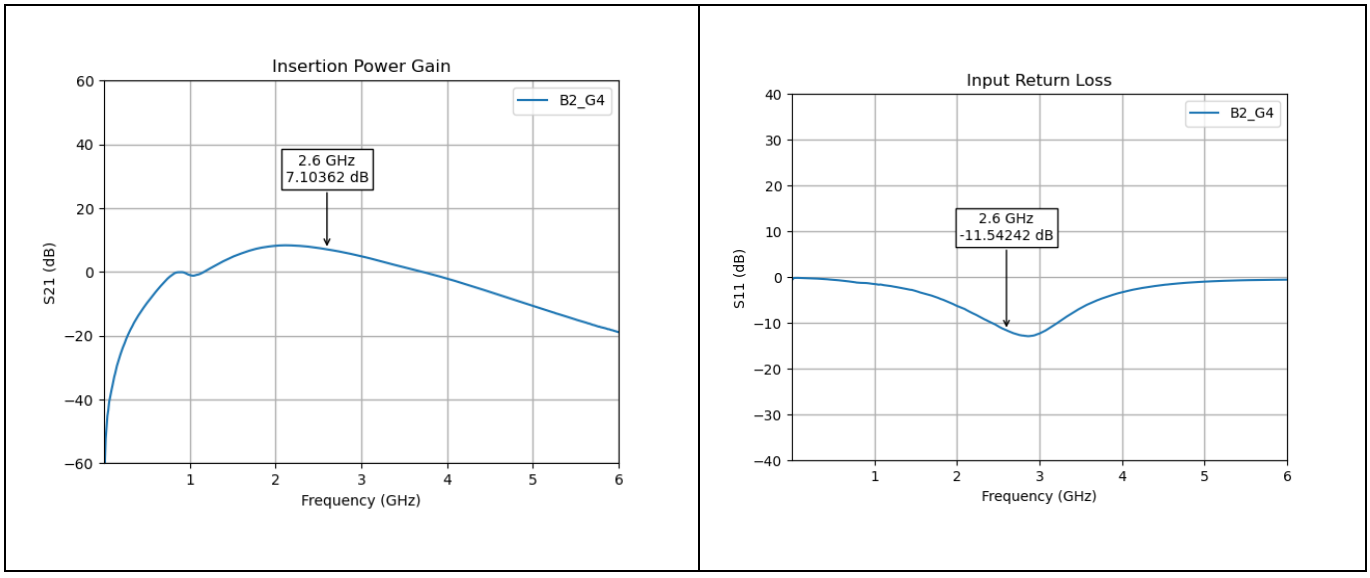


Figure 42 S-Parameters @ 1.8V in Gain 3 Bias 2 Mode



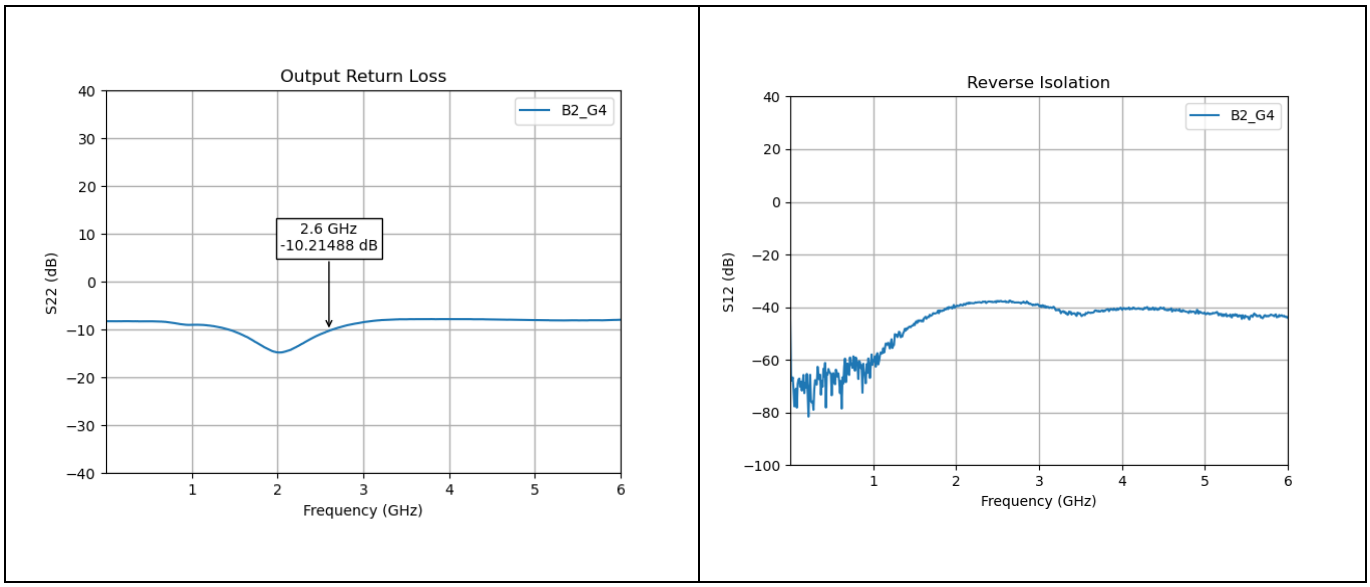


Figure 43 S-Parameters @ 1.8V in Gain 4 Bias 2 Mode

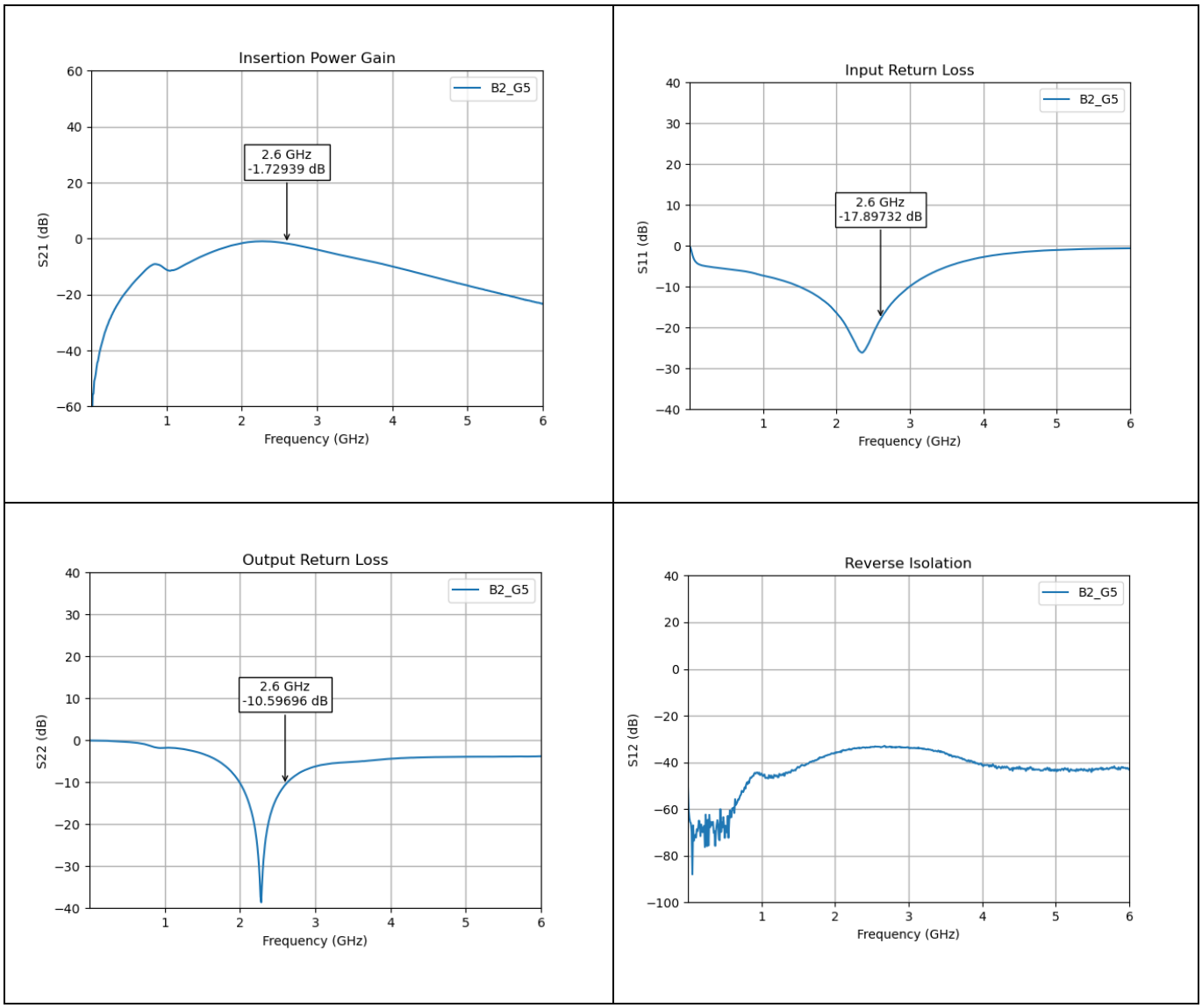


Figure 44 S-Parameters @ 1.8V in Gain 5 Bias 2 Mode

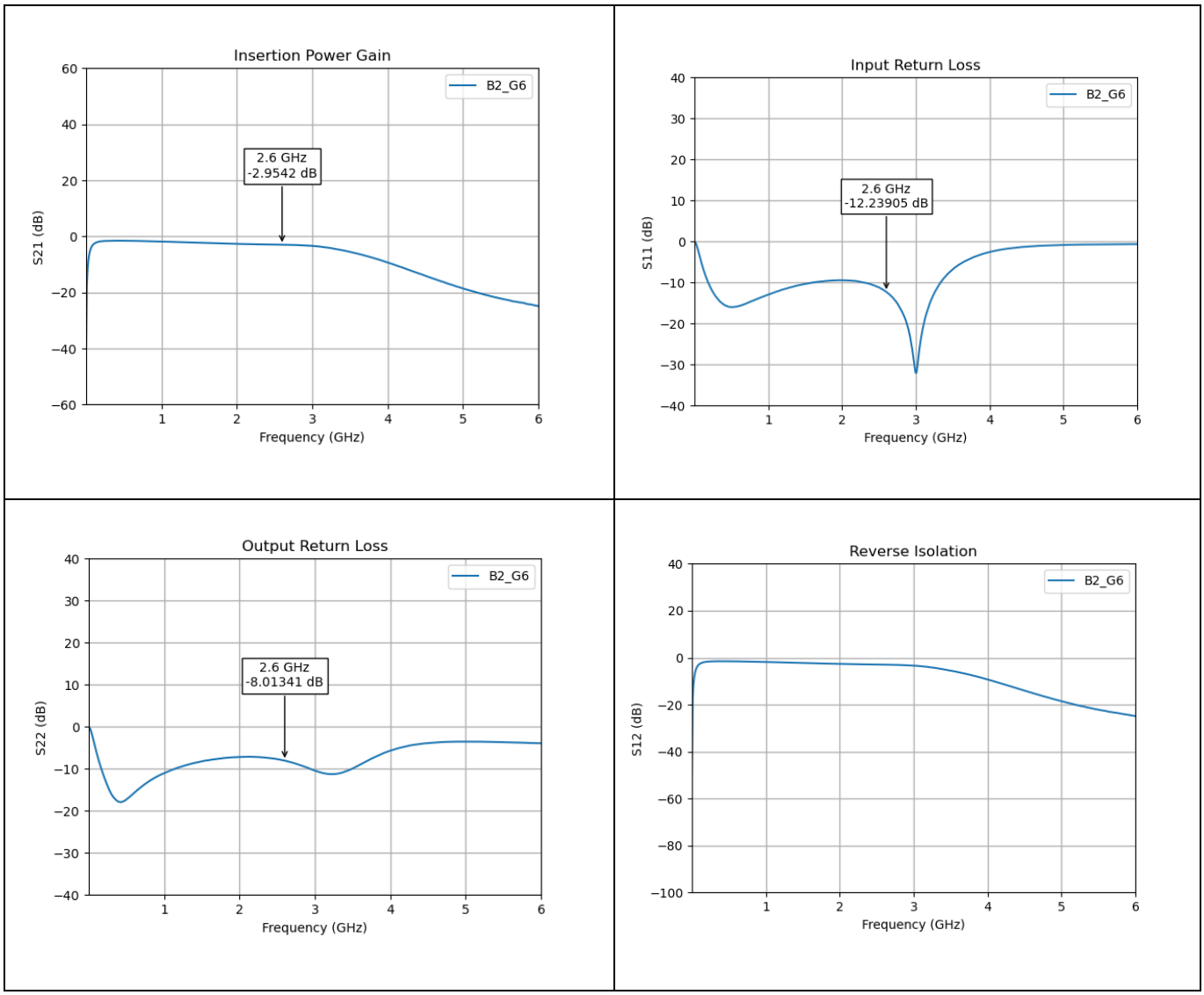


Figure 45 S-Parameters @ 1.8V in Gain 6 Bypass

4.3.2 Noise Figure Results

All NF measurements show the chip performance (de-embedded NF) at T = 25 ◦C, $Power_{RF}$ = -30 dBm and V_{cc} = 1.8V for Gain modes 2 through 5 using Bias mode 6 and Gain modes 0 and 1 using Bias mode 2.

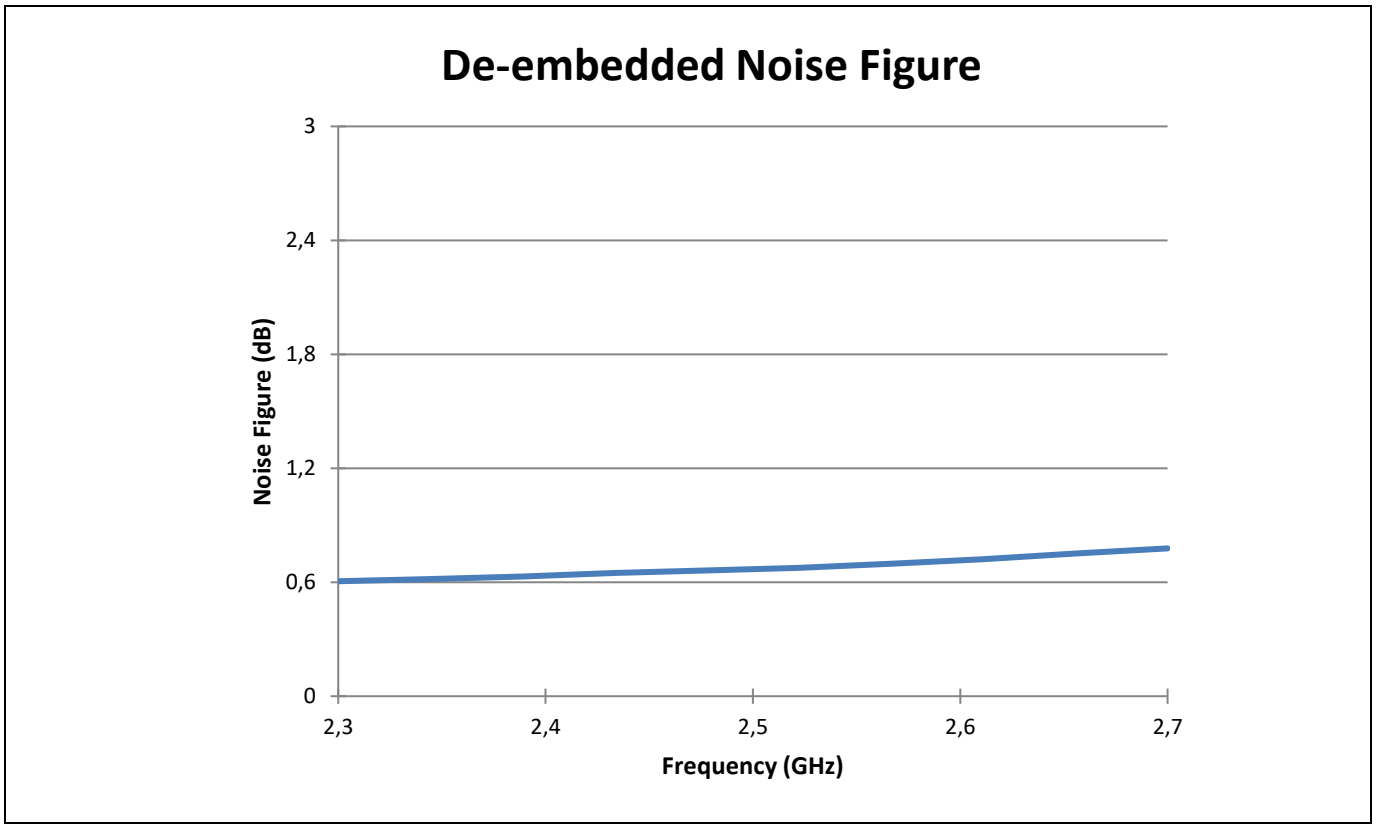


Figure 46 Noise Figure @ 1.8V in Gain 0 Bias 6 Mode

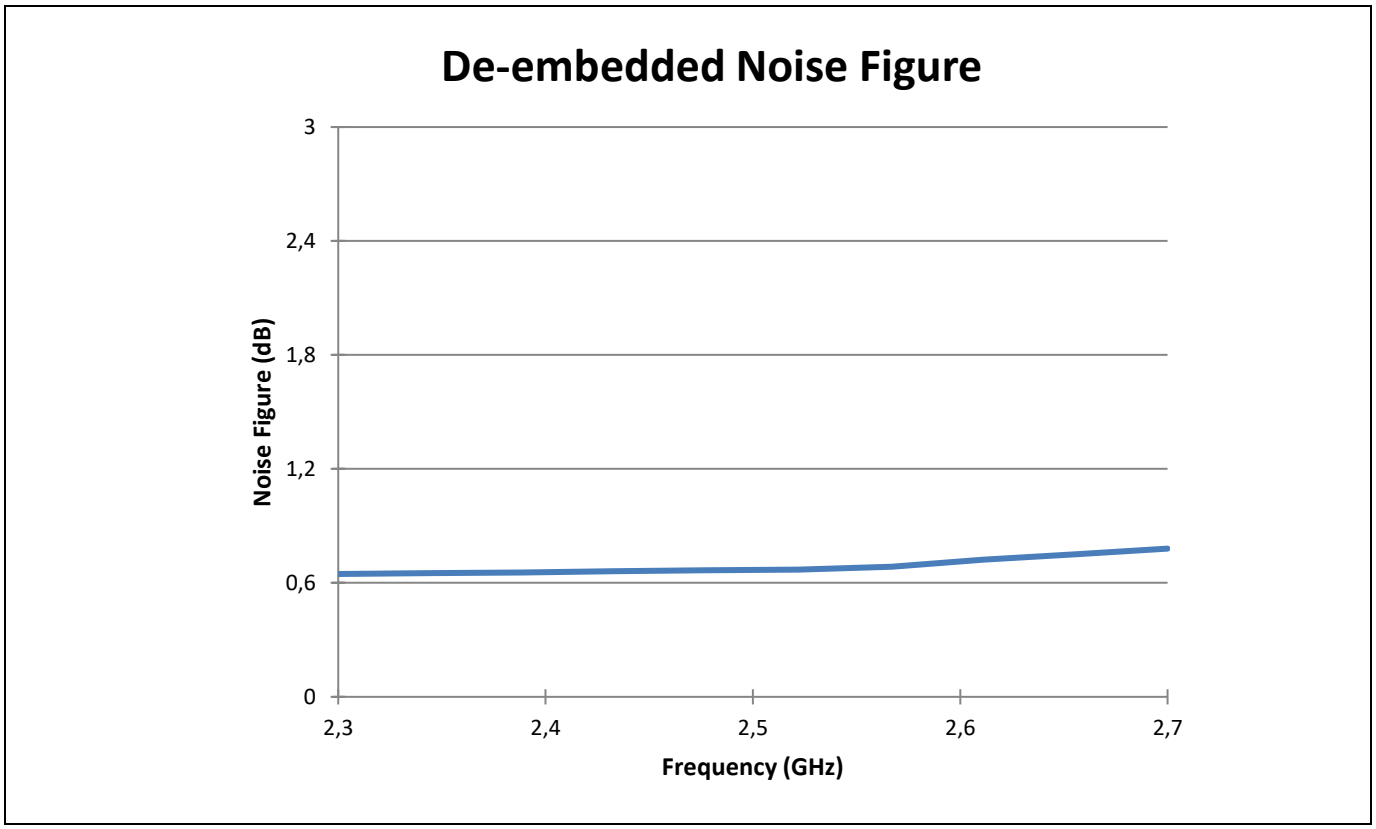


Figure 47 Noise Figure @ 1.8V in Gain 1 Bias 6 Mode

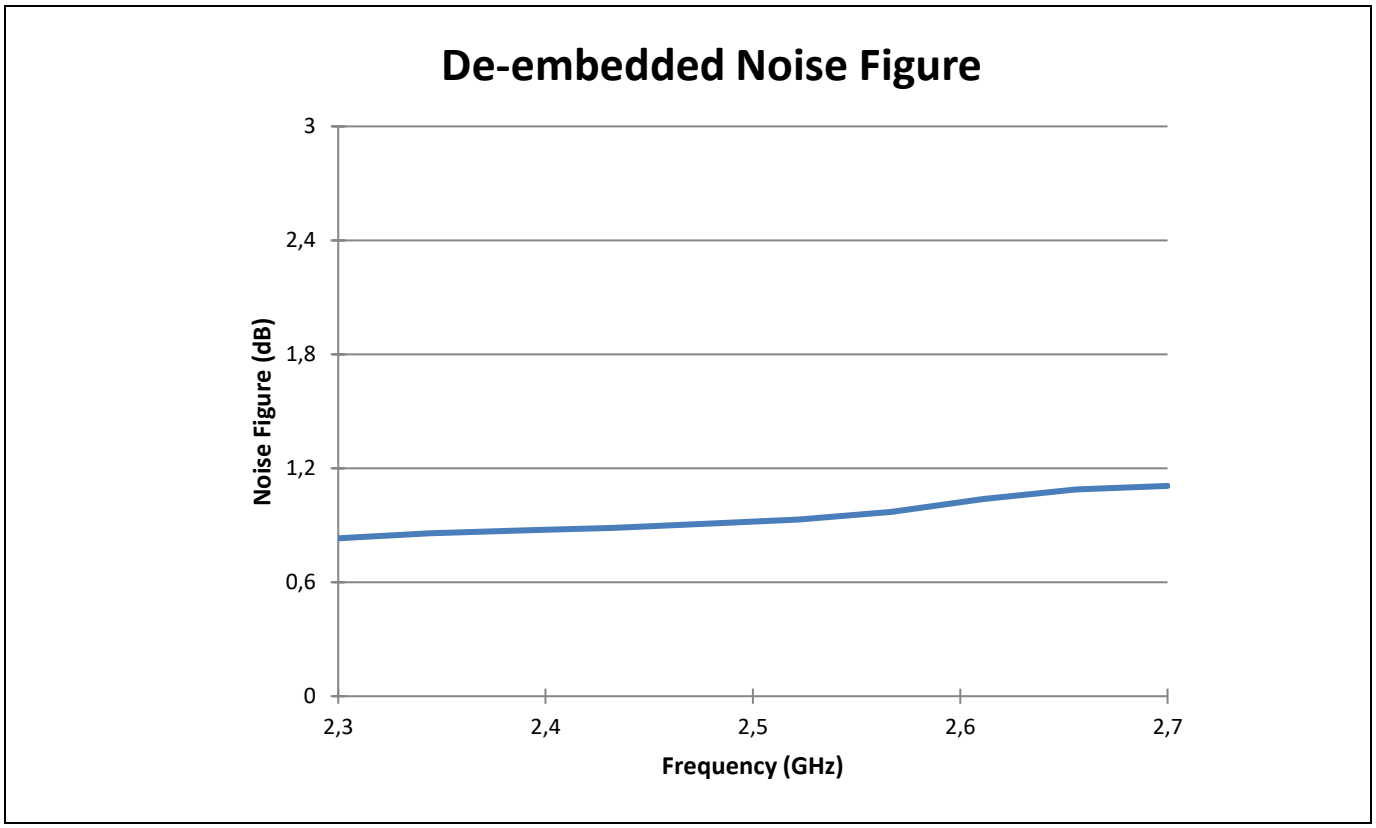


Figure 48 Noise Figure @ 1.8V in Gain 2 Bias 2 Mode

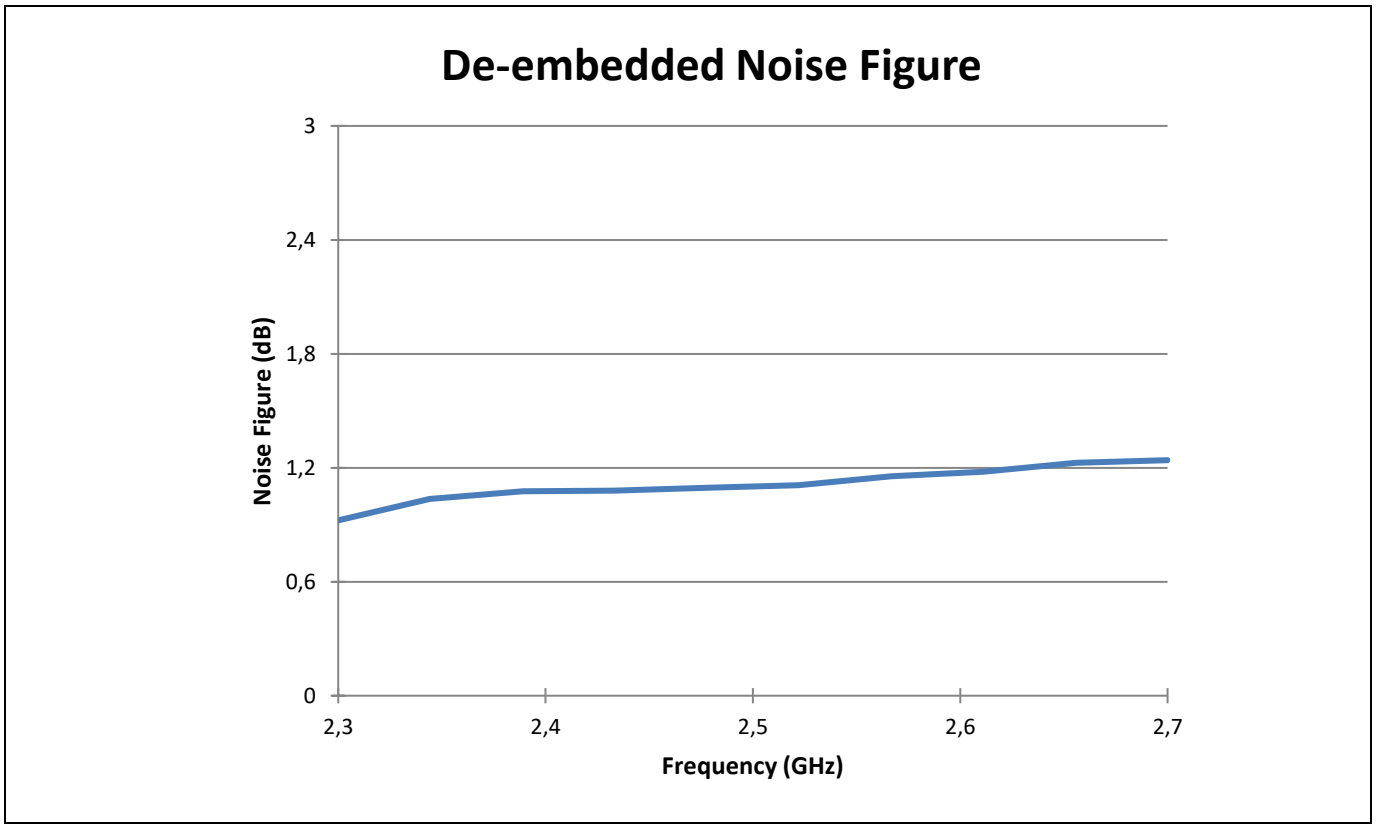


Figure 49 Noise Figure @ 1.8V in Gain 3 Bias 2 Mode

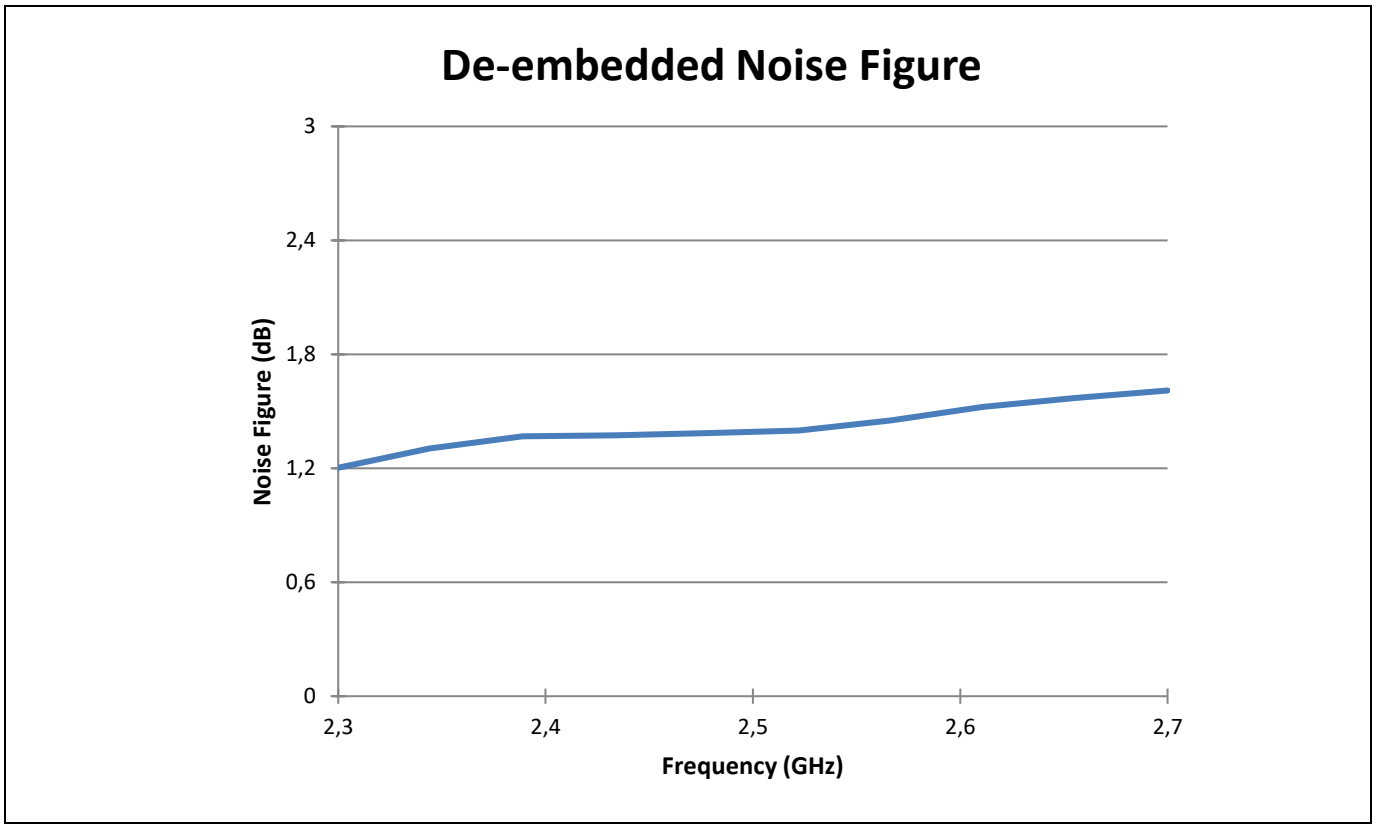


Figure 50 Noise Figure @ 1.8V in Gain 4 Bias 2 Mode

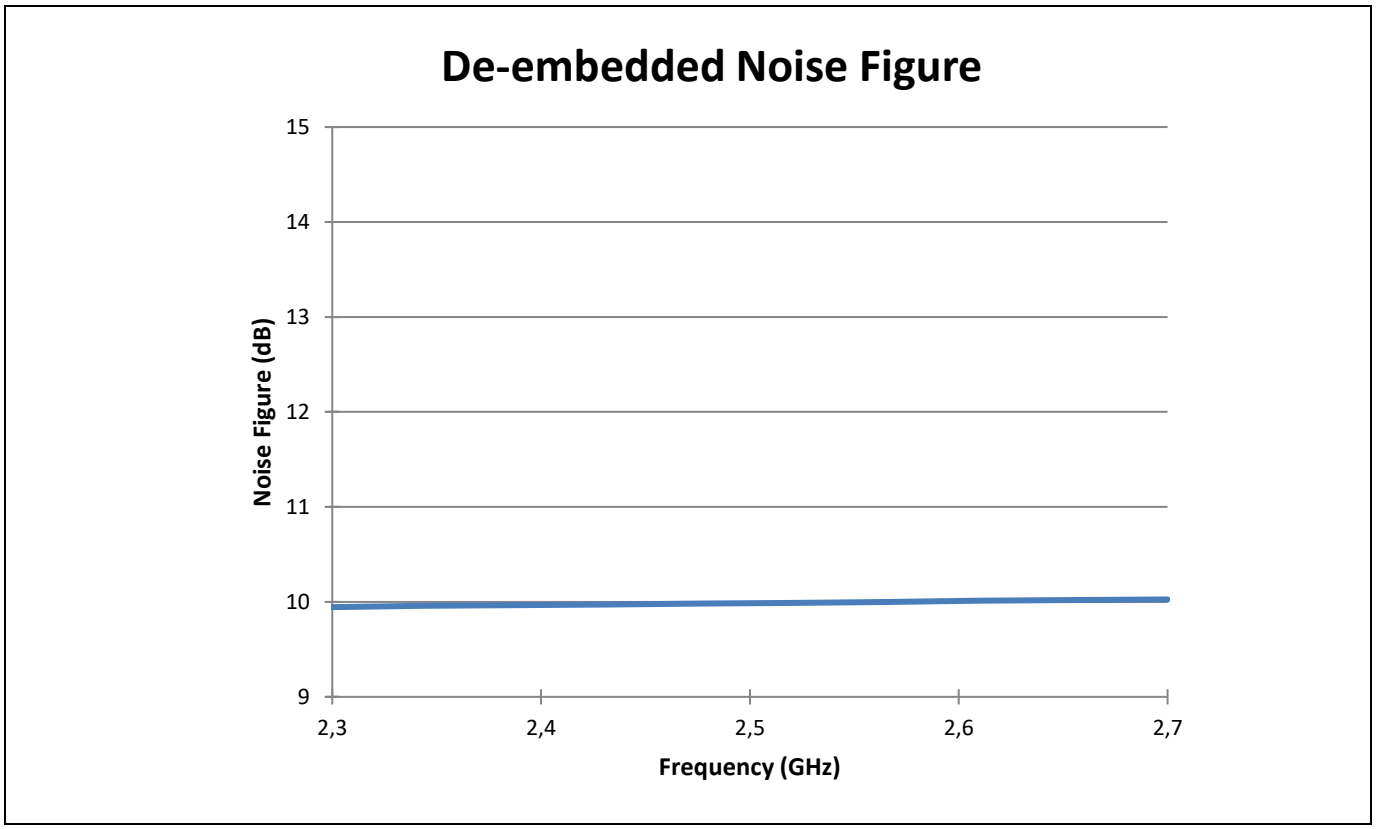


Figure 51 Noise Figure @ 1.8V in Gain 5 Bias 2 Mode

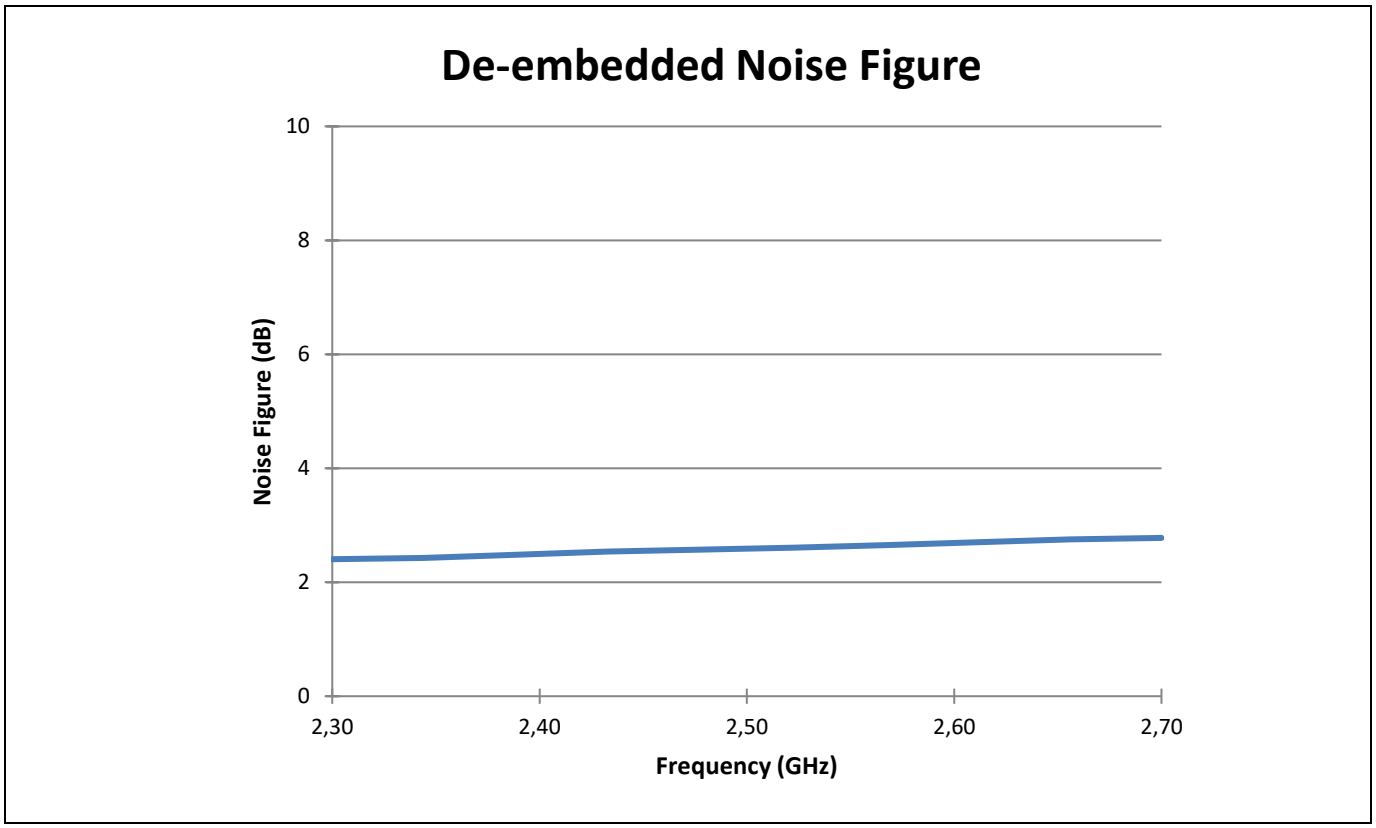


Figure 52 Noise Figure @ 1.8V in Gain 6 Bypass

Abbreviations

EVB	Evaluation Board
LNA	Low Noise Amplifier
PCB	Printed Circuit Board
RF	Radio-Frequency
MIPI	Mobile Industry Processor Interface
SMA	Subminiature Connector
VNA	Vector Network Analyzer
DUT	Device Under Test
GND	Ground

References

More information about the PCB Layout (footprints, schematics, Altium projects), standard S-Parameters and Noise Figure as well as the datasheets can be found here.

Revision history

Document version	Date of release	Description of changes
V1.0	2022-10-26	Final User Guide

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Edition 2022-04-27

Published by

Infineon Technologies AG

81726 Munich, Germany

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