3300 W CCM totem pole with 650 V CoolSiC™ in TOLL package and XMC™

REF_3K3W_TP_SIC_TOLL

About this document

Scope and purpose

This document presents a system solution based on Infineon silicon carbide trench gate (CoolSiC™) and superjunction (CoolMOS™) power semiconductors, drivers and microcontroller for a bridgeless totem-pole power factor correction (PFC) converter operated in continuos conduction mode (CCM). The REF_3K3W_TP_SIC_TOLL, thanks to the high efficiency and high-power density, is intended to be used in applications where space and efficiency are key parameters, such as high-end servers and telecoms.

The REF_3K3W_TP_SIC_TOLL has a full digital control implemented with an Infineon XMC1000 series microcontroller.

Infineon components used in this 3300 W bridgeless CCM totem-pole PFC board are:

- First-generation 650 V CoolSiC™ in TOLL package
- 600 V CoolMOS™ S7 in TOLL package
- EiceDRIVER™ 1EDB8275F, 1EDB9275F safety isolated gate drivers
- XMC1402 microcontroller
- 950 V CoolMOS™ P7 superjunction MOSFET
- ICE5QSAG CoolSET™ quasi-resonant (QR) flyback controller

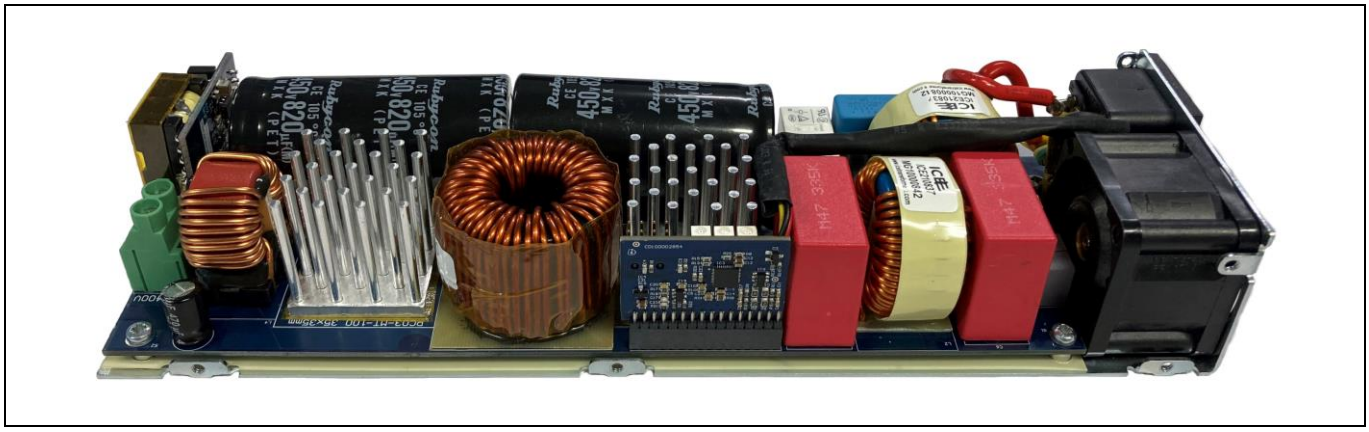

Figure 1 **3300 W bridgeless totem-pole PFC with CoolSiC™, CoolMOS™, and XMC™ digital control. The plastic enclosure has been removed for a better view.**

Table of contents

Safety information

Please read this document carefully before starting up the device.

Figure 2 Electrical hazard and hot surface warnings

Important notice

"Evaluation Boards and Reference Boards" shall mean products embedded on a printed circuit board (PCB) for demonstration and/or evaluation purposes, which include, without limitation, demonstration, reference and evaluation boards, kits and design (collectively referred to as "Reference Board").

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Operating instructions

Do not touch the device during operation, and keep a safe distance.

Do not touch the device after disconnecting the power supply, as several components may still store electrical voltage and can discharge through physical contact. Several parts, like heatsinks and transformers, may still be very hot. Allow the components to cool before touching or servicing.

All work such as construction, verification, commissioning, operation, measurements, adaptations and other work on the device (applicable national accident prevention rules must be observed) must be done by trained personnel. The electrical installation must be completed in accordance with the appropriate safety requirements

Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Warning:** *The evaluation or reference board contains DC bus capacitors, which take time to discharge after removal of the main supply. Before working on the converter system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation or reference board is connected to the AC input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the converter before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heatsink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the converter, power electronics and associated equipment should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A converter that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the cabling, supplying an incorrect or inadequate AC supply or excessive ambient temperatures may result in system malfunction.*

1 System description

The REF_3K3W_TP_SIC_TOLL board is a system solution enabled by Infineon Technologies power semiconductors as well as drivers and microcontroller. The evaluation board consists of a bridgeless totem-pole topology and it is intended for high-end applications in which high efficiency and high power density are required. Furthermore, the totem-pole topology is simple and offers a reduced part count and full utilization of the PFC inductor and switches [1]. For these reasons, totem-pole PFC allows high power density and limited system cost for high-performance systems.

The totem-pole topology in PFC applications with CCM operation is made possible through the use of wide-bandgap semiconductors [2]; in this case, the Infineon CoolSiC™ MOSFET in TOLL package. The converter operates exclusively at high-line (176 V_{RMS} minimum, 230 V_{RMS} nominal) in CCM with 65 kHz switching frequency. It implements the surface-mount device (SMD) TOLL package in both high-frequency branch with CoolSiC™ and low-frequency branch with CoolMOS™ to enble a high power density (80 W/in^3 including fan and connectors and 92 W/in^3 without).

The PFC function to achieve bulk voltage regulation while demanding high-quality current from the grid is implemented with an Infineon XMC1402 microcontroller [3]. Further detail on PFC control implementation in the XMC™ 1000 family can be found in the application notes of other Infineon PSU and PFC evaluation boards with classic or dual-boost topologies [4][5][6].

The 3300 W bridgeless totem-pole PFC in TOLL package presented in this application note is a system solution developed with Infineon power semiconductors as well as Infineon drivers and controllers.

The Infineon devices used in the implementation of the REF_3K3W_TP_SIC_TOLL board are listed below:

- 650 V CoolSiC™ 48 mΩ typical (IMT65R048M1H) with TOLL package, as totem-pole PFC high-frequency switches
- 600 V CoolMOS™ 22 mΩ maximum S7 (IPT60R022S7) with TOLL package, for the totem-pole PFC return path (low-frequency branch)
- 1EDB8275F and 1EDB9275F isolated gate drivers (EiceDRIVER™)
- ICE5QSAG QR flyback controller and 950 V CoolMOS™ P7 (IPU95R3K7P7) for the bias auxiliary supply
- XMC1402 microcontroller for PFC control implementation

A simplified block diagram of the bridgeless topology with the devices mentioned from the Infineon portfolio is shown in Figure 3.

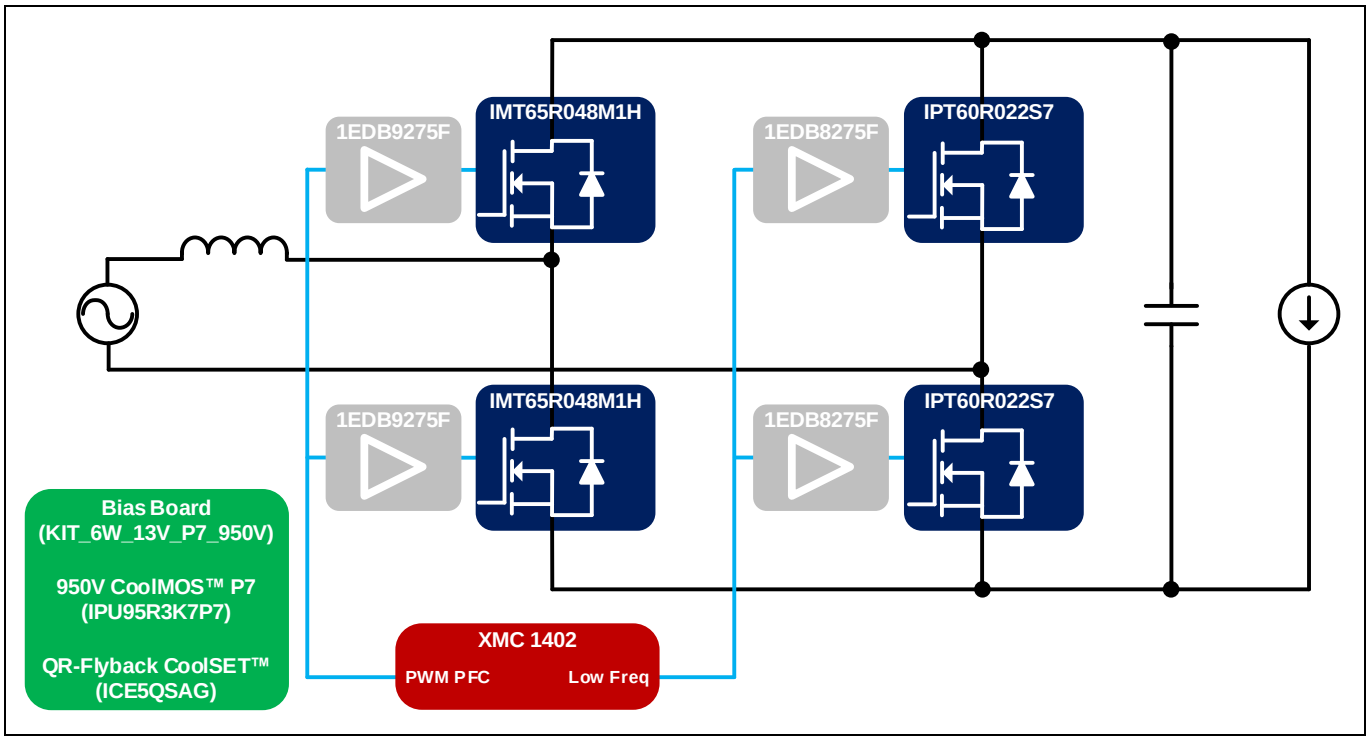

Figure 3 **3300 W bridgeless totem-pole PFC board (REF_3K3W_TP_SIC_TOLL) – simplified diagram showing the topology and the Infineon semiconductors used**

This document will describe the REF_3K3W_TP_SIC_TOLL board implementation, as well as the specifications and main test results. For further information on Infineon semiconductors visit the Infineon website, the Infineon evaluation board search, and the websites for the different implemented components:

- CoolSiC™ MOSFET
- CoolMOS™ power MOSFET
- Gate driver ICs
- QR CoolSET™ (bias board KIT_6W_13V_P7_950V)
- XMC™ microcontrollers

1.1 Board description

The evaluation board REF_3K3W_TP_SiC_TOLL is mounted over a metallic chassis and covered by a plastic enclosure to suit the fan. Figure 4 shows placement of the different sections of the bridgeless totem-pole PFC with Infineon 650 V CoolSiC™ and 600 V CoolMOS™. The board is 240 mm long, with a width of 70 mm and a height of 40 mm (1U), for a power density of 80 W/in^3. The dimensions shown include the fan as well as the input and output.

Immediately after the AC input connector, a two-stage EMI filter is placed as well as a fuse and negative temperature coefficient (NTC) inrush current limiter, together with the input relay. The fan is placed at the side of the AC connector and sucks the air from the evaluation board. The DC output connector is placed on the other side of the board from the AC connector. Close to the output connector, a common-mode choke is placed to guarantee proper acquisition of the output variables in efficiency measurements.

Two daughter cards are introduced: the bias board and the control card. The bias board (KIT_6W_13V_P7_950V) uses a QR CoolSET™ controller and 950 V CoolMOS™ P7 switch to generate the required voltages for the control card, driving, relay and fan supply. The control card implements the required current,

voltage and polarity sensing. The full digital control is implemented in the Infineon XMC™ microcontroller, which is in charge of the proper operation of the bridgeless totem-pole topology.

The rest of the board is occupied by the bridgeless totem pole itself, which comprises the PFC choke, the bulk capacitor and a bridge with 650 V CoolSiC™ and 600 V CoolMOS™ S7. The bulk capacitance is designed to comply with the hold-up time shown in Table 2. The semiconductors in SMD TOLL package are mounted on the bottom side of the board (Figure 5). Two heatsinks, at both sides of the PFC choke, help to remove the heat dissipation of the SMD semiconductors mounted in the bottom side. The choke is designed with high-flux GT material in order to comply with the height requirement, high-efficiency performance, and high power density.

Figure 4 **Placement of the different sections in the 3300 W bridgeless totem-pole PFC with Infineon CoolSiC™ 650 V MOSFET and XMC™ control**

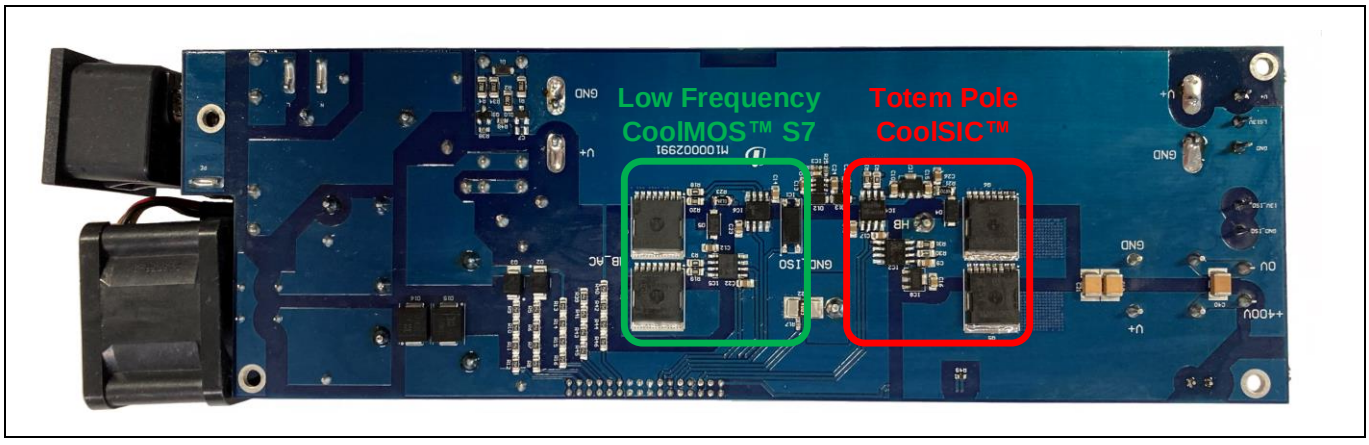

Figure 5 **SMD power semiconductors mounted on the PCB bottom side**

1.2 Signal conditioning for digital control of totem-pole CCM PFC

The evaluation board REF_3K3W_TP_SIC_TOLL implements CCM average current mode control with duty feed-forward (DFF). It follows a control structure similar to that implemented for a classic PFC presented in [4] and [5] or the dual boost introduced in [6].

Unlike the classic PFC in which the AC voltage is rectified by the diode bridge, in the bridgeless totem-pole PFC converter the inductor current is both positive and negative. The most simple and cost-effective way to sense this current is to use a shunt resistor in series with the inductor as shown in Figure 6. In addition, in the REF_3K3W_TP_SIC_TOLL board, the control reference (GND_iso in Figure 6) is placed in the AC-line after the

shunt resistor. Therefore, the current sense voltage (CS+) is positive and negative according to the positive reference current shown by the red arrow in Figure 6.

Since the ADC of the microcontroller used for the control implementation (XMC1402 from Infineon Technologies [3]) only allows input voltages between zero and the supply voltage (Vcc_XMC in Figure 6), an offset is included together with the current sense gain in order to properly use the input span of the ADC. In this case the offset is 2.5 V, which corresponds to half the supply voltage for the used XMC™ controller. The differential gain (Ki) is adjusted to consider not only inductor average current but also the high-frequency ripple, since this signal is used for CCM average current control and peak current limitation.

In the totem-pole operation, the return path transistors (HS_SR and LS_SR on Figure 6) are switched at the AC zero crossing according to the AC polarity: HS_SR for positive AC and LS_SR for negative AC cycle. The polarity of the input voltage is set according to the control reference GND_iso. Since the control reference is in one of the AC input rails, the polarity detection is significantly simplified and the internal ESD diode protection of the XMC™ controller is used to transform the input capacitor voltage into a digital signal.

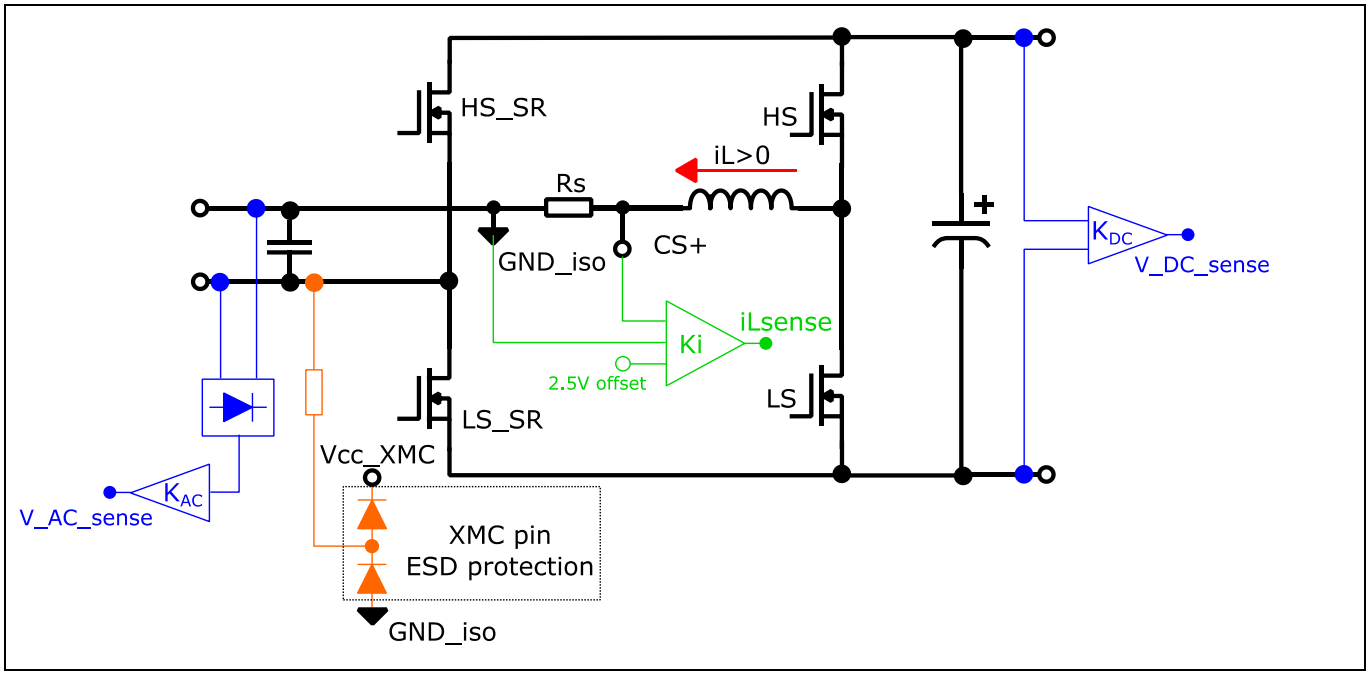

Figure 6 Block diagram of the sensing circuitry required for totem-pole control with XMC™ and control reference in the AC rail in series with the PFC choke

Due to the control reference location, the bulk voltage sense requires a differential amplifier with gain K DC as shown in Figure 6. In the case of the of AC voltage sense, the control reference location allows a simple sense. In this case, the voltage has been rectified (positive ADC input is required) and adapted to the ADC input range with a differential gain K AC.

Since the AC voltage is used for the current reference generation in the selected average current mode structure (Figure 7), the current reference is a full wave rectified sinusoidal sequence. However, the current sense after the ADC is a sinusoidal sequence with offset at half of the ADC span. Therefore, the ADC result from the current sense first requires the offset to be removed and then rectified according to the AC polarity. These two steps, together with extra gain, are implemented by software in the XMC™ controller.

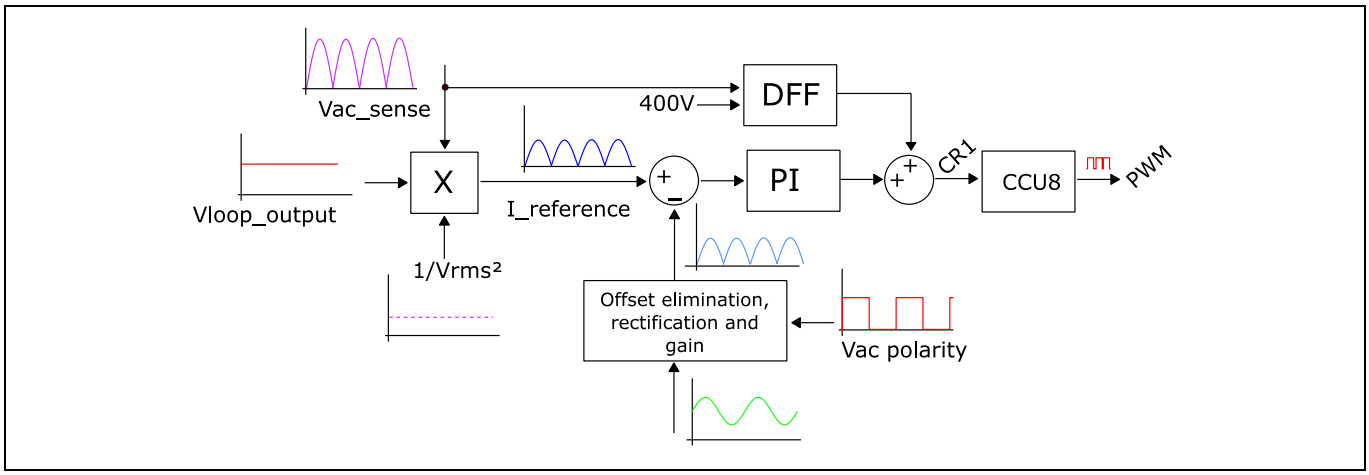

Figure 7 Current loop structure with DFF and the required current manipulation

2 Bridgeless PFC specifications and test results

This chapter presents the specifications, performance and behavior of the 3300 W bridgeless totem pole with average current mode control in CCM for PFC operation. The results were obtained with 48 mΩ 650 V CoolSiC™ devices in TOLL package and 22 mΩ 600 V CoolMOS™ S7 in TOLL package as low-frequency switches. Table 2 shows the demonstrator performance and specifications under several steady-state and dynamic conditions. The converter operates at 65 kHz switching frequency and only for high-line AC input (176 V min. RMS voltage).

Table 2 Summary of specifications and test conditions for the 3300 W totem pole in CCM

Test		Conditions	Specification	
Efficiency test		230 V_{RMS}, 50 Hz/60 Hz	η_{pk} ≈ 98.9% at 1650 W (50% load)	
Current THD		230 V_{RMS}, 50 Hz/60 Hz	THDi less than 10% from 10% load	
Power factor			PF more than 0.95 from 20% load	
Rated DC voltage		230 V_{RMS}, 50 Hz/60 Hz	400 V	
Steady-state V_{OUT} ripple		230 V_{RMS}, 50 Hz/60 Hz, 100% load	$\lvert\Delta V_{Out}\rvert$ less than 20 $V_{pk\text{-}pk}$	
Inrush current		230 V_{RMS}, 50 Hz/60 Hz, measured on the first AC cycle	I_{in_peak} less than 30 A	
Power line disturbance	AC lost (hold-up time)	230 V_{RMS}, 50 Hz/60 Hz, 10 ms at 100% load, 20 ms at 50% load	V_{OUT_min} = 300 V (UVP)	No damage: *PFC soft-start if bulk voltage under 300 V *PFC soft-start if AC out of range for cetain time
	Voltage sag	200 V_{RMS}, 50 Hz/60 Hz, different sag conditions, 100% load		
Brown-out	AC voltage		174 V_{RMS} on; 168 V_{RMS} off	
Load transient		7.4 A (90%) ↔ 0.8 (10%), 0.2 A/µs	V_{OUT_min} = 300 V (UVP) V_{OUT_max} = 450 V (OVP)	
Overcurrent protection (OCP)			Peak current limit 40 A	
			AVG current limit 28 A	

2.1 Steady-state performance and waveforms

Figure 8 shows the efficiency measurements for PFC operation at different AC voltages. The efficiency measurements have been obtained with a WT3000 power analyzer (no line filter applied in the efficiency measurement) and include the bias consumption as well as the fan.

Note: Due to production variations and measurement set-up, efficiency variations of up to ±0.2 percent can be seen in the results.

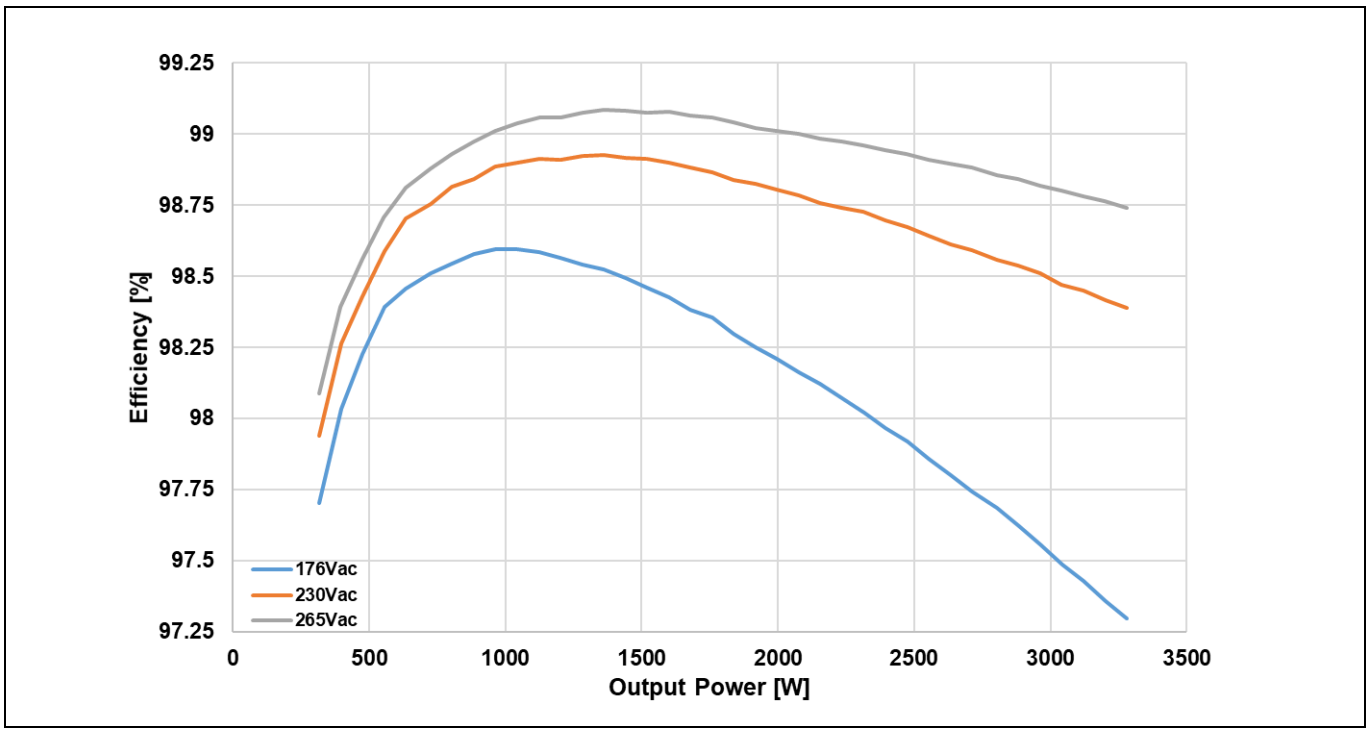

Figure 8 Measured efficiency (without any line filter applied in the power analyzer) at different RMS input voltage and 50 Hz. The measurements include bias and fan consumption.

Figure 9 depicts the total harmonic distortion (THD) and power factor measured at different AC voltages at 50 Hz. Only 50 Hz results are shown because the high-line AC voltage typically operates at such a frequency. However, the REF_3K3W_TP_SIC_TOLL board is prepared to operate at 60 Hz, and similar results can be expected.

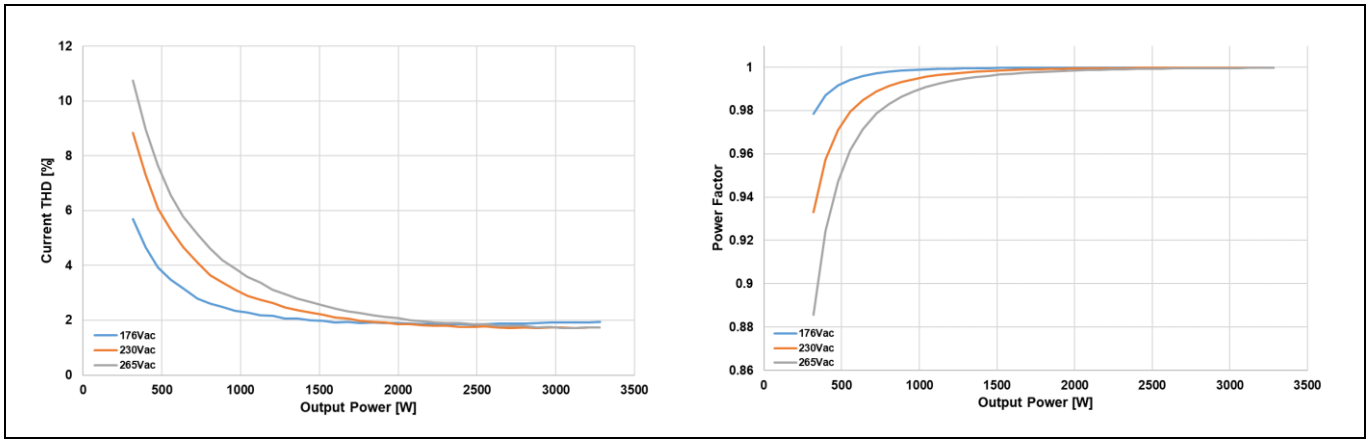

Figure 9 Measured THDi (left) and power factor (right) at different RMS voltages for 50 Hz high-line AC voltage

Figure 10 and Figure 11 show the PFC steady-state operation for different AC voltages in amplitude as well as power levels.

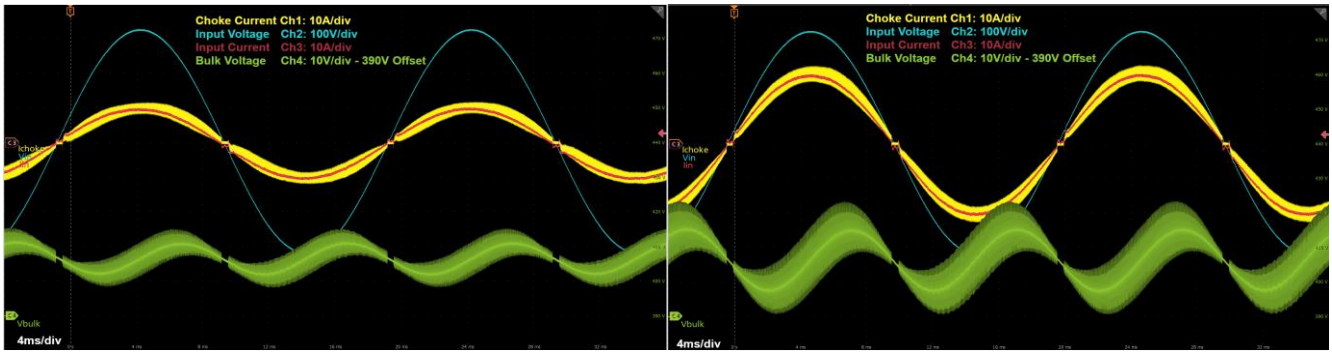

Figure 10 Steady-state waveforms at 230 V, 50 Hz AC voltage, 50 percent load (left) and 100 percent load (right)

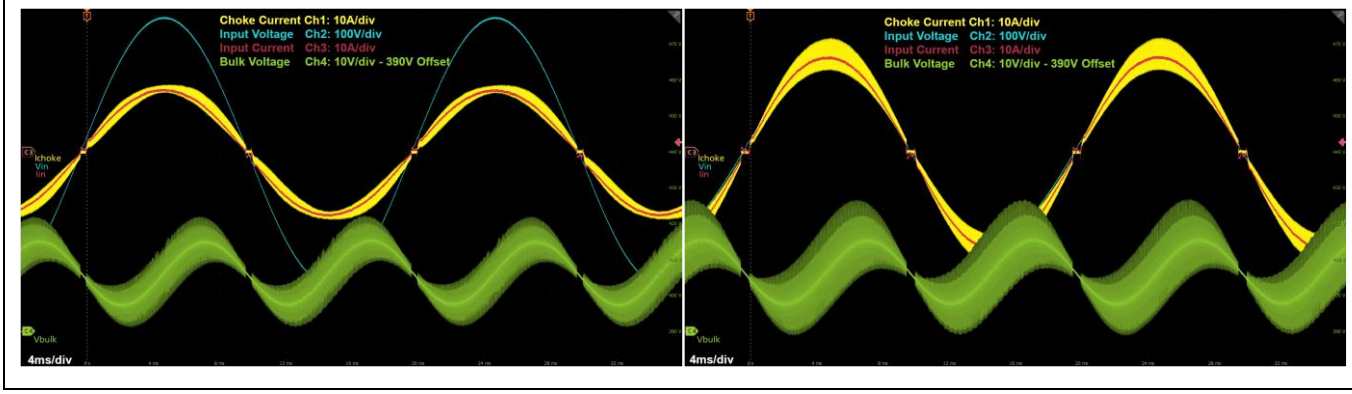

Figure 11 Steady-state waveforms at 265 V (left) and 176 V (right) for 50 Hz AC voltage and 100 percent load

2.2 Power line disturbance

Two main line disturbance conditions can occur when connected to the grid. On one side the AC can be lost during a certain time – line cycle dropout (LCDO) – and, on the other side, the AC voltage can suddenly decrease to an abnormal value – voltage sag. This section introduces the test conditions for both disturbances as well as the REF_3K3W_TP_SIC_TOLL bridgeless PFC board performance when those conditions are applied. For these tests of the PFC operation a programmable AC source and a high-voltage electronic load have been used.

2.2.1 Line cycle dropout (LCDO)

The 3300 W totem pole CCM PFC operates exclusively in high-line. Therefore, the AC LCDO capability is tested from 230 V to 0 V. Different timing, related to the specified hold-up time and the line frequency, is applied as shown in Table 3. The output voltage is within the specified dynamic variation regardless of the start angle of the voltage dropout. Figure 12 shows an example of LCDO operation at full load starting at an AC angle of 45 degrees, which corresponds to the point of lowest DC voltage in steady-state conditions. In case the dropout is longer than specified, output undervoltage (300 V) can be triggered and a turn-off and restart of the unit will occur.

Note: The electronic load used during the test is configured in such a way that it demands current only when the voltage applied to the load is over 300 V, which is the undervoltage setting of the bridgeless PFC and emulates the typical behavior of a back-end DC-DC converter.

Table 3 Applied voltage cycles for LCDO test at different loads with 50 Hz AC input voltage

		1st to 10th time	
Applied voltage	230 V AC	0 V AC	230 V AC
Timing at different load conditions	50 % load	20 ms	100 ms
	100 % load	10 ms	100 ms

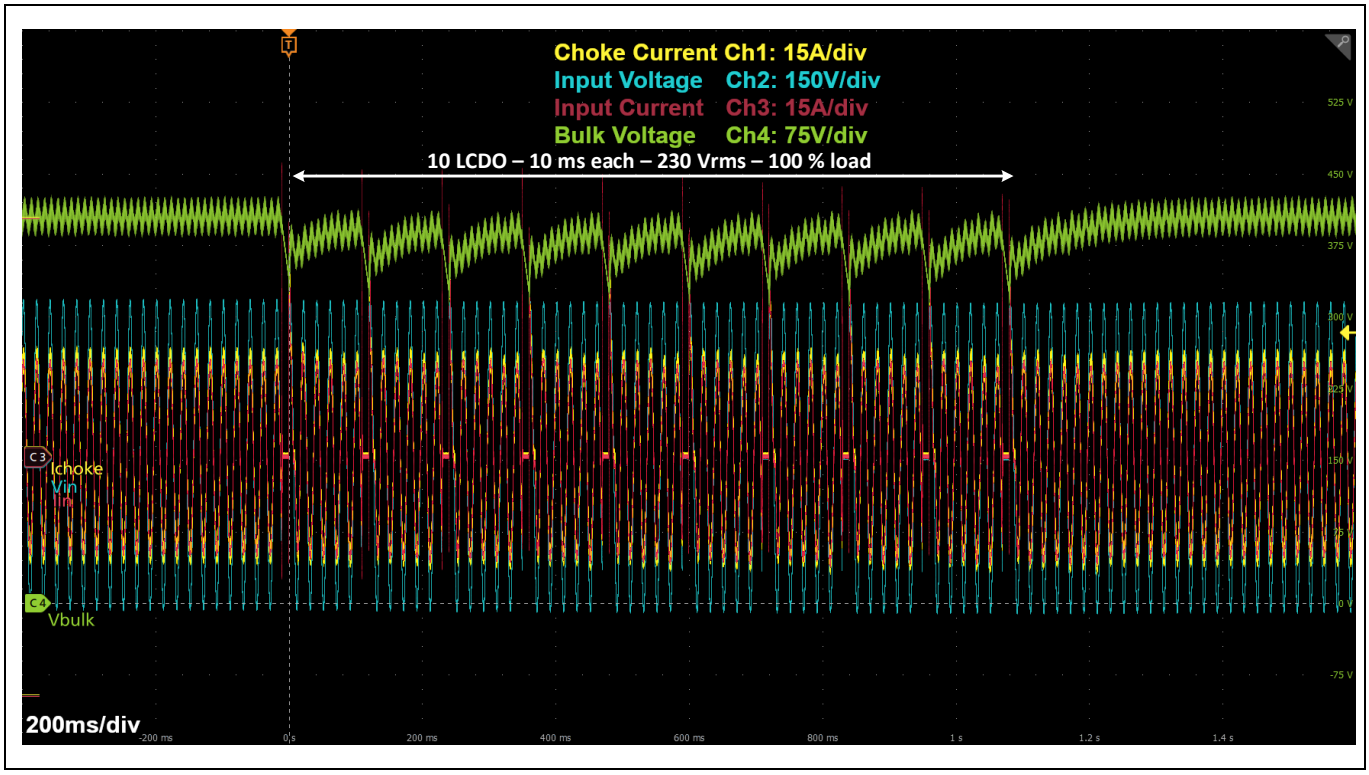

Figure 12 10 ms LCDO test at 230 V AC, 50 Hz, and 100 percent load with a starting angle of 45 degrees

More detailed waveforms of a full-load 10 ms LCDO are presented in Figure 13. It shows the peak current limitation when the AC returns, set to 40 A, as well as the initial and final bulk voltages during the hold-up time. This high current is demanded by the voltage loop in order to quickly increase the bulk voltage to its target value. Figure 14 and Figure 15 show the test results of the 20 ms LCDO at 50 percent load with a starting angle of 0 degrees.

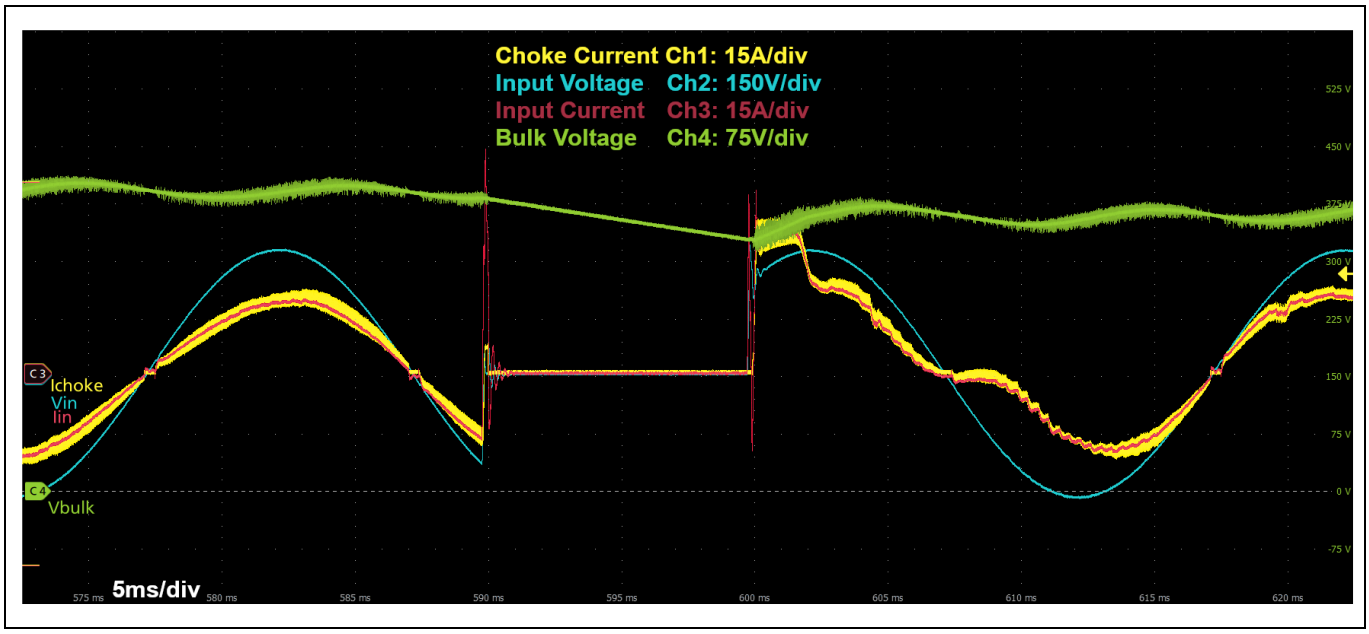

Figure 13 Detail of a 10 ms LCDO test at 230 V AC, 50 Hz and full load with a starting angle of 45 degrees

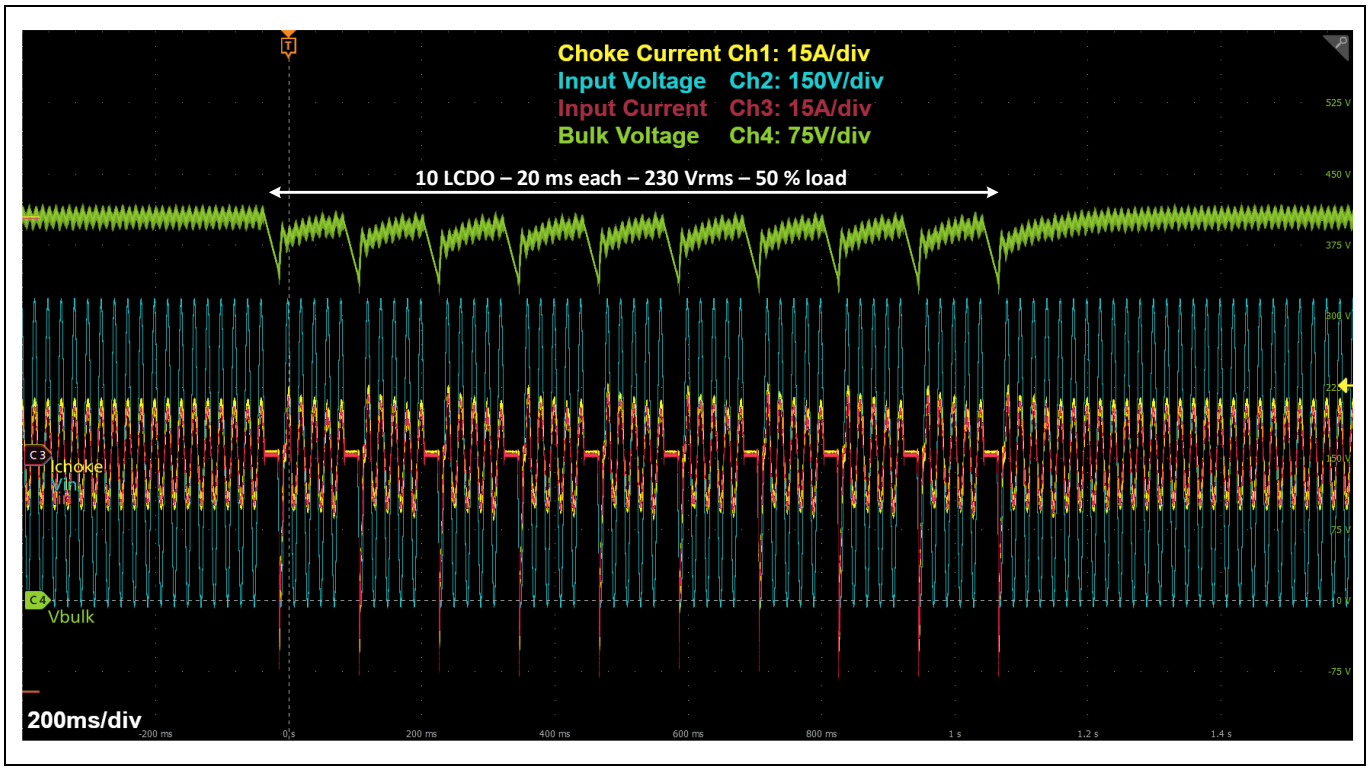

Figure 14 20 ms LCDO test at 230 V AC, 50 Hz, and 50 percent load with a starting angle of 0 degrees

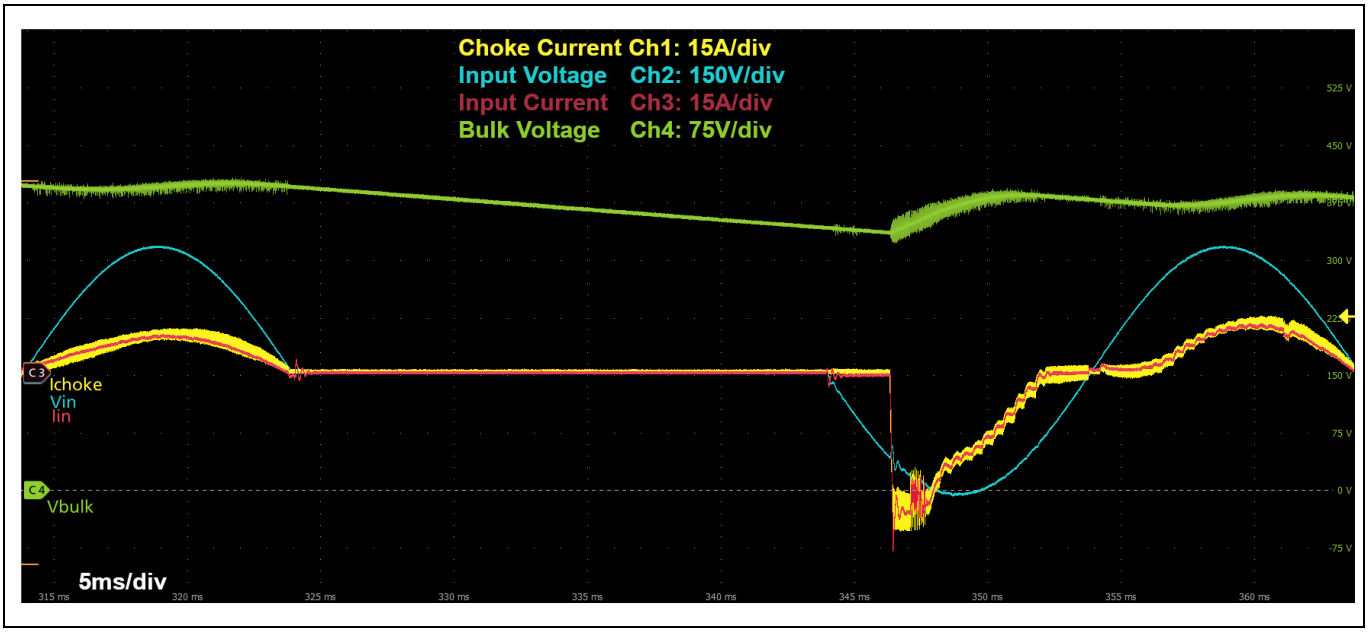

Figure 15 **Detail of a 20 ms LCDO test at 230 V AC, 50 Hz and 50 percent load with a starting angle of 0 degrees**

2.2.2 Voltage sag

For high-line operation, two different voltage sag conditions are considered and tested.

Table 4 **Voltage sag conditions for high-line applied to the REF_3K3W_TP_SIC_TOLL board**

		1st to 10th time	
	Steady AC input	Voltage sag (time)	Period
AC input	200 V AC	130 V AC (0.5 s)	5 s
	200 V AC	150 V AC (2 s)	20 s

Figure 16 shows the totem-pole PFC behavior with 130 V_{RMS} voltage sag during 500 ms. As can be seen by the bulk voltage waveform, the output voltage cannot be regulated to 400 V in this condition since the inductor average current is limited to 28 A. Not only is average current limitation applied in the REF_3K3W_TP_SIC_TOLL board, but also the peak current is limited to 40 A (Figure 17).

Note: *The electronic load used during the test is configured in such a way that it demands current only when the voltage applied is over 300 V, which is the undervoltage setting of the bridgeless PFC.*

However, if the voltage is under the nominal range for longer than specified in the table, the PFC turns off and restarts with soft-start after an idle time. Figure 18 shows this behavior when a voltage sag to 130 V_{RMS} is applied for longer than 500 ms (750 ms) at full load.

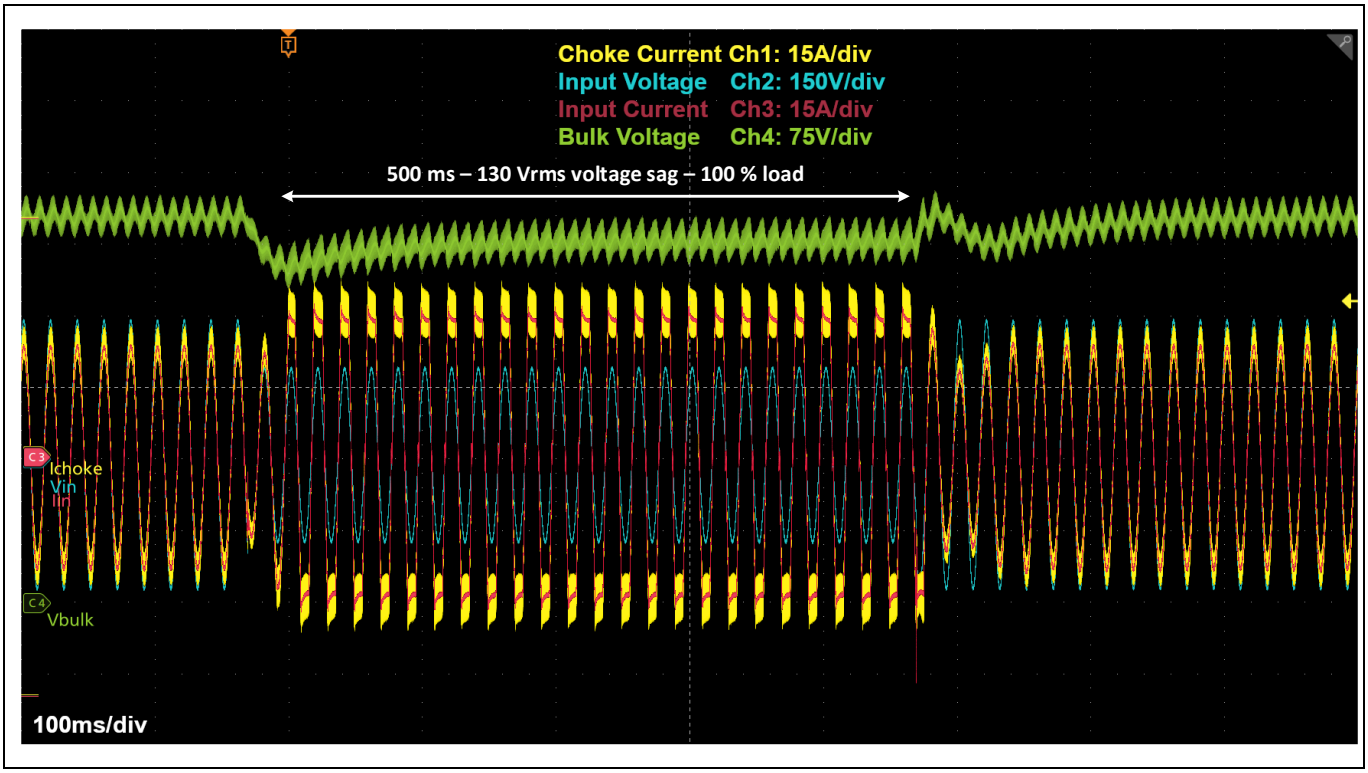

Figure 16 Main waveforms during a 500 ms and 130 V_{RMS} voltage sag at full load and 200 V_{RMS}

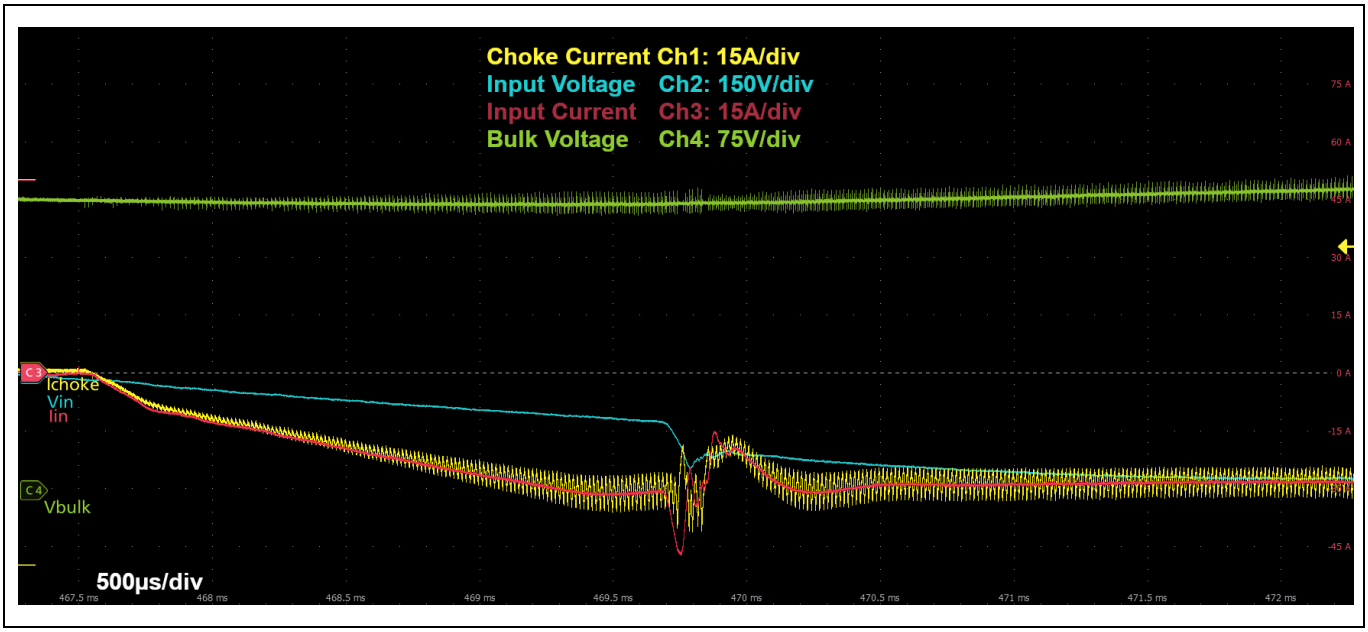

Figure 17 Detail of peak current limitation when returning to nominal voltage after 130 V_{RMS} voltage sag at full load

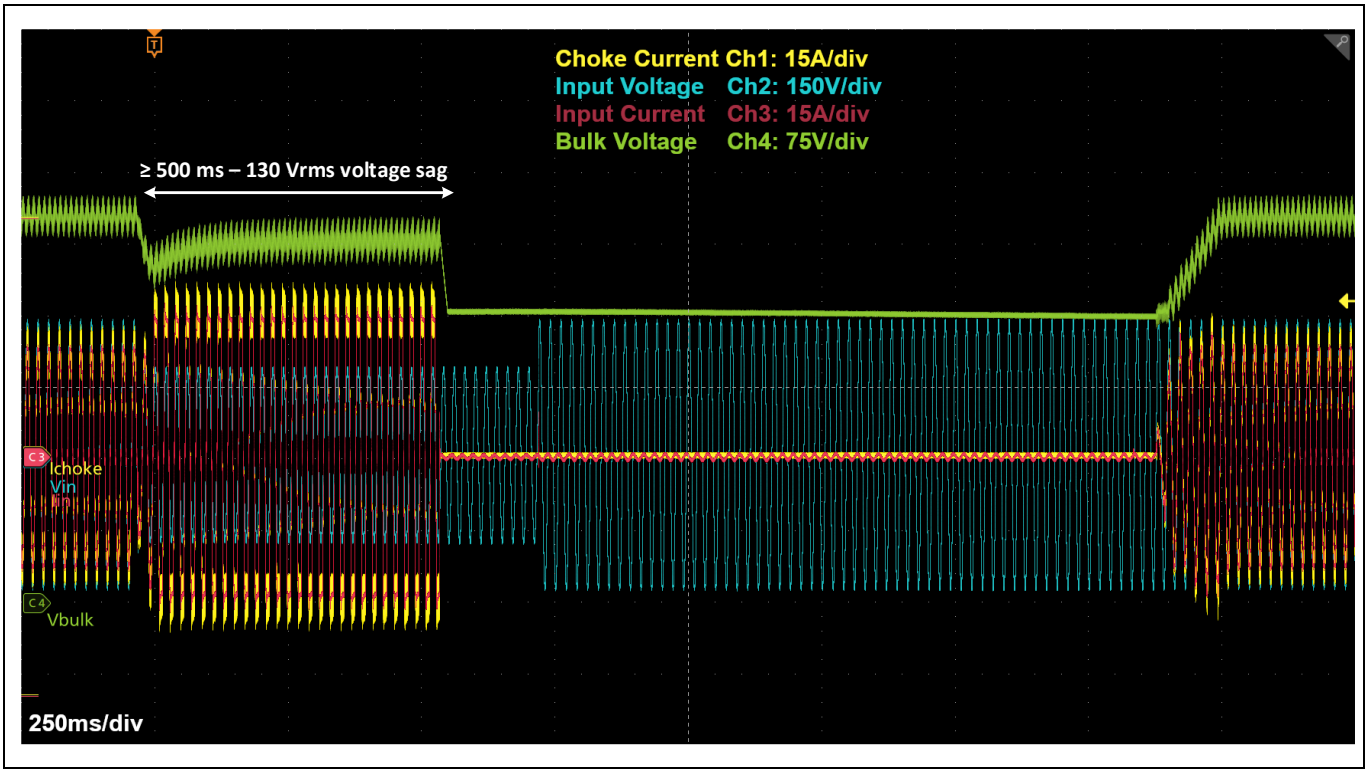

Figure 18 PFC resumes operation after 130 V_{RMS} voltage sag applied for 750 ms at full load

In Figure 19 the waveforms when a 150 V_{RMS} voltage sag is applied for 2 s at full load are shown. The detail of the average choke current (i.e., input current) is limited to 28 A (Figure 20). In this case the demanded current is lower and therefore the average current limitation occurs for a shorter time, and thus the bulk voltage decreases less than in the 130 V_{RMS} case.

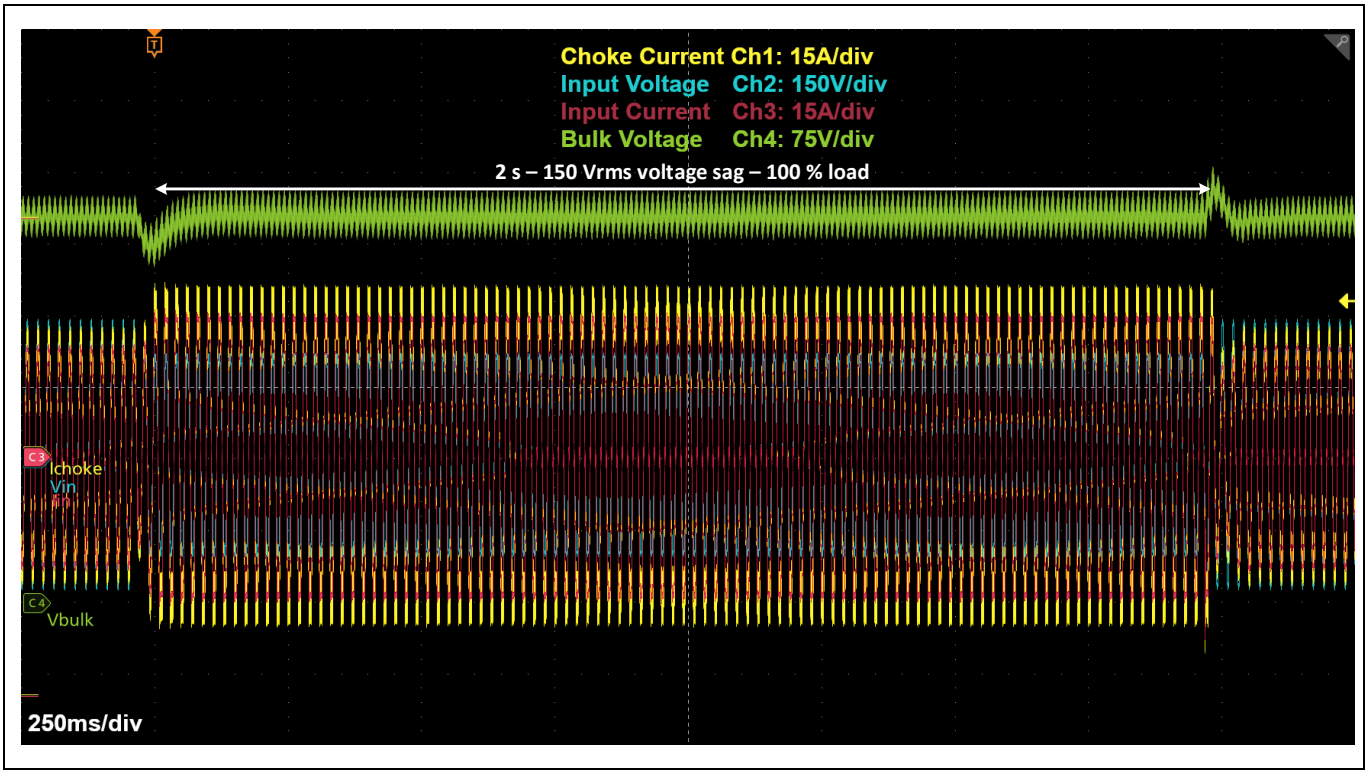

Figure 19 Main waveforms during a 2 s and 150 V_{RMS} voltage sag at full load and 200 V_{RMS}

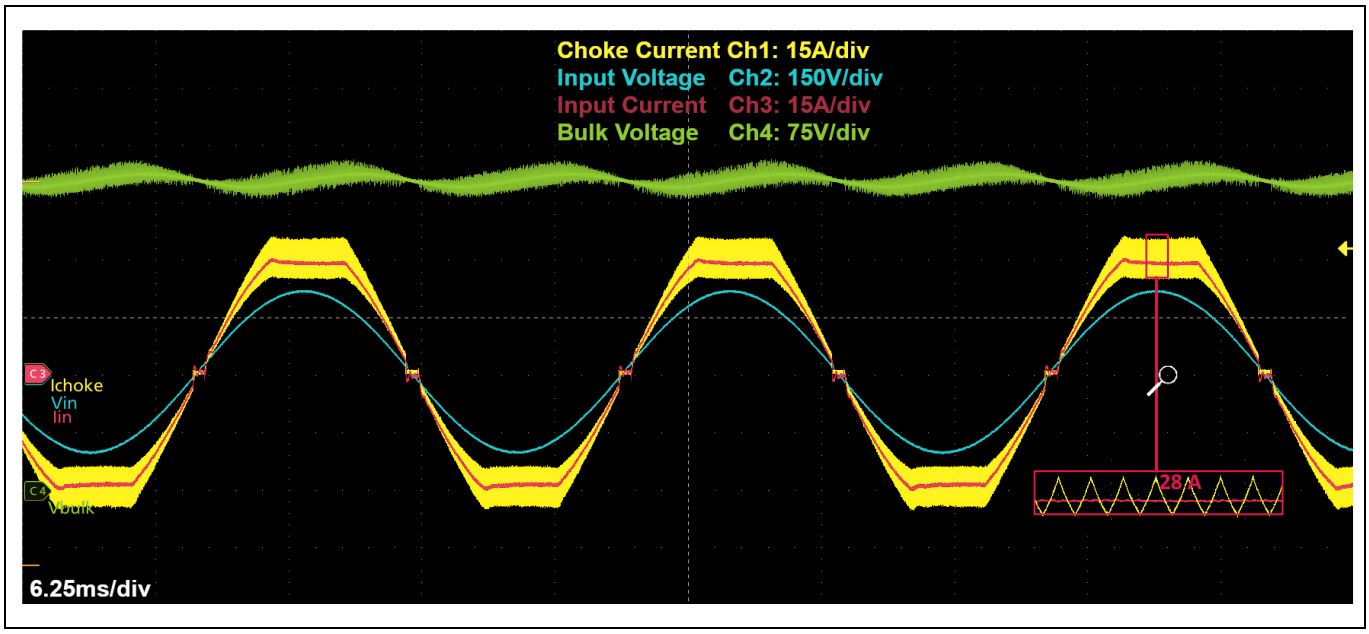

Figure 20 Detail of the voltage sag operation at 150 V_{RMS} for 2 s

2.3 Output voltage dynamic behavior

In addition to power line disturbance, two other dynamic perturbances can affect the performance of the power supply shown: load and input voltage variation.

2.3.1 Load-transient response in PFC mode

As specified in Table 2, 10 percent load (0.8 A) to 90 percent load (7.4 A) steps and vice-versa with 0.2 A/µs slope are considered in PFC mode. Figure 21 and Figure 22 show the REF_3K3W_TP_SIC_TOLL board behavior under these load steps. The implemented voltage loop has a 35 Hz crossover frequency. In this firmware version of totem-pole control, neither extra gain nor non-linear current variation have been implemented. The output voltage dynamic range is for the specified load variation, 350 V and 450 V. When the 90 percent to 10 percent load step is applied, the overshoot is below 450 V. The converter manages to reduce the voltage without pulse-width modulation (PWM) interruption.

2.3.2 AC voltage variation

Input voltage variations, as seen in the power line disturbance section, can modify the bulk voltage. This can also occur when the input voltage varies even within the normal operation range, as shown in Figure 23. In this condition, the bulk voltage is in the range 330 V to 440 V when an AC voltage variation from 265 V_{RMS} to 176 V_{RMS} and vice-versa at full load happens, as shown by the test result.

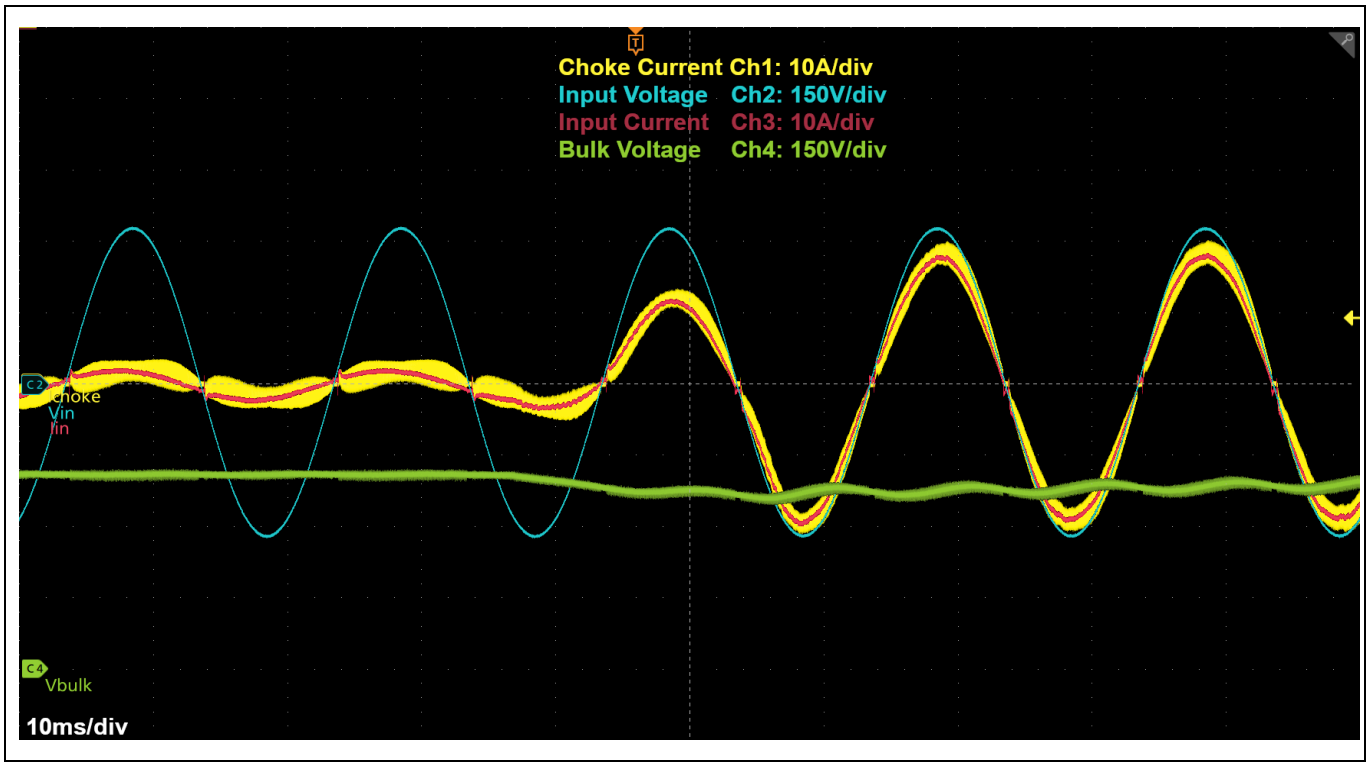

Figure 21 Load-transient response 10 percent to 90 percent load step with 0.2 A/µs current slope

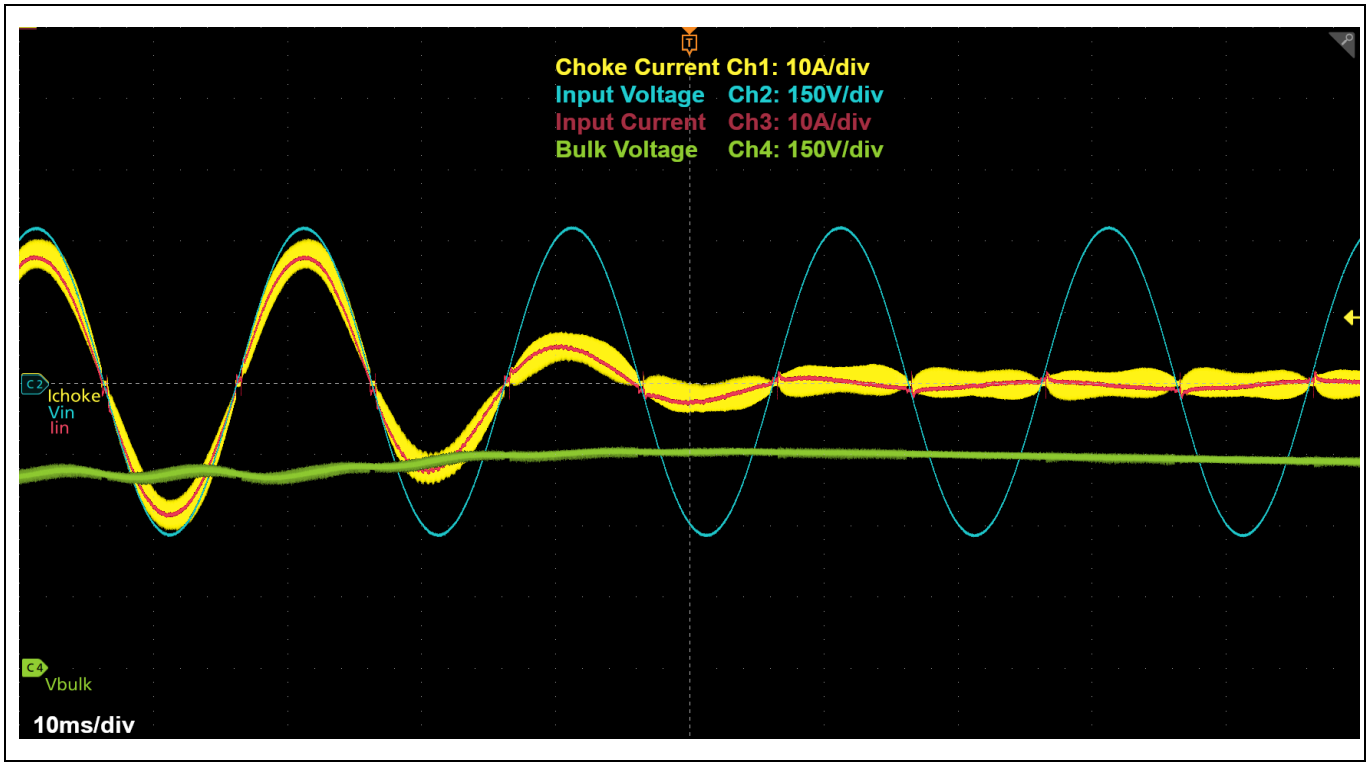

Figure 22 Load-transient response 90 percent to 10 percent load step with 0.2 A/µs current slope

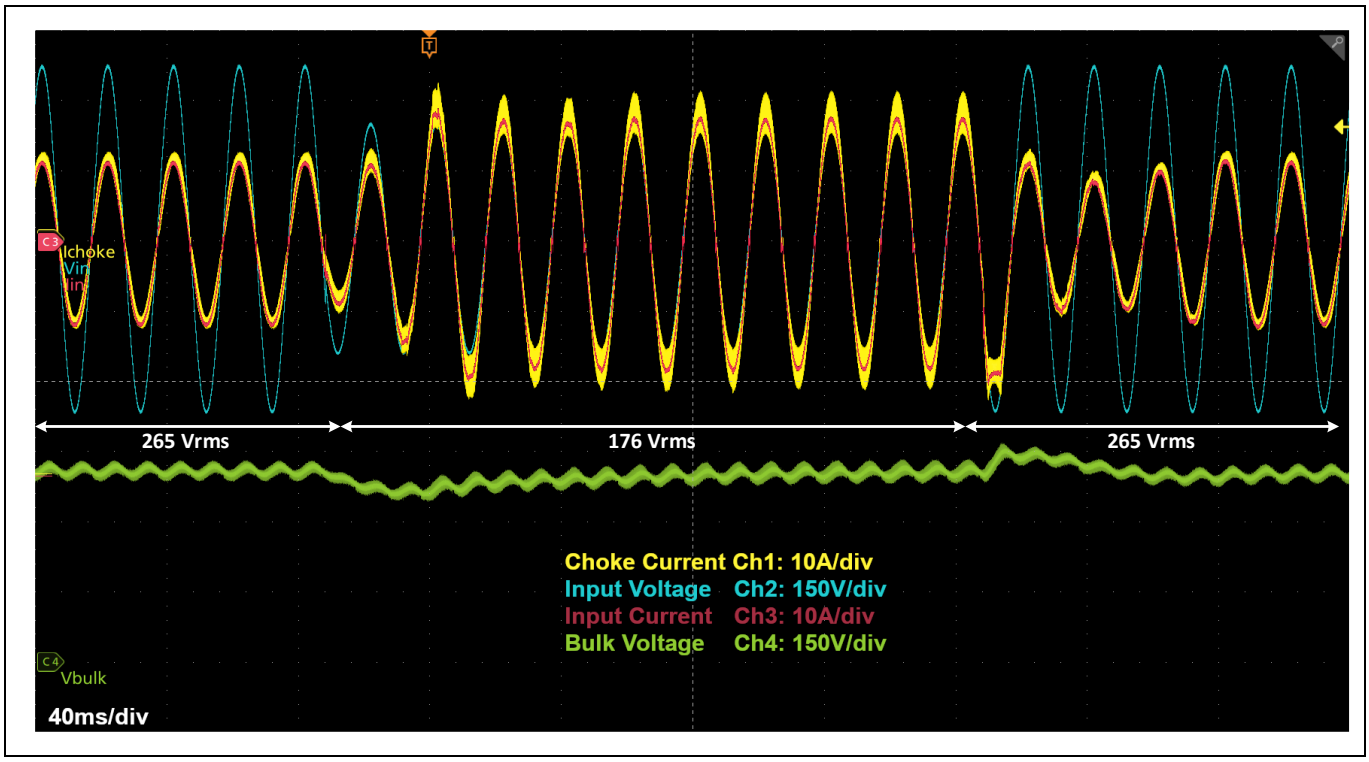

Figure 23 Maximum (265 V_{RMS}) to minimum (176 V_{RMS}) high-line voltage variation at full-load operation

2.4 Inrush current and PFC start-up

Figure 24 shows the start-up of the bridgeless totem pole in PFC mode for full-load operation. The test has been performed with programmable AC source and high-voltage electronic load. The load is configured with a 350 V threshold to start sinking current. This threshold emulates the behavior of the DC-DC converter, which would be the load for the PFC (Figure 25). The inrush current when connecting to the AC source is limited with an NTC. This resistor is short-circuited by a parallel relay before start-up if the input and output voltage conditions to start the bridgeless PFC are met. The in-rush current is measured at the first AC cycle and it is independent of the output load. Figure 26 shows the inrush current at full-load start-up. According to the measurement the inrush current is significantly under the specified 30 A in Table 2.

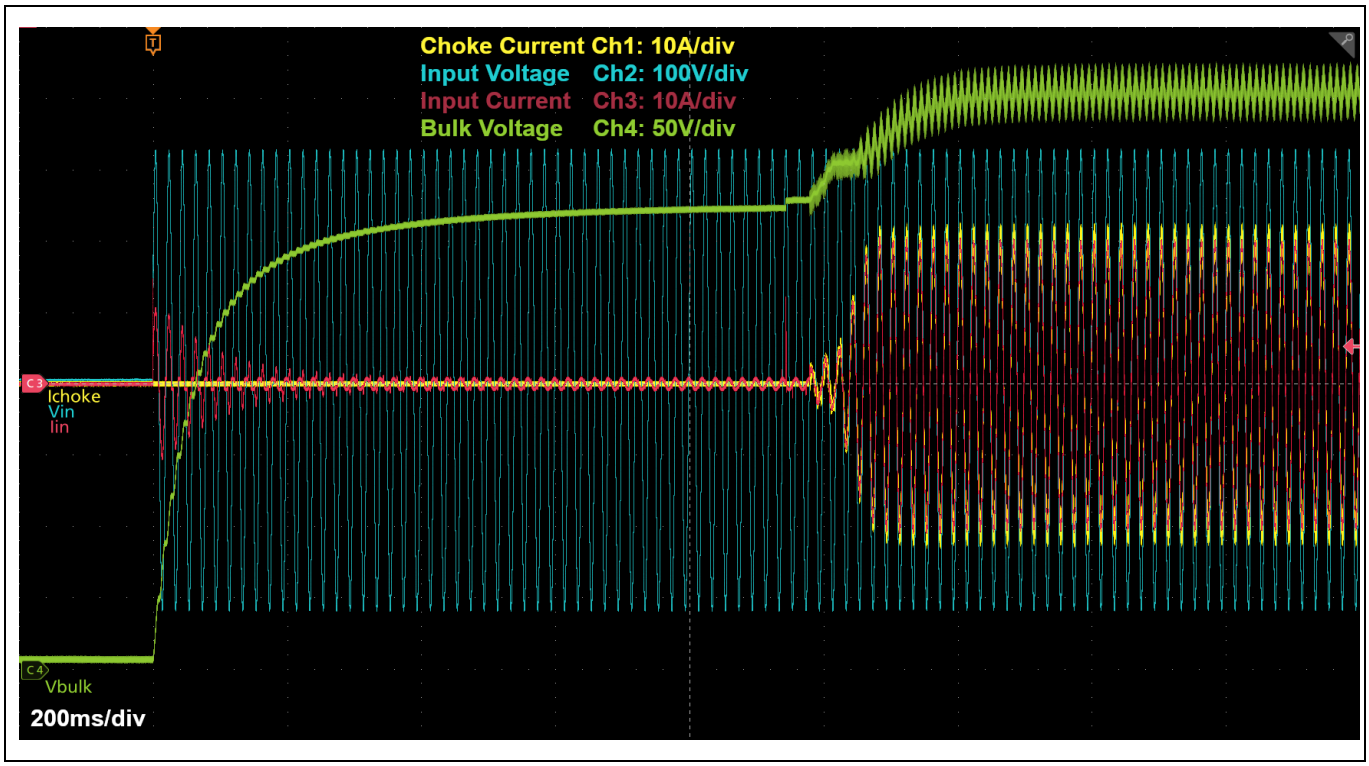

Figure 24 **REF_3K3W_TP_SIC_TOLL start-up at full load for 230 V, 50 Hz input voltage**

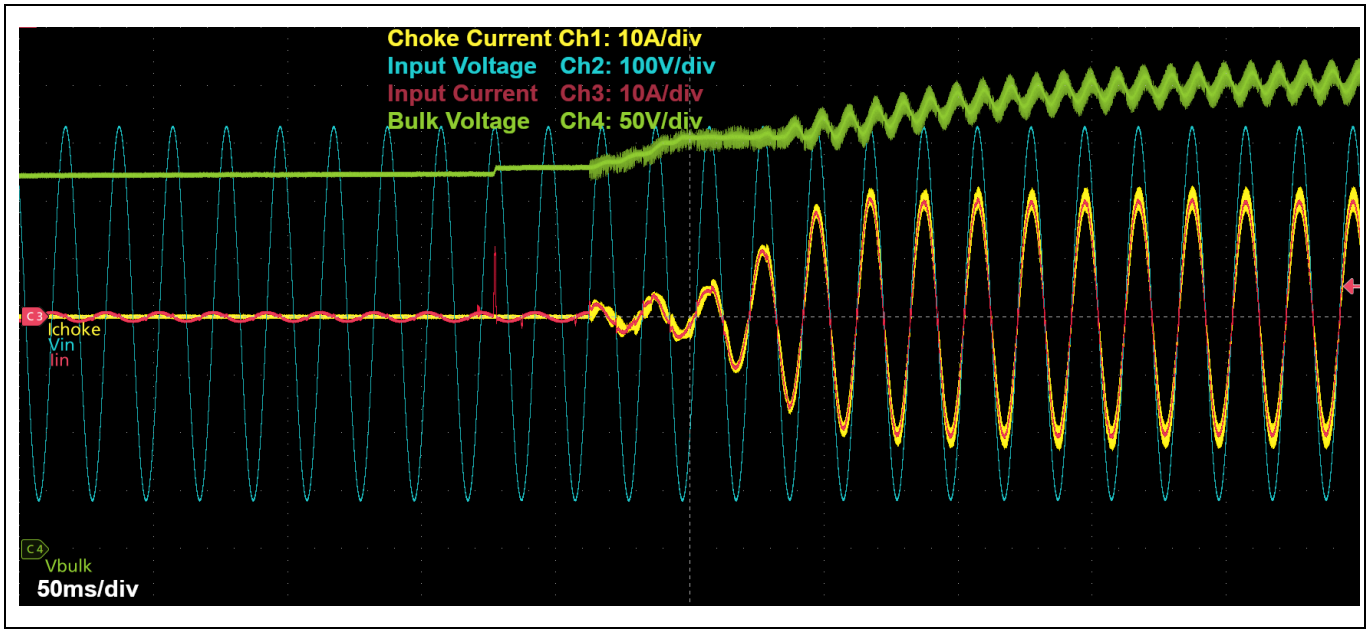

Figure 25 **Detail of the bulk voltage soft-start from AC peak voltage to steady-state voltage after relay is closed (230 V, 50 Hz at full load)**

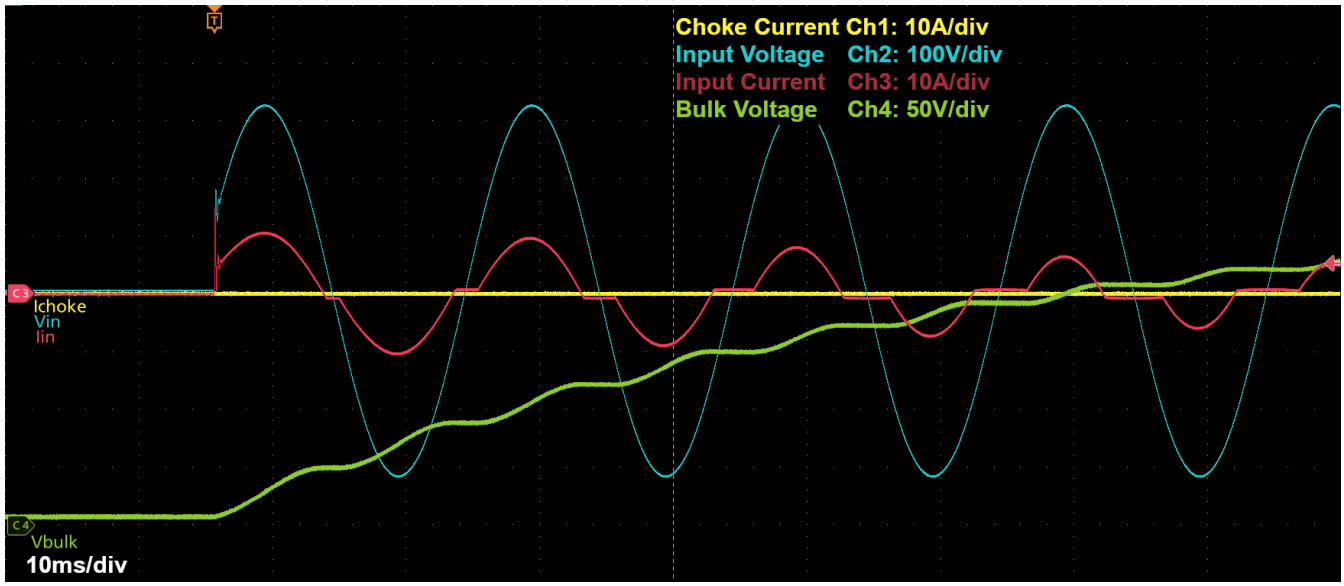

Figure 26 Inrush current of REF_3K3W_TP_SIC_TOLL at full-load start-up

3 CoolSiC™ gate driving scheme

This chapter shows the gate driver circuit used in the REF_3K3W_TP_SIC_TOLL for the high-frequency branch with 650 V CoolSIC™.

3.1 Bootstrap

Bootstrap circuits are often used in half-bridge configuration in order to supply the high-side gate driver. The main reason for the use of this method is that it is simple and cheap to implement. In fact, implementing the bootstrap can generate the high-side gate driver voltage supply by adding only few components (one high-voltage diode and one resistor) from the low-side gate driver supply. An example of a bootstrap circuit to supply CoolSiC™ with an Infineon Technologies isolated gate driver is shown in Figure 27. Only the low-side supply (LS18) is from an auxiliary circuit, while the high-side voltage supply (HS18) comes from the bootstrap circuit.

Note: In the low-side position it is possible to also use a non-isolated gate driver.

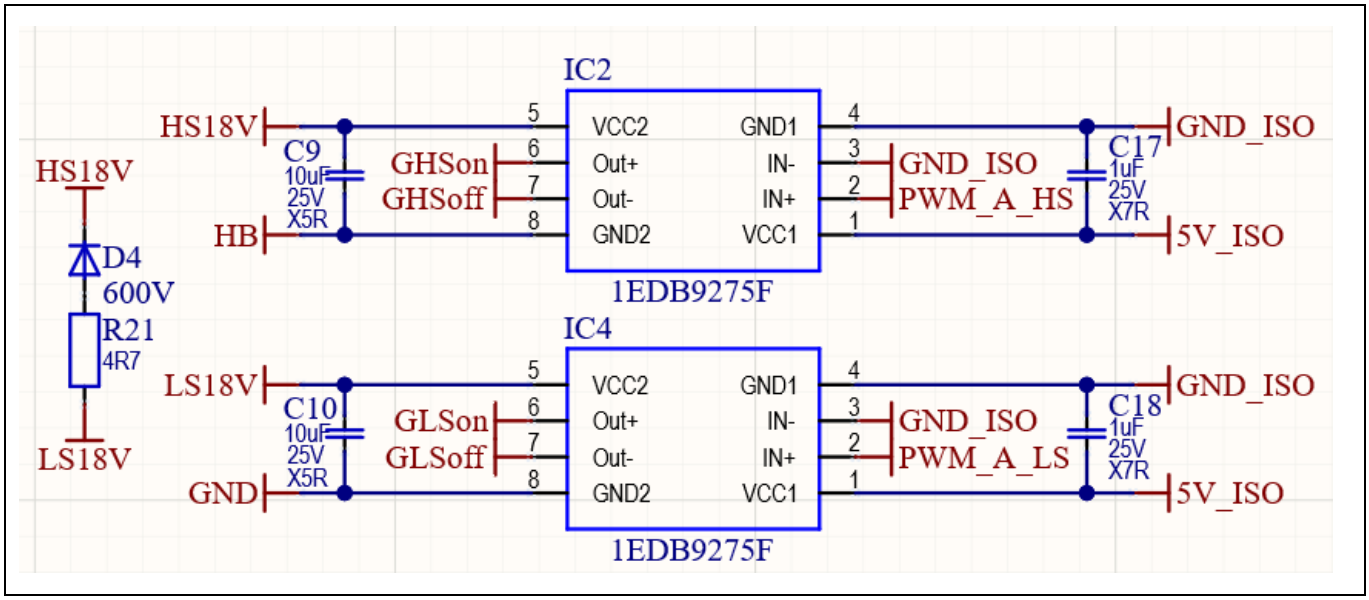

Figure 27 Example of a classic bootstrap circuit schematic for 650 V CoolSiC™ with EiceDRIVER™ 1EDB9275F

SiC MOSFETs are sensitive to the gate voltage supply, so reducing the recommended voltage will lead to a channel resistance increase. Using a bootstrap circuit in PFC CCM totem-pole topology could generate (under some conditions) a modulation of the high-side gate voltage. This modulation, show in Figure 28, comes from the body diode conduction of the SiC MOSFETs. Clearly, while the high-side MOSFET device acts as a “diode”, the gate voltage decreases following the shape of the input AC. When the input peaks, the high-side gate has the minimum voltage and has the biggest duty cycle. This leads to an increase in conduction losses in the high-side device when acting as diode and conducting with the channel. Conversely, when the high-side works as an active switch the gate voltage increases. The voltage increase can reach the maximum allowed derating gate voltage. To overcome this problem of the classic bootstrap circuit, the circuit proposed in Figure 29 is implemented in the REF_3K3W_TP_SIC_TOLL. The difference between this and the classic bootstrap is the low-dropout regulator (LDO) in the high-side gate driver supply.

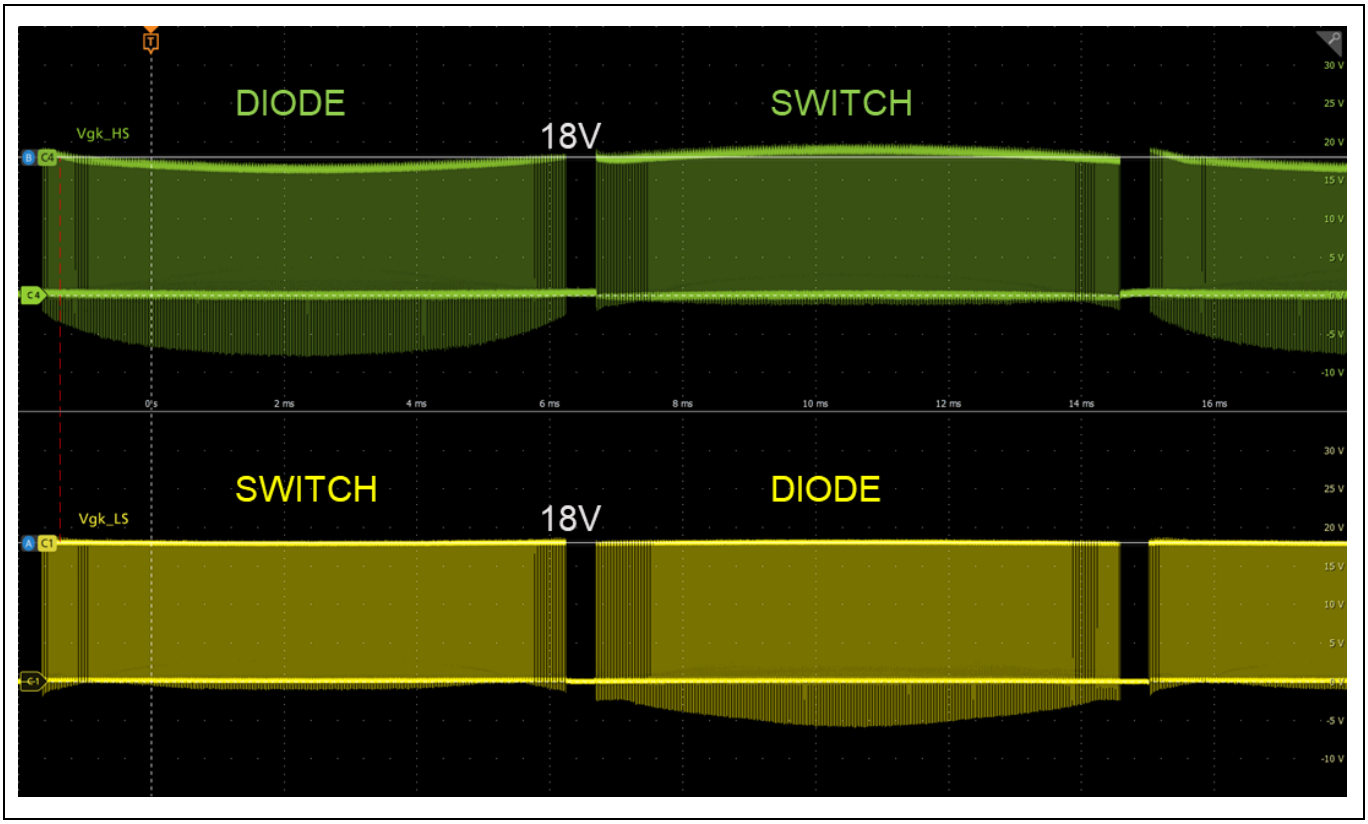

Figure 28 **Waveforms of the gate voltages in the high-frequency branch (low-side in yellow, high-side in green), with 176 V_{RMS} and full load when classic bootstrap is used**

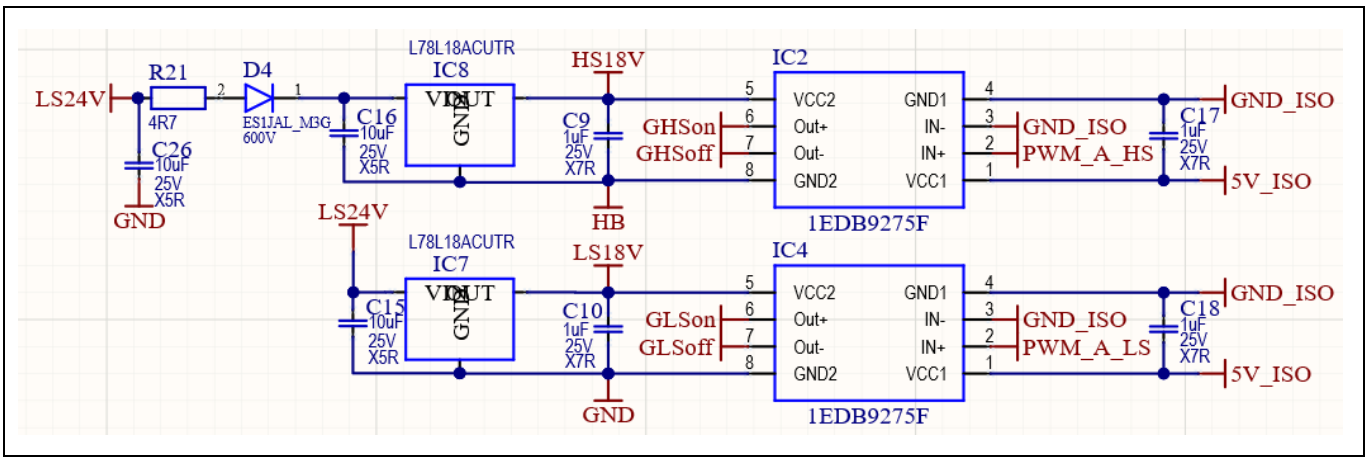

Figure 29 **Bootstrap plus HS LDO circuit schematic used in the REF_3K3W_TP_SIC_TOLL**

As shown in Figure 30, the bootstrap circuit plus LDO solves the problem of the high-side gate driver supply modulation, fixing the gate-source voltage to 18 V across the whole range.

In both Figure 28 and Figure 30 the gate voltage of the low-side device is sensed with the TPP1000 (1 GHz bandwidth) voltage probe and for the high-side with the TIVP1 plus TIVPMX10X (1 GHz bandwidth) isolated voltage probe (both from Tektronix).

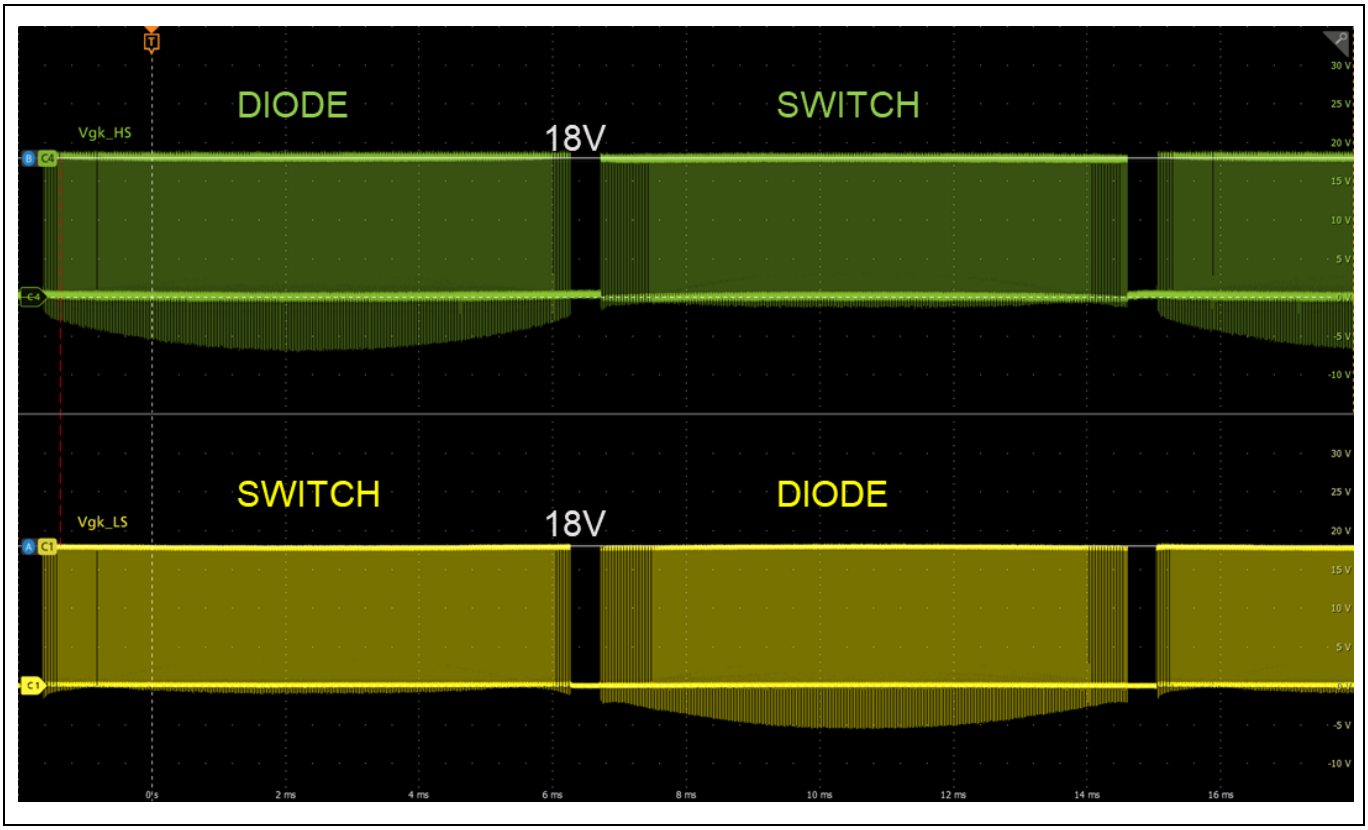

Figure 30 **Waveforms of the gate voltages in the high-frequency branch (low-side in yellow, high-side in green), with 176 V_{RMS} and full load when bootstrap plus LDO in the HS is used**

3.2 Three-pin configuration with CoolSiC™ in TOLL package

With leaded packages like TO-247 using the Kelvin source is mandatory, especially with newest technologies such as SiC MOSFETs, to decrease the switching losses and increase the overall efficency of the converter. TOLL is a leadless package with very small inductance value in the source pin connection (around 2.2 nH), giving the possibility to drive SiC MOSFETs in this package with the source pin as reference instead of the Kelvin source. The switching performances of the 650 V CoolSiC™ in TOLL using the source are comparable with ones using the Kelvin. Furthermore, using the source instead of the Kelvin as reference for the gate drive will help to remove spurious turn-on during hard-switching events when the driving voltage is 0 V. In fact, with the source inductance in the gate driving loop when the current starts to commutate from the body diode to the switch, the di/dt pulls down the gate of the device working as a diode. Once the current is commutated, the voltage starts to rise. Due the C_{GD} feedback the voltage on the gate increases, but thanks to the previous pull-down any unwanted spurious turn-on is avoided. To see this gate modulation in the correct way, using the correct sense point is crucial. In the REF_3K3W_TP_SIC_TOLL, the CoolSiC™ are driven between gate and source, while the Kelvin source is left not connected. Sensing the gate voltage between the gate and the floating Kelvin source gives the possibility to see clearly how the gate is modulated during the different phases of the body diode hard commutation turn-off (Figure 31). In Figure 32 instead the source is used as reference to sense the gate voltage. It is possible to see that the gate voltage is totally different from the one reported in Figure 31, because also the stray source inductance is in the measurement. Figure 33 to Figure 36 show the CoolSiC™ waveforms during PFC CCM operation at 230 V_{RMS} and full load. Ch1 (yellow trace) is the gate-Kelvin source low-side voltage (TPP1000 1 GHz); Ch2 (cyan trace) is the drain-Kelvin source low-side voltage (TPP0850 800MHz); Ch3 (red trace) is the choke current (TCP0030A 120 MHz); Ch4 (green trace) is the gate-Kelvin source high-side voltage (TIVP1 plus TIVPMX10X 1 GHz); Ch5 (blue trace) is the drain-Kelvin source high-side voltage (TIVP1 plus TIVPWS500X 1 GHz).

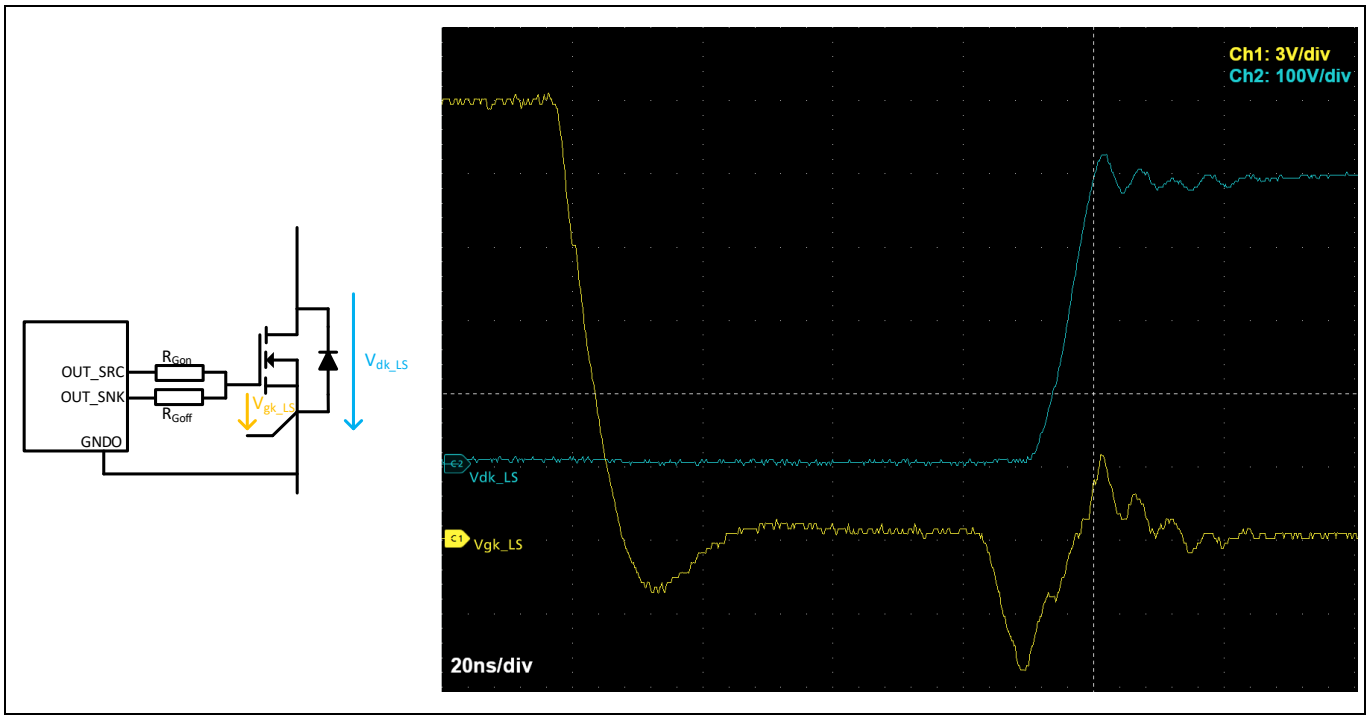

Figure 31 Gate-Kelvin source (yellow) and drain-Kelvin source (cyan) voltage waveforms during diode turn-off

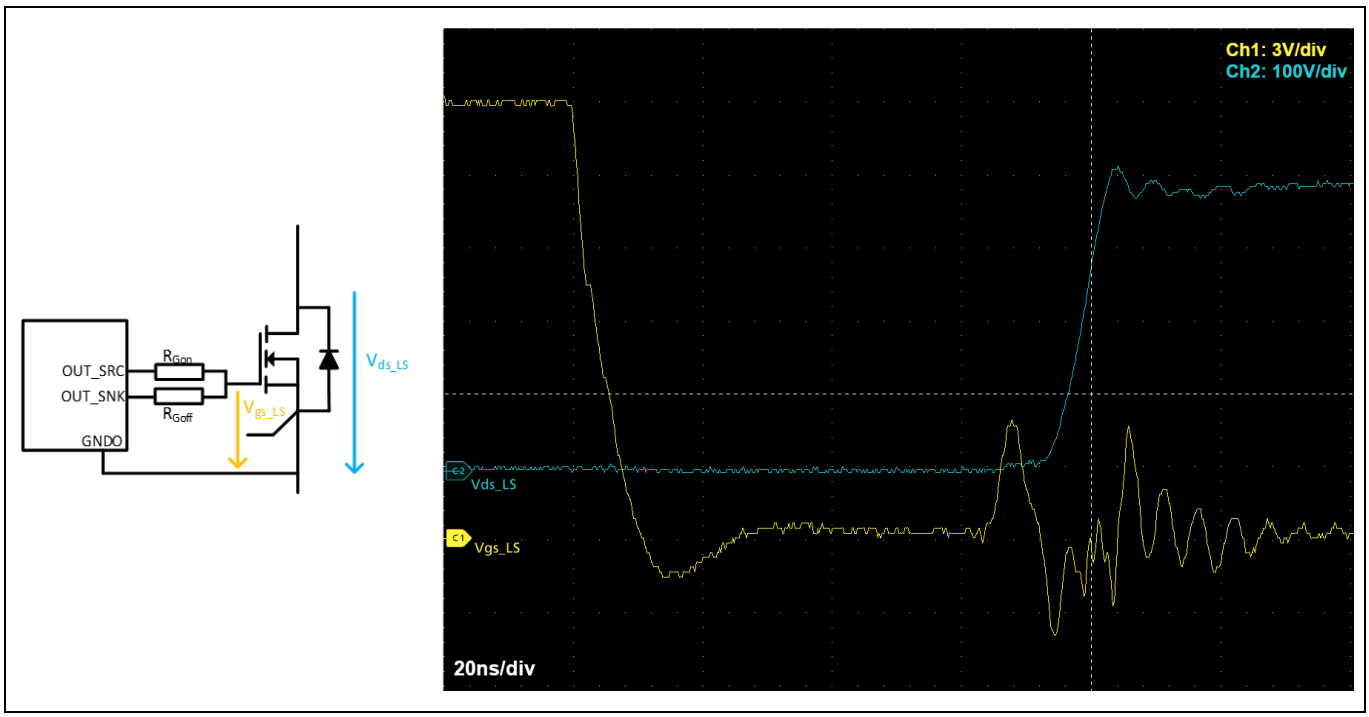

Figure 32 Gate-source (yellow) and drain-source (cyan) voltage waveforms during diode turn-off

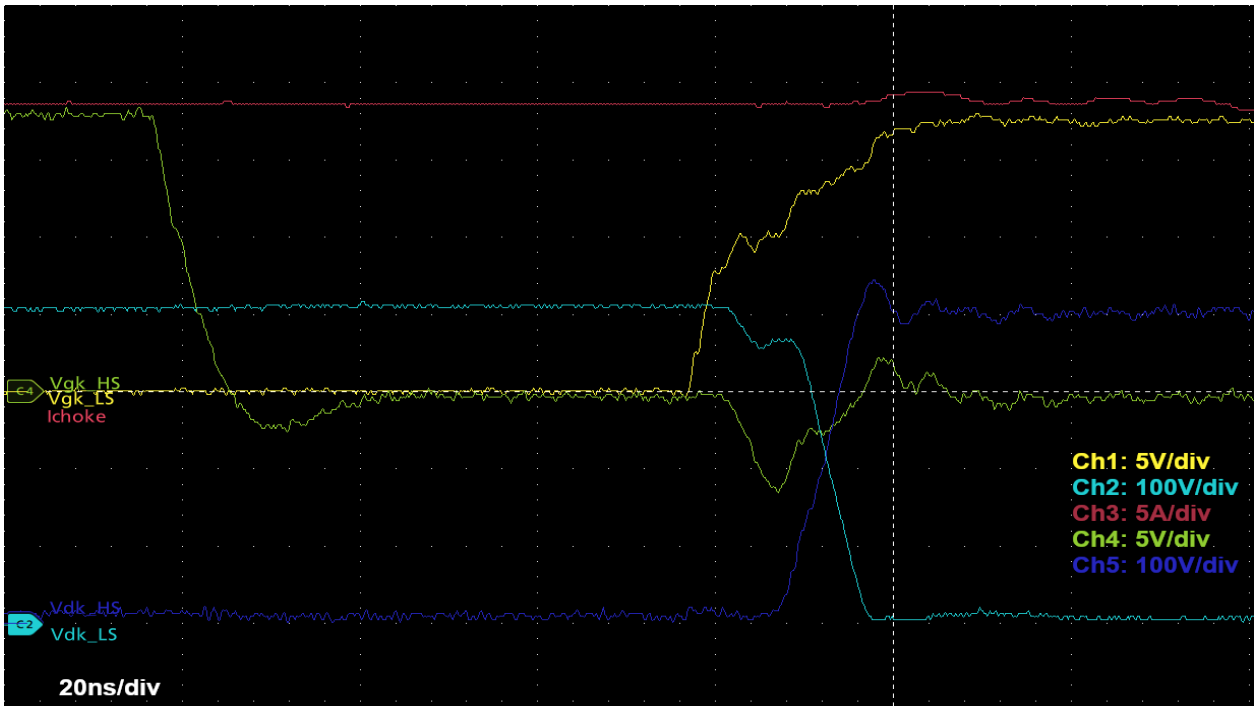

Figure 33 Low-side turn-on with 230 V_{RMS} input and full load

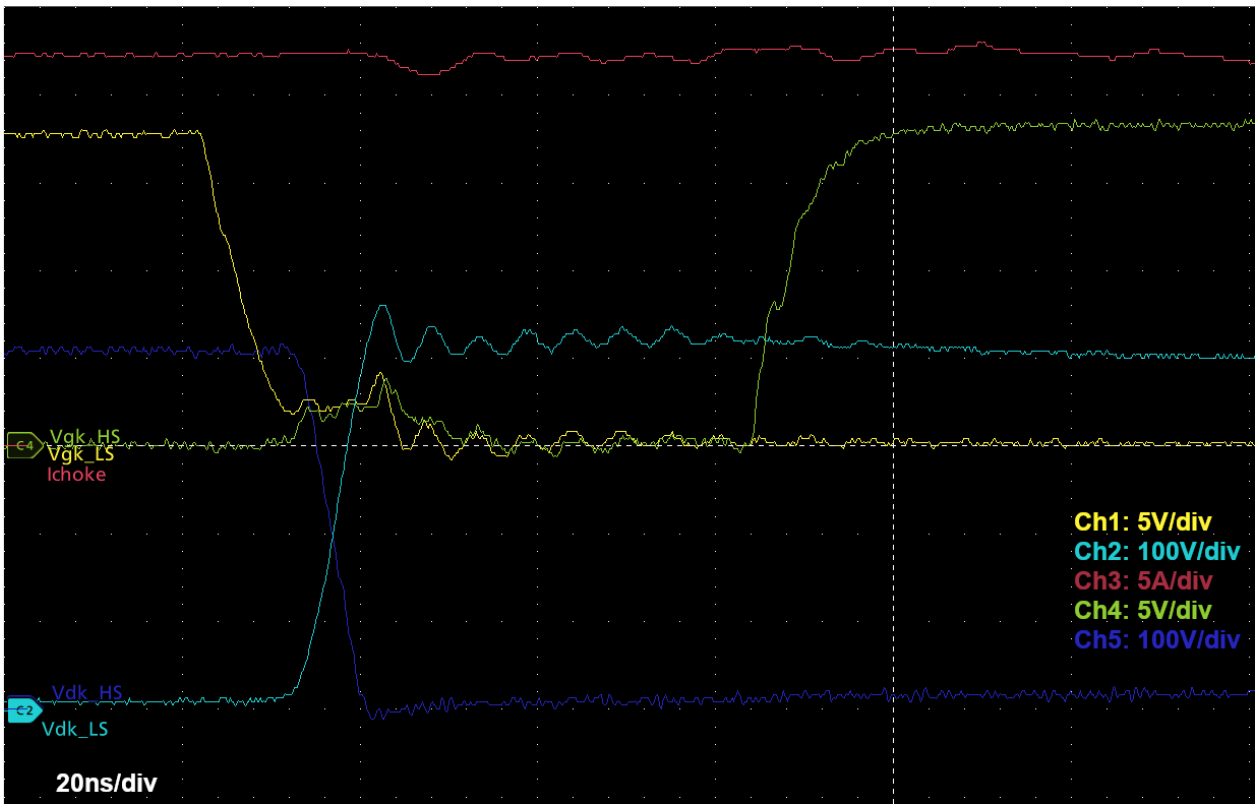

Figure 34 Low-side turn-off with 230 V_{RMS} input and full load

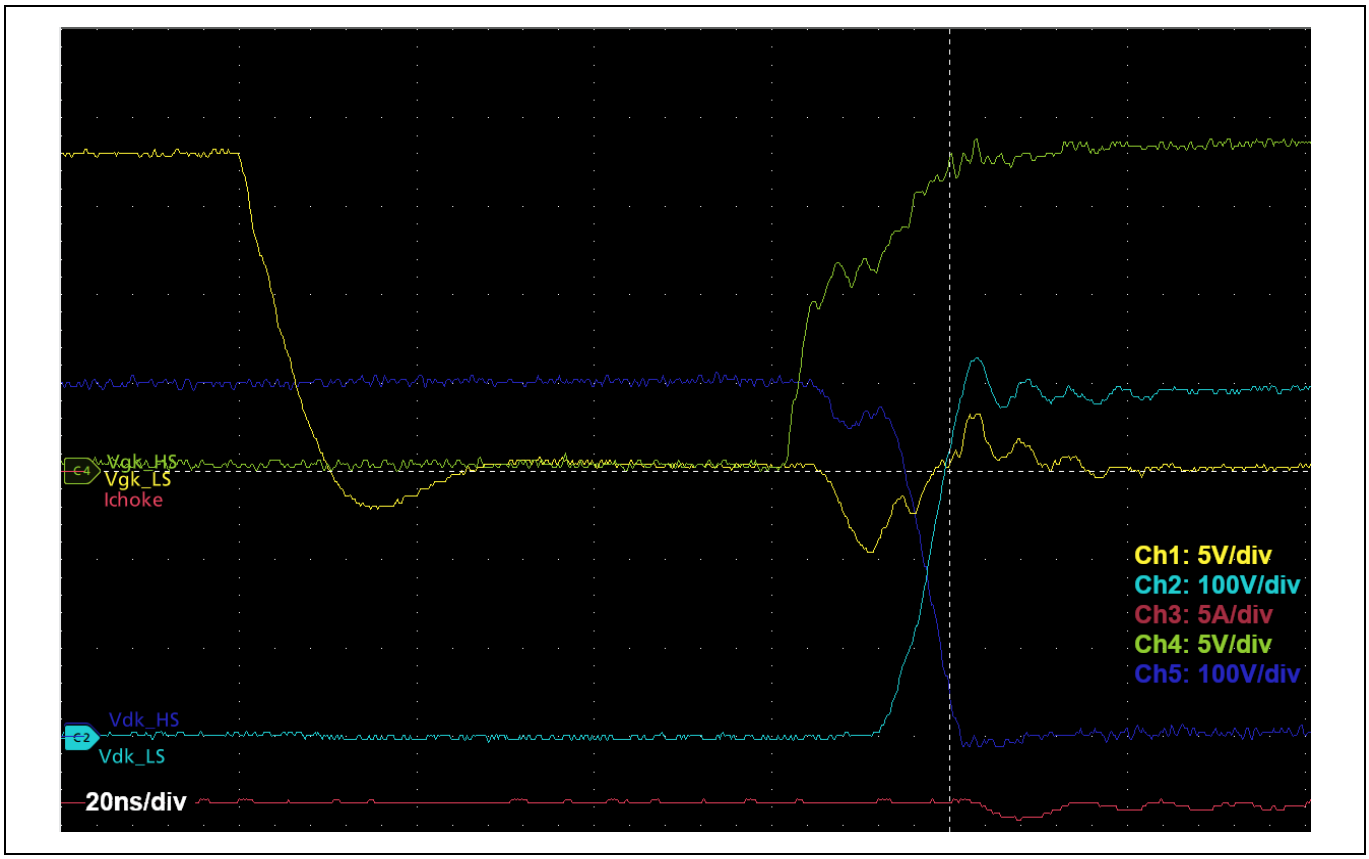

Figure 35 High-side turn-on with 230 V_{RMS} input and full load

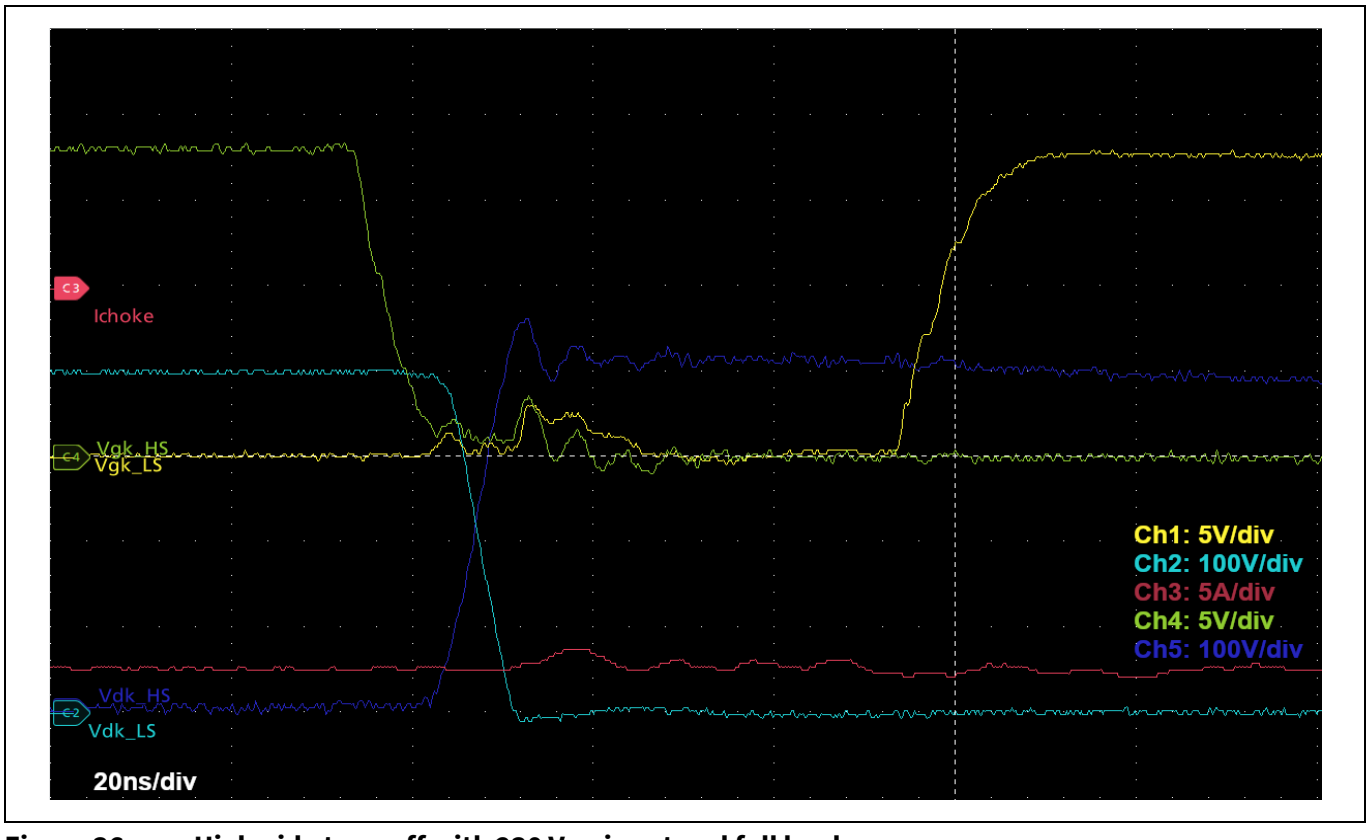

Figure 36 High-side turn-off with 230 V_{RMS} input and full load

4 Thermal measurements

The REF_3K3W_TP_SIC_TOLL is provided with an enclosure. The fan, positioned next to the AC input, sucks the air from outside. In order to have the correct functionality in terms of efficiency and thermals, the board must be used with the enclosure mounted. Since the semiconductor devices are positioned at the bottom side of the power board, the temperatures are measured with J-type thermocouples attached to the TOLL case of all semiconductors. In Figure 37 the temperatures are reported for two different V_{RMS} input conditions (230 V_{RMS} and 176 V_{RMS}) with output power sweep from 10 percent to 100 percent load. There are two temperatures reported in the charts (one for the CoolSiC™ and one for the CoolMOS™), since the low-side device and high-side device of each leg have similar temperatures.

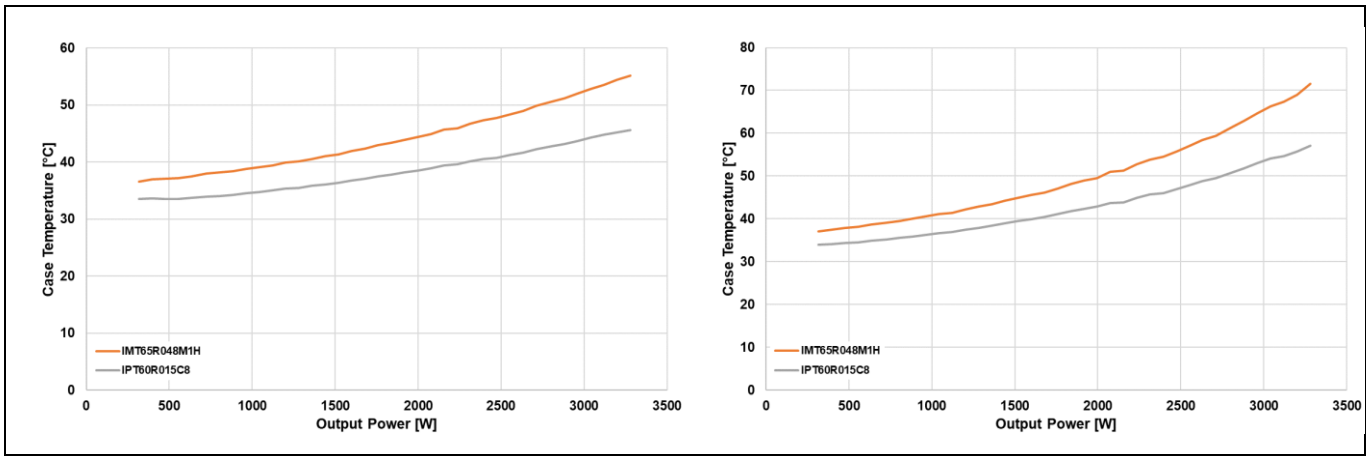

Figure 37 Semiconductor case temperature with 230 V_{RMS} (left) and 176 V_{RMS} (right) input voltage at ambient temperature of 27°C

5 EMI measurement

The conducted electromagnetic interference (EMI) of the PFC was measured with the setup shown in Figure 38. The AC voltage is generated by an AC source and the connection to the PFC is done with a line impedance stabilization network (LISN). The spectrum analyzer is connected to the LISN. The load used for the test is a passive resistive load.

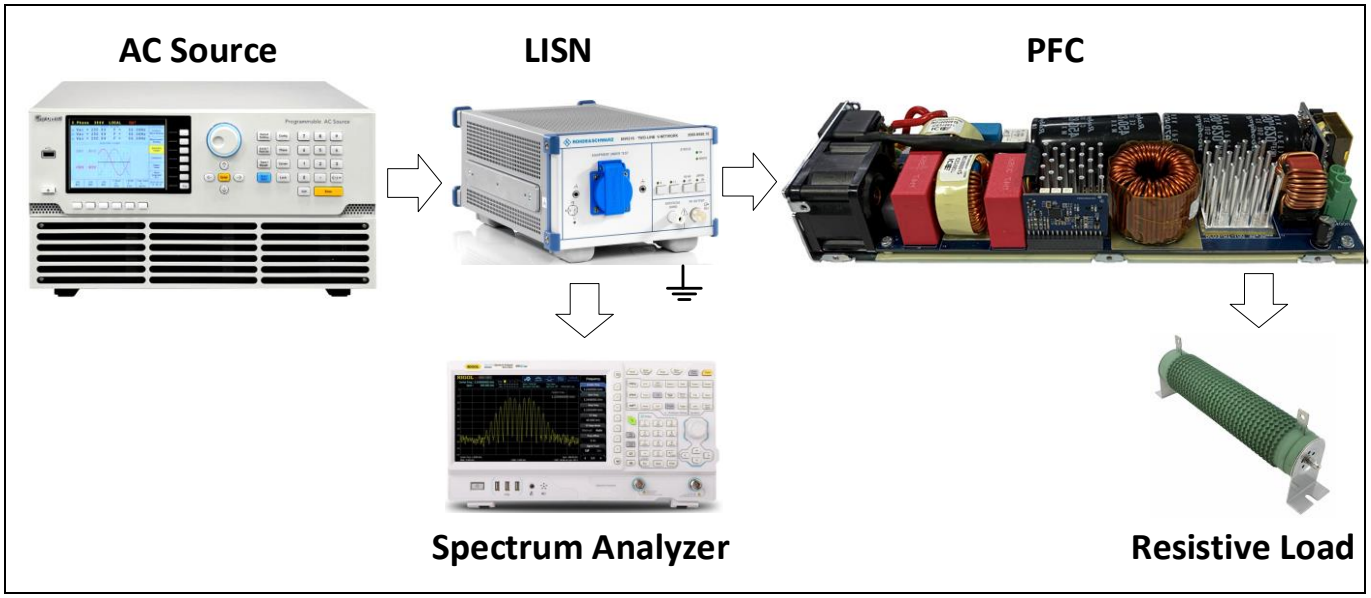

Figure 38 EMI measurement setup scheme

The EMI tests were performed for both line and neutral with an input of 230 V_{RMS} and 3 kW output power. The results for the positive peak and average for class B standard are reported from Figure 39 to Figure 42. Note that positive peak measurements represent a worst-case scenario compared to the quasi-peak request from the standard.

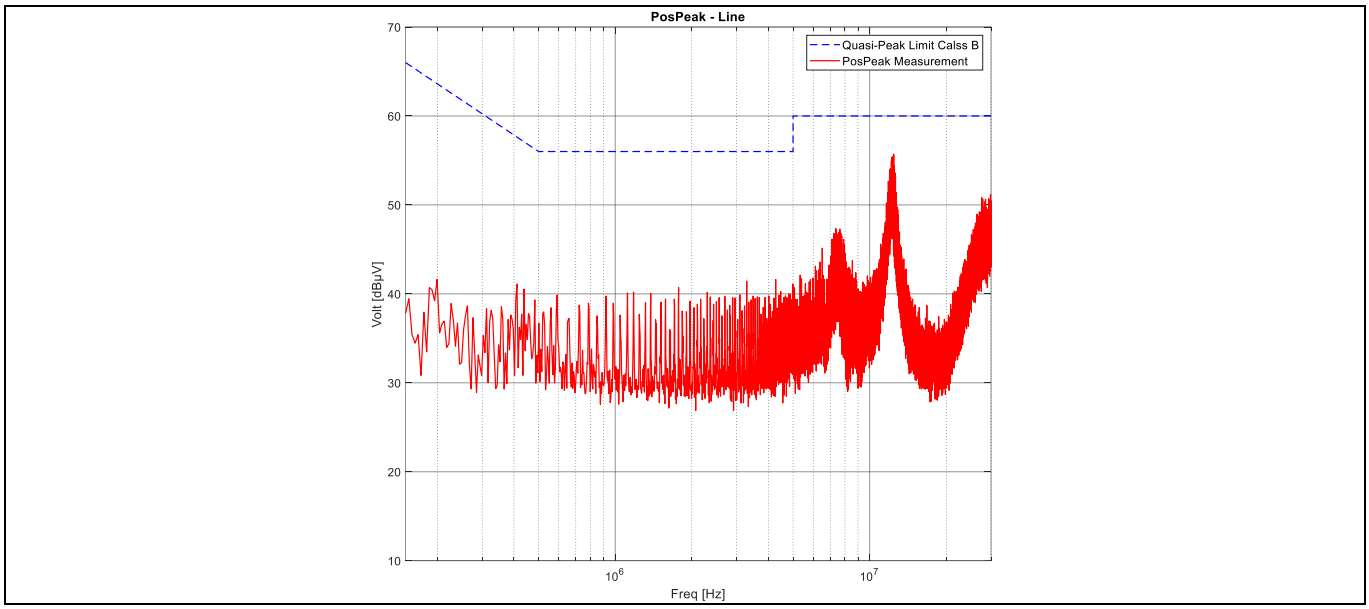

Figure 39 Positive peak in the line measurement EMI spectrum at 230 V AC input and 3 kW

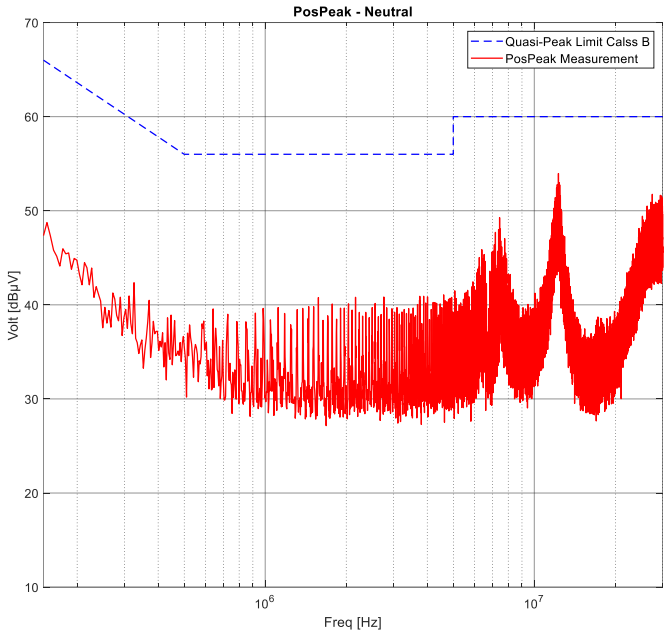

Figure 40 Positive peak neutral measurement EMI spectrum at 230 V AC input and 3 kW

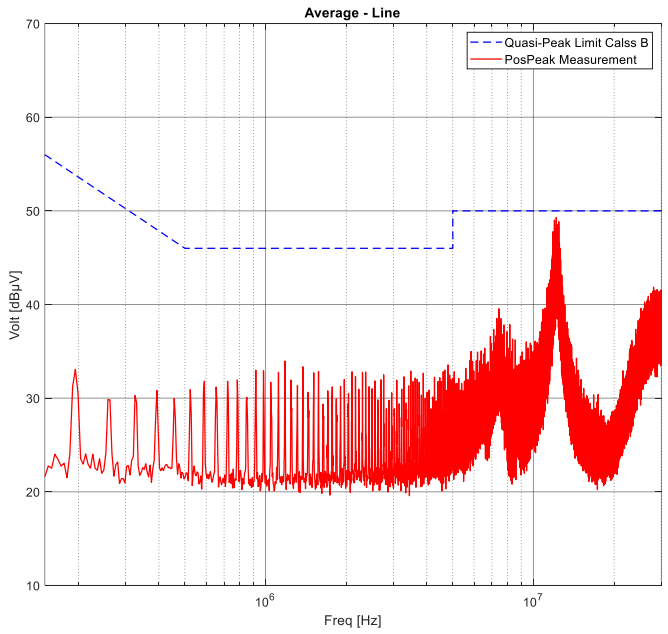

Figure 41 Average line measurement EMI spectrum at 230 V AC input and 3 kW

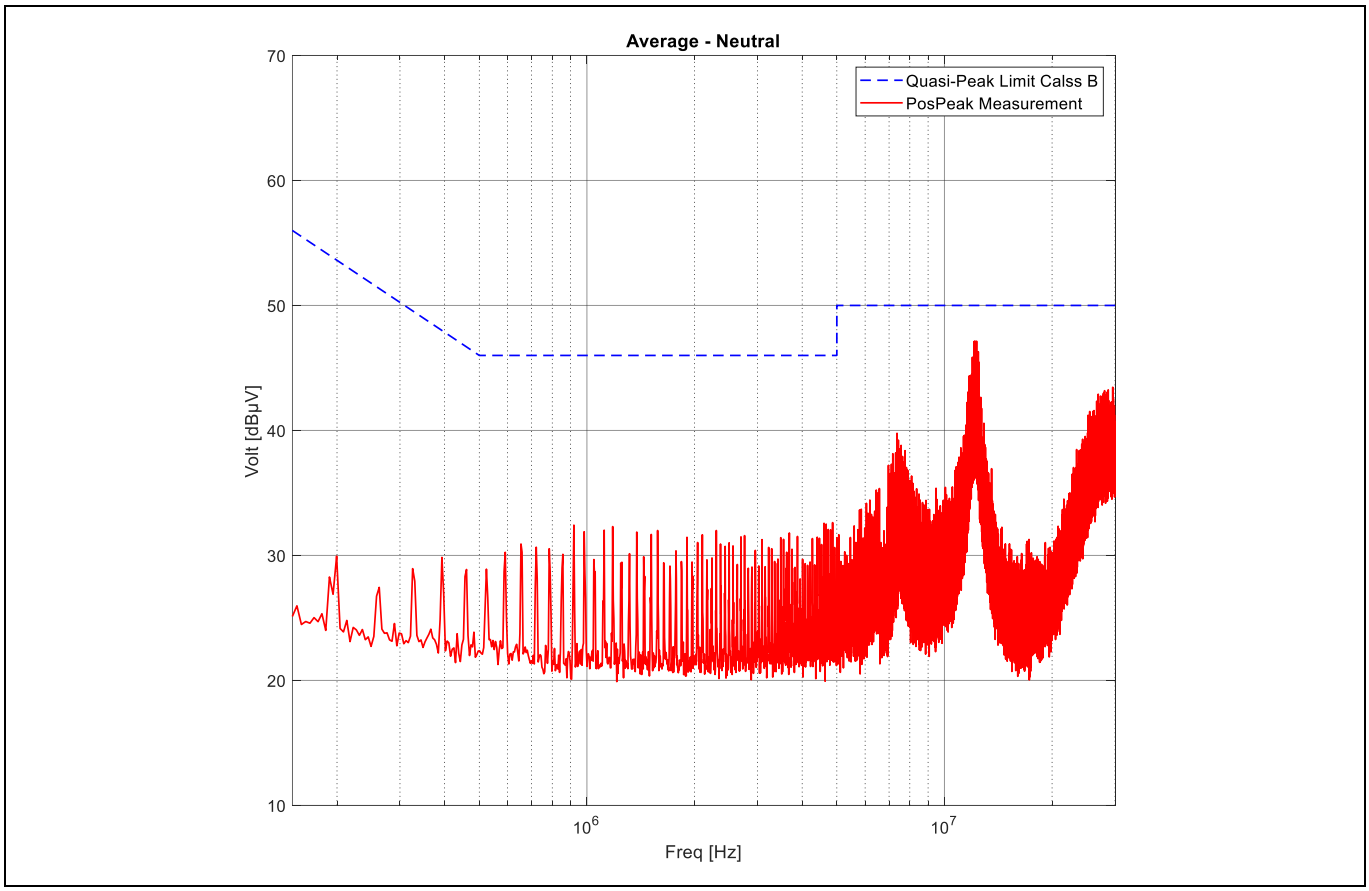

Figure 42 Average neutral measurement EMI spectrum in neutral at 230 V AC input and 3 kW

6 Summary

This document has introduced an Infineon system solution for bridgeless totem-pole PFC, which achieves a peak efficiency of 98.9 percent with a 1U form factor and a power density of 80 W/in^3. The REF_3K3W_TP_SIC_TOLL evaluation board implements Infineon 650 V CoolSiC™ and 600 V CoolMOS™ MOSFETs in TOLL package. The combination of CoolSiC™ and CoolMOS™ enables high performance in a compact form factor, as shown in this application note. The bridgeless topology implements full digital control on an XMC™ 1000 series Infineon microntroller.

The performance of the board in PFC operation is not only outstanding in steady-state conditions, offering high efficiency and high-quality input current, but also complies with power line disturbance and hold-up time requirements.

The REF_3K3W_TP_SIC_TOLL board has been tested using programmable AC source and electronic load. Efficiency, THD and PF results were obtained using the WT3000 power analyzer from Yokogawa, and waveforms with the MSO58 (1 GHz; 6.25 GS/s) oscilloscope from Tektronix.

7 Bill of materials

Table 5 Main board components in REF_3K3W_TP_SIC_TOLL

Designator	Value	Tolerance	Voltage	Description
Q1, Q2	IPT60R022S7		600 V	600 V CoolMOS™
Q3, Q4	IMT65R048M1H		650 V	650 V CoolSiC™
C1	1 µF X2	20%	305 V AC	Foil capacitor
C4, C5	4.7 nF	Y2	300 V	Ceramic capacitor
C6, C11	3.3 µF X2	10%	305 V AC	Foil capacitor
C8	470 µF	20%	16 V	Polarized capacitor
C9, C10, C17, C18, C22, C23	1 µF	X7R	25 V	Ceramic capacitor
C12, C13, C14, C15, C16, C24, C25, C26	10 µF	X5R	25 V	Ceramic capacitor
C19, C21, C40	100 nF	X7R	630 V	Ceramic capacitor
C20	1 nF	X7R	50 V	Ceramic capacitor
C36, C37	820 µF	20%	450 V	Polarized capacitor
D1, D12, D13	DFLS140L-7		40 V	Standard diode
D2, D3	MURS160BT3G		600 V	Standard diode
D4, D5	ES1JAL_M3G		600 V	Diode
D15, D16	S8KCDICT		800 V	Standard diode
F1	25 A			Fuse
H1, H2	HT100002854			Heatsink
IC1	VOL617A-3			Integrated circuit
IC2, IC4	1EDB9275F			Integrated circuit
IC3	1EDN8511B			Integrated circuit
IC5, IC6	1EDB8275F			Integrated circuit
IC7, IC8	L78L18ACUTR			Integrated circuit
L1, L2	2.5 mH			Inductor
L3	518 µH			Inductor
L4	1 mH			Inductor
NTC1, NTC2	14R	25%		NTC resistor
Q5, Q6	BSS138N		60 V	MOSFET
R1, R2, R4, R34	270R	1%		Resistor
R3, R18	560R	1%		Resistor
R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R39, R40, R41, R42, R43, R44, R45, R46	750 k	0.1%		Resistor
R17	0R	1%		Resistor
R19, R20	10R	1%		Resistor
R21	4R7	1%		Resistor
R22	R003	1%		Resistor
R23	15R	1%		Resistor
R25	43 k	1%		Resistor

R26	12 k	1%		Resistor
R30, R32	2R2	1%		Resistor
R31, R33	1R	1%		Resistor
R38, R48	12 k	1%		Resistor
R49	10K NTC	3%		NTC SMD resistor
REL1	G2RL-1A-E2-CV-HA - DC12		12 V	Relay
X1	MOD100002740 KIT_6W_13V_P7_950V		13 V	Female header, 6 contacts
X2, X8	Fuse clip			Connector
X3	MKDS 5/ 3-6,35 - 1714955			Connector
X4	SQW-116-01-L-D			Pin header, 2x16
X5, X6, X7	Power-Element M6 mit Innengewinde für LP - 8 PIN			TE Connectivity AMP connectors

Table 6 Control board components in REF_3K3W_TP_SIC_TOLL

Designator	Value	Tolerance	Voltage	Description
C1, C2, C20	330 pF	X7R	50 V	Ceramic capacitor
C3, C4, C16, C17, C23	100 pF	X7R	50 V	Ceramic capacitor
C5, C6, C7, C11	1 nF	X7R	25 V	Ceramic capacitor
C8, C9	1 µF	X7R	25 V	Ceramic capacitor
C10, C13, C15, C18, C19, C22, C24	100 nF	X7R	25 V	Ceramic capacitor
C12, C14, C21	10 µF	X5R	6.3 V	Ceramic capacitor
D1	Orange LED			LED
D2	Green LED			LED
D3	Bat54S			Diode
D4	Red LED			LED
IC1	OPA2376AIDR			Integrated circuit
IC2	L78L05ACUTR			Integrated circuit
IC3	XMC1402Q040X0064AAXUMA1			XMC™ microcontroller
IC4	TL431B	0.5%		Integrated circuit
IC5	LMH6642MF			Integrated circuit
IC6	SN74LVC2G34DBVR			Integrated circuit
R1, R2, R25	510R	1%		Resistor
R3, R4, R9, R11	37k4	0.1%		Resistor
R5, R6, R7, R10	750 k	0.1%		Resistor
R8, R13, R15	1k4	1%		Resistor
R12, R16, R20, R24	1 k	1%		Resistor
R14	10R	1%		Resistor
R17, R19	510R	1%		Resistor
R18, R21	750R	0.1%		Resistor
R22, R23	47R	0.1%		Resistor

Bill of materials

R26	22k	1%		Resistor
X1	TSM-104-01-F-DH-A			Female header, 8 contacts
X2	TMM-116-03-L-D			Pin header, 2x16 contacts
X3	PicoBlade 4-pin SMD			Pin header, 5 contacts

8 Schematics

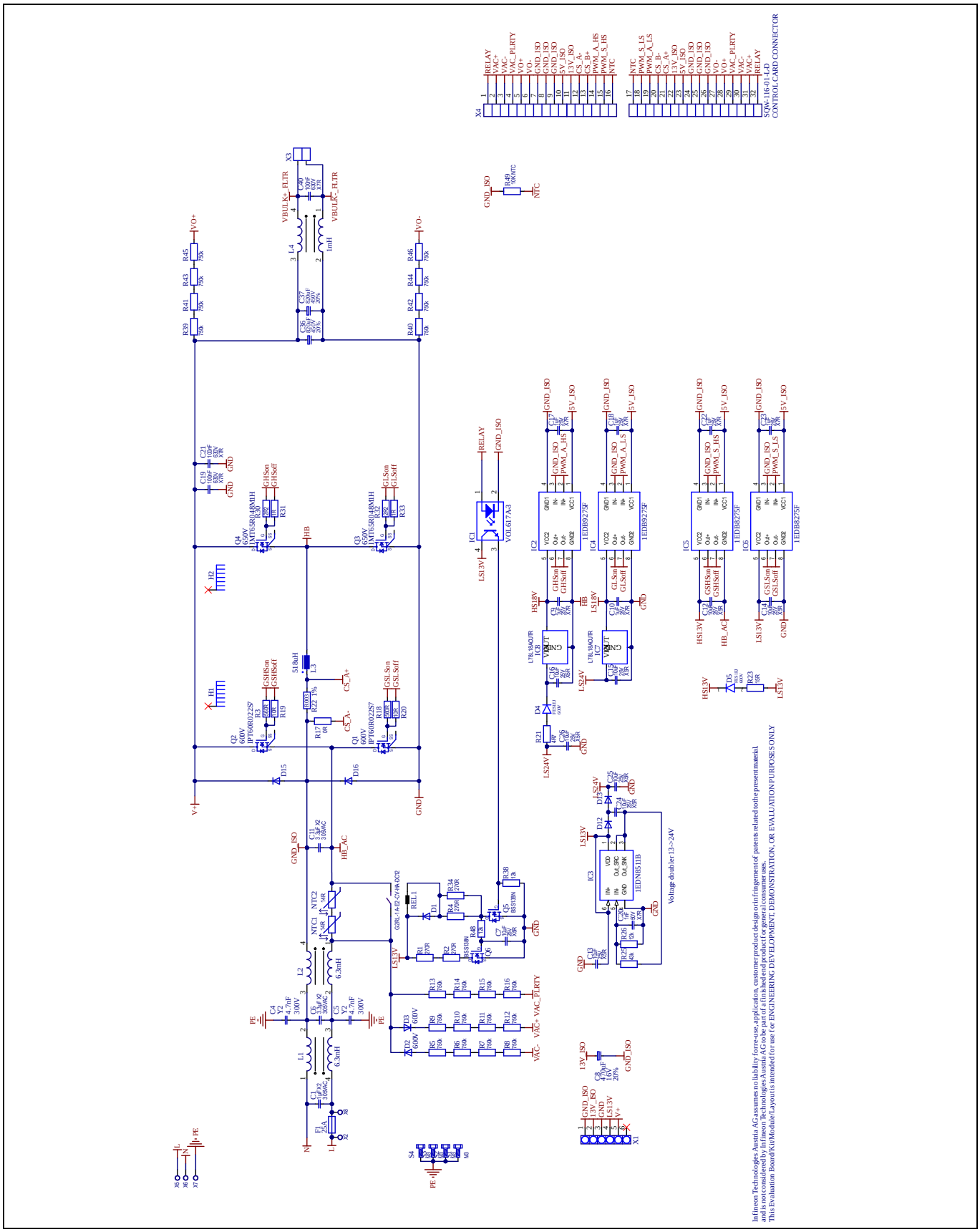

Figure 43 REF_3K3W_TP_SIC_TOLL main board schematic, which includes connectors to the control card and bias board (KIT_6W_13V_P7_950V)

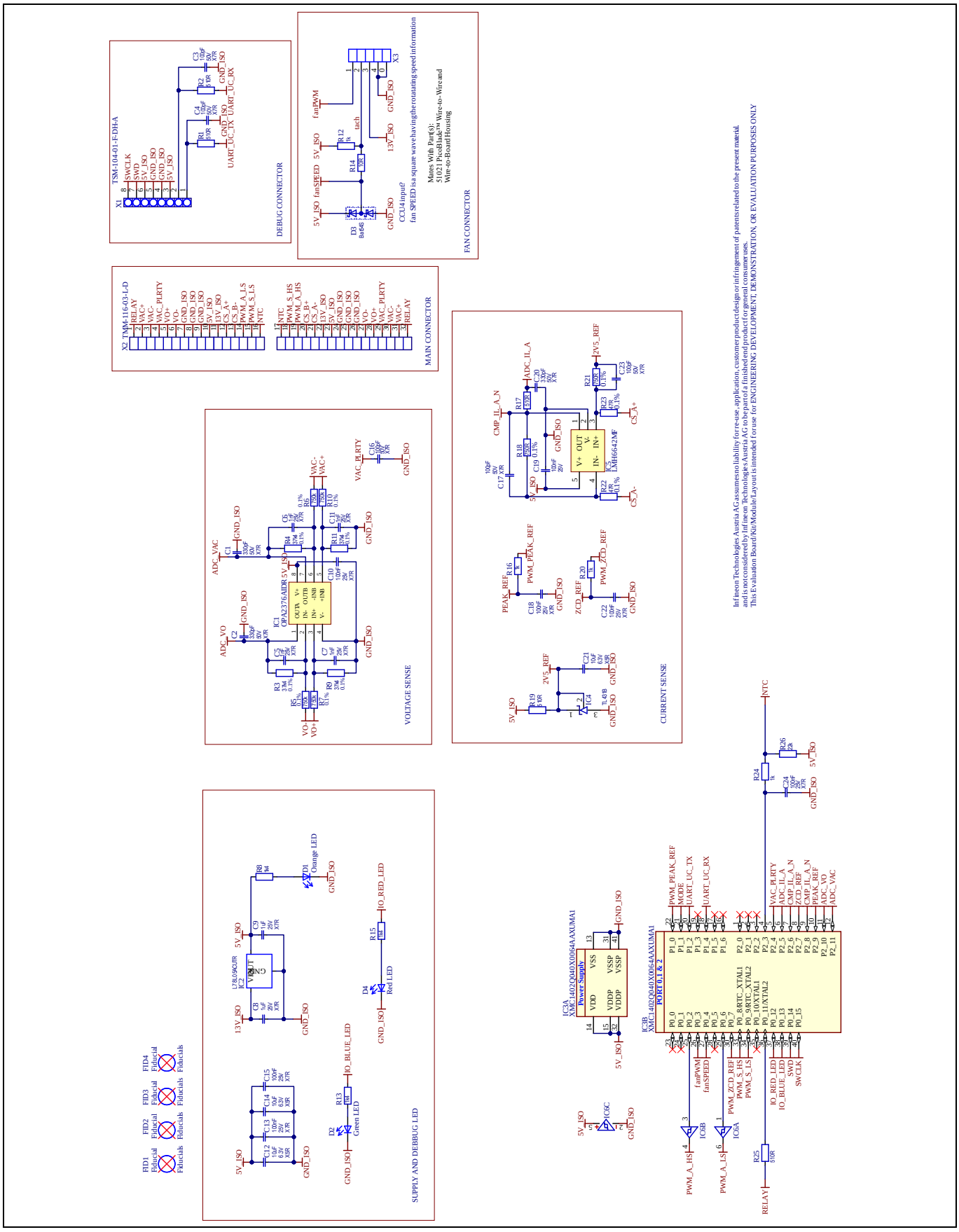

Figure 44 REF_3K3W_TP_SIC_TOLL control card schematic with XMC™

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[1] Infineon Technologies AG: *3300 W CCM bi-directional totem pole with 650 V CoolSiC™ and XMC™ ;* Available online

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Revision history

Document version	Date of release	Description of changes
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