

6EDL04x065xR and 6EDL04N03PR family

650 V and 300 V three-phase gate driver with Over Current Protection (OCP), Enable (EN), Fault and Integrated Bootstrap Diode (BSD)

Features

- Infineon thin-film-SOI-technology
- Maximum blocking voltage +650 V
- Output source/sink current +0.165 A/-0.375 A
- Integrated ultra-fast, low $R_{DS(ON)}$ Bootstrap Diode
- Insensitivity of the bridge output to negative transient voltages up to -50 V given by SOI-technology
- Separate control circuits for all six drivers
- Detection of over current and under voltage supply
- Externally programmable delay for fault clear after over current detection
- 'Shut down' of all switches during error conditions
- CMOS and LSTTL compatible input (negative logic)
- Signal interlocking of every phase to prevent cross-conduction

Potential applications

- Home appliance, refrigeration compressors, air-conditioning
- Fans, pumps
- Motor drives, general purpose inverters
- Power tools, light electric vehicles

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The device 6ED family – 3rd generation is a full bridge driver to control power devices like MOS-transistors or IGBTs in 3-phase systems with a maximum blocking voltage of +650 V. Based on the used SOI-technology there is an excellent ruggedness on transient voltages. No parasitic thyristor structures are present in the device. Hence, no parasitic latch-up may occur at all temperatures and voltage conditions.

The six independent drivers are controlled at the low-side using CMOS resp. LSTTL compatible signals, down to 3.3 V logic. The device includes an under-voltage detection unit with hysteresis characteristic and an over-current detection. The over-current level is adjusted by choosing the resistor value and the threshold level at pin ITRIP. Both error conditions (under-voltage and over-current) lead to a definite shut down off all six switches. An error signal is provided at the FAULT open drain output pin. The blocking time after over-current can be adjusted with an RC-network at pin RCIN. The input RCIN owns an internal current source of 2.8 μ A. Therefore, the resistor RRCIN is optional. The typical output current can be given with 165 mA for pull-up and 375 mA for pull down. Because of system safety reasons a 310 ns interlocking time has been realised. The function of input EN can optionally be extended with over-temperature detection, using an external NTC-resistor (see Figure 1). The monolithic integrated bootstrap diode structures between pins VCC and VBx can be used for power supply of the high side.

Product summary

| | |
|-----------------------------------|-----------------------|
| V_{OFFSET} (6EDL04x065xR) | = 670 V max. |
| V_{OFFSET} (6EDL04N03PR) | = 300 V max. |
| $I_{O+/-}$ (typ.) | = +0.165 A / -0.375 A |
| t_{on} / t_{off} (6EDL04I065xR) | = 490 ns / 490 ns |
| t_{on} / t_{off} (6EDL04N0xPR) | = 490 ns / 530 ns |
| t_r / t_f (typ. $C_L=1$ nF) | = 60 ns / 26 ns |

Package

PG-TSSOP-25



Ordering information

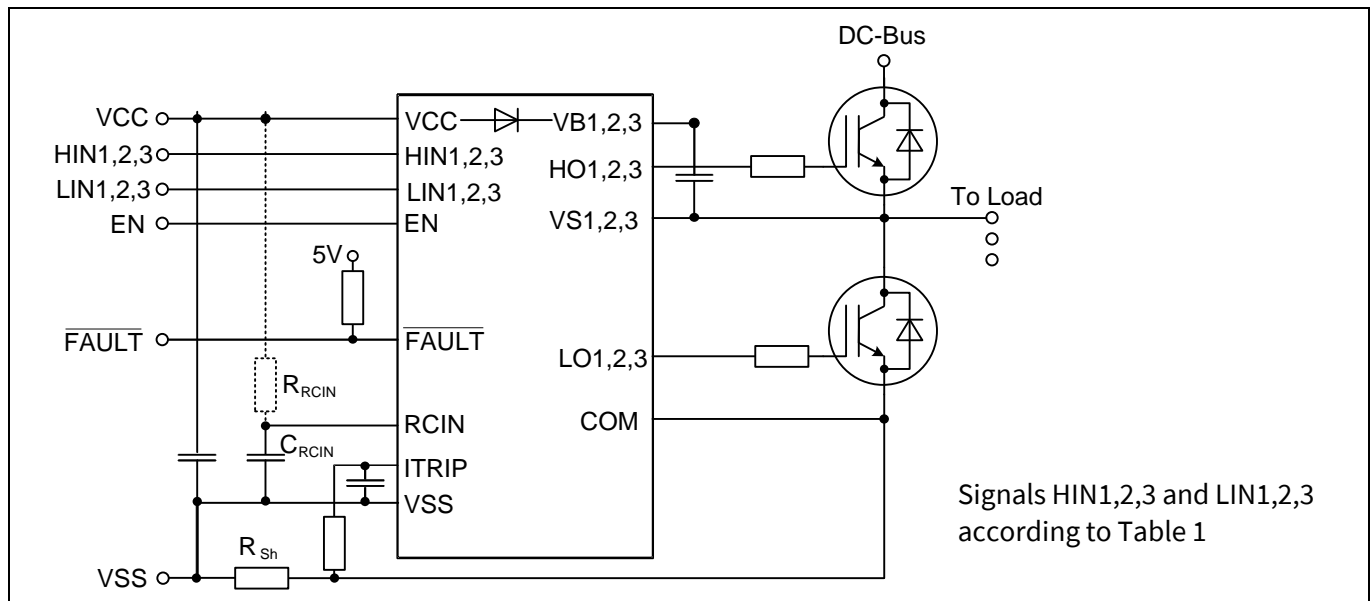


Figure 1 Typical application diagram

Ordering information

Table 1 Members of 6EDL04 family – 3rd generation

| Sales Name | Control input HIN and LIN | Target transistor | Typ. UVLO-Thresholds | Bootstrap diode | Package | Orderable part number |
|------------------------------|---------------------------|-------------------|----------------------|-----------------|-------------|-----------------------|
| 6EDL04I065NR | negative logic | IGBT | 11.7 V / 9.8 V | Yes | PG-TSSOP-25 | 6EDL04I065NRXUMA1 |
| 6EDL04I065PR | positive logic | IGBT | 11.7 V / 9.8 V | Yes | PG-TSSOP-25 | 6EDL04I065PRXUMA1 |
| 6EDL04N065PR | positive logic | MOSFET | 9 V / 8.1 V | Yes | PG-TSSOP-25 | 6EDL04N065PRXUMA1 |
| 6EDL04N03PR | positive logic | MOSFET | 9 V / 8.1 V | Yes | PG-TSSOP-25 | 6EDL04N03PRXUMA1 |

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1 Block diagram

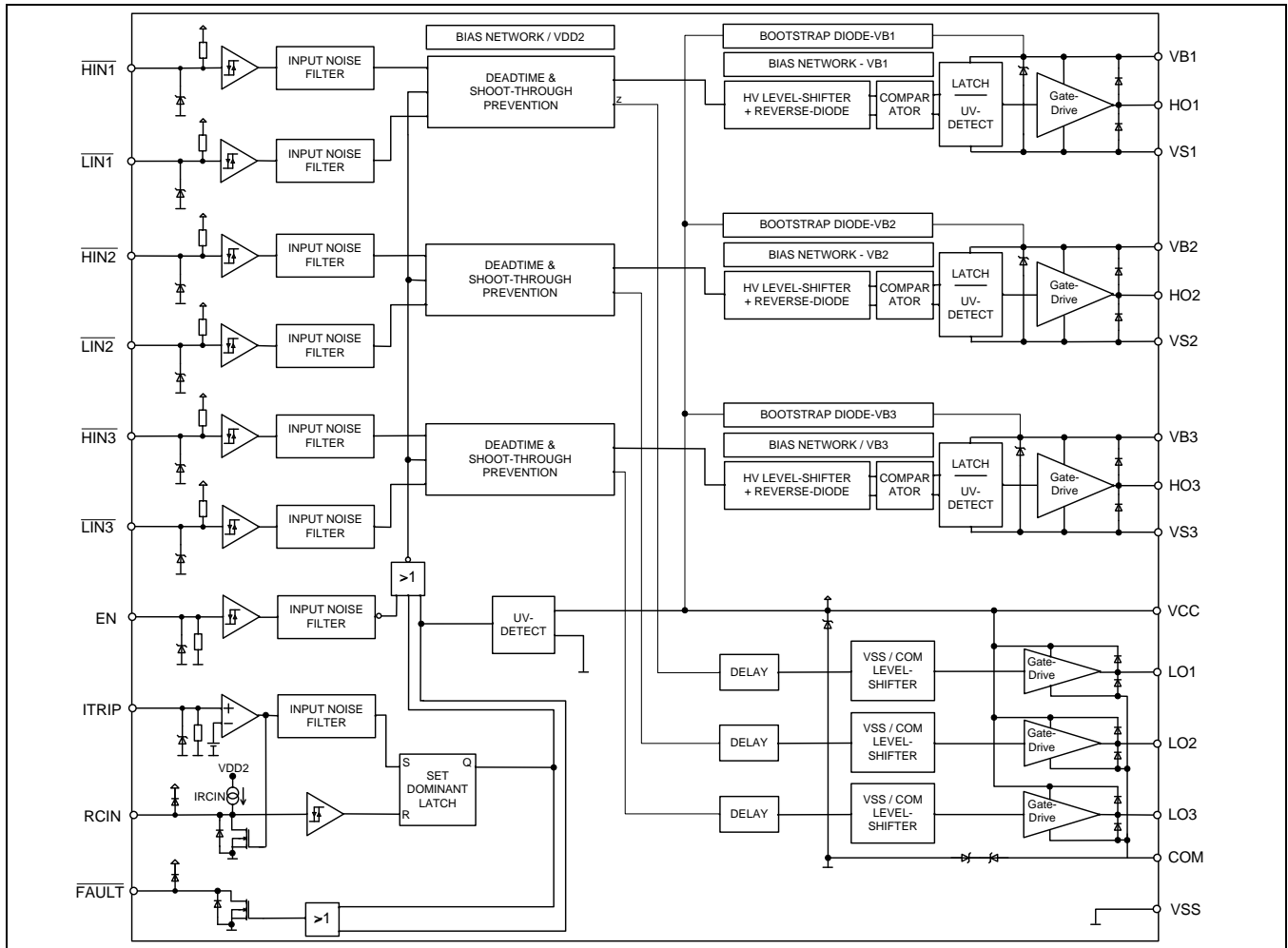


Figure 2 Functional block diagram for 6EDL041065NR

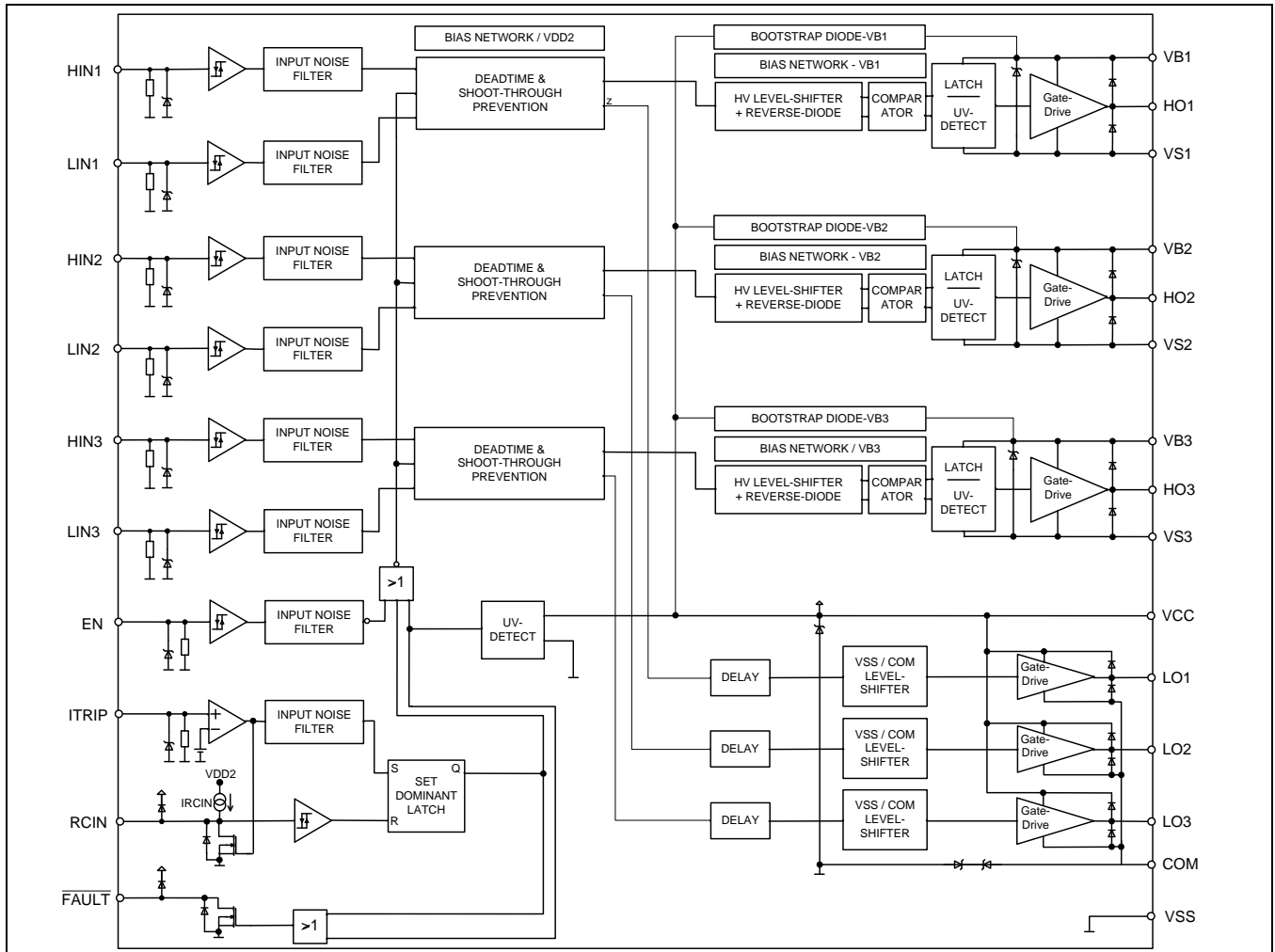


Figure 3 Functional block diagram for 6EDL04I065PR, 6EDL04N065PR and 6EDL04N03PR

2 Lead definitions

Table 2 6EDL04 family lead definitions

| Pin no. | Name | Function |
|----------|----------|---|
| 1 | VCC | Low side power supply |
| 2,3,4 | HIN1,2,3 | High side logic input (positive or negative logic according to Table 1) |
| 5,6,7 | LIN1,2,3 | Low side logic input (positive or negative logic according to Table 1) |
| 8 | /FAULT | Indicates over-current and under-voltage (negative logic, open-drain output) |
| 9 | ITRIP | Analog input for over-current shut down, activates FAULT and RCIN to VSS |
| 10 | EN | Enable I/O functionality (positive logic) |
| 11 | RCIN | External RC-network to define FAULT clear delay after FAULT-Signal (T_{FLTCLR}) |
| 12 | VSS | Logic ground |
| 13 | COM | Low side gate driver reference |
| 25,22,19 | VB1,2,3 | High side positive power supply |
| 24,21,18 | HO1,2,3 | High side gate driver output |
| 23,20,17 | VS1,2,3 | High side negative power supply |
| 16,15,14 | LO1,2,3 | Low side gate driver output |

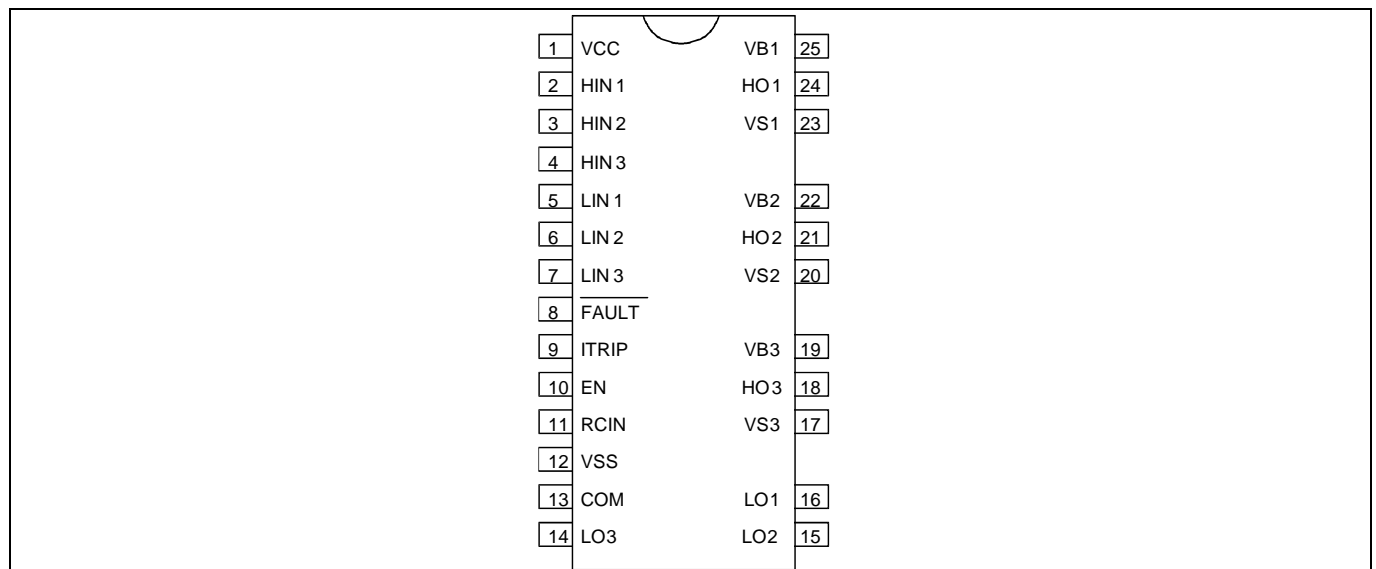


Figure 4 Pin Configuration of 6ED family (signals HIN1,2,3 and LIN1,2,3 according to Table 1)

3 Functional description

3.1 Low Side and High Side Control Pins (Pin 2, 3, 4, 5, 6, 7)

The Schmitt trigger input threshold of them is such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. Input Schmitt trigger and noise filter provide beneficial noise rejection to short input pulses according to Figure 5 and Figure 6.

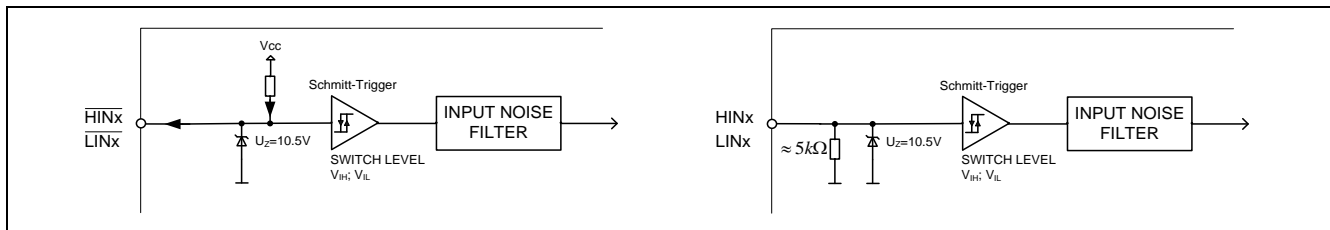


Figure 5 Input pin structure for negative logic (left) and positive logic (right)

An internal pull-up of about 75 kΩ (negative logic) pre-biases the input during supply start-up and a ESD zener clamp is provided for pin protection purposes. The zener diodes are therefore designed for single pulse stress only and not for continuous voltage stress over 10V. For versions with positive, a 5 kΩ pull-down resistor is used for this function.

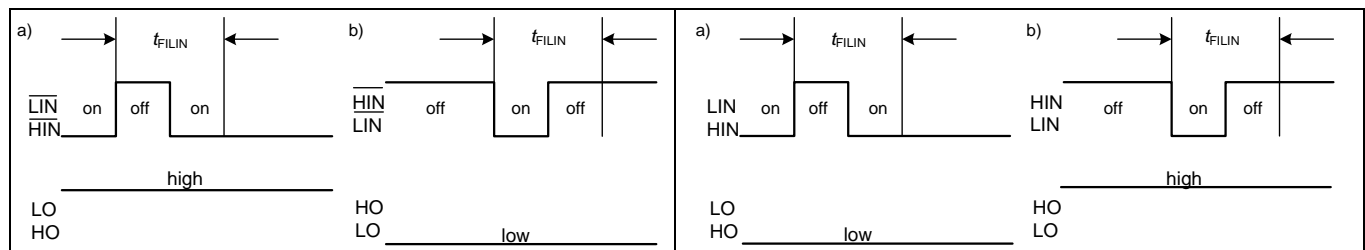


Figure 6 Input filter timing diagram for negative logic (left) and positive logic (right)

It is anyway recommended for proper work of the driver not to provide input pulse-width lower than 1 μs.

The 6ED family – 3rd generation provides additionally a shoot through prevention capability which avoids the simultaneous on-state of two channels of the same leg (i.e. HO1 and LO1, HO2 and LO2, HO3 and LO3). When two inputs of a same leg are activated, only one leg output is activated, so that the leg is kept steadily in a safe state.

A minimum dead time insertion of typ. 310 ns is also provided, in order to reduce cross-conduction of the external power switches.

3.2 EN (Gate Driver Enable, Pin 10)

The signal applied to pin EN controls directly the output stages. All outputs are set to LOW, if EN is at LOW logic level. The internal structure of the pin is given in Figure 7. The switching levels of the Schmitt-Trigger are here $V_{EN,TH+} = 2.1\text{ V}$ and $V_{EN,TH-} = 1.3\text{ V}$. The typical propagation delay time is $t_{EN} = 780\text{ ns}$. There is an internal pull down resistor (75 kΩ), which keeps the gate outputs off in case of broken PCB connection.

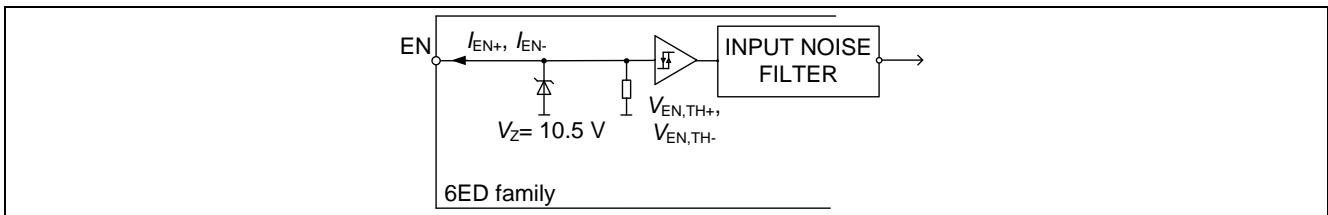


Figure 7 EN pin structures

3.3 /FAULT (Fault Feedback, Pin 8)

/Fault pin is an active low open-drain output indicating the status of the gate driver (see Figure 8). The pin is active (i.e. forces LOW voltage level) when one of the following conditions occur:

- Under-voltage condition of VCC supply: In this case the fault condition is released as soon as the supply voltage condition returns in the normal operation range (please refer to VCC pin description for more details).
- Over-current detection (ITRIP): The fault condition is latched until current trip condition is finished and RCIN input is released (please refer to ITRIP pin).

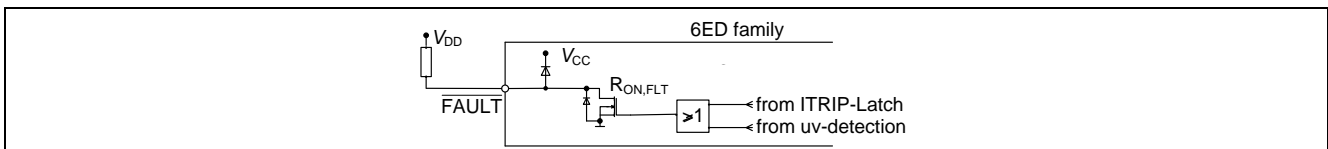


Figure 8 /FAULT pin structures

3.4 ITRIP and RCIN (Over-Current Detection Function, Pin 9, 11)

The 6ED family – 3rd generation provides an over-current detection function by connecting the ITRIP input with the motor current feedback. The ITRIP comparator threshold (typ 0.44 V) is referenced to VSS ground. An input noise filter (typ. $t_{ITRIPMIN} = 230$ ns) prevents the driver to detect false over-current events.

Over-current detection generates a hard shut down of all outputs of the gate driver and provides a latched fault feedback at /FAULT pin. RCIN input/output pin is used to determine the reset time of the fault condition. As soon as ITRIP threshold is exceeded the external capacitor connected to RCIN is fully discharged. The capacitor is then recharged by the RCIN current generator when the over-current condition is finished. As soon as RCIN voltage exceeds the rising threshold of typ $V_{RCIN,TH} = 5.2$ V, the fault condition releases and the driver returns operational following the ontrol input pins according to Section 3.1.

3.5 VCC, VSS and COM (Low Side Supply, Pin 1, 12, 13)

VCC is the low side supply and it provides power both to input logic and to low side output power stage. Input logic is referenced to VSS ground as well as the under-voltage detection circuit. Output power stage is referenced to COM ground. COM ground is floating respect to VSS ground with a maximum range of operation of +/-5.7 V. A back-to-back zener structure protects grounds from noise spikes.

The under-voltage circuit enables the device to operate at power on when a typical supply voltage higher than V_{CCUV+} is present.

The IC shuts down all the gate drivers power outputs, when the VCC supply voltage is below $V_{CCUV-} = 9.8$ V respectively 8.1 V. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

3.6 VB1, 2, 3 and VS1, 2, 3 (High Side Supplies, Pin 17, 19, 20, 22, 23, 25)

VB to VS is the high side supply voltage. The high side circuit can float with respect to VSS following the external high side power device emitter/source voltage. Due to the low power consumption, the floating driver stage can be supplied by bootstrap topology connected to VCC.

The device operating area as a function of the supply voltage is given in Figure 30 and Figure 31.

3.7 LO1,2,3 and HO1,2,3 (Low and High Side Outputs, Pin 14, 15, 16, 18, 21, 24)

Low side and high side power outputs are specifically designed for pulse operation such as gate drive of IGBT and MOSFET devices. Low side outputs (i.e. LO1,2,3) are state triggered by the respective inputs, while high side outputs (i.e. HO1,2,3) are edge triggered by the respective inputs. In particular, after an under voltage condition of the VBS supply, a new turn-on signal (edge) is necessary to activate the respective high side output, while after a under voltage condition of the VCC supply, the low side outputs switch to the state of their respective inputs.

4 Electrical parameters

4.1 Absolute maximum ratings

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. All parameters are valid for $T_a=25\text{ }^\circ\text{C}$.

Table 3 Absolute maximum ratings

| Parameter | Symbol | Min. | Max. | Unit |
|--|---------------|--------------------|----------------|------------------|
| High side offset voltage ¹ | V_S | $V_{CC}-V_{BS}-6$ | 650 | V |
| 6EDL04x065xR 6EDL04N03PR | | | 280 | |
| High side offset voltage ($t_p<500\text{ns}$) ¹ | | $V_{CC}-V_{BS}-50$ | - | |
| High side offset voltage ¹ | V_B | $V_{CC}-6$ | 670 | |
| 6EDL04x065xR 6EDL04N03PR | | | 300 | |
| High side offset voltage ($t_p<500\text{ns}$) ¹ | | $V_{CC}-50$ | - | |
| High side floating supply voltage (V_B vs. V_S) (internally clamped) | V_{BS} | -1 | 20 | |
| High side output voltage (V_{HO} vs. V_S) | V_{HO} | -0.5 | $V_B+0.5$ | |
| Low side supply voltage (internally clamped) | V_{CC} | -1 | 20 | |
| Low side supply voltage (V_{CC} vs. V_{COM}) | V_{CCOM} | -0.5 | 25 | |
| Gate driver ground | V_{COM} | -5.7 | 5.7 | |
| Low side output voltage (V_{LO} vs. V_{COM}) | V_{LO} | -0.5 | $V_{CCOM}+0.5$ | |
| Input voltage LIN,HIN,EN,ITRIP | V_{IN} | -1 | 10 | |
| FAULT output voltage | V_{FLT} | -0.5 | $V_{CC}+0.5$ | |
| RCIN output voltage | V_{RCIN} | -0.5 | $V_{CC}+0.5$ | |
| Power dissipation (to package) ² | P_D | - | 0.6 | W |
| Thermal resistance (junction to ambient) | $R_{th(j-a)}$ | - | 165 | K/W |
| Junction temperature | T_J | - | 150 | $^\circ\text{C}$ |
| Storage temperature | T_S | -40 | 150 | |
| offset voltage slew rate ³ | dV_S/dt | | 50 | V/ns |

¹ In case $V_{CC} > V_B$ there is an additional power dissipation in the internal bootstrap diode between pins VCC and VBx. Insensitivity of bridge output to negative transient voltage up to -50 V is not subject to production test – verified by design / characterization.

² Consistent power dissipation of all outputs. All parameters inside operating range.

³ Not subject of production test, verified by characterisation

4.2 Required operation conditions

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. All parameters are valid for $T_a=25\text{ °C}$.

Table 4 Required Operation Conditions

| Parameter | | Symbol | Min. | Max. | Unit |
|--|-----------------------------|------------|------|--------------|------|
| High side offset voltage ¹ | 6EDL04x065xR 6EDL04N03PR | V_B | 7 | 667.5 300 | V |
| Low side supply voltage (V_{CC} vs. V_{COM}) | | V_{CCOM} | 10 | 25 | |

4.3 Operating Range

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. All parameters are valid for $T_a=25\text{ °C}$.

Table 5 Operating range

| Parameter | | Symbol | Min. | Max. | Unit |
|---|------------------------------|------------|----------------------------|----------|--------------------|
| High side floating supply offset voltage | | V_S | $V_{CC} -$ $V_{BS} - 1$ | 650 | V |
| High side floating supply offset voltage (V_B vs. V_{CC} , statically) | | V_{BCC} | -1.0 | 650 | |
| High side floating supply voltage (V_B vs. V_S , Note 1) | 6EDL04I065NR 6EDL04I065PR | V_{BS} | 13 | 17.5 | V |
| | 6EDL04N065PR 6EDL04N03PR | | 10 | 17.5 | |
| High side output voltage (V_{HO} vs. V_S) | | V_{HO} | 0 | V_{BS} | |
| Low side output voltage (V_{LO} vs. V_{COM}) | | V_{LO} | 0 | V_{CC} | |
| Low side supply voltage | 6EDL04I065NR 6EDL04I065PR | V_{CC} | 13 | 17.5 | |
| | 6EDL04N065PR 6EDL04N03PR | | 10 | 17.5 | |
| Low side ground voltage | | V_{COM} | -2.5 | 2.5 | |
| Logic input voltages LIN,HIN,EN,ITRIP ² | | V_{IN} | 0 | 5 | |
| FAULT output voltage | | V_{FLT} | 0 | V_{CC} | |
| RCIN input voltage | | V_{RCIN} | 0 | V_{CC} | |
| Pulse width for ON or OFF ³ | | t_{IN} | 1 | - | μs |
| Ambient temperature | | T_a | -40 | 105 | $^{\circ}\text{C}$ |

¹ Logic operational for V_B (V_B vs. V_S) > 7.0 V

² All input pins (HINx, LINx) and EN, ITRIP pin are internally clamped (see abs. maximum ratings)

³ In case of input pulse width at LINx and HINx below 1 μ the input pulse may not be transmitted properly

4.4 Static logic function table

| VCC | VBS | RCIN | ITRIP | ENABLE | FAULT | LO1,2,3 | HO1,2,3 |
|---------------------|---------------------|------------------------|-----------------------|--------|----------|-----------|-----------|
| <V _{CCUV-} | X | X | X | X | 0 | 0 | 0 |
| 15 V | <V _{BSUV-} | X | 0 | 3.3 V | High imp | LIN1,2,3* | 0 |
| 15 V | 15 V | <3.2 V ↓ | 0 | 3.3 V | 0 | 0 | 0 |
| 15 V | 15 V | X | > V _{IT,TH+} | 3.3 V | 0 | 0 | 0 |
| 15 V | 15 V | > V _{RCIN,TH} | 0 | 3.3 V | High imp | LIN1,2,3* | HIN1,2,3* |
| 15 V | 15 V | > V _{RCIN,TH} | 0 | 0 | High imp | 0 | 0 |

* according to Table 1

4.5 Static parameters

V_{CC} = V_{BS} = 15V unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 6 Static parameters

| Parameter | Symbol | Values | | | Unit | Test condition |
|--|------------------------------|--|-----------------------------|--------------------------|--------------------------|--------------------------------|
| | | Min. | Typ. | Max. | | |
| High level input voltage | V _{IH} | 1.7 | 2.1 | 2.4 | V | |
| Low level input voltage | V _{IL} | 0.7 | 0.9 | 1.1 | | |
| EN positive going threshold | V _{EN,TH+} | 1.9 | 2.1 | 2.3 | | |
| EN negative going threshold | V _{EN,TH-} | 1.1 | 1.3 | 1.5 | | |
| ITRIP positive going threshold | V _{IT,TH+} | 380 | 445 | 510 | mV | |
| ITRIP input hysteresis | V _{IT,HYS} | 45 | 70 | | | |
| RCIN positive going threshold | V _{RCIN,TH} | - | 5.2 | 6.4 | V | |
| RCIN input hysteresis | V _{RCIN,HYS} | - | 2.0 | - | | |
| Input clamp voltage (HIN and LIN acc. Table 1, EN, ITRIP) | V _{IN,CLMAP} | 9 | 10.3 | 12 | | I _{IN} = 4mA |
| Input clamp voltage at high impedance (/HIN, /LIN negative logic only) | V _{IN,FLOAT} | - | 5.3 | 5.8 | | controller output pin floating |
| High level output voltage | V _{OH} | LO1,2,3 HO1,2,3 | V _{CC} -1.4 | V _{CC} -0.7 | - | I _O = 20mA |
| | | | V _B -1.4 | V _B -0.7 | - | |
| Low level output voltage | V _{OL} | LO1,2,3 HO1,2,3 | - | V _{COM+} 0.2 | V _{COM+} 0.6 | I _O = -20mA |
| | | | - | V _S + 0.2 | V _S + 0.6 | |
| V _{CC} and V _{BS} supply undervoltage positive going threshold | 6EDL04I065NR 6EDL04I065PR | V _{CCUV+} V _{BSUV+} | 11 | 11.7 | 12.5 | V |
| | | | 6EDL04N065PR 6EDL04N03PR | 8.3 | 9 | |
| V _{CC} and V _{BS} supply undervoltage negative going threshold | 6EDL04I065NR 6EDL04I065PR | V _{CCUV-} V _{BSUV-} | 9.5 | 9.8 | 10.8 | |
| | | | 6EDL04N065PR 6EDL04N03PR | 7.5 | 8.1 | |

Table 6 Static parameters

| Parameter | | Symbol | Values | | | Unit | Test condition |
|---|---|--|--------|------|------|------|--|
| | | | Min. | Typ. | Max. | | |
| V _{CC} and V _{BS} supply undervoltage lockout hysteresis | 6EDL04I065NR 6EDL04I065PR | V _{CCUVH} V _{BSUVH} | 1.2 | 1.9 | - | V | |
| | 6EDL04N065PR 6EDL04N03PR | | 0.5 | 0.9 | - | | |
| High side leakage current betw. VS and VSS | | I _{LVS+} | | 1 | 12.5 | μA | V _S = 650V |
| High side leakage current betw. VS and VSS | | I _{LVS+¹} | - | 10 | - | | T _J = 125°C, V _S = 650V |
| High side leakage current between VS _x and VS _y (x=1,2,3 and y=1,2,3) | | I _{LVS-¹} | - | 10 | - | | T _J = 125°C V _{Sx} - V _{Sy} = 650V |
| Quiescent current V _{BS} supply (VB only) | | I _{QBS1} | - | 210 | 400 | μA | HO=low |
| Quiescent current V _{BS} supply (VB only) | | I _{QBS2} | - | 210 | 400 | | HO=high |
| Quiescent current V _{CC} supply (VCC only) | 6EDL04I065NR | I _{QCC1} | - | 1.1 | 1.8 | mA | V _{LIN} =float. (all) V _{VSx} =50V (only bootstrap types) |
| | 6EDL04I065PR 6EDL04N065PR 6EDL04N03PR | | - | 0.75 | 1.5 | | |
| Quiescent current V _{CC} supply (VCC only) | 6EDL04I065NR | I _{QCC2} | - | 1.3 | 2 | mA | V _{LIN} =0, V _{HIN} =3.3 V V _{VSx} =50V |
| | 6EDL04I065PR 6EDL04N065PR 6EDL04N03PR | | - | 0.75 | 1.5 | | V _{LIN} =3.3 V, V _{HIN} =0 V _{VSx} =50V |
| Quiescent current V _{CC} supply (VCC only) | 6EDL04I065NR | I _{QCC3} | - | 1.3 | 2 | mA | V _{LIN} =3.3 V, V _{HIN} =0 V _{VSx} =50V |
| | 6EDL04I065PR 6EDL04N065PR 6EDL04N03PR | | - | 0.75 | 1.5 | | V _{LIN} =0, V _{HIN} =3.3 V V _{VSx} =50V |
| Input bias current | 6EDL04I065NR | I _{LIN+} | - | 70 | 100 | μA | V _{LIN} =3.3 V |
| | 6EDL04I065PR 6EDL04N065PR 6EDL04N03PR | | 400 | 700 | 1100 | | |
| Input bias current | 6EDL04I065NR | I _{LIN-} | - | 110 | 200 | μA | V _{LIN} =0 |
| | 6EDL04I065PR 6EDL04N065PR 6EDL04N03PR | | - | 0 | | | |
| Input bias current | 6EDL04I065NR | I _{HIN+} | - | 70 | 100 | μA | V _{HIN} =3.3 V |
| | 6EDL04I065PR 6EDL04N065PR 6EDL04N03PR | | 400 | 700 | 1100 | | |
| Input bias current | 6EDL04I065NR | I _{HIN-} | - | 110 | 200 | μA | V _{HIN} =0 |
| | 6EDL04I065PR 6EDL04N065PR 6EDL04N03PR | | - | 0 | | | |

¹ Not subject of production test, verified by characterisation

Table 6 Static parameters

| Parameter | Symbol | Values | | | Unit | Test condition |
|---|---------------|--------|------|------|---------------|--|
| | | Min. | Typ. | Max. | | |
| Input bias current (ITRIP=high) | I_{ITRIP+} | | 45 | 120 | μA | $V_{ITRIP}=3.3\text{ V}$ |
| Input bias current (EN=high) | I_{EN+} | - | 45 | 120 | | $V_{ENABLE}=3.3\text{ V}$ |
| Input bias current RCIN (internal current source) | I_{RCIN} | | 2.8 | | | $V_{RCIN} = 2\text{ V}$ |
| Mean output current for load capacity charging in range from 3 V (20%) to 6 V (40%) | I_{O+} | 120 | 165 | - | mA | $C_L=10\text{ nF}$ |
| Peak output current turn on (single pulse) | I_{Opk+}^1 | | 240 | | | $R_L = 0\ \Omega, t_p < 10\ \mu\text{s}$ |
| Mean output current for load capacity discharging in range from 12 V (80%) to 9 V (60%) | I_{O-} | 250 | 375 | - | | $C_L=10\text{ nF}$ |
| Peak output current turn off (single pulse) | I_{Opk-}^1 | | 420 | | | $R_L = 0\ \Omega, t_p < 10\ \mu\text{s}$ |
| Bootstrap diode forward voltage between VCC and VB | $V_{F,BSD}$ | - | 1.0 | 1.3 | V | $I_F=0.5\text{ mA}$ |
| Bootstrap diode forward current between VCC and VB | $I_{F,BSD}$ | 40 | 65 | 90 | mA | $V_F=4\text{ V}$ |
| Bootstrap diode resistance | R_{BSD} | 24 | 40 | 60 | Ω | $V_{F1}=4\text{ V}, V_{F2}=5\text{ V}$ |
| RCIN low on resistance of the pull down transistor | $R_{on,RCIN}$ | - | 40 | 100 | | $V_{RCIN}=0.5\text{ V}$ |
| FAULT low on resistance of the pull down transistor | $R_{on,FLT}$ | - | 45 | 100 | | $V_{FAULT}=0.5\text{ V}$ |

4.6 Dynamic parameters

$V_{CC} = V_{BS} = 15\text{ V}$, $V_S = V_{SS} = V_{COM}$ unless otherwise specified. All parameters are valid for $T_a=25\text{ }^\circ\text{C}$.

Table 7 Dynamic parameters

| Parameter | Symbol | Values | | | Unit | Test condition |
|-----------------------------------|----------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Turn-on propagation delay | t_{on} | 360 | 490 | 760 | ns | $V_{LIN/HIN} = 0\text{ or }3.3\text{ V}$ |
| Turn-off propagation delay | t_{off} | 360 | 490 | 760 | | |
| | | 400 | 530 | 800 | | |
| Turn-on rise time | t_r | - | 60 | 100 | ns | $V_{LIN/HIN} = 0\text{ or }3.3\text{ V}$ |
| Turn-off fall time | t_f | - | 26 | 45 | | $C_L = 1\text{ nF}$ |
| Shutdown propagation delay ENABLE | t_{EN} | - | 780 | 1100 | ns | $V_{EN}=0$ |
| Shutdown propagation delay ITRIP | t_{ITRIP} | 400 | 670 | 1000 | | $V_{ITRIP}=1\text{ V}$ |
| Input filter time ITRIP | $t_{ITRIPMIN}$ | 155 | 230 | 380 | | |

¹ Not subject of production test, verified by characterisation

Table 7 Dynamic parameters

| Parameter | Symbol | Values | | | Unit | Test condition |
|--|------------------------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Propagation delay ITRIP to FAULT | t_{FLT} | - | 420 | 700 | | |
| Input filter time at LIN/HIN for turn on and off | t_{FILIN} | 120 | 300 | - | | $V_{LIN/HIN} = 0 \text{ \& } 3.3 \text{ V}$ |
| Input filter time EN | t_{FILEN} | 300 | 600 | - | | |
| Fault clear time at RCIN after ITRIP-fault, ($C_{RCin}=1nF$) | t_{FLTCLR} | 1.0 | 1.9 | 4.0 | ms | $V_{LIN/HIN} = 0 \text{ \& } 3.3 \text{ V}$ $V_{ITRIP} = 0$ |
| Dead time | DT | 150 | 310 | - | ns | $V_{LIN/HIN} = 0 \text{ \& } 3.3 \text{ V}$ |
| Matching delay ON, max(ton)-min(ton), ton are applicable to all 6 driver outputs | MT_{ON} | - | 20 | 100 | | external dead time > 500 ns |
| Matching delay OFF, max(toff)-min(toff), toff are applicable to all 6 driver outputs | MT_{OFF} | - | 40 | 100 | | external dead time >500 ns |
| Output pulse width matching. $PW_{in}-PW_{out}$ | 6EDL04I065NR 6EDL04I065PR | PM | | 40 | 100 | $PW_{in} > 1 \mu s$ |
| | 6EDL04N065PR 6EDL04N03PR | | | 10 | 100 | |

5 Application information

5.1 IGBT / MOSFET gate drive

The 6EDL04 family HVIC is designed to drive MOSFET or IGBT power devices. Figures 9 and 10 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as I_o . The voltage that drives the gate of the external power switch is defined as V_{HO} for the high-side power switch and V_{LO} for the low-side power switch; this parameter is sometimes generically called V_{OUT} and in this case does not differentiate between the high-side or low-side output voltage.

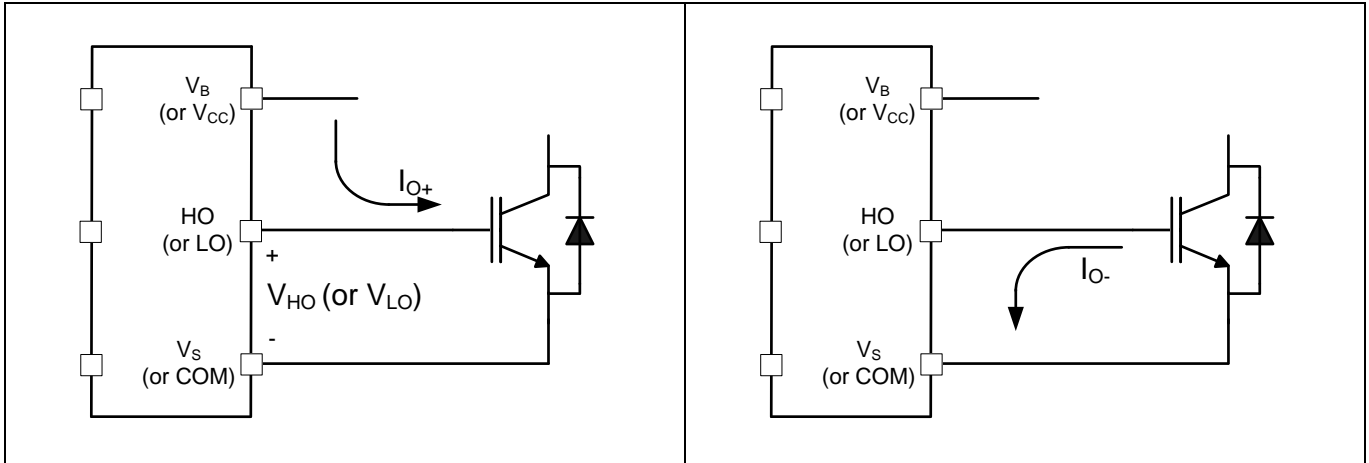


Figure 9 HVIC Sourcing current

Figure 10 HVIC Sinking current

5.2 Switching and timing relationships

The relationships between the input and output signals of the 6EDL04 are illustrated below in Figure 11 and Figure 12. From these figures, we can see the definitions of several timing parameters (i.e. t_{ON} , t_{OFF} , t_R , and t_F) associated with this device, and the interlock function that is used to prevent shoot-through.

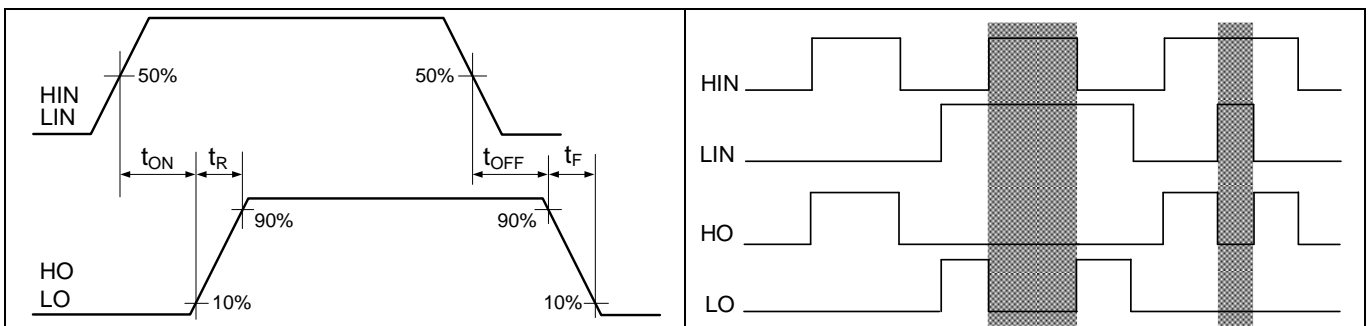


Figure 11 Switching timing diagram

Figure 12 Input/output logic diagram

5.3 Deadtime

This family of HVICs features integrated deadtime protection circuitry. The deadtime is fixed for 6EDL04. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserted whenever the external deadtime is shorter than internal deadtime; external deadtimes larger than internal deadtime are not modified by the gate driver. Figure 13 illustrates the deadtime period and the relationship between the output gate signals.

The deadtime circuitry of 6EDL04 is matched with respect to the high- and low-side outputs. Figure 13 defines the two deadtime parameters (i.e., DT_{LO-HO} and DT_{HO-LO}).

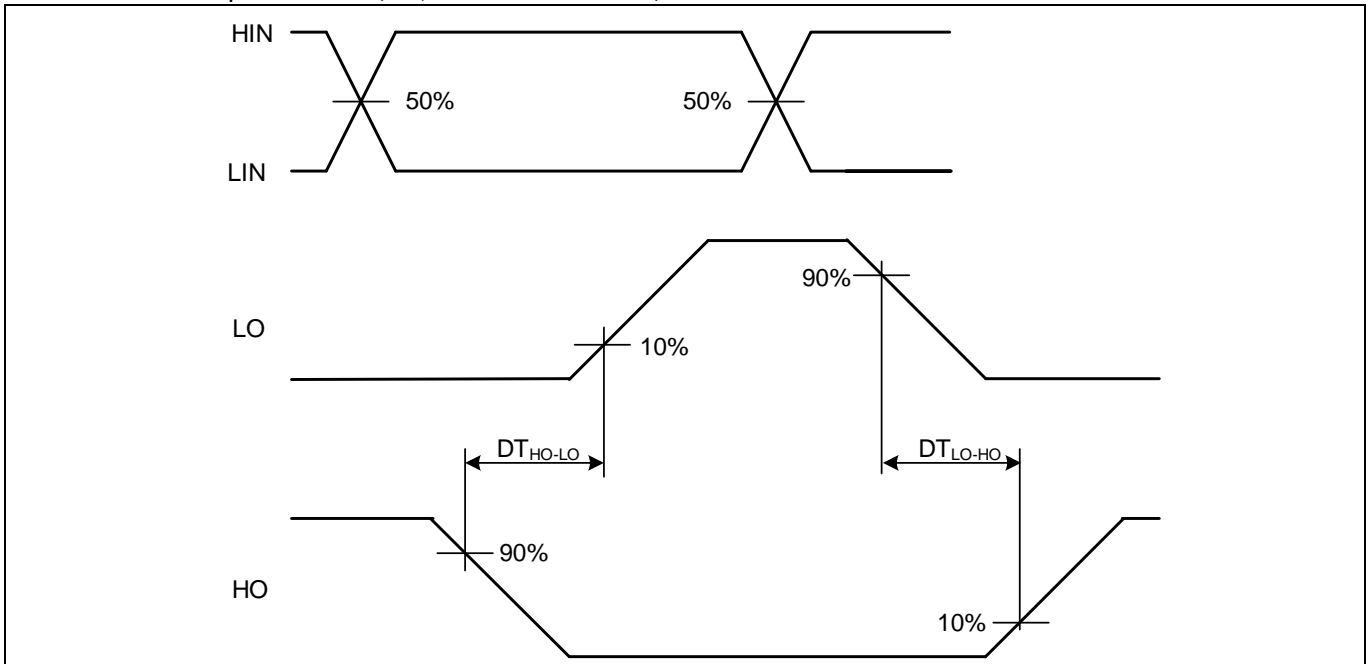


Figure 13 Deadtime matching waveform definition

5.4 Matched propagation delays

The 6EDL04 family is designed with propagation delay matching circuitry across all 6 driver outputs. With this feature, the IC’s response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON} , t_{OFF}) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT_{ON} for turn on, and MT_{OFF} for turn off.)

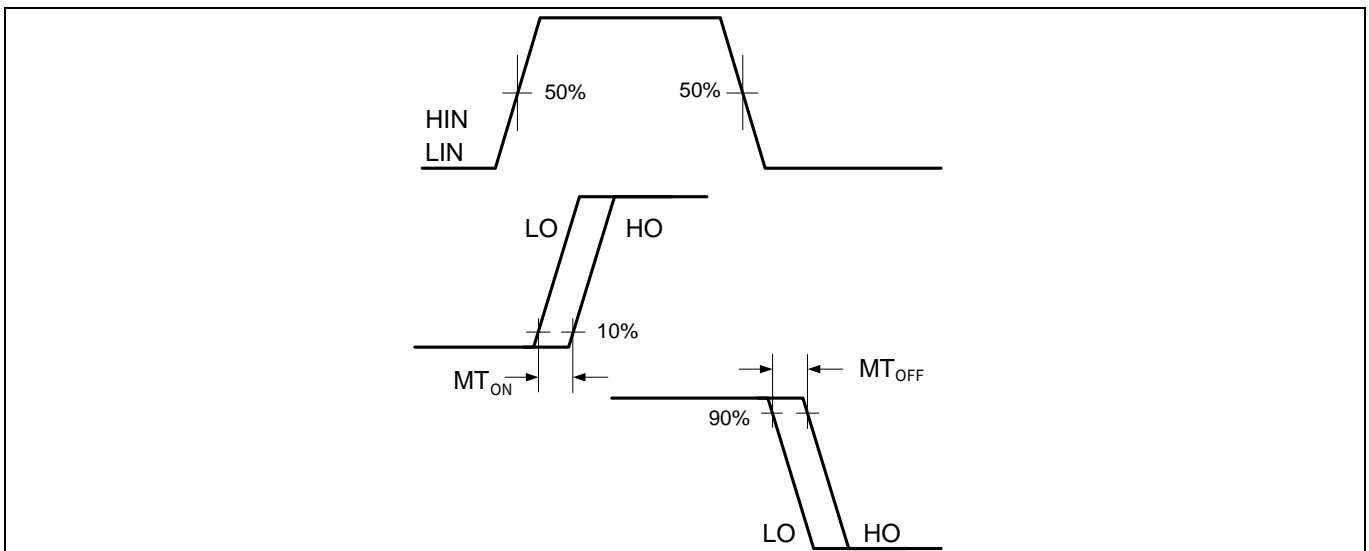


Figure 14 Delay matching waveform definition

5.5 Input logic compatibility

The input pins of are based on a TTL and CMOS compatible input-threshold logic that is independent of the V_{CC} supply voltage. With typical high threshold (V_{IH}) of 2.1 V and typical low threshold (V_{IL}) of 0.9 V, along with very little temperature variation as summarized in Figure 15, the input pins are conveniently driven with logic level

PWM control signals derived from 3.3 V and 5 V digital power-controller devices. Wider hysteresis (typically 0.9 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. 6EDL04 also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The 6EDL04 features floating input protection wherein if any of the input pin is left floating, the output of the corresponding stage is held in the low state. This is achieved using pull-down resistors on all the input pins (HIN, LIN) for positive logic parts, and pull-up resistors for negative logic part as shown in the block diagram.

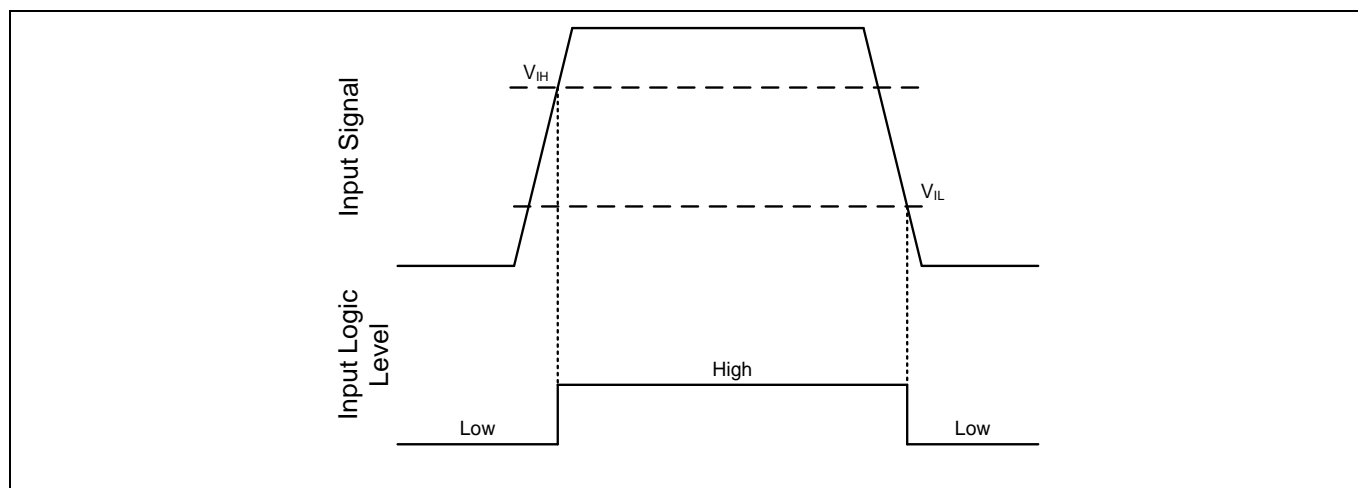


Figure 15 HIN & LIN input thresholds

5.6 Undervoltage lockout

This IC provides undervoltage lockout protection on both the V_{CC} (logic and low-side circuitry) power supply and the V_{BS} (high-side circuitry) power supply. Figure 16 is used to illustrate this concept; V_{CC} (or V_{BS}) is plotted over time and as the waveform crosses the UVLO threshold ($V_{CCUV+/-}$ or $V_{BSUV+/-}$) the undervoltage protection is enabled or disabled.

Upon power-up, should the V_{CC} voltage fail to reach the V_{CCUV+} threshold, the IC won't turn-on. Additionally, if the V_{CC} voltage decreases below the V_{CCUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high and low-side gate drive outputs.

Upon power-up, should the V_{BS} voltage fail to reach the V_{BSUV+} threshold, the IC won't turn-on. Additionally, if the V_{BS} voltage decreases below the V_{BSUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

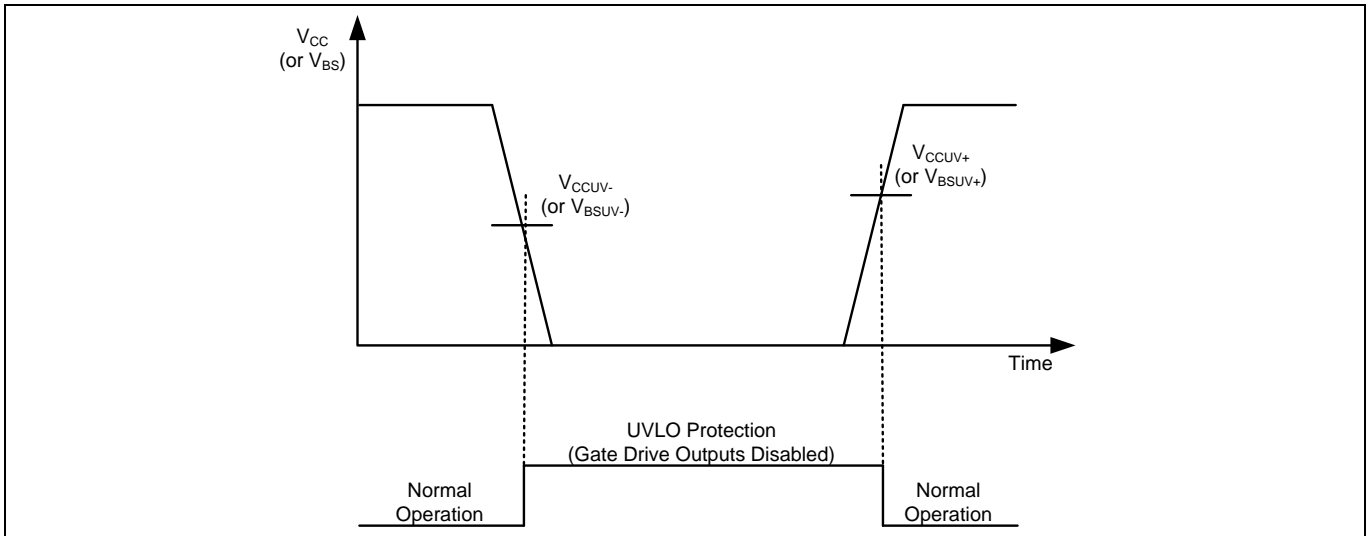


Figure 16 UVLO protection

5.7 Bootstrap diode

An ultra-fast bootstrap diode is monolithically integrated for establishing the high side supply. The differential resistor of the diode helps to avoid extremely high inrush currents when initially charging the bootstrap capacitor. The integrated diode with its resistance helps save cost and improve reliability by reducing external components as shown below Figures 17 and 18.

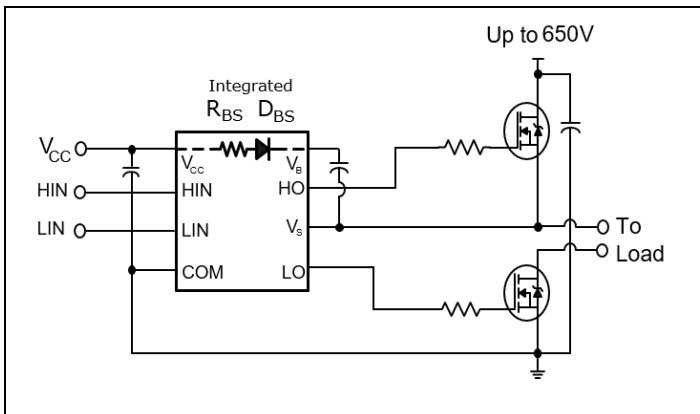


Figure 17 6EDL04 with integrated components

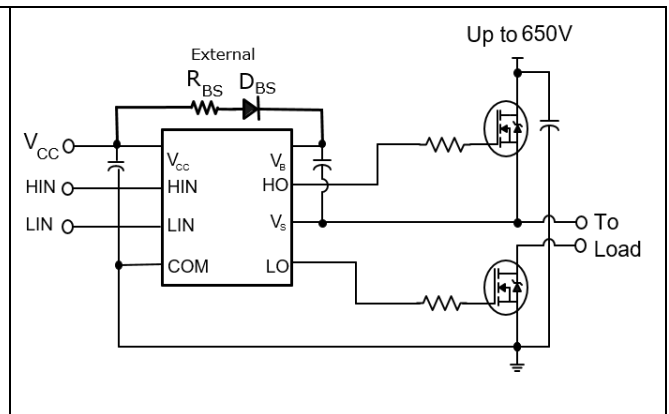


Figure 18 Standard bootstrap gate driver

The low ohmic current limiting resistor provides essential advantages over other competitor devices with high ohmic bootstrap structures. A low ohmic resistor such as in the 6EDL04 allows faster recharging of the bootstrap capacitor during periods of small duty cycles on the low side transistor. The bootstrap diode is usable for all kind power electronic converters. The bootstrap diode is a real pn-diode and is temperature robust. It can be used at high temperatures with a low duty cycle of the low side transistor.

The bootstrap diode of the 6EDL04 works with all control algorithms of modern power electronics, such as trapezoidal or sinusoidal motor drives control.

5.8 Calculating the bootstrap capacitance C_{BS}

Bootstrapping is a common method of pumping charges from a low potential to a higher one. With this technique a supply voltage for the floating high side sections of the gate drive can be easily established according to Figure

19. This method has the advantage of being simple and low cost but may force some limitations on duty-cycle and on-time since they are limited by the requirement to refresh the charge in the bootstrap capacitor. Proper capacitor choice can reduce drastically these limitations.

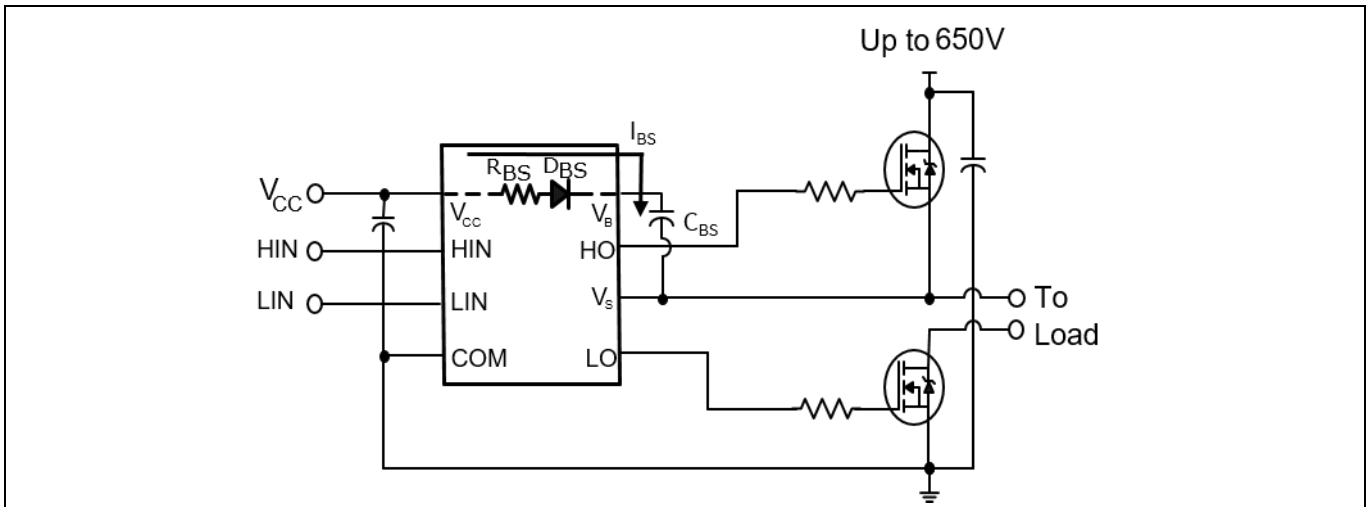


Figure 19 Bootstrap circuit in 6EDL04

When the low side MOSFET turns on, it will force the potential of pin V_S to GND. The existing difference between the voltage of the bootstrap capacitor $V_{C_{BS}}$ and V_{CC} results in a charging current I_{BS} into the capacitor C_{BS} . The current I_{BS} is a pulse current and therefore the ESR of the capacitor C_{BS} must be very small in order to avoid losses in the capacitor that result in lower lifetime of the capacitor. This pin is on high potential again after low side is turned off and high side is conducting current. But now the bootstrap diode D_{BS} blocks a reverse current, so that the charges on the capacitor cannot flow back to the capacitor V_{CC} . The bootstrap diode D_{BS} also takes over the blocking voltage between pin V_B and V_{CC} . The voltage of the bootstrap capacitor can now supply the high side gate drive sections. It is a general design rule for the location of bootstrap capacitors C_{BS} , that they must be placed as close as possible to the IC. Otherwise, parasitic resistors and inductances may lead to voltage spikes, which may trigger the undervoltage lockout threshold of the individual high side driver section. However, all parts of the 6EDL04 family, which have the UVLO also contain a filter at each supply section in order to actively avoid such undesired UVLO triggers.

The current limiting resistor R_{BS} according to Figure 19 reduces the peak of the pulse current during the low side MOSFET turn-on. The pulse current will occur at each turn-on of the low side MOSFET, so that with increasing switching frequency the capacitor C_{BS} is charged more frequently. Therefore a smaller capacitor is suitable at higher switching frequencies. The bootstrap capacitor is mainly discharged by two effects: The high side quiescent current and the gate charge of the high side MOSFET to be turned on.

The minimum size of the bootstrap capacitor is given by

$$C_{BS} = \frac{Q_{GTOT}}{\Delta V_{BS}}$$

ΔV_{BS} is the maximum allowable voltage drop at the bootstrap capacitor within a switching period, typically 1 V. It is recommended to keep the voltage drop below the undervoltage lockout (UVLO) of the high side and limit

$$\Delta V_{BS} \leq (V_{CC} - V_F - V_{GSmin} - V_{Dson})$$

$V_{GSmin} > V_{BSUV-}$, V_{GSmin} is the minimum gate source voltage we want to maintain and V_{BSUV-} is the high-side supply undervoltage negative threshold.

V_{CC} is the IC voltage supply, V_F is bootstrap diode forward voltage and V_{Dson} is drain-source voltage of low side MOSFET.

Please note, that the value Q_{TOT} may vary to a maximum value based on different factors as explained below and the capacitor shows voltage dependent derating behavior of its capacitance.

The influencing factors contributing V_{BS} to decrease are:

- MOSFET turn on required Gate charge (Q_G)
- MOSFET gate-source leakage current (I_{LK_GS})
- Floating section quiescent current (I_{QBS})
- Floating section leakage current (I_{LK})
- Bootstrap diode leakage current (I_{LK_DIODE})
- Charge required by the internal level shifters (Q_{LS}): typical 1nC
- Bootstrap capacitor leakage current (I_{LK_CAP})
- High side on time (T_{HON})

Considering the above,

$$Q_{TOT} = Q_G + Q_{LS} + (I_{QBS} + I_{LK_GS} + I_{LK} + I_{LK_DIODE} + I_{LK_CAP}) * T_{HON}$$

I_{LK_CAP} is only relevant when using an electrolytic capacitor and can be ignored if other types of capacitors are used. It is strongly recommend using at least one low ESR ceramic capacitor (paralleling electrolytic capacitor and low ESR ceramic capacitor may result in an efficient solution).

The above C_{BS} equation is valid for pulse by pulse considerations. It is easy to see, that higher capacitance values are needed, when operating continuously at small duty cycles of low side. The recommended bootstrap capacitance is therefore in the range up to 4.7 μF for most switching frequencies. The performance of the integrated bootstrap diode supports the requirement for small bootstrap capacitances.

5.9 Negative voltage transient tolerance of VS pin

A common problem in today’s high-power switching converters is the transient response of the switch node’s voltage as the power switches transition on and off quickly while carrying a large current. A typical 3-phase inverter circuit is shown in Figure 20, here we define the power switches and diodes of the inverter.

If the high-side switch (e.g., the IGBT Q1 in Figures 21 and 22) switches from on to off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1} , swings from the positive DC bus voltage to the negative DC bus voltage.

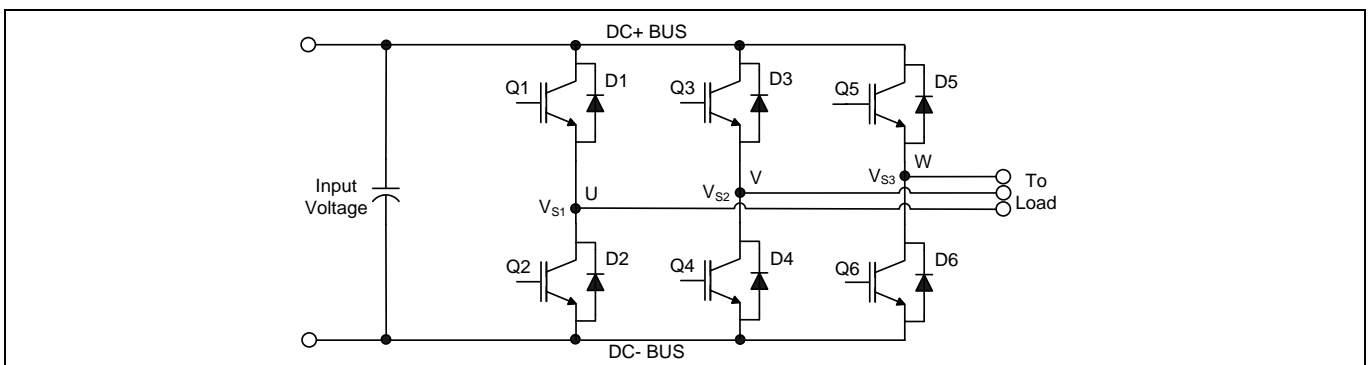


Figure 20 Three-phase inverter

Also when the V phase current flows from the inductive load back to the inverter (see Figures 21 C) and D)), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2} , swings from the positive DC bus voltage to the negative DC bus voltage.

However, in a real inverter circuit, the VS voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called “negative V_S transient”

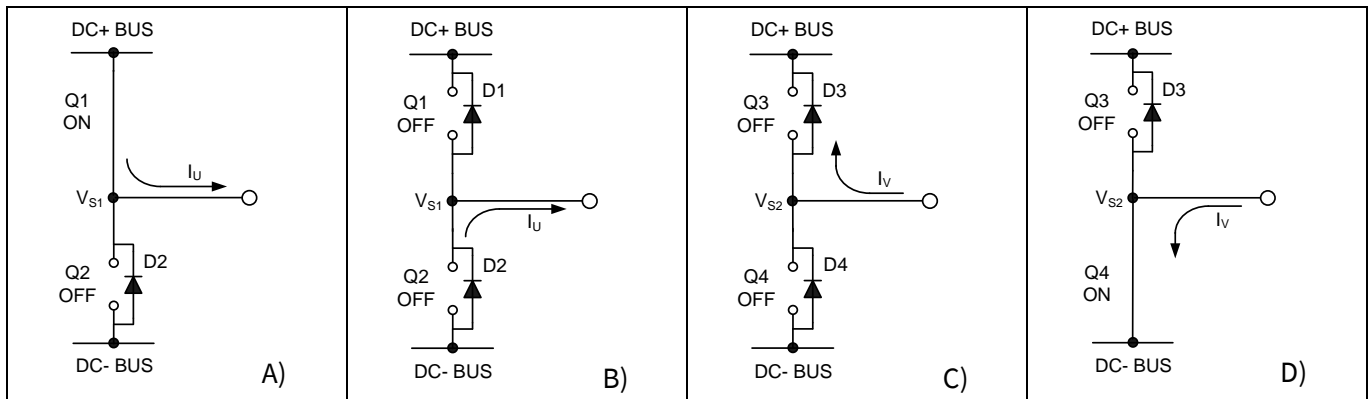


Figure 21 A) Q1 conducting B) D2 conducting C) D3 conducting D) Q4 conducting

The circuit shown in Figure 22-A depicts one leg of the three-phase inverter; Figures 22-B and 22-C show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

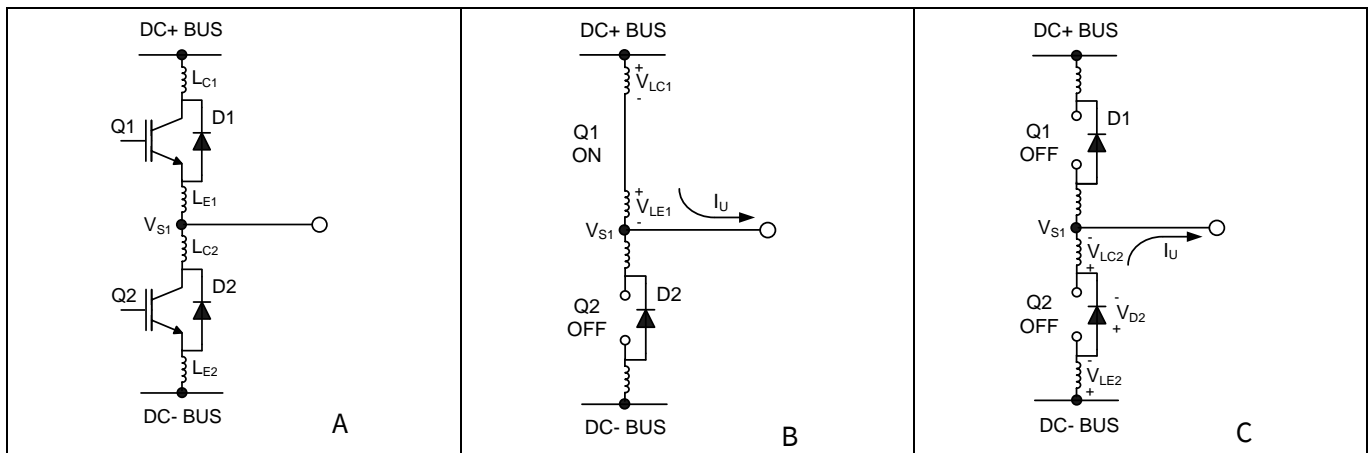


Figure 22 Figure A shows the Parasitic Elements. Figure B shows the generation of V_S positive. Figure C shows the generation of V_S negative

5.10 NTSOA – Negative Transient Safe Operating Area

In a typical motor drive system, dV/dt is typically designed to be in the range of 3 – 5 V / ns. The negative V_S transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

Infineon’s HVICs have been designed for the robustness required in many of today’s demanding applications. An indication of the 6EDL04’s robustness can be seen in Figure 23, where the 6EDL04’s Safe Operating Area is shown at $V_{BS}=15V$ based on repetitive negative V_S spikes. A negative V_S transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; viceversa unwanted functional anomalies or permanent damage to the IC do not appear if negative V_S transients fall inside the SOA.

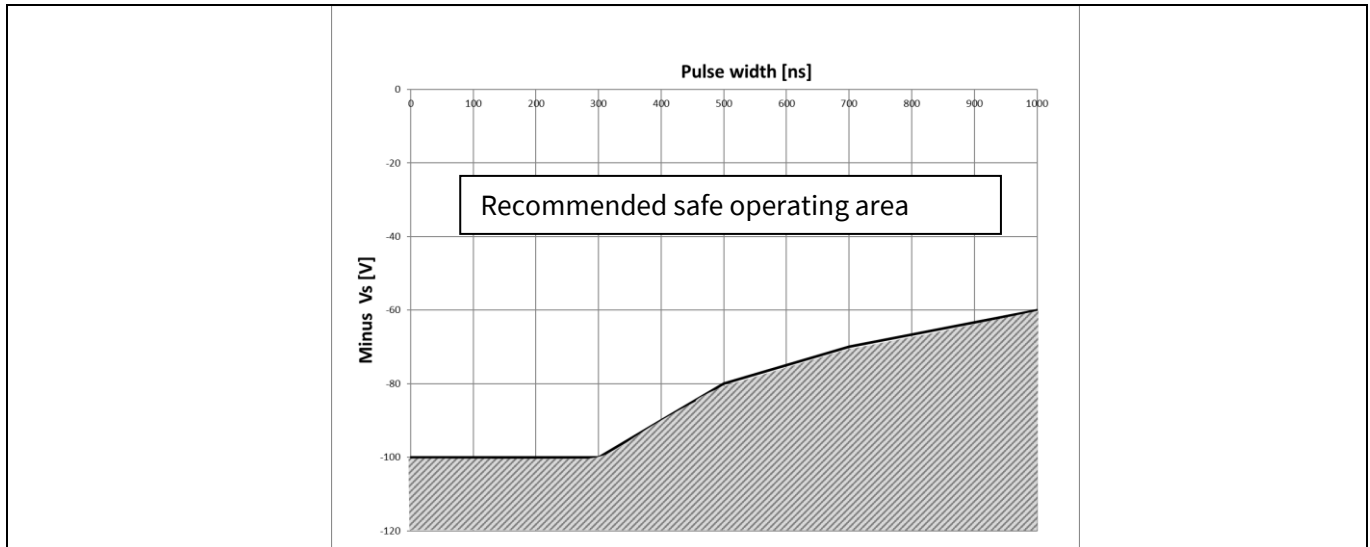


Figure 23 Negative VS transient SOA for 6EDL04 @ VBS=15 V

Even though the 6EDL04 has been shown able to handle these large negative VS transient conditions, it is highly recommended that the circuit designer always limit the negative VS transients as much as possible by careful PCB layout and component use.

5.11 Maximum switching frequency

The 6EDL04 is capable of switching at higher frequencies as compared to standard three-phase gate drivers. They are available in PG-DSO-8 package. It is essential to ensure that the component is not thermally overloaded when operating at higher frequencies. This can be checked by means of the thermal resistance junction to ambient and the calculation or measurement of the dissipated power. The thermal resistance is given in the datasheet (section 4) and refers to a specific layout. Changes of this layout may lead to an increased thermal resistance, which will reduce the total dissipated power of the driver IC. One should therefore do temperature measurements in order to avoid thermal overload under application relevant conditions of ambient temperature and housing.

The maximum chip temperature T_J can be calculated with

$$T_J = P_d \cdot R_{thJA} + T_{A,max}, \text{ where } T_{A,max} \text{ is the maximum ambient temperature.}$$

The dissipated power P_d by the driver IC is a combination of several sources. These are explained in detail in the application note “Advantages of Infineon’s Silicon on Insulator (SOI) technology based High Voltage Gate Driver ICs (HVICs)”.

5.12 Creepage

The clearance distance of the PG-TSSOP-25 package is 1.0mm according to the package drawing. It depends on the individual application standard, such as IEC 60335-1, as well as the application conditions, such as pollution degree, etc. to identify the relevant requirements for the system.

The mentioned standards and similar ones describe in detail the relevant considerations for an appropriate calculation of the creepage distance for the target system.

5.13 PCB layout tips

Distance between high and low voltage components: It’s strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device. Please see the Case Outline information in this datasheet for the details.

Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 21). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

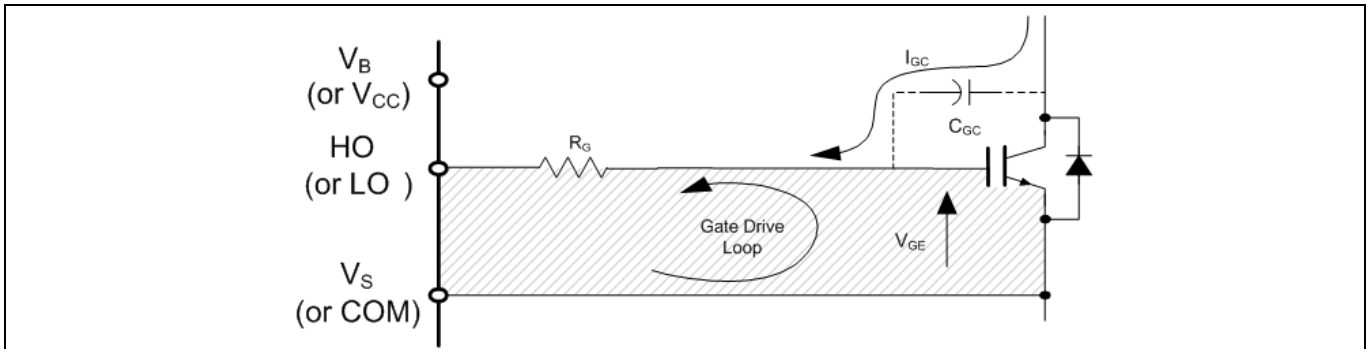
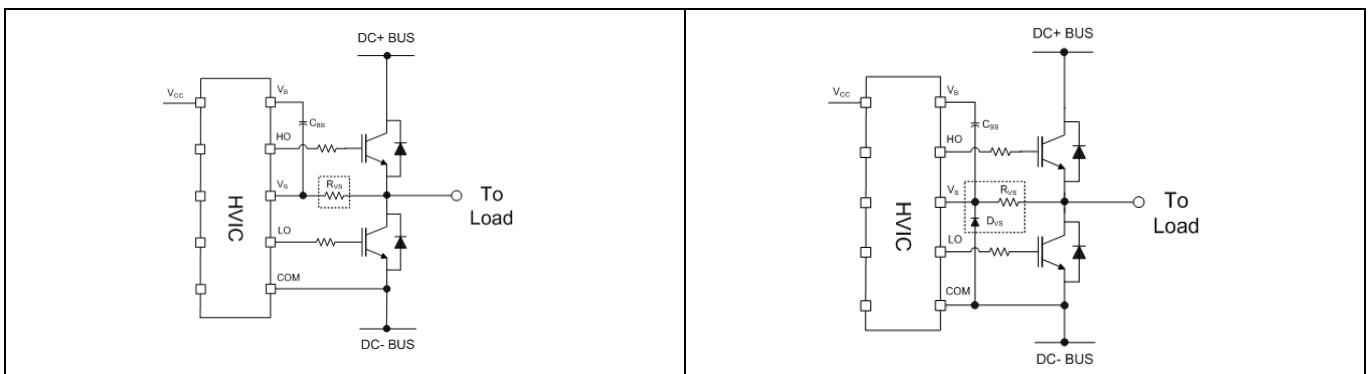


Figure 24 Avoid antenna loops

Supply Capacitor: It is recommended to place a bypass capacitor (C_{IN}) between the V_{CC} and COM pins. A ceramic $1\mu F$ ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative V_S spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor ($5\ \Omega$ or less) between the V_S pin and the switch node (see Figure 23 - A), and in some cases using a clamping diode between COM and V_S (see Figure 23 - B). See Design Tip DT04-4 “[Using Monolithic High Voltage Gate Drivers](http://www.infineon.com)” at www.infineon.com for more detailed explanations.



Resistor between the V_S pin and the switch node and clamping diode between COM and V_S

6 Timing diagrams

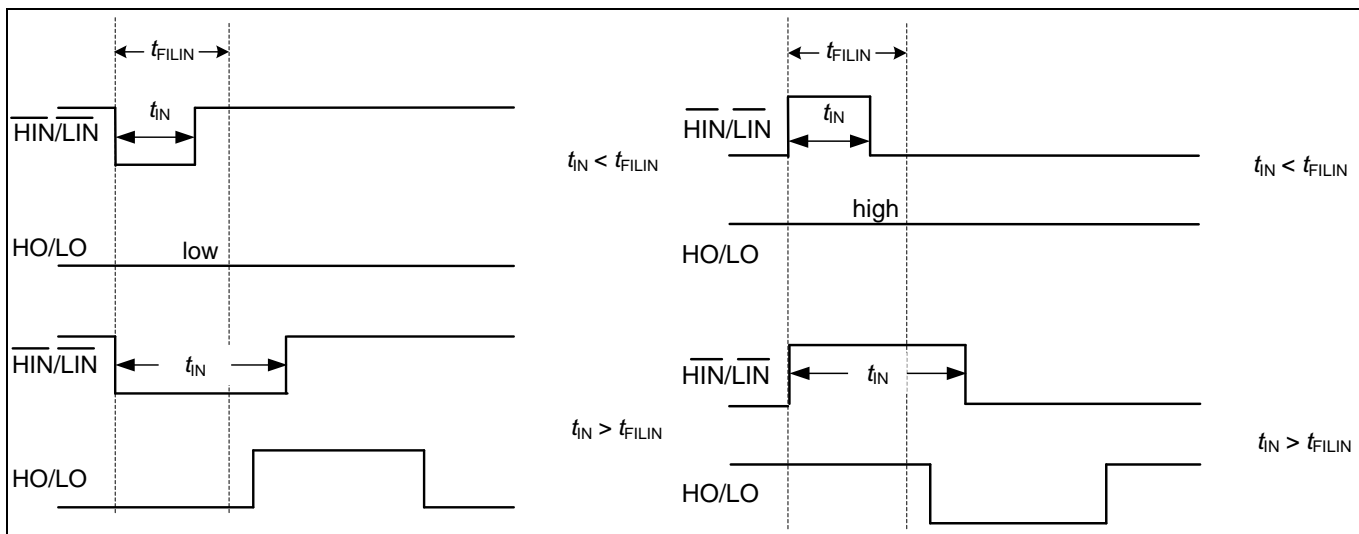


Figure 25 Timing of short pulse suppression (6EDL04I065NR)

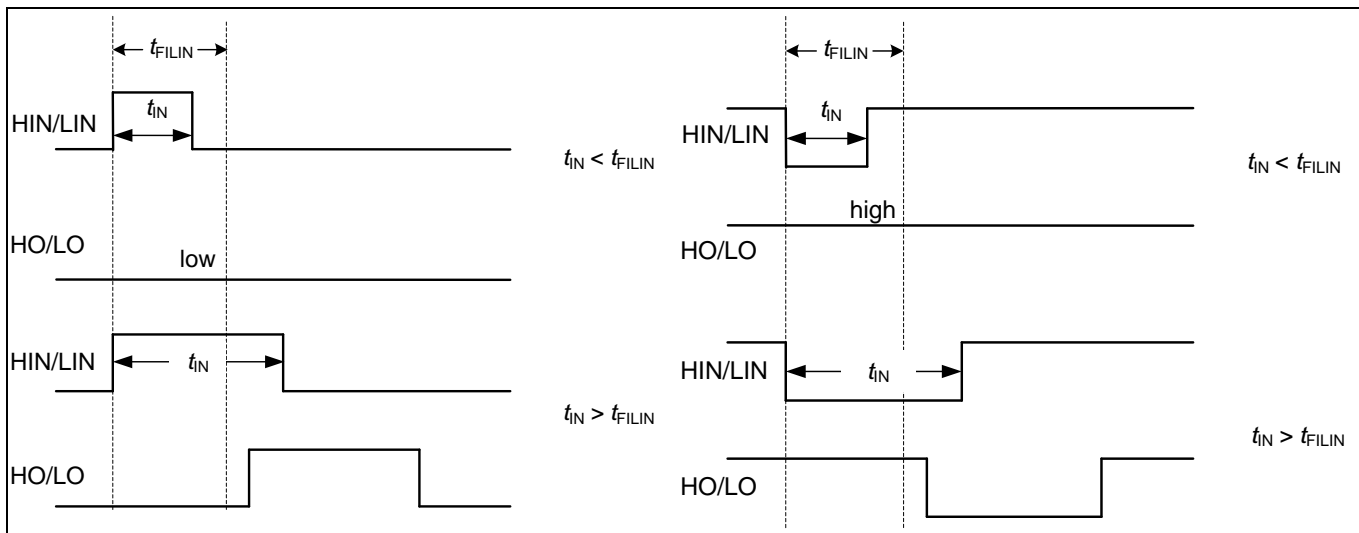


Figure 26 Timing of short pulse suppression (6EDL04I065PR, 6EDL04N065PR and 6EDL04N03PR)

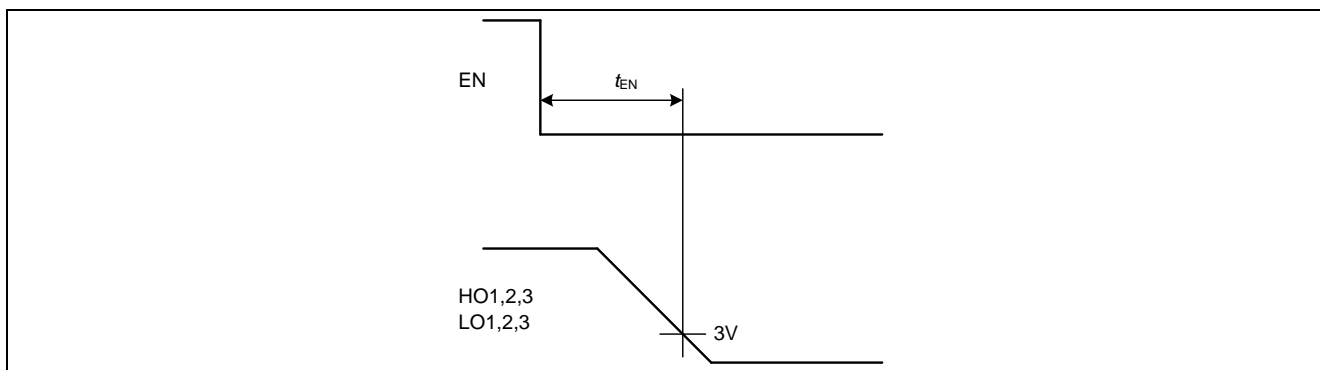


Figure 27 Enable delay time definition

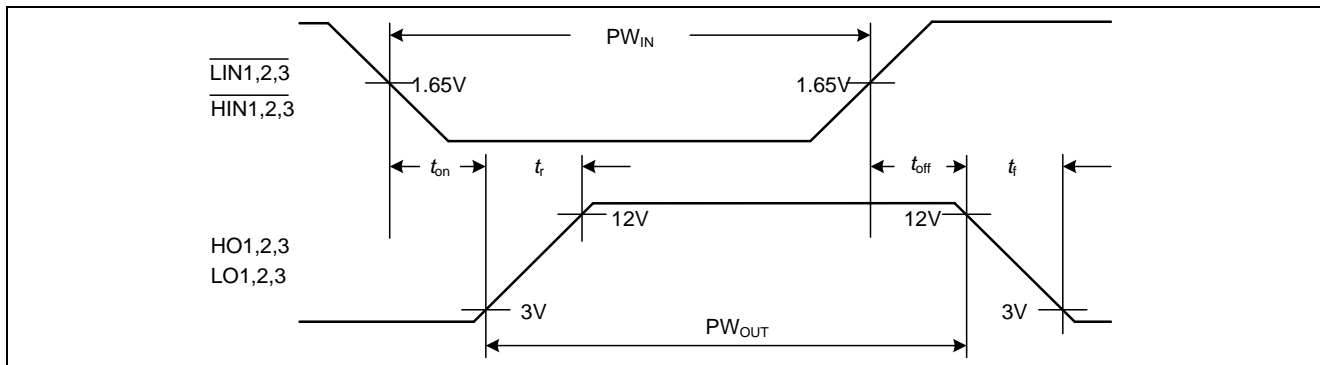


Figure 28 Input to output propagation delay times and switching times definition (6EDL04I065NR)

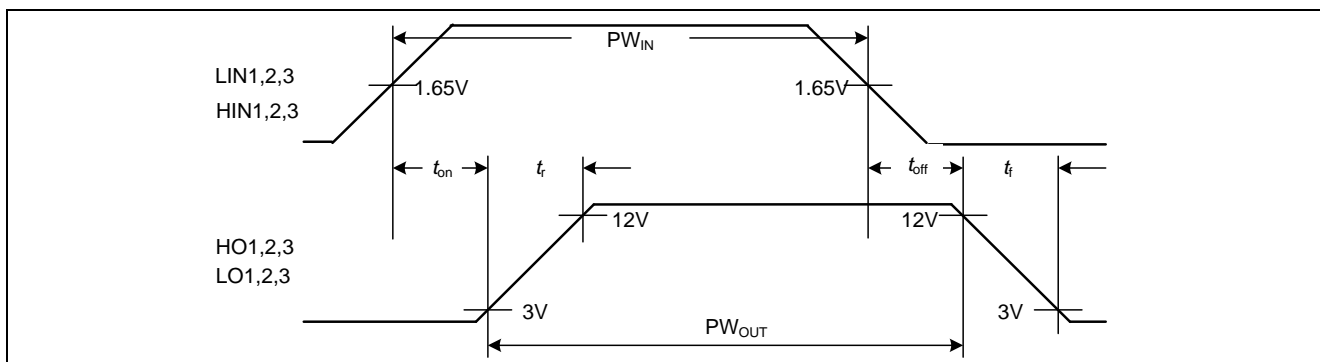


Figure 29 Input to output propagation delay times and switching times definition (6EDL04I065PR, 6EDL04N065PR and 6EDL04N03PR)

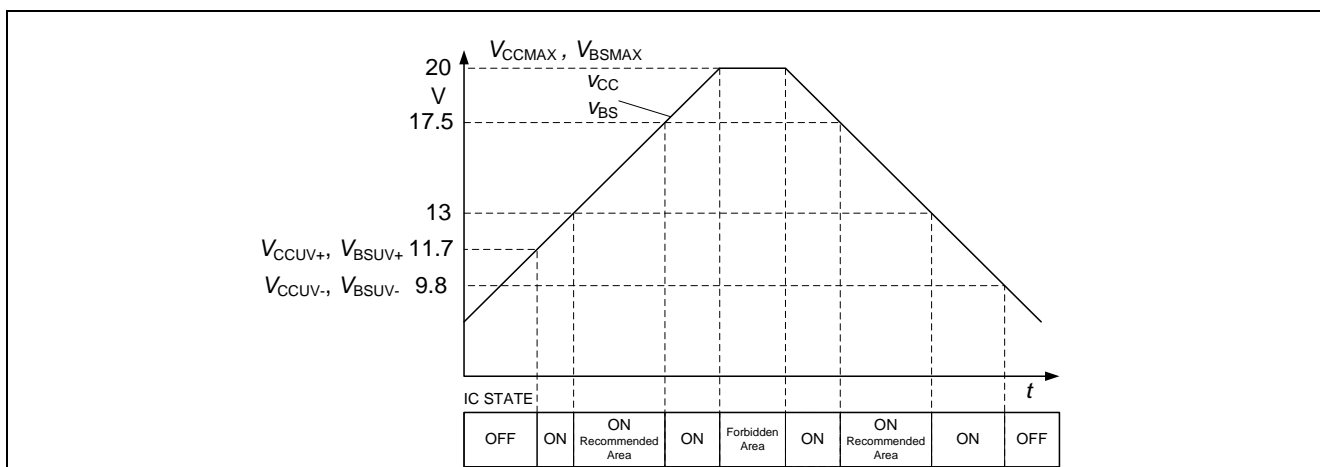


Figure 30 Operating areas (6EDL04I065NR, 6EDL04I065PR)

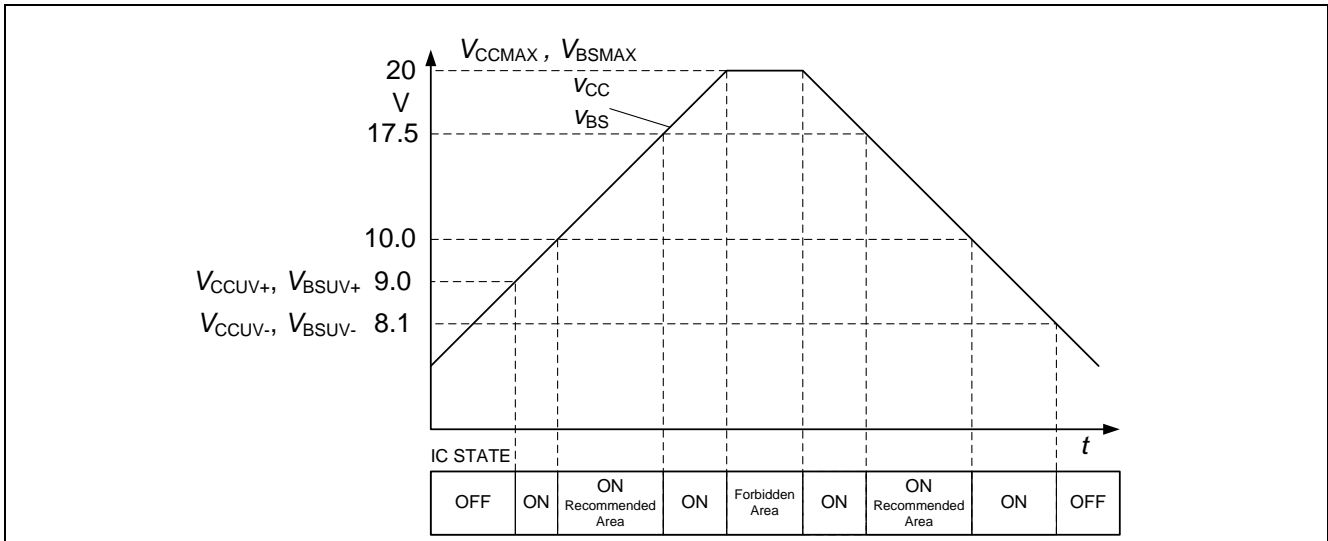


Figure 31 Operating areas (6EDL04N065PR, 6EDL04N03PR)

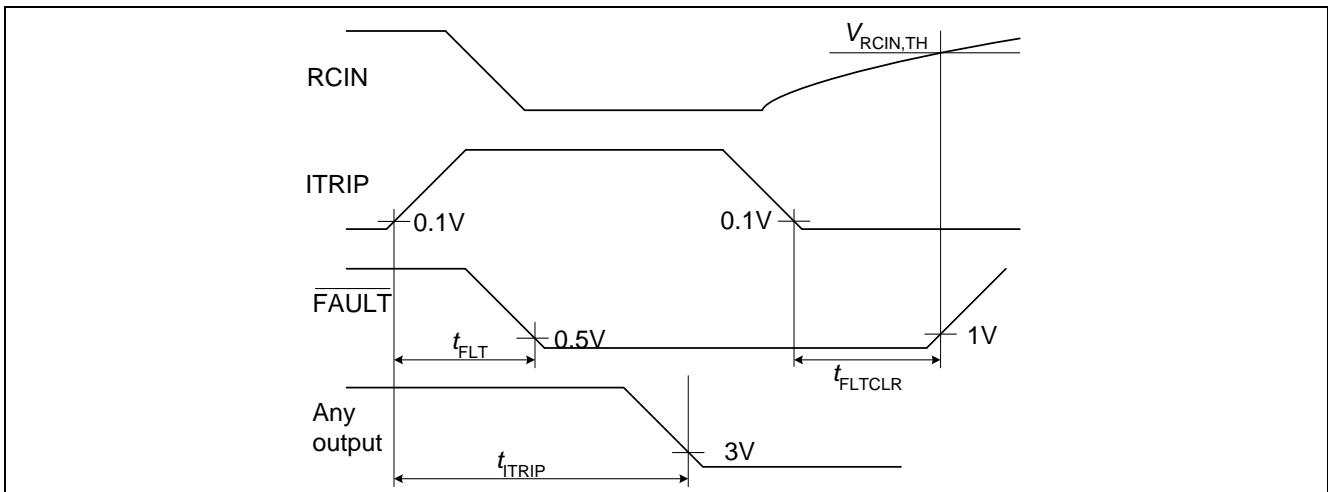


Figure 32 ITRIP timing

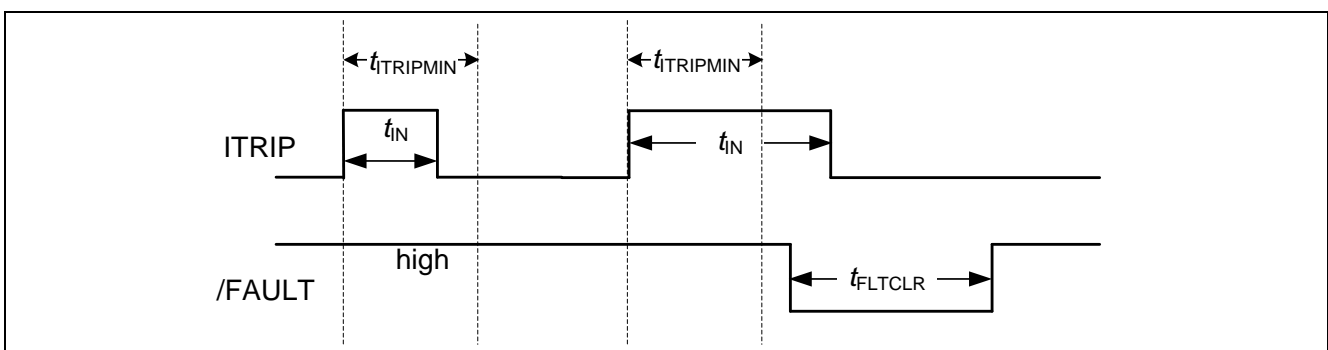


Figure 33 ITRIP input timing

7 Qualification information¹

Table 8 Qualification information

| | | Industrial ² |
|-----------------------------------|----------------------|--|
| Qualification level | | Note: This family of ICs has passed JEDEC's Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level. |
| Moisture sensitivity level | | MSL ³ , 260°C (per IPC/JEDEC J-STD-020) |
| ESD | Charged device model | Class C3 (1.0 kV) (per ANSI/ESDA/JEDEC JS-002-2018) |
| | Human body model | Class 2 (2.0 kV) (per ANSI/ESDA/JEDEC JS-001-2017) |
| RoHS compliant | | Yes |

¹ Qualification standards can be found at Infineon's web site www.infineon.com

² Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.

³ Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon sales representative for further information.

8 Related products

Table 9

| Gate Driver ICs | |
|---|--|
| 2EDL05I06 / 2EDL05N06 | 600 V, half-bridge thin-film SOI level shift gate driver with integrated high speed, low $R_{DS(ON)}$ bootstrap diode, 0.36/0.7 A source/sink current driver, 8pins/14pins package, for MOSFET or IGBT. |
| 2EDL23I06 / 2EDL23N06 | 600 V, half-bridge thin-film SOI level shift gate driver with integrated high speed, low $R_{DS(ON)}$ bootstrap diode, with over-current protection (OCP), 2.3/2.8 A source/sink current driver, and one pin Enable/Fault function for MOSFET or IGBT. |
| Power Switches | |
| IKD06N60RC2 | 600 V, 6 A IGBT Discrete with Reverse Conducting Drive 2-diode in TO-252 package |
| IPN60R1K0PFD7S | 600V CoolMOS™ PFD7 superjunction MOSFET in SOT-223 |
| iMOTION™ Controllers | |
| IRMCK099 | iMOTION™ Motor control IC for variable speed drives utilizing sensor-less Field Oriented Control (FOC) for Permanent Magnet Synchronous Motors (PMSM). |
| IMC101T | High performance Motor Control IC for variable speed drives based on field oriented control (FOC) of permanent magnet synchronous motors (PMSM). |

9 Package information

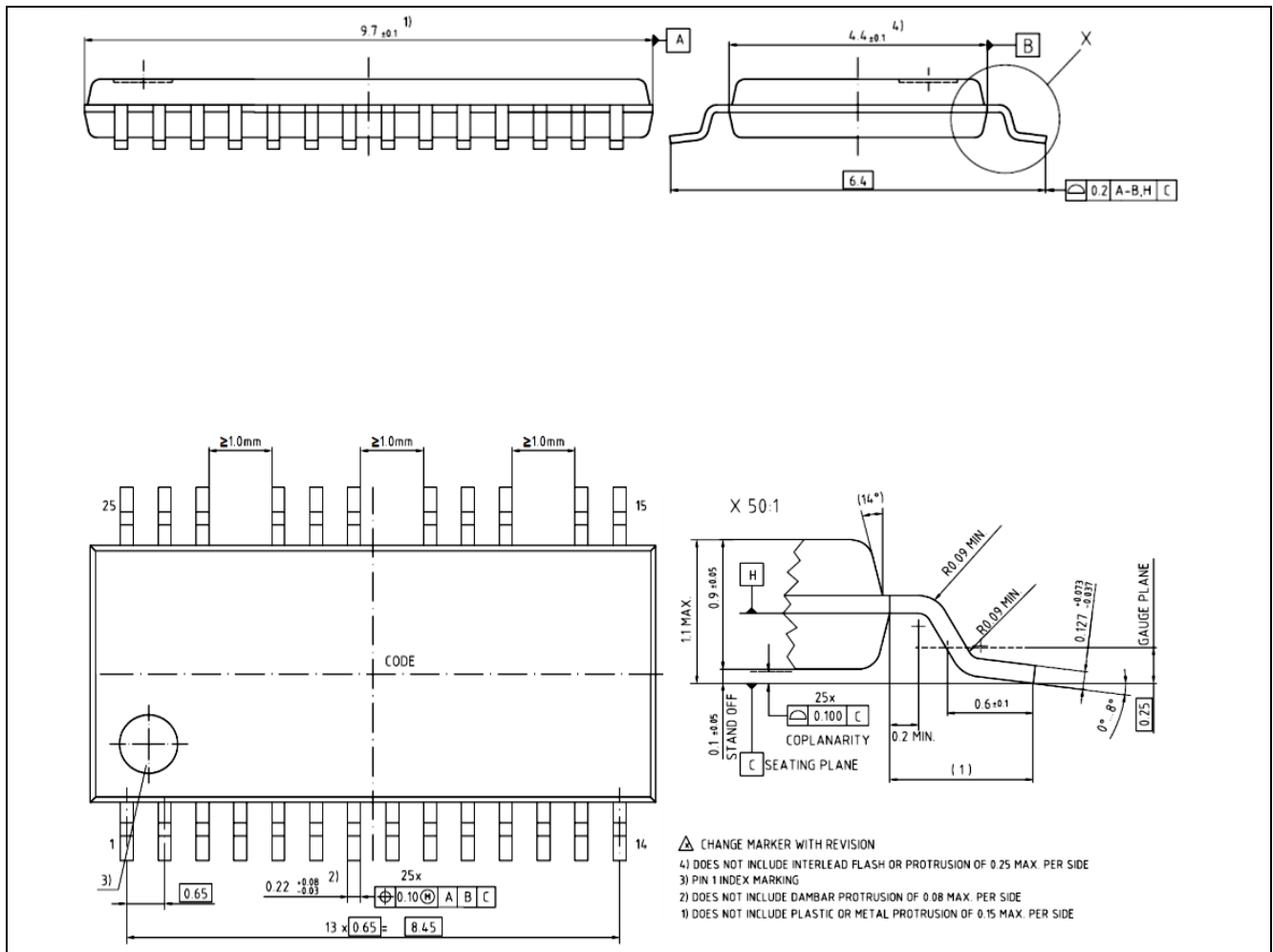


Figure 34 PG-TSSOP-25 package drawing

10 Part marking information

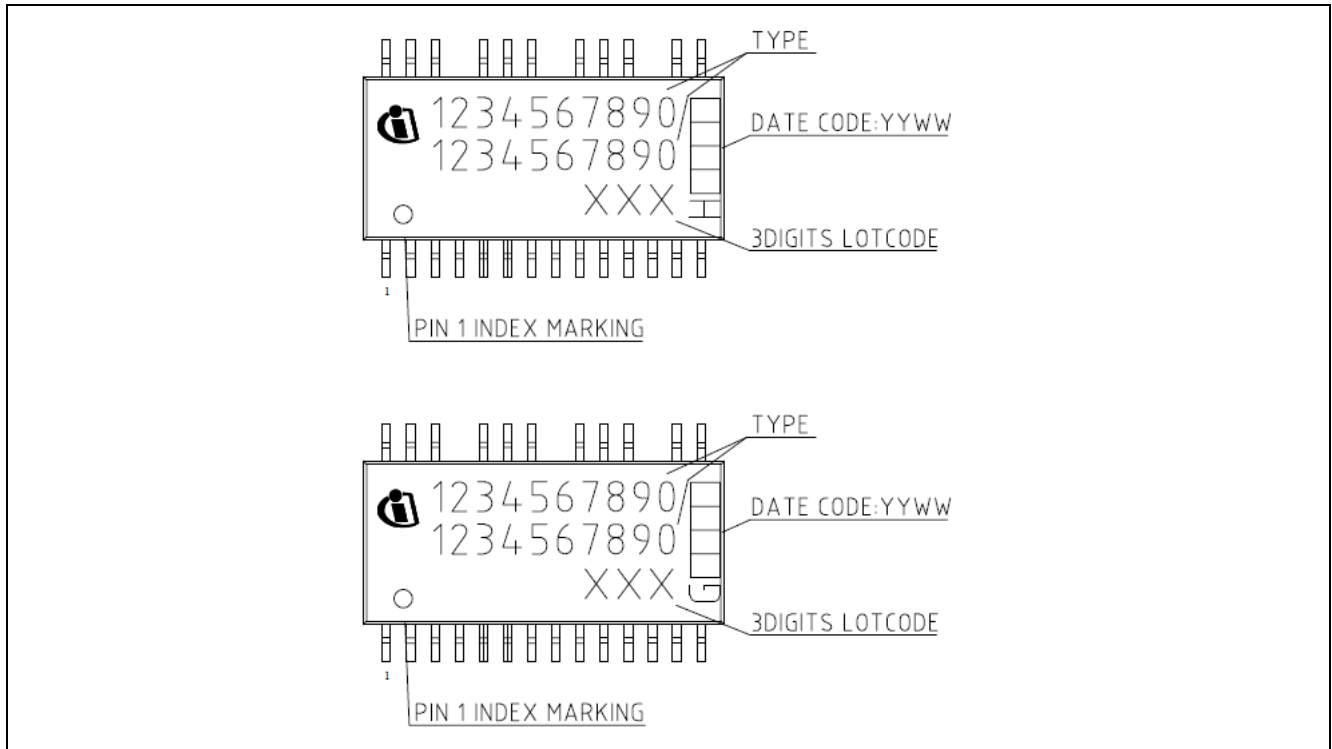


Figure 35 PG-TSSOP-25 marking information

11 Additional documentation and resources

Several technical documents related to the use of HVICs are available at www.infineon.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

Application Notes:

[Understanding HVIC Datasheet Specifications](#)

[HV Floating MOS-Gate Driver ICs](#)

[Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and IGBTs](#)

[Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality](#)

Design Tips:

[Using Monolithic High Voltage Gate Drivers](#)

[Alleviating High Side Latch on Problem at Power Up](#)

[Keeping the Bootstrap Capacitor Charged in Buck Converters](#)

[Managing Transients in Control IC Driven Power Stages](#)

[Simple High Side Drive Provides Fast Switching and Continuous On-Time](#)

11.1 Infineon online forum resources

The Gate Driver Forum is live at Infineon Forums (www.infineonforums.com). This online forum is where the Infineon gate driver IC community comes to the assistance of our customers to provide technical guidance – how to use gate drivers ICs, existing and new gate driver information, application information, availability of demo boards, online training materials for over 500 gate driver ICs. The Gate Driver Forum also serves as a repository of FAQs where the user can review solutions to common or specific issues faced in similar applications.

Register online at the Gate Driver Forum and learn the nuances of efficiently driving a power switch in any given power electronic application.



12 Revision history

| Document version | Date of release | Description of changes |
|------------------|-----------------|------------------------|
| 2.0 | 2024-10-11 | Final datasheet. |
| | | |
| | | |
| | | |

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