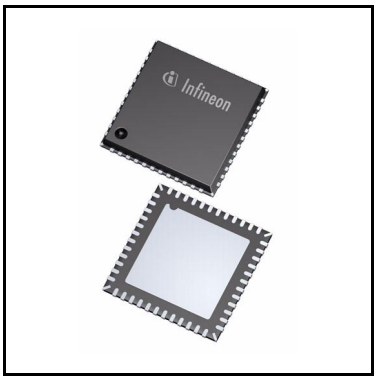
TLE9278-3BQX V33

Multi-CAN Power+ System Basis Chip



1 Overview

Features

- SMPS with integrated switches up to 750 mA (DC/DC buck) with 3.3 V output voltage
- DC/DC Boost converter for low V_{sup} supply voltage with integrated switch at 6.5 V, 8 V, 10 V and 12 V
- Low-Drop Voltage Regulator with external PNP device with configurable 5.0 V, 3.3 V, 1.8 V and 1.2 V output voltage, protected for off-board usage
- Very low quiescent current consumption in Stop and Sleep Mode
- Four CAN Transceivers compliant to CAN Flexible Data-rate (FD)
- ISO 11898-2: 2016 standard up to 5 Mb
- Partial Networking (PN) support
- One universal High-Voltage Wake Input for voltage level monitoring including wake up capability
- Cyclic wake feature via an integrated timer
- Reset Output to ensure stable supply to the MCU
- Fail Output to activate external load in case of system malfunctions are detected
- Output voltage supervision functions in all output supply voltages
- Fast Battery Voltage Monitoring Feature
- 16-bit Serial Perpheral Interface (SPI)
- Overtemperature and short circuit protection feature
- Wide input voltage and temperature range
- Software Compatibility to other SBC family members for the TLE926x and TLE927x families
- Green Product (RoHS compliant) & AEC Qualified
- 7 × 7 mm PG-VQFN-48 package

Potential applications

- Gateways
- Body control modules
- Driver assistance
- Chasis control

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

Description

Infineon's TLE9278-3BQX V33 offers the highest level of integration at smallest footprint for automotive applications requiring multiple channels of CAN transceivers like gateways and high-end Body Control Modules (BCM). A high-efficient Switch Mode Power Supply (SMPS) buck regulator provides an external 3.3 V output voltage at up to 750 mA while an additional DC/DC boost converter supports applications or conditions at low supply input voltages. The device is controlled and monitored via a 16-bit Serial Peripheral Interface (SPI). Additional features include a time-out/window watchdog circuit with reset, fail output and undervoltage reset. The device offers low-power modes in order to support applications that are connected permanently to the battery. A wake-up from the low-power mode is possible via a message on the buses, via the bi-level sensitive monitoring/wake-up input as well as via the timer. The TLE9278-3BQX V33 is offered in a very small footprint, exposed pad PG-VQFN-48 (7 × 7 mm) power package.

Type	Package	Marking
TLE9278-3BQX V33	PG-VQFN-48	TLE9278-3BQXV33

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2 Block Diagram

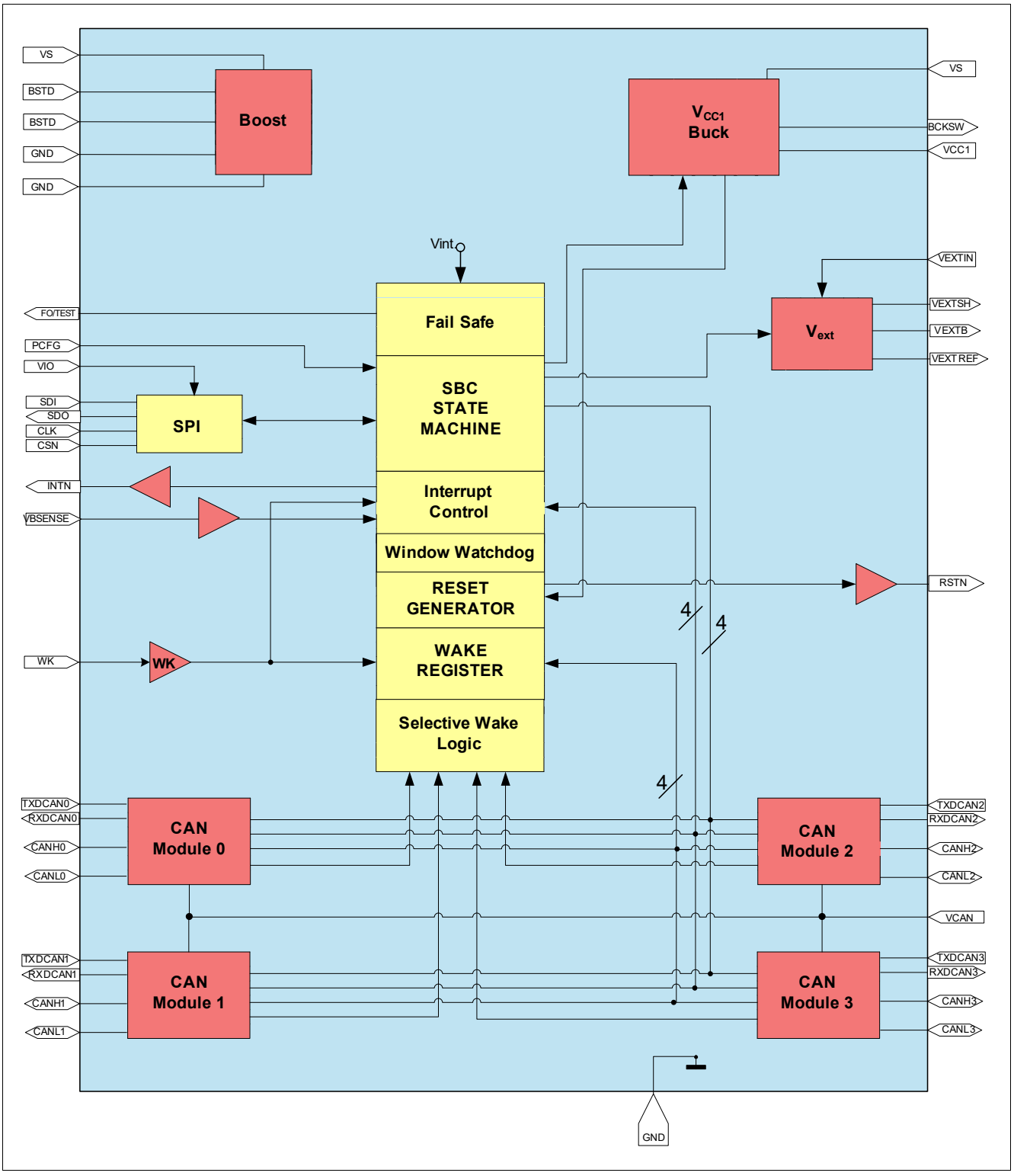


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

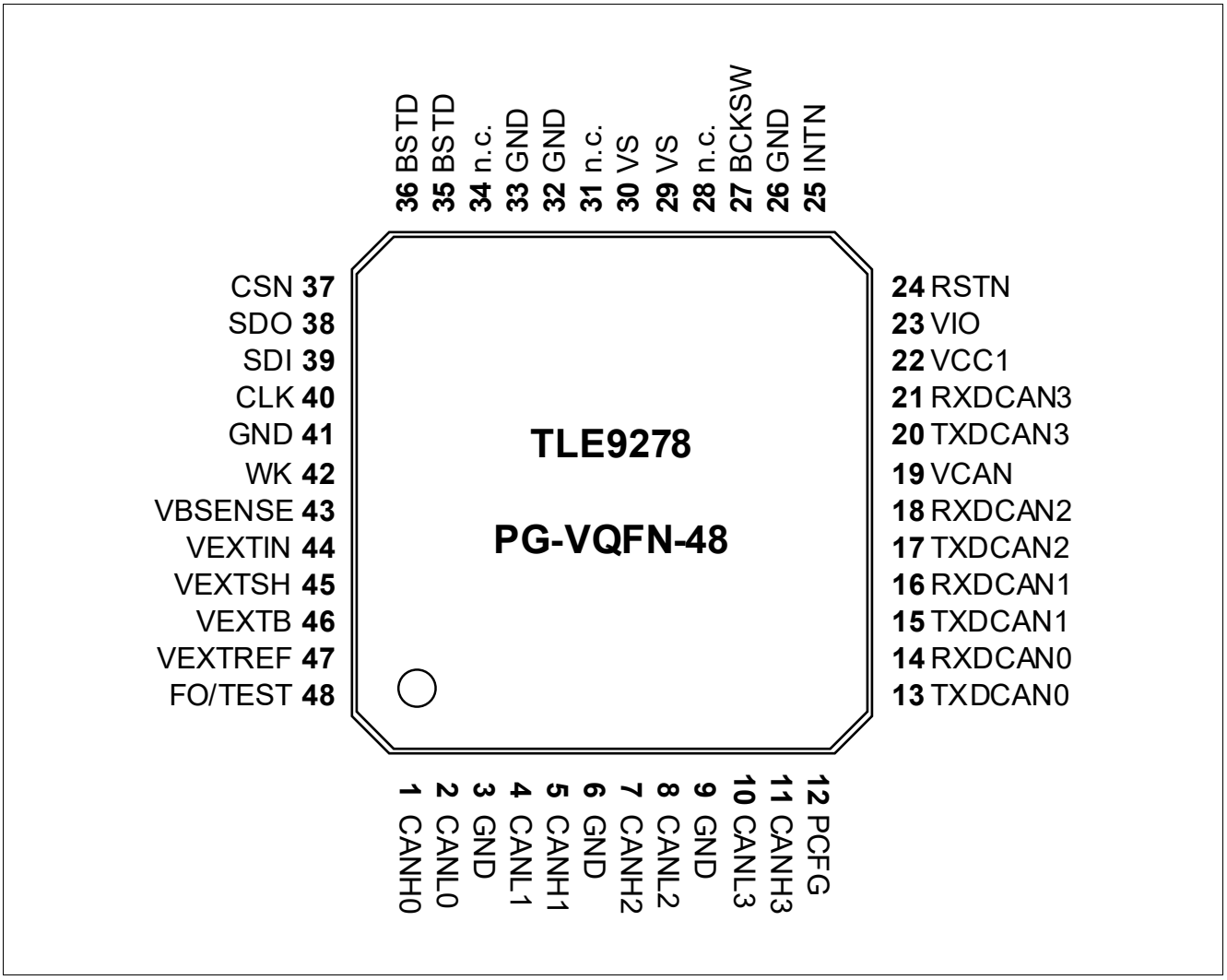


Figure 2 Pin Configuration TLE9278-3BQX V33

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	CANH0	**CAN High 0 Bus Pin.**
2	CANL0	**CAN Low 0 Bus Pin.**
3	GND	Ground. CAN0 and CAN1 common ground.
4	CANL1	**CAN Low 1 Bus Pin.**
5	CANH1	**CAN High 1 Bus Pin.**
6	GND	**Ground.** Analog GND.
7	CANH2	**CAN High 2 Bus Pin.**
8	CANL2	**CAN Low 2 Bus Pin.**
9	GND	Ground. CAN2 and CAN3 common ground.
10	CANL3	**CAN Low 3 Bus Pin.**
11	CANH3	**CAN High 3 Bus Pin.**
12	PCFG	Configuration pin. For power up hardware configuration (refer to **Chapter 5.1.1**).
13	TXDCAN0	**Transmit CAN0.**
14	RXDCAN0	**Receive CAN0.**
15	TXDCAN1	**Transmit CAN1.**
16	RXDCAN1	**Receive CAN1.**
17	TXDCAN2	**Transmit CAN2.**
18	RXDCAN2	**Receive CAN2.**
19	VCAN	**Supply Input** for internal HS-CAN modules.
20	TXDCAN3	**Transmit CAN3.**
21	RXDCAN3	**Receive CAN3.**
22	VCC1	**Buck Regulator.** Input feedback for Buck Converter.
23	VIO	**I/O voltage supply, reference voltage for over-/undervoltage monitoring (see Chapter 5.1.1).**
24	RSTN	**Reset Output.** Active LOW, internal pull-up.
25	INTN	**Interrupt Output**. Active LOW.
26	GND	**Ground.** Buck regulator ground.
27	BCKSW	**Buck regulator switch node output.**
28	n.c.	**not connected.** Not bondend internally.
29	VS	**Buck Supply Voltage.** Connected to Battery Voltage or Boost output voltage with reverse protection diode. Use a filter against EMC in case that the Boost is not used.
30	VS	**Buck Supply Voltage.** Connected to Battery Voltage or Boost output voltage with reverse protection diode. Use a filter against EMC in case that the Boost is not used.
31	n.c.	**not connected.** Not bondend internally.
32	GND	**Ground.** Boost regulator ground.
33	GND	**Ground.** Boost regulator ground.

Pin Configuration

Pin	Symbol	Function
34	n.c.	**not connected.** Not bondend internally.
35	BSTD	**Boost Transistor Drain.** Connected between inductor and diode for boost functionality (refer to **Chapter 14.1** for additional information). Connect to ground if the Boost regulator is not used.
36	BSTD	**Boost Transistor Drain.** Connected between inductor and diode for boost functionality (refer to **Chapter 14.1** for additional information). Connect to ground if the Boost regulator is not used.
37	CSN	**SPI Chip Select Not Input.**
38	SDO	**SPI Data Output.** Out of SBC (=MISO).
39	SDI	**SPI Data Input.** Into SBC (=MOSI).
40	CLK	**SPI Clock Input.**
41	GND	**Ground.** Common digital ground.
42	WK	**Wake Input.**
43	VBSENSE	**Battery Voltage Monitoring Input.**
44	VEXTIN	**Input Supply Voltage for VEXT.** Connected to Battery Voltage with Reverse Protection Diode and Filter against EMC.
45	VEXTSH	**VEXTSH.** Emitter connection for external PNP, shunt connection to VEXTIN.
46	VEXTB	**VEXTB.** Base connection for external PNP.
47	VEXTREF	**VextREF.** Collector connection for external PNP, reference input.
48	FO/TEST	**Fail Output.** active LOW, open-drain; **TEST.** Connect to GND to activate SBC Development Mode; Integrated pull-up resistor. Connect to VS with a pull-up resistor or leave open for normal operation.
Cooling Tab	GND	Cooling Tab - Exposed Die Pad; For cooling purposes only, do not use as an electrical ground.[1)]

1) The exposed die pad at the bottom of the package allows better power dissipation of heat from the SBC via the PCB. The exposed die pad is not connected to any active part of the IC and can be left floating or it can be connected to GND (recommended) for the best EMC performance.

Note: All VS pins must be connected to battery potential or insert a reverse polarity diodes where required; All GND pins as well as the Cooling Tab must be connected to one common GND potential.

3.3 Unused Pins

It must be ensured that the correct configurations are also selected, i.e. in case functions are not used that they are disabled via SPI:

- CANHx, CANLx, TXDCANx, RXDCANx: leave pins open.
- BSTD: connect to GND.
- WK: connect to GND and disable WK input via SPI.
- RSTN / INTN: leave open.
- FO/TEST: connect to GND during power-up to activate SBC Development Mode; connect to VS or leave open for normal user mode operation.
- VBSENSE: connect to VS in case that Fast Battery Voltage Monitoring and Boost deactivation features are not used and keep them disabled.
- VEXT: See **Chapter 7.5**.
- n.c.: leave open.
- Unused pins routed to an external connector which leaves the ECU should feature a zero ohm jumper (depopulated if unused) or ESD protection.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings[1)]

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply Voltage VS and VEXTIN pin	$V_{S1, max}$	-0.3	–	28	V	–	P_4.1.1
Supply Voltage VS and VEXTIN pin	$V_{S2, max}$	-0.3	–	40	V	Load Dump, max. 400 ms	P_4.1.2
Boost drain Voltage BSTD pin	$V_{BSTD2, max}$	-0.3	–	28	V	–	P_4.1.3
Boost drain Voltage BSTD pin	$V_{BSTD2, max}$	-0.3	–	40	V	Load Dump, max. 400 ms	P_4.1.4
Buck switch BCKSW pin	$V_{BCKSW, max}$	-0.3	–	V_S + 0.3	V	–	P_4.1.8
Buck Regulator feedback, pin VCC1	$V_{CC1, max}$	-0.3	–	5.5	V	–	P_4.1.9
External Voltage Regulator (VEXTREF)	$V_{EXTREF, max}$	-0.3	–	28	V	V_{EXTREF} = 40 V for Load Dump, max. 400 ms	P_4.1.26
External Voltage Regulator (VEXTB)	$V_{EXTB, max}$	-0.3	–	V_{EXTIN} + 10	V	V_{EXTB} = 40 V for Load Dump, max. 400 ms	P_4.1.27
External Voltage Regulator (VEXTSH)	$V_{EXTSH, max}$	V_{EXTIN} - 0.3	–	V_{EXTIN} + 0.3	V	–	P_4.1.11
Battery Voltage Monitoring	$V_{VBSENSE, max}$	-18	–	40	V	–	P_4.1.12
Wake Input	$V_{WK, max}$	-0.3	–	40	V	–	P_4.1.13
Fail Pins FO/TEST	$V_{HV, max}$	-0.3	–	40	V	–	P_4.1.14
Interrupt/Configuration Pin INTN	$V_{INTN, max}$	-0.3	–	5.5	V	–	P_4.1.15
Configuration Pin PCFG	$V_{PCFG, max}$	-0.3	–	40	V	–	P_4.1.25
Configuration Pin VIO	$V_{VIO, max}$	-0.3	–	5.5	V	–	P_4.1.28
CANH, CANL	$V_{BUS, max}$	-40	–	40	V	–	P_4.1.16
Digital Input / Output pin's	$V_{IO, max}$	-0.3	–	5.5	V	–	P_4.1.17
VCAN Input Voltage	$V_{VCAN, max}$	-0.3	–	5.5	V	–	P_4.1.18
Maximum Differential CAN Bus Voltage	$V_{CAN\_DIFF, max}$	-5	–	10	V	–	P_4.1.30

Table 1 Absolute Maximum Ratings[1)] (cont'd)

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_4.1.19
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.20
ESD Susceptibility							
ESD Resistivity to GND	V_{ESD}	-2	–	2	kV	HBM[2)]	P_4.1.21
ESD Resistivity to GND, CANH, CANL	V_{ESD}	-8	–	8	kV	HBM[2)3)]	P_4.1.22
ESD Resistivity to GND	V_{ESD}	-500	–	500	V	CDM[4)]	P_4.1.23
ESD Resistivity Pin 1, 12,13,24,25,36,37,48 (corner pins) to GND	$V_{ESD1,12,13,24,25,36,37,48}$	-750	–	750	V	CDM[4)]	P_4.1.24

1) Not subject to production test, specified by design.
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF).
3) ESD "GUN" Resistivity with ±6 KV (according to IEC61000-4-2 "GUN test" (300 Ω, 150 pF)) it is shown in Application Information and test will be provided from IBEE institute.
4) ESD susceptibility, Charged Device Model "CDM" EIA/JESD22-C101 or ESDA STM5.3.1, usually not tested but rather ESD SDM.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage	$V_{S,func}$	V_{POR}	–	28	V	[1] V_{POR} see section **Chapter 12.12**	P_4.2.1
CANx Supply Voltage	V_{CAN}	4.75	–	5.25	V	–	P_4.2.2
SPI frequency	f_{SPI}	–	–	4	MHz	see **Chapter 13.7** for $f_{SPI,max}$	P_4.2.3
Junction Temperature	T_j	-40	–	150	°C	–	P_4.2.4

1) Including Power-On Reset, Over- and Undervoltage Protection.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

Device Behavior Outside of Specified Functional Range:

- 28 V < $V_{S,func}$ < 40 V: Device will still be functional; the specified electrical characteristics might not be ensured anymore. The absolute maximum ratings are not violated. However, a thermal shutdown might occur due to high power dissipation.
- V_{CAN} < 4.75 V: The undervoltage bit **VCAN_UV** will be set in the SPI register **BUS_STAT_0** and the transmitter will be disabled as long as the UV condition is present.
- 5.25 V < V_{CAN} < 5.5 V: CANx transceiver still functional. However, the communication might fail due to out-of-spec operation.
- $V_{POR,f}$ < V_S < 5.5 V: Device will be still functional; the specified electrical characteristics might not be ensured anymore:
  - The voltage regulators will enter the low-drop operation mode.
  - **VIO_UV** reset could be triggered depending on the VRTx settings.

4.3 Thermal Resistance

Table 3 Thermal Resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Soldering Point	R_{thJSP}	–	7	–	K/W	Exposed Pad	P_4.3.1
Junction to Ambient	R_{thJA}	–	33	–	K/W	2)	P_4.3.2

1) Not subject to production test, specified by design.

2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board for 1.5 W. Board: 76.2 × 114.3 × 1.5 mm^3 with 2 inner copper layers (35 µm thick), with thermal via array under the exposed pad . Top and bottom layers are 70 µm thick.

4.4 Current Consumption

Table 4 Current Consumption

Current consumption values are specified at T_j = 25°C, V_S = 13.5 V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SBC Normal Mode							
Normal Mode current consumption	I_{Normal}	–	10	16	mA	V_S = 5.5 V to 28 V; T_j = -40°C to +150°C; BOOST/VEXT/CANx = OFF	P_4.4.1
SBC Stop Mode							
Stop Mode current Consumption	$I_{Stop,25}$	–	55	70	µA	1) Buck in PFM BOOST/VEXT = OFF; No load on VCC1 **VBSENSE_EN** = 0_B CANx/WK not wake capable Watchdog = OFF	P_4.4.2
Stop Mode current Consumption, T_j = 85°C	$I_{Stop,85}$	–	95	–	µA	2) T_j = 85°C; Buck in PFM BOOST/VEXT = OFF; No load on VCC1 **VBSENSE_EN** = 0_B CANx/WK not wake capable Watchdog = OFF	P_4.4.3
SBC Sleep Mode							
Sleep Mode current consumption	$I_{Sleep,25}$	–	30	50	µA	BOOST/VEXT = OFF; **VBSENSE_EN** = 0_B CANx/WK not wake capable	P_4.4.4

Table 4 Current Consumption (cont'd)

Current consumption values are specified at T_j = 25°C, V_S = 13.5 V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Sleep Mode current consumption, T_j = 85°C	$I_{Sleep,85}$	–	65	–	µA	2) T_j = 85°C; BOOST/VEXT = OFF; **VBSENSE_EN** = 0_B CANx/WK not wake capable	P_4.4.5
Feature Incremental Current Consumption							
Current consumption per CAN module, recessive state	$I_{CAN,rec}$	–	2	3	mA	SBC Normal Mode; CAN Normal Mode; V_{CAN} = 5 V; V_{TXDCAN} = V_{IO}; no RL on CANx	P_4.4.6
Current consumption per CAN module, dominant state	$I_{CAN,dom}$	–	3	4.5	mA	2) SBC Normal Mode; CAN Normal Mode; V_{CAN} = 5 V; V_{TXDCAN}= GND; no RL on CANx	P_4.4.7
Current consumption per CAN module, Receive Only Mode, SBC Normal Mode	$I_{CAN,RcvOnly,NM}$	–	0.4	0.6	mA	2) CAN Receive Only Mode; V_{CAN} = 5 V; V_{TXDCAN} = V_{IO}; no RL on CANx	P_4.4.8
Current consumption per CAN module, Receive Only Mode, SBC Stop Mode	$I_{CAN,RcvOnly,StM}$	–	1	1.4	mA	2) CAN Receive Only Mode; V_{CAN} = 5 V; V_{TXDCAN} = V_{IO}; no RL on CANx	P_4.4.25
Current consumption during CAN Partial Networking frame detect mode for one CAN module	$I_{CAN,SWK,25}$	–	700	790	µA	2)3)4) T_j = 25°C; VEXT = OFF; WK not wake capable; CAN SWK wake capable, SWK Receiver enabled, WUF detect; no RL on CANx	P_4.4.9
Current consumption during CAN Partial Networking frame detect mode for one CAN module	$I_{CAN,SWK,85}$	–	750	830	µA	2)3)4) T_j = 85°C; VEXT= OFF; WK not wake capable; CAN SWK wake capable, SWK Receiver enabled, WUF detect; no RL on CANx	P_4.4.10

Table 4 Current Consumption (cont'd)

Current consumption values are specified at T_j = 25°C, V_S = 13.5 V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption during CAN Partial Networking frame detect mode per additional CAN module	$I_{CAN,SWK2,25}$	–	250	300	µA	2) T_j = 25°C; SBC Stop Mode; VEXT = OFF; WK not wake capable; CAN SWK wake capable, WUF detect; no RL on CANx	P_4.4.22
Current consumption for WK wake capability	$I_{Wake,WK,25}$	–	0.5	1.5	µA	4)5) SBC Sleep Mode; CANx = OFF	P_4.4.11
Current consumption for WK wake capability T_j = 85°C	$I_{Wake,WK,85}$	–	2.0	4.0	µA	2)4)5) SBC Sleep Mode; T_j = 85°C; CANx = OFF	P_4.4.12
Current consumption for CAN wake capability	$I_{Wake,CAN,25}$	–	4.5	6	µA	1)4) SBC Sleep Mode; WK = OFF $t_{SILENCE}$ expired	P_4.4.13
Current consumption for CAN wake capability	$I_{Wake,CAN,85}$	–	6	10	µA	1)2)4) SBC Sleep Mode; T_j = 85°C; WK = OFF $t_{SILENCE}$ expired	P_4.4.14
Current consumption for VEXT in SBC Sleep Mode	$I_{Sleep,VEXT,25}$	–	45	60	µA	4) SBC Sleep Mode; VEXT = ON (no load); CANx / WK = OFF	P_4.4.15
Current consumption for VEXT in SBC Sleep Mode, T_j = 85°C	$I_{Sleep,VEXT,85}$	–	55	70	µA	2)4) SBC Sleep Mode; T_j = 85°C; VEXT = ON (no load); CANx / WK = OFF	P_4.4.16
Current consumption for cyclic wake function	$I_{Stop,C25}$	–	20	26	µA	4)6) SBC Stop Mode; WD = OFF	P_4.4.17
Current consumption for cyclic wake function, T_j = 85°C	$I_{Stop,C85}$	–	24	35	µA	2)4)6) SBC Stop Mode; T_j = 85°C; WD = OFF	P_4.4.18
Current consumption for watchdog active in Stop Mode	$I_{Stop,WD25}$	–	20	26	µA	2) SBC Stop Mode; Watchdog running	P_4.4.19
Current consumption for watchdog active in Stop Mode	$I_{Stop,WD85}$	–	24	35	µA	2) SBC Stop Mode; T_j = 85°C; Watchdog running	P_4.4.20
Current consumption for active fail output (FO)	$I_{Stop,FO}$	–	0.5	1.5	mA	2) All SBC Modes; T_j = 25°C; FO = ON (no load);	P_4.4.21

Table 4 Current Consumption (cont'd)

Current consumption values are specified at T_j = 25°C, V_S = 13.5 V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption Fast Battery Monitoring in SBC Stop Mode	$I_{Stop,FBM}$	–	5	–	µA	2) SBC Stop Modes; **VBSENSE_EN** = 1_B T_j = 25°C;	P_4.4.30
Additional V_S current consumption with Boost Module Active	$I_{BOOST,ON}$	–	10	20	mA	2) SBC Normal / Stop Modes; $V_{BSTx} < V_S < V_{BST,thx}$ **BOOST_EN** = 1_B;	P_4.4.31

1) Current consumption for CANx transceiver and WK input to be added if set to be wake capable or receiver only.
2) Not subject to production test, specified by design.
3) Current consumption adder applies during WUF detection (frame detect mode) when CAN Partial Networking is activated. The current consumption will be reduced per module when multiple CAN transceivers are activated for SWK.
4) Current consumption adders of features defined for SBC Sleep Mode also apply for SBC Stop Mode and vice versa (unless otherwise specified).
5) No pull-up or pull-down configuration selected.
6) Cyclic wake configuration: Timer with 20 ms period.

5 System Features

This chapter describes the system features and behavior of the TLE9278-3BQX V33:

- State machine and SBC mode control.
- Device configurations.
- State of supply and peripherals.
- Wake features.
- Supervision and diagnosis functions.

The System Basis Chip is controlled via a 16-bit SPI interface. A detailed description can be found in **Chapter 13**. The configuration as well as the diagnosis is handled via the SPI. The SPI mapping of the TLE9278-3BQX V33 is compatible to other devices of TLE926x and TLE927x family.

The System Basis Chip (SBC) offers six operating modes:

- SBC Init Mode: power-up of the device and after soft reset.
- SBC Normal Mode: the main operating mode of the device.
- SBC Stop Mode: the first-level power saving mode with the main voltage regulator enabled.
- SBC Sleep Mode: the second-level power saving mode with Buck regulator disable.
- SBC Restart Mode: an intermediate mode after a wake event from SBC Sleep or SBC Fail-Safe Mode or after a failure (e.g. WD failure in config 1/3) to bring the microcontroller into a defined state via a reset. Once the failure condition is not present anymore, the device will automatically change to SBC Normal Mode after a delay time (t_{RD1}).
- SBC Fail-Safe Mode: a safe-state mode after critical failures (e.g. TSD2 thermal shutdown) to bring the system into a safe state and to ensure a proper restart of the system. Buck regulator is disabled.

A special mode called SBC Development Mode is available during software development or debugging of the system. All of the operating modes mentioned above can be accessed in this mode. However, the watchdog counter is stopped and does not need to be triggered. This mode can be accessed by setting the TEST pin to GND during SBC Init Mode.

5.1 State Machine Description and SBC Mode Control

The different SBC Modes are selected via SPI by setting the respective SBC **MODE** bits in the register **M_S_CTRL**.

The SBC **MODE** bits are cleared when going trough SBC Restart Mode, so the current SBC mode is always shown.

Figure 3**Figure 4** shows the SBC State Diagram.

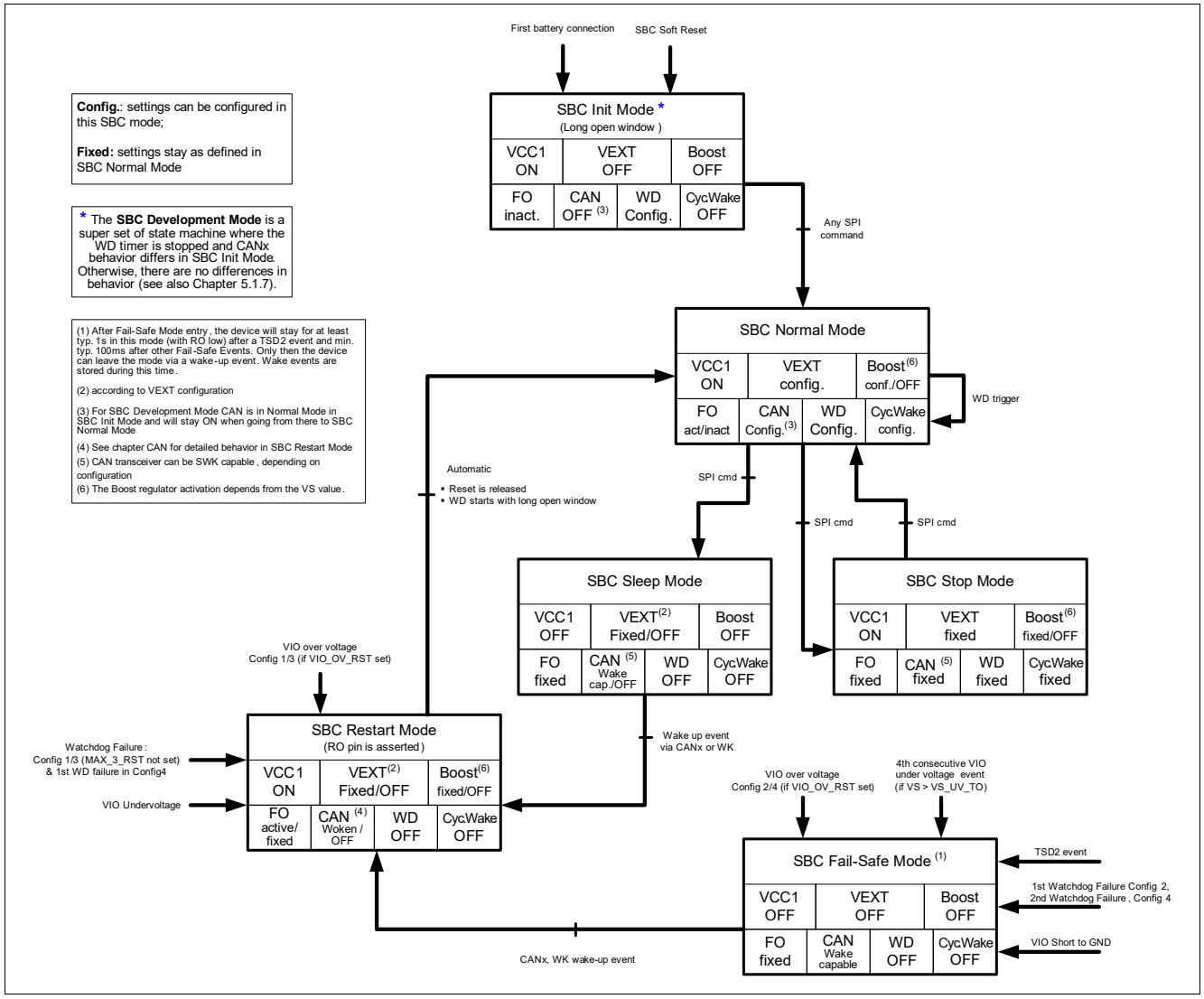


Figure 3 State Diagram showing the SBC Operating Modes

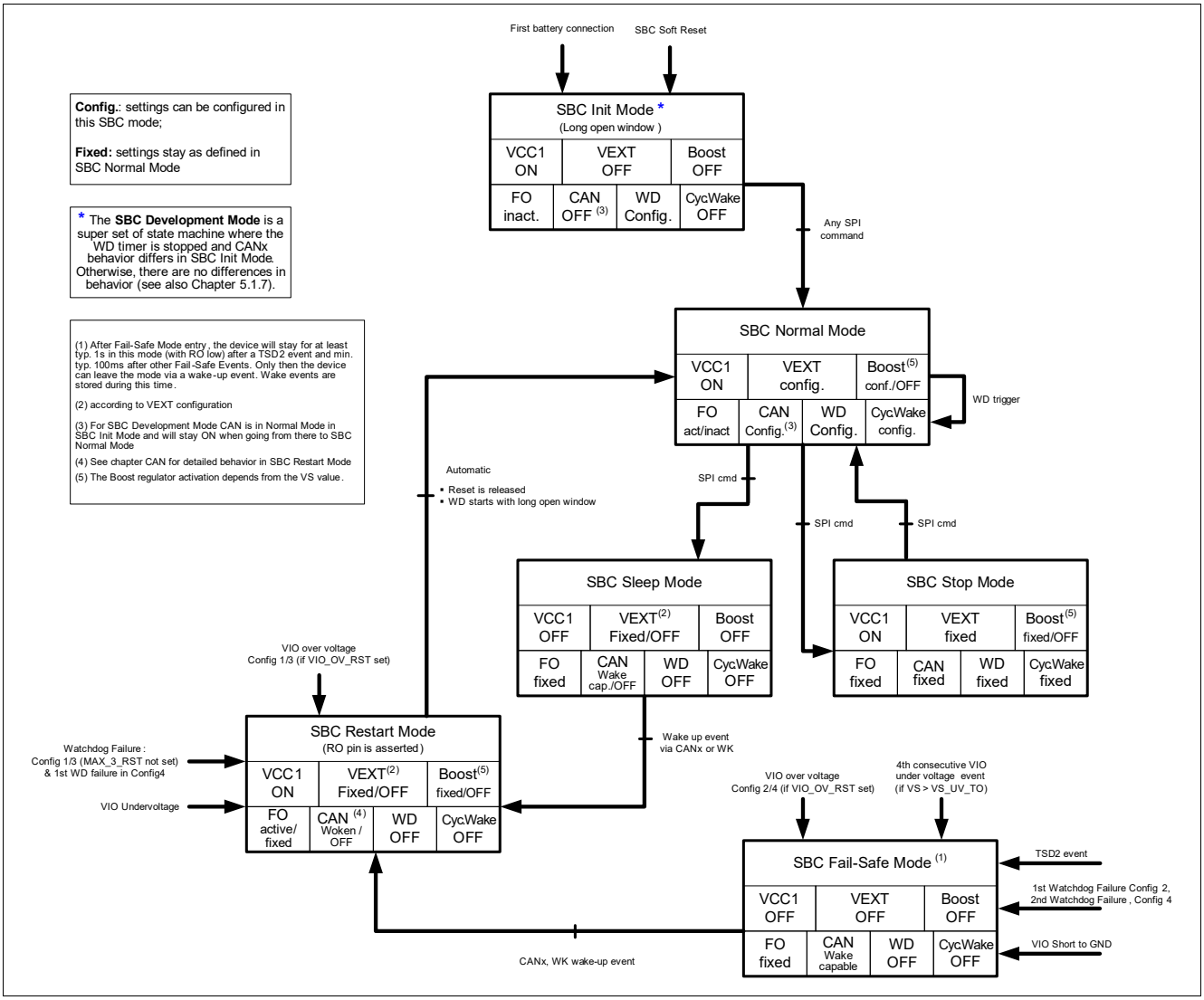


Figure 4 State Diagram showing the SBC Operating Modes

5.1.1 Device Configuration and SBC Init Mode

The SBC Init Mode is the mode where the hardware configuration of the SBC is stored and where the microcontroller finishes the initialization phase.

The SBC starts up in SBC Init Mode after crossing the power-on reset $V_{POR,r}$ threshold (see also **Chapter 12.3**) and the watchdog will start with a long open window (t_{LW} typical 200ms) after the RSTN is released.
During this power-on phase following configurations are stored in the device:

- Supply and Power up configurability.
- The device behavior regarding a watchdog trigger failure and a VIO overvoltage condition is determined by the external circuitry on the INTN pin (see below).
- The selection of the normal device operation or the SBC Development Mode (watchdog disabled for debugging purposes) will be set depending on the voltage level of the FO/TEST pin (see also **Chapter 5.1.7**).

5.1.1.1 Supply and Power up configurability

The pin VIO of TLE9278-3BQX V33 has to be connected to VCC1. The pin PCFG can be left open or connected to GND.

The **Table 5** shows the only allowed combinations and related behavior.

Table 5 Supply and power up Configurability

VCC1 Output Voltage	PCFG pin	VIO Supply	µC Supply	VEXT Output voltage	VEXT Behavior	Supervision Functions
V_{CC1} = 3.3 V	Open	VCC1	VCC1	Configurable via SPI using **VEXT_VCFG**	SPI configurable, OFF after Power Up	Supervision functions on VIO with 3.3 V level; **VREG_UV** SPI status bit active
V_{CC1} = 3.3 V	GND	VCC1	VCC1	Configurable via SPI using **VEXT_VCFG**	SPI configurable, OFF after Power Up	Supervision functions on VIO with 3.3 V level; **VREG_UV** SPI status bit active

Note: VIO can be connected only to VCC1.

5.1.1.2 Watchdog trigger failure configuration

There are four different device configurations (**Table 6**) available defining the watchdog failure and the VIO overvoltage behavior. The configurations can be selected via the external connection on the INTN pin and the SPI bit **CFG2** in the **HW_CTRL_0** register (see also **Chapter 13.4**):

- A watchdog trigger failures leads to SBC Restart Mode (Config 1/3) and depending on **CFG2** the Fail Output (FO) are activated after the 1st or 2nd watchdog trigger failure;
  If **VIO_OV_RST** is set and in Config 1/3, then SBC Restart Mode will be entered in case of **VIO_OV** and the FO is activated.
- A watchdog trigger failures leads to SBC Fail-Safe Mode (Config 2/4) and depending on **CFG2** the Fail Output (FO) are activated after the 1st or 2nd watchdog trigger failure. The first watchdog trigger failure in Config 4 will lead to SBC Restart Mode;

If **VIO_OV_RST** is set and in Config 2/4, then SBC Fail-Safe Mode will be entered in case of **VIO_OV** and the FO is activated.

The respective device configuration can be identified by reading the SPI bits **CFG2_STATE** and **CFG1_STATE** in the **WK_LVL_STAT** register.

Table 6 Watchdog Trigger Failure Configuration

Config	Event	FO Activation	SBC Mode Entry	SPI Bit CFG2	INTN Pin (CFG1_STATE)
1	1 × Watchdog Failure	after 1st WD Failure	SBC Restart Mode	1	External pull-up
2	1 × Watchdog Failure	after 1st WD Failure	SBC Fail-Safe Mode	1	No ext. pull-up
3	2 × Watchdog Failure	after 2nd WD Failure	SBC Restart Mode	0	External pull-up
4	2 × Watchdog Failure	after 2nd WD Failure	SBC Fail-Safe Mode	0	No ext. pull-up

The respective configuration will be stored for all conditions and can only be changed by powering down the device ($V_S < V_{POR,f}$).

Table 7 shows the possible SBC hardware configurations.

Table 7 SBC Configuration

Configuration	Description	FO/Test Pin	INTN Pin (CFG1_STATE)	CFG2_STATE	CFG1_STATE
Config 0	SBC Development Mode: no reset is triggered in case of watchdog trigger failure. After the Power Up, one arbitrary SPI command must be sent.	0	-	X	X
Config 1	After missing the WD trigger for the first time, the state of VCC1 remains unchanged, FO pin is active, SBC in Restart Mode	Open or $>V_{TEST,H}$	External pull-up to V_{IO}	1	1
Config 2	After missing the WD trigger for the first time,VCC1 turns OFF, FO pin are active, SBC in Fail-Safe mode	Open or $>V_{TEST,H}$	Open or GND	1	0
Config 3	After missing the WD trigger for the second time, the state of VCC1 remains unchanged, FO pin is active, SBC in Restart Mode	Open or $>V_{TEST,H}$	External pull-up to V_{IO}	0	1
Config 4	After missing the WD trigger for the second time,VCC1 turns OFF, FO pin is active, SBC in Fail-Safe mode	Open or $>V_{TEST,H}$	Open or GND	0	0

In case of 3 consecutive resets due to WD fail, it is possible in Config 1 and 3 not to generate additional reset by setting the **MAX_3_RST** on **WD_CTRL**.

Figure 5 shows the timing diagram of the hardware configuration selection. The hardware configuration is defined during SBC Init Mode. The INTN pin is internally pulled LOW with a weak pull-down resistor during the reset delay time t_{RD1}, i.e. after VIO crosses the reset threshold VRT1 and before the RSTN pin goes HIGH. The

INTN pin is monitored during this time and the configuration (depending on the voltage level at INTN) is read and stored at the rising edge of RSTN (with a filter time of t_{CFG_F}).

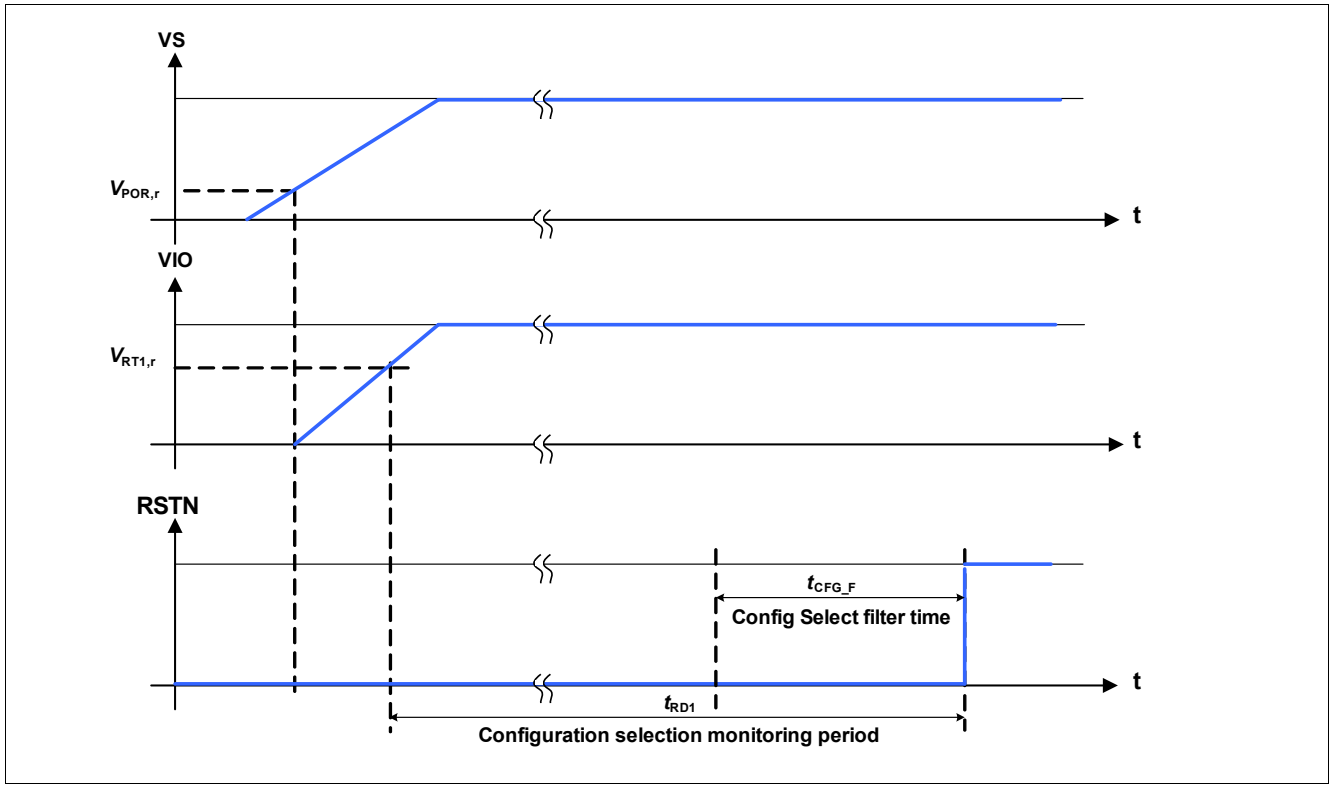


Figure 5 Hardware Selection Timing Diagram

*Note: If the **POR** bit is not cleared then the internal pull-down resistor will be reactivated every time RSTN is pulled LOW the configuration will be updated at the rising edge of RSTN. Therefore it is recommended to clear the **POR** bit right after initialization.*

5.1.1.3 SBC Init Mode

In SBC Init Mode, the device waits for the microcontroller to finish its startup and initialization sequence. In the SBC Init Mode any SPI command will bring the SBC to SBC Normal Mode. During the long open window the watchdog has to be triggered. Thereby the watchdog will be automatically configured. A missing watchdog trigger during the long open window will cause a watchdog failure and the device will enter SBC Restart Mode.

Wake events are ignored during SBC Init Mode and will therefore be lost.

*Note: Any SPI command will bring the SBC to SBC Normal Mode even if non-valid (see **Chapter 13.2**).*

*Note: For a safe start-up, it is recommended to use the first SPI command to trigger and to configure the watchdog (see **Chapter 12.2**).*

*Note: At power up, no **VIO_UV** will be issued nor will FO be triggered as long as VIO is below the V_{RT1} threshold and V_S is below the VIO short circuit detection threshold $V_{S,UV}$. The RSTN pin will be kept low as long as VIO is below the selected V_{RT1} threshold. As soon as the VIO is higher than V_{RT1}, the RSTN is released after t_{RD1}.*

5.1.2 SBC Normal Mode

The SBC Normal Mode is the standard operating Mode for the SBC. All configurations have to be done in SBC Normal Mode before entering a low-power mode (see also **Chapter 5.1.6** for the device configuration defining the Fail-Safe Mode behavior). A wake-up event on CANx and WK will create an interrupt on pin INTN however, no change of SBC Mode will occur. The configuration options are listed below:

- VCC1 is active, Buck in PWM Mode.
- VEXT can be switched ON or OFF .
- CANx is configurable (OFF coming from SBC Init Mode; OFF or wake capable coming from SBC Restart Mode, see also **Chapter 5.1.5**).
- Wake pin level can be monitored and can be selected to be wake capable.
- Cyclic wake period can be configured using **TIMER_CTRL_0** and enabled by setting **TIMER1_WK_ EN**.
- Watchdog is configurable.
- FO is OFF by default.

In SBC Normal Mode, there is the possibility of testing the FO output, i.e. to verify if setting the FO pin to low will create the intended behavior within the system. The FO output can be enabled and then disabled again by the microcontroller by setting the **FO_ON** SPI bit. This feature is only intended for testing purposes.

5.1.3 SBC Stop Mode

The SBC Stop Mode is the first level technique to reduce the overall current consumption. All kind of settings have to be done before entering SBC Stop Mode. In SBC Stop Mode any kind of SPI write commands are ignored and the **SPI_FAIL** bit is set, except for changing to SBC Normal Mode, triggering a SBC Soft Reset, refreshing the watchdog, changing modulation of the buck. The configuration options are listed below:

- VCC1 is ON, Buck in PFM Mode if $I_{VCC1} < I_{PFM\text{-}PWM,TH}$.
- VEXT is fixed ON or OFF in accordance with SPI configuration.
- CANx can be selected for ‘Receive Only Mode’, to be wake capable or OFF.
- WK pin can be selected to be wake capable, PWM_BY_WK (switch PFM/PWM buck modulation) or OFF.
- Wake capability via cyclic wake can be selected.
- Watchdog is fixed or OFF (if WD disable sequence was executed).

A wake-up event on CANx and WK will create an interrupt on pin INTN however, no change of SBC Mode will occur.

In SBC Stop Mode, it is allowed to use the Boost module (enabled before to enter in SBC Stop Mode) in case of the V_S is dropping. The Boost works only in PWM and therefore the total amount of current consumption will increase.

*Note: It is not possible to switch directly from SBC Stop Mode to SBC Sleep Mode. Doing so will also set the **SPI_FAIL** flag and will bring the SBC into Normal Mode via SBC Restart Mode.*

5.1.4 SBC Sleep Mode

The SBC Sleep Mode is the second level technique to reduce the overall current consumption to a minimum needed to react on wake-up events.

All settings must be done before entering SBC Sleep Mode. In case that SPI configurations in Sleep Mode have been sent to the SBC, the commands are ignored and no reactions from the SBC.

The configuration options are listed below:

- VCC1 is OFF.
- VEXT is fixed ON or OFF in accordance with SPI configuration.
- CANx can be selected to be wake capable or OFF.
- WK pin can be selected to be wake capable or OFF.

A wake-up event on CANx or WK pin will bring the device via SBC Restart Mode into SBC Normal Mode again and signal the wake event and corresponding sources.

It is not possible to switch off all wake sources in Sleep Mode. This will lead to SBC Normal Mode via SBC Restart Mode instead.

In order to enter SBC Sleep Mode successfully, all wake source signalization flags from **WK_STAT_0** and **WK_STAT_2** need to be cleared. If a failure to do so, will result in an immediate wake-up from SBC Sleep Mode by going via SBC Restart to Normal Mode.

Note: As soon as the Sleep Command is sent, the Reset will go low to avoid any undefined behavior between SBC and microcontroller.

5.1.5 SBC Restart Mode

There are multiple reasons to enter the SBC Restart Mode. The purpose of the SBC Restart Mode is to reset the microcontroller:

- From SBC Normal and Stop Mode, it is reached in case of undervoltage on VIO. In case of 4 consecutive **VIO_UV** events, SBC Fail-Safe Mode is entered.
- From SBC Normal and Stop Mode it is reached in case of overvoltage on VIO in config 1/3 if **VIO_OV_RST** is set.
- Incorrect Watchdog triggering (depending of the configuration).
- From SBC Sleep and Fail-Safe Mode to ramp up VIO supply after wake event.

From SBC Restart Mode, the SBC goes automatically to SBC Normal Mode, i.e the mode is left automatically by the SBC without any microcontroller influence once the VIO_UV condition is not present anymore and when the reset delay time (t_{RD1}) has expired. The Reset Output (RSTN) is released at the transition.

Entering or leaving the SBC Restart Mode will not result in deactivation of the Fail output.

The following functions are not changed in SBC Restart mode:

- VEXT is fixed ON or OFF in accordance with SPI configuration.
- VCC1 is ON or ramping up.
- BOOST is fixed or OFF.

Table 8 contains detailed descriptions of the reason to restart:

Table 8 Reasons for Restart - State of SPI Status Bits after Return to Normal Mode

SBC Mode	Event	DEV_STAT	WD_FAIL	VIO_UV	VIO_OV
Normal	Watchdog Failure	01	01	x	x
Normal	VIO undervoltage reset	01	xx	1	x
Normal	VIO overvoltage (**VIO_OV_RST**=1)	01	xx	x	1
Sleep Mode	Wake-up event	10	xx	x	x
Stop Mode	Watchdog Failure	01	01	x	x

Table 8 Reasons for Restart - State of SPI Status Bits after Return to Normal Mode (cont'd)

SBC Mode	Event	DEV_STAT	WD_FAIL	VIO_UV	VIO_OV
Stop Mode	VIO undervoltage reset	01	xx	1	x
Stop Mode	VIO overvoltage (**VIO_OV_RST**=1)	01	xx	x	1
Fail-Safe	Wake-up event	01	see "Reasons for Fail-Safe, **Table 9**"		

5.1.6 SBC Fail-Safe Mode

The purpose of this mode is to bring the system in a safe status after a failure condition by turning off the VCC1 and VEXT supply and the FO pin is automatically activated. After a wake-up event the system is then able to restart again.

The Fail-Safe Mode is automatically reached in case of:

- Overtemperature condition (TSD2).
- After 1 or 2 watchdog fails (depending on config setting).
- At the 4th consecutive VIO undervoltage event.
- From SBC Normal and Stop Mode, in case of overvoltage on VIO in config 2/4, if **VIO_OV_RST** is set.
- VIO is shorted to GND.
- VIO is below the VRTx for time longer than $t_{VIO,SC}$.

In this case, the default wake sources are activated, the wake-up events are cleared in the register **WK_STAT_0** and **WK_STAT_2**.

The mode will be maintained for at least t_{TSD2} in case of TSD2 event and $t_{FS,min}$ in case of other failure events to avoid any fast toggling behavior. All wake sources will be masked during this time but the wake-up events will be stored. Stored wake-up events and wake-up event after this minimum waiting time, will lead to SBC Restart Mode. Leaving the SBC Fail-Safe Mode will not result in deactivation of the Fail Output pin.

The following functions are influenced during SBC Fail-Safe Mode:

- FO output is activated.
- VCC1 is OFF.
- VEXT is OFF.
- CANx is wake capable.
- WK is wake capable (in case that **PWM_BY_WK** was set, moving to SBC Fail-Safe Mode will clear the bit).
- Cyclic wake is disabled.

Table 9 Reasons for Fail-Safe - State of SPI Status Bits after Return to Normal Mode

Mode	Config	Event	DEV_STAT	TSD2	WD_FAIL	VIO_UV	VIO_SC	VIO_OV
Normal	2	1 × watchdog failure	01	x	01	x	0	x
Normal	4	2 × watchdog failure	01	x	10	x	0	x
Normal	1, 2, 3, 4	TSD2	01	1	xx	x	0	x
Normal	1, 2, 3, 4	VIO short to GND	01	x	xx	1	1	x
Normal	2, 4	VIO overvoltage (**VIO_OV_RST**=1, **CFG2**=1)	01	x	xx	x	0	1

Table 9 Reasons for Fail-Safe - State of SPI Status Bits after Return to Normal Mode (cont'd)

Mode	Config	Event	DEV_STAT	TSD2	WD_FAIL	VIO_UV	VIO_SC	VIO_OV
Stop Mode	2	1 × watchdog failure	01	x	01	x	0	x
Stop Mode	4	2 × watchdog failure	01	x	10	x	0	x
Stop Mode	1, 2, 3, 4	TSD2	01	1	xx	x	0	x
Stop Mode	1, 2, 3, 4	VIO short to GND	01	x	xx	1	1	x
Stop Mode	2, 4	VIO overvoltage (**VIO_OV_RST**=1, **CFG2**=1)	01	x	xx	x	0	1

5.1.7 SBC Development Mode

The SBC Development Mode is used during development phase of the application, especially for software development.

Compared to the default SBC user mode operation, this mode is a super set of the state machine. The device will start also in SBC Init Mode and it is possible to use all the SBC Modes and functions with following differences:

- Watchdog is stopped and does not need to be triggered. Therefore no reset is triggered due to watchdog failure.
- SBC Fail-Safe and Restart Mode are not reached due to watchdog failure but the other reasons to enter these modes are still valid.
- CANx default value in SBC INIT MODE is ON instead of OFF.

The mode is reached by setting the FO/TEST pin to LOW for the entire SBC INIT Mode and by sending an arbitrary SPI command. The SBC Init Mode is reachable after the power-up or sending a software reset.

SBC Development Mode can only be left by a power-down or by providing a SBC Software Reset using the **MODE** bits on **M_S_CTRL** register regardless the FO/TEST pin level.

When the FO/TEST pin is left open, or connected to V_S during the start-up, the SBC starts into normal operation. The FO/TEST pin has an integrated pull-up resistor (switched ON only during SBC Init Mode) to prevent the SBC device from starting in SBC Development Mode during normal life of the vehicle. To avoid any disturbances, the FO/TEST pin is monitored during the SBC Init Mode when the RSTN is HIGH until SBC Init Mode is left. Only if the FO/TEST pin is LOW for the Init Mode time when the RSTN is HIGH, SBC Development Mode is reached and stored.

5.2 Wake Features

Following wake sources are implemented in the device:

- Static Sense: WK input is permanently active (see **Chapter 9**).
- Cyclic Wake: internal wake source controlled via internal timer (see **Chapter 5.2.1**).
- CANx wake: wake-up via CAN message (see **Chapter 8**).

The wake source must be set before entering in SBC Sleep Mode. In case of critical situation, when the device will be set into SBC Fail-Safe mode, all default wake sources will be activated. For additional information about setting, refer to the respective chapters.

5.2.1 Cyclic Wake

The cyclic wake feature is intended to reduce the quiescent current of the device and application.

When the cyclic wake is enabled, a periodic INTN is generated in SBC Normal and Stop Mode based on the setting of **TIMER_CTRL_0**.

The correct sequence to configure the cyclic wake is shown in **Figure 6**. The sequence is as follows:

- Disable the cyclic wake feature to ensure that there is not unintentional interrupt when activating cyclic wake (**TIMER1_WK_ EN** = 0).
- Configure the cyclic wake timer period in **TIMER_CTRL_0** register.
- Enable the cyclic wake as a wake-up source in the register **WK_CTRL_0** (**TIMER1_WK_ EN** = 1).

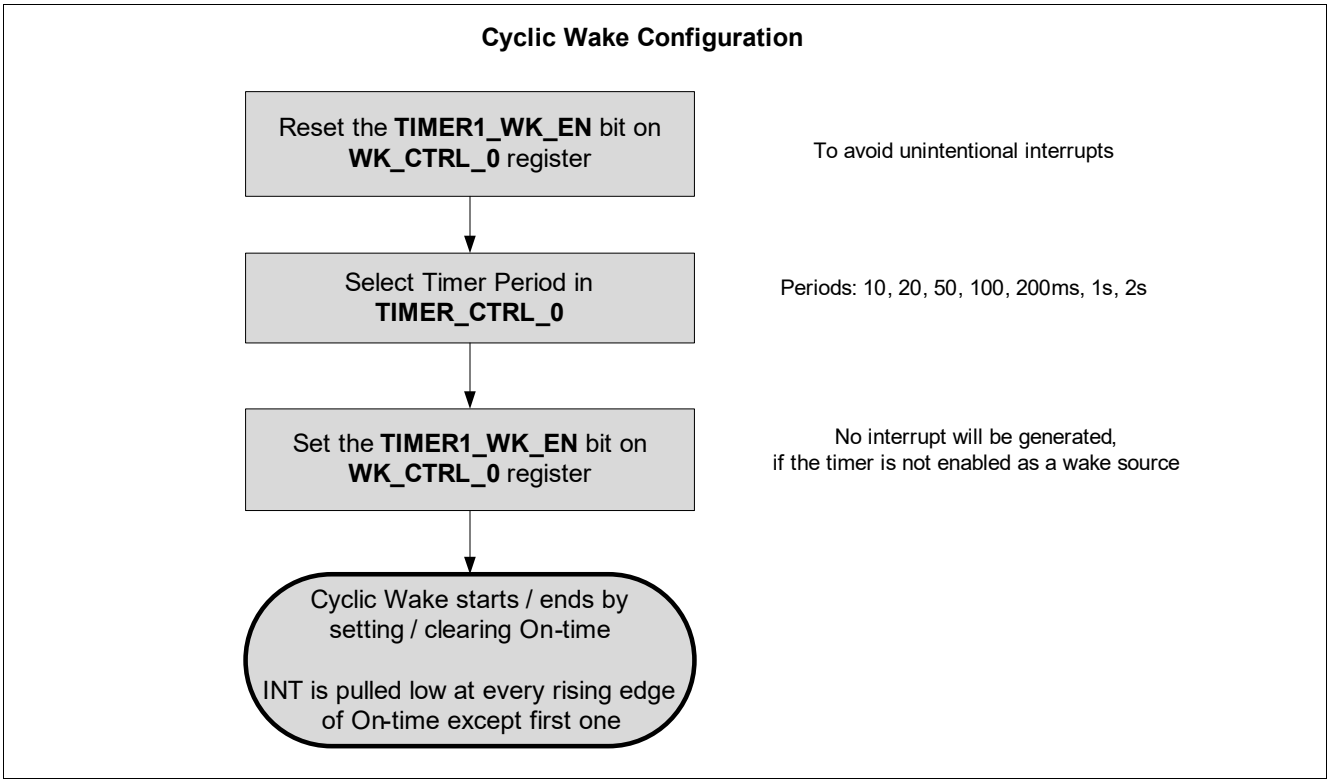


Figure 6 Cyclic Wake: Configuration and Sequence

5.2.2 Internal Timer

The integrated timer is typically used to wake up the microcontroller periodically (cyclic wake).

Following periods can be selected via the register **TIMER_CTRL_0**:

- Period: 10ms / 20ms / 50ms / 100ms / 200ms / 1s / 2s

5.3 CAN Partial Networking

5.3.1 CAN Partial Networking - Selective Wake Feature

The CAN Partial Networking feature can be activated for SBC Normal Mode, in SBC Sleep Mode and in SBC Stop Mode. For SBC Sleep Mode the Partial Networking has to be activated before sending the SBC to Sleep Mode. For SBC Stop Mode the Partial Networking has to be activated before going to SBC Stop Mode.

There are 2 detection mechanism available:

- WUP (Wake-Up Pattern) this is a CAN wake, that reacts on the CAN dominant time, with 2 dominant signals as defined in ISO WG11898-6.
- WUF (Wake-Up frame) this is the wake-up on a CAN frame that matches the programmed message filter configured in the SBC via SPI.

The default baud rate is set to 500 kBaud. Besides the commonly used baud rate of 125 kBaud and 250 kBaud, other baud rate up to 1 MBaud can be selected (see **Chapter 13.5.2** and **Chapter 13.6.2** for more details).

5.3.2 SBC Partial Networking Function

The CAN Partial Networking Modes are shown in **Figure 7**.

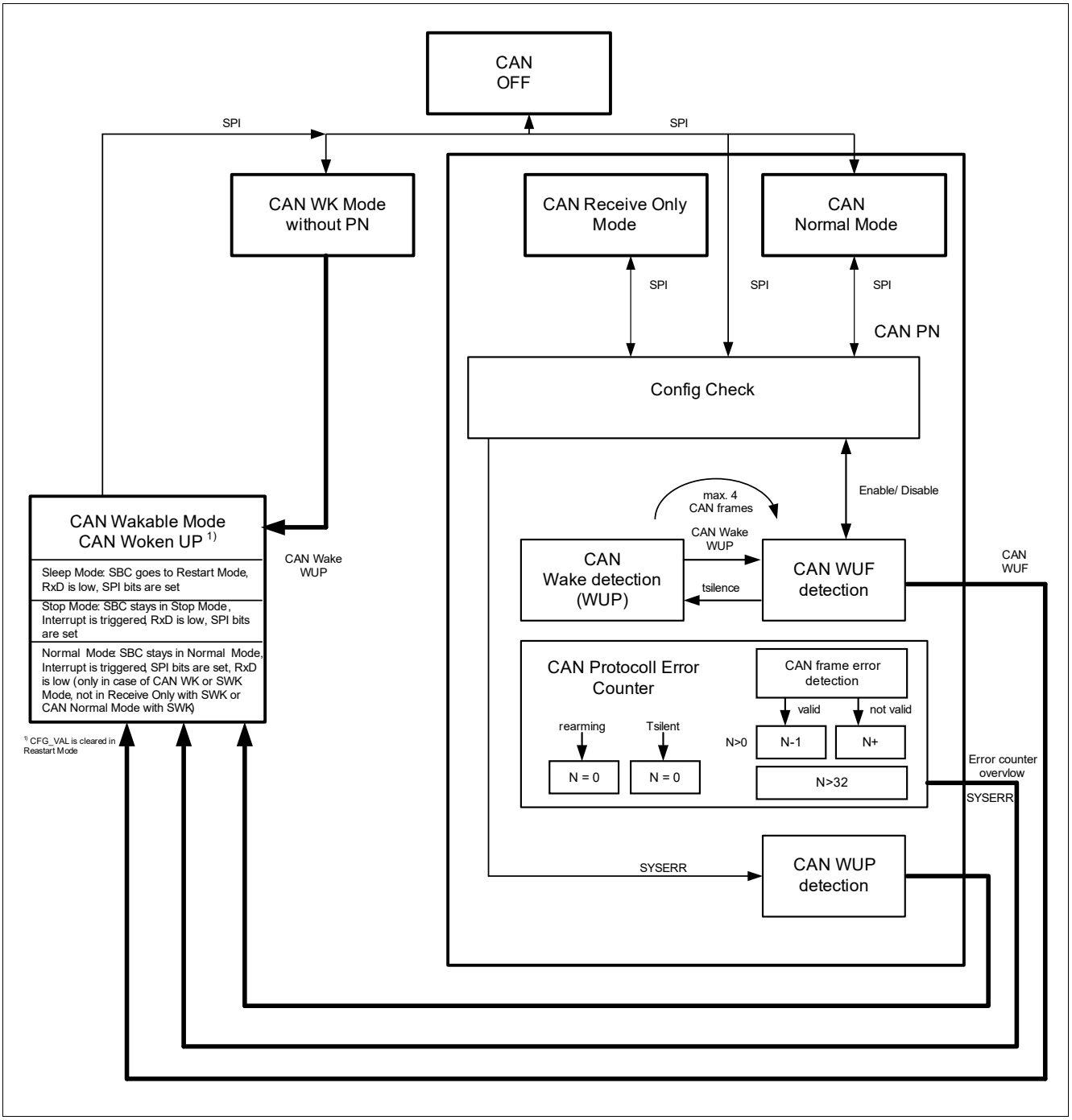


Figure 7 CAN Selective Wake State Diagram

5.3.2.1 Activation of SWK

Figure 8 shows the principal of the SWK activation.

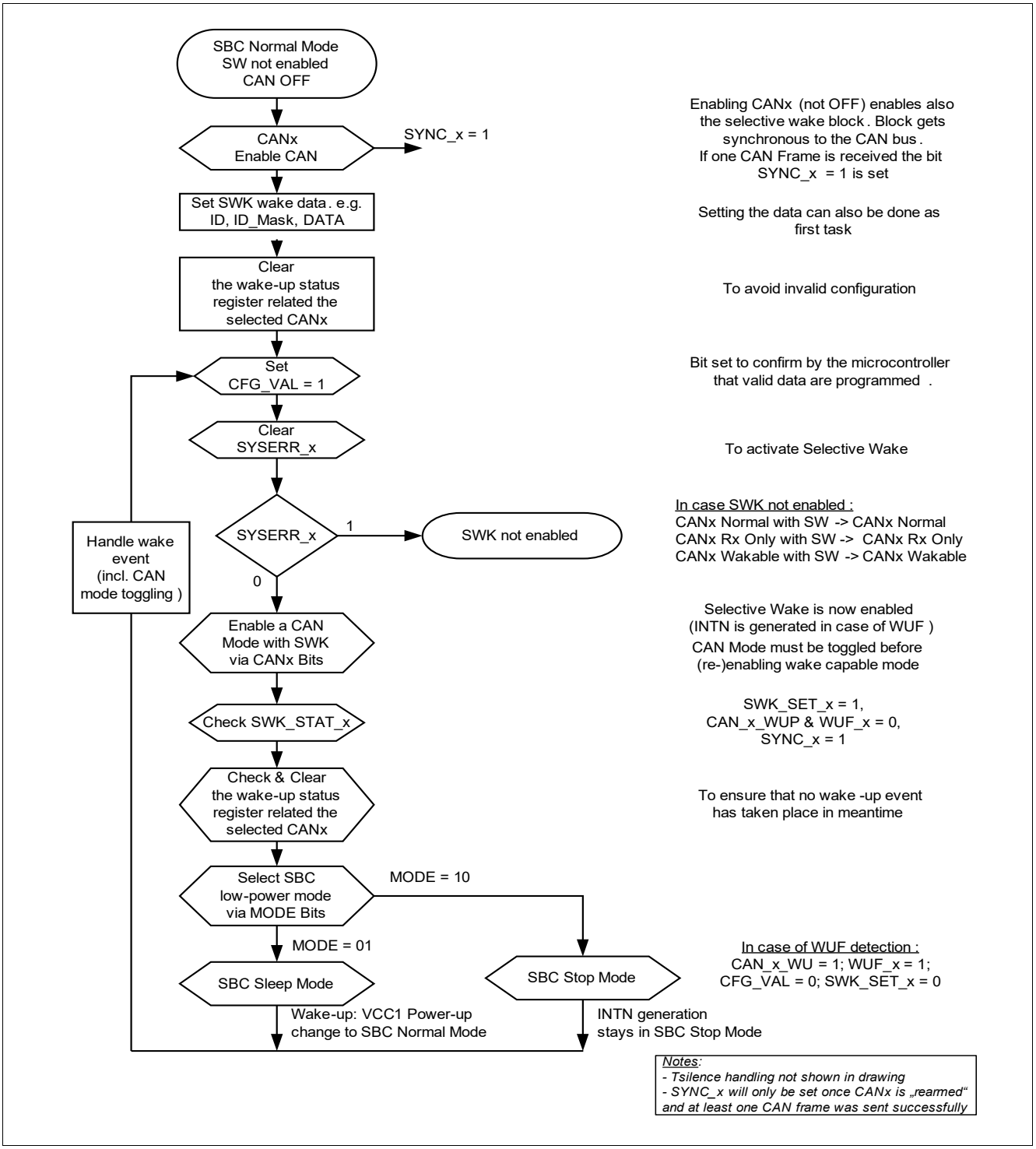


Figure 8 Flow for activation of SWK

5.3.2.2 Wake-up Pattern (WUP)

A WUP is signaled on the bus by two consecutive dominant bus levels for at least t_{Wake1}, each separated by a recessive bus level.

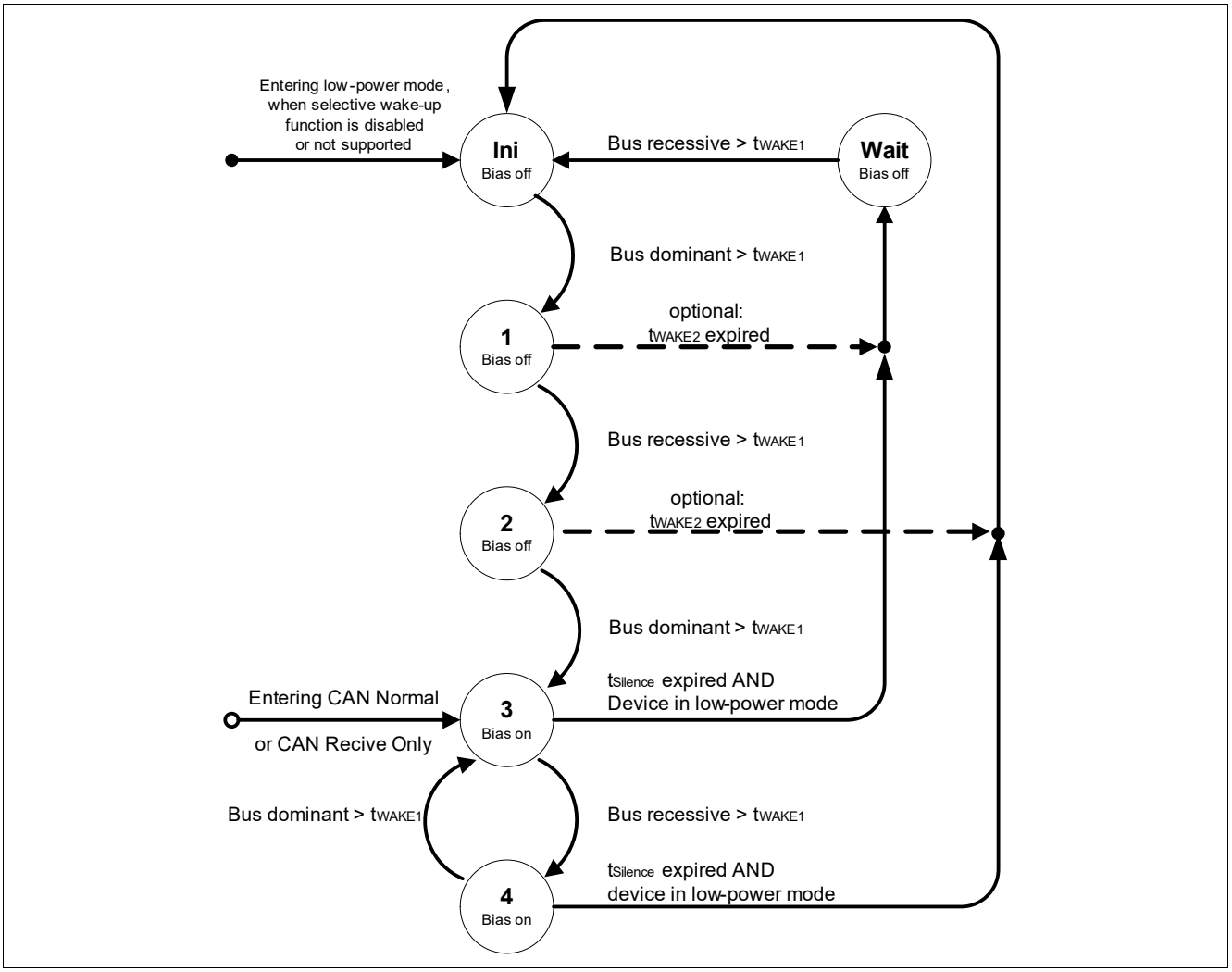


Figure 9 WUP detection following the definition in ISO 11898-5

5.3.2.3 Wake-up Frame (WUF)

The wake-up frame is defined in ISO11898-6.

Only CAN frames according ISO11898-1 are considered as potential wake-up frames.

A bus wake-up shall be performed, if selective wake-up function is enabled and a “valid WUF” has been received. The transceiver may ignore up to four consecutive CAN data frames that start after switching on the bias.

A received frame is a “valid WUF” in case all of the following conditions are met:

- The ID of the received frame is exactly matching a configured ID in the relevant bit positions. The relevant bit positions are given by an ID mask. The ID and the ID mask might have either 11 bits or 29 bits.
- The DLC of the received frame is exactly matching the configured DLC.
- In case DLC is greater than 0, the data field of the received frame has at least one bit set in a bit position, where also in the configured data mask in the corresponding bit position the bit is set.
- No error exists according to ISO 11898-1 excepting errors which are signalled in the ACK field and EOF field.

5.3.2.4 CAN Protocol Error Counter

The counter is incremented when a bit stuffing, CRC or form error according to ISO11898-1 is detected. If a frame has been received that is valid up to the end of the CRC field and the counter is not zero, the counter is decremented. If the counter has reached a value of 31, the following actions is performed on the next increment of this counter:

- The selective wake function is disabled.
- The CANx transceiver is woken.
- SYSERR_x is set and the error counter value = 32 can be read.

On each increment or decrement of the counter the decoder unit waits for at least 6 and most 10 recessive bits before considering a dominant bit as new start of frame.

The error counter is enabled:

- Whenever the CANx is in Normal Mode, Receive Only Mode or in WUF detection state.

The error counter is cleared under the following conditions:

- At the transition from WUF detection to WUP detection 1 (after $t_{SILENCE}$ expiration, while SWK is correctly enabled).
- When WUF detection state is entered (in this way the counter will start from 0 when SWK is enabled).
- At SBC or CANx rearming (when exiting the woken state).
- When the CANx Mode bits are selected ‘000’, ‘100’ (CANx OFF) or ‘001’ (CANx Wake Capable without SWK function enabled).
- While **CAN_FD_EN** = ‘1’ and **DIS_ERR_CNT** = ‘1’ (the counter is cleared and stays cleared when these two bits are set in the SPI registers).

The Error Counter us frozen:

- After a wake-up being in woken state.

The counter value can be read out of the bits ECNT_x_0 to ECNT_x_5.

5.3.3 Diagnoses Flags

5.3.3.1 PWRON/RESET-FLAG

The power-on reset can be detected and read by the **POR** bit in the SBC Status register.

The VS power on resets all register in the SBC to reset value. SWK is not configured.

5.3.3.2 BUSERR-Flag

Bus Dominant Time-out detection is implemented and signaled by CAN_x_Fail bits in the status register related the selected CAN transceiver (**BUS_STAT_0** or **BUS_STAT_2** or **BUS_STAT_3**).

5.3.3.3 TxD Dominant Time-out flag

TxD Dominant Time-out is shown in the SPI bit CAN_x_FAIL in register in the status register related the selected CAN transceiver.

5.3.3.4 WUP_x Flag

The WUP_x bit in the SWK_STAT_x register shows that a Wake-Up Pattern (WUP) has caused a wake of the CAN transceiver. It can also indicate an internal mode change from WUP detection to WUF detection after a valid WUP.

In the following case the bit is set:

- SWK is activated: due to $t_{SILENCE}$, the CAN goes into WUP detection. If a WUP is detected in this state, then the WUP_x bit is set.
- SWK is deactivated: the WUP_x bit is set if a WUP wakes up the CAN. In addition, the CAN_x_WU bit is set.
- In case WUP is detected during WUP detection 2 state (after a SYSERR_x) the bits WUP_x and CAN_x_WU are set.

The WUP_x bit is cleared automatically by the SBC at the next rearming of the CAN transceiver.

*Note: It is possible that WUF and WUP bit are set at the same time if a WUF causes a wake out of SWK, by setting the interrupt or by restart out of SBC Sleep Mode. The reason is because the CAN has been in WUP detection mode during the time of SWK mode (because of $t_{SILENCE}$). See also **Figure 10**.*

5.3.3.5 WUF Flag (WUF_x)

The WUF_x bit in the SWK_STAT_x register shows that a Wake-Up frame (WUF) has caused a wake of the CANx block. In SBC Sleep Mode this wake causes a restart, in SBC Normal Mode and in SBC Stop Mode it causes an interrupt. Also in case of this wake the bit CAN_x_WU in the register WK_STAT_x is set.

The WUF_x bit is cleared automatically by the SBC at the next rearming of the CAN SWK function.

5.3.3.6 SYSERR Flag (SYSERR_x)

The bit SYSERR_x is set in case of an configuration error and in case of an error counter overflow. The bit is only updated (set to 1) if a CANx mode with SWK is enabled via CANx bits.

When programming selective wake via CANx, SYSERR_x = 0 signals that the SWK function has been enabled. The bit can be cleared via SPI. The bit is ‘0’ after Power on reset of the SBC.

5.3.3.7 Configuration Error

A configuration error sets the SYSERR_x bit to 1. When enabling SWK via the bits CANx a config check is done. If the check is successful SWK is enabled, the bit SYSERR_x is set to 0. In SBC Normal Mode it is also possible to detect a Configuration Error while SWK is enabled, this will happen if the **CFG_VAL** bit is cleared, e.g. by changing the SWK register (from address 010 0001 to address 011 0011). In SBC Stop Mode and SBC Sleep Mode this is not possible as the SWK registers can not be changed.

Configuration Check:
in SBC Restart Mode, the **CFG_VAL** bit is cleared by the SBC. If the SBC Restart Mode was not triggered by a WUF wake up from SBC Sleep Mode and the CAN was with SWK enabled, than the SYSERR_x bit will be set.
The SYSERR_x bit has to be cleared by the microcontroller.
The SYSERR_x bit cannot be cleared when CANx_2 is '1' and below conditions occur:

- Data Valid bit not set by the microcontroller, e.g. **CFG_VAL** is not set to '1'. The **CFG_VAL** bit is reset after SWK wake and needs to be set by the microcontroller before activation SWK again.
- **CFG_VAL** bit reset by the SBC when data are changed via SPI programming. (Only possible in SBC Normal Mode).

*Note: The SWK configuration is still valid if only the **SWK_CTRL** register is modified.*

5.3.3.8 CAN BUS Time-out-Flag (CANTO_x)

In CAN WUF detection and CAN WUP detection 2 state, the bit CANTO_x is set to 1 if the time $t_{SILENCE}$ expires. The bit can be cleared by the microcontroller. If the interrupt function for CANTO_x is enabled an Interrupt is generated in SBC Stop and SBC Normal Mode when the CANTO_x set to 1. The interrupt is enabled by setting the bit **CANTO_MASK** to 1. Each CANTO_x event will trigger a interrupt even if the CANTO_x bit is not cleared.

There is no wake out of SBC Sleep Mode because of CAN time-out.

5.3.3.9 CAN BUS Silence-Flag (CANSIL_x)

In CAN WUF detection and CAN WUP detection 2 state the bit CANSIL_x is set to '1' if the time $t_{SILENCE}$ expires. The CANSIL_x bit is set back to '0' with a WUP. With this bit the microcontroller can monitor if there is activity on the CAN bus while being in SWK Mode. The bit can be read in SBC Stop and Normal Mode.

5.3.3.10 SYNC-FLAG (SYNC_x)

The bit SYNC_x shows that SWK is working and synchronous to the CAN bus. To get a SYNC_x bit set it is required to enable the CAN (CANx bits), no CAN Mode with SWK needs to be enabled.

The bit is set to 1 if a valid CAN frame has been received. It is set back to 0 if a CAN protocol error is detected. When switching into SWK mode the SYNC_x bit indicates to the µC that the frame detection is running and the next CAN frame can be detected as a WUF, CAN wake-up can now be handled by the SBC. It is possible to enter a SBC low-power mode with SWK even if the bit is not set to 1, as this is necessary in case of a silent bus.

5.3.3.11 SWK_SET FLAG (SWK_SET_x)

The status bit SWK_SET_x is set to signalize the following states (see also **Figure 7**):

- When SWK was correctly enabled in WUF Detection state.
- When SWK was correctly enabled when WUP Detection 1 state.
- After a SYSERR_x before a wake event in WUP Detection 2 state.

The bit is cleared if following conditions:

- After a wake-up (ECNT_x overflow, WUP_x in WUP detection 2, WUF_x in WUF detection).
- If CANx_2 is cleared.

5.3.4 SBC Modes for Selective Wake (SWK)

The SBC mode is selected via the **MODE** bits as described in **Chapter 5.1**.

The mode of the CAN transceiver needs to be selected in SBC Normal Mode. The CAN mode is programed the bits CANx_0, CANx_1 and CANx_2. In the low-power modes (SBC Stop and Sleep Mode) the CAN mode can not be changed via SPI.

The detailed SBC state machine diagram including the CAN selective wake feature is shown in **Figure 3**.

The application must now distinguish between the normal CAN operation an the selective wake function:

- WK Mode: This is the normal CAN wake capable mode without the selective wake function.
- SWK Mode: This is the CAN wake capable mode with the selective wake function enabled.

Figure 10 shows the possible CAN transceiver modes.

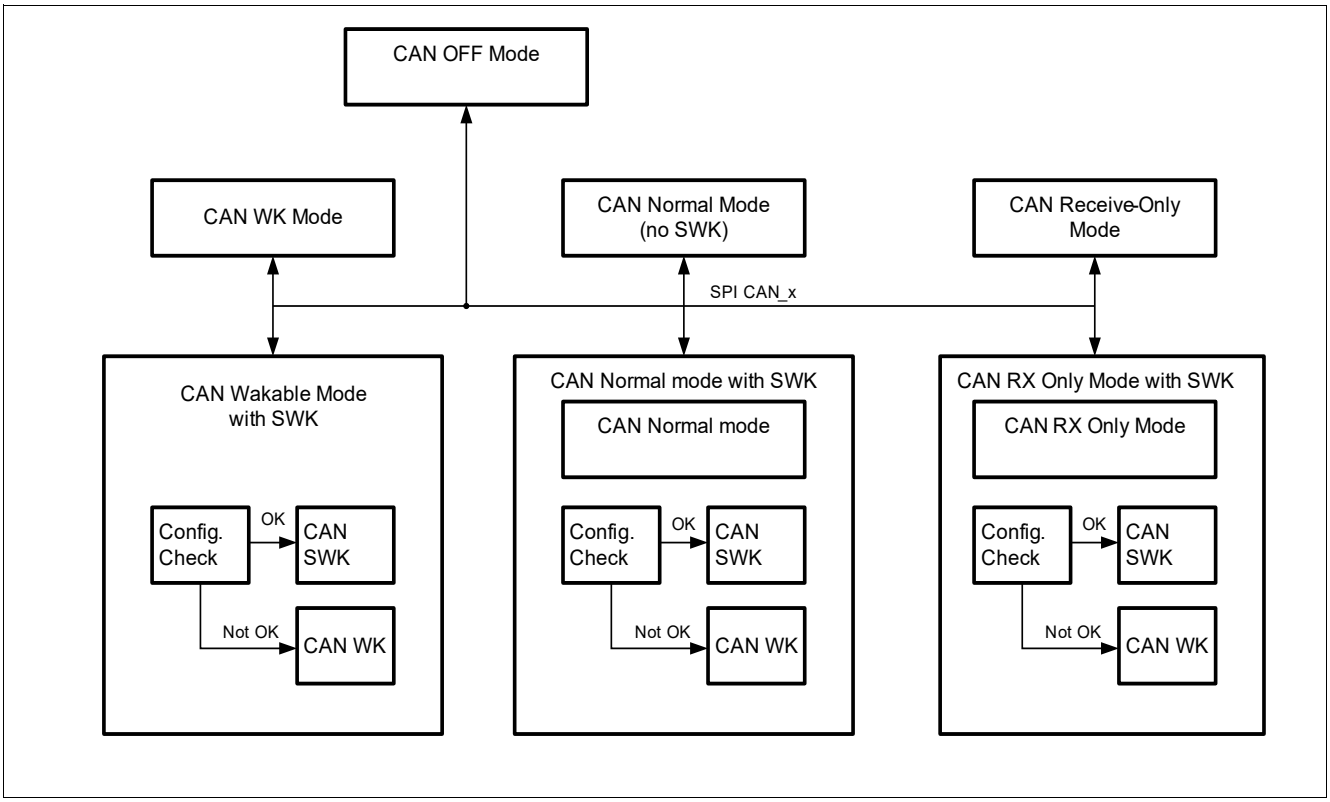


Figure 10 CAN SWK State Diagram

5.3.4.1 SBC Normal Mode with SWK

In SBC Normal Mode the CANx Transceiver can be switched into the following CAN Modes:

- CAN OFF
- CAN WK Mode (without SWK)
- CAN SWK Mode
- CAN Receive Only (No SWK activated)
- CAN Receive Only Mode with SWK
- CAN Normal Mode (No SWK activated)

- CAN Normal Mode with SWK

In the CAN Normal Mode with SWK the CANx Transceiver works as in SBC Normal Mode, so bus data is received through RXDCANx, data is transmitted through TXDCANx and sent to the bus. In addition the SWK block is active. It monitors the data on the CAN bus, updates the error counter and sets the CANSIL_x flag if there is no communication on the bus.
It will generate an CAN Wake interrupt in case a WUF is detected (RXDCANx is not pulled to LOW in this configuration).

In CAN Receive Only Mode with SWK, CAN data can be received on RXDCANx and SWK is active, no data can be sent to the bus.

The bit SYSERR_x = 0 indicates that the SWK function is enabled, and no frame error counter overflow is detected.

Table 10 CAN Modes selected via SPI in SBC Normal Mode

CAN Mode	CANx_2	CANx_1	CANx_0
CAN OFF	0	0	0
CAN WK Mode (no SWK)	0	0	1
CAN Receive Only (no SWK)	0	1	0x
CAN Normal Mode (no SWK)	0	1	1
CAN OFF	1	0	0
CAN SWK Mode	1	0	1
CAN Receive Only with SWK	1	1	0
CAN Normal Mode with SWK	1	1	1

When reading back CAN_x the programmed mode is shown in SBC Normal Mode. To read the real CAN mode the bits SYSERR_x, SWK_SET_x and CAN_x have to be evaluated. A change out of SBC Normal Mode can change the CAN_x_0 and CAN_x_1 bits.

5.3.4.2 SBC Stop Mode with SWK

In SBC Stop Mode the CANx Transceiver can be operated with the following CAN Modes:

- CAN OFF
- CAN WK Mode (no SWK)
- CAN SWK Mode
- CAN Receive Only (no SWK)

To enable CAN SWK Mode the CANx has to be switched to “CAN Normal Mode with SWK”, “CAN Receive Only Mode with SWK” or to “CAN SWK Mode” in SBC Normal Mode before sending the SBC to SBC Stop Mode. The bit SYSERR_x = 0 indicates that the SWK function is enabled. The table shows the change of CAN Mode when switching from SBC Normal Mode to SBC Stop Mode.

Note: CAN Receive Only Mode in SBC Stop Mode is implemented to also enable pretended networking (Partial networking done in the microcontroller).

Table 11 CAN Modes change when switching from SBC Normal Mode to SBC Stop Mode

Programmed CAN Mode in SBC Normal Mode	CANx Modes	SYSERR_x bit	CAN Mode in SBC Stop Mode	CANx Modes
CAN OFF	000	0	CAN OFF	000
CAN WK Mode (no SWK)	001	0	CAN WK Mode (no SWK)	001
CAN Receive Only (no SWK)	010	0	CAN Receive Only (no SWK)	010
CAN Normal Mode (no SWK)	011	0	CAN WK Mode (no SWK)	001
CAN OFF	100	0	CAN OFF	100
CAN SWK Mode	101	0	CAN SWK Mode	101
CAN SWK Mode	101	1	CAN WK Mode (no SWK)	101
CAN Receive Only with SWK	110	0	CAN Receive Only with SWK	110
CAN Receive Only with SWK	110	1	CAN Receive Only (no SWK)	110
CAN Normal Mode with SWK	111	0	CAN WK Mode with SWK	101
CAN Normal Mode with SWK	111	1	CAN WK Mode (no SWK)	101

Note: When SYSERR_x is set it is true that we will not detect WUF frames, so no selective wake function active (no SWK), but the MSB of CAN mode is not changed in the register.

5.3.4.3 SBC Sleep Mode with SWK

In SBC Sleep Mode the CANx Transceiver can be switched into the following CAN Modes:

- CAN OFF
- CAN WK Mode (without SWK)
- CAN SWK Mode

To enable “CAN SWK Mode” the CAN has to be switched to “CAN Normal Mode with SWK”, “CAN Receive Only Mode with SWK” or to “CAN SWK Mode” in SBC Normal Mode before sending the device to SBC Sleep Mode. The table shows the change of CAN mode when switching from SBC Normal Mode to Sleep Mode.

A wake from Sleep Mode with Selective Wake (Valid WUF) leads to SBC Restart Mode. In SBC Restart Mode the CFG_VAL bit will be cleared by the SBC, the SYSERR_x bit is not set. In the BUS_CTRL_x register, the programmed CAN SWK Mode (101) can be read.

To enable the CAN SWK Mode again and to enter SBC Sleep Mode the following sequence can be used; Program a CAN Mode different from CAN SWK Mode (101, 110, 111), set the CFG_VAL, clear SYSERR_x bit, set CANx transceiver to CAN SWK Mode (101), switch SBC to SBC Sleep Mode.

To enable the CAN WK Mode or CAN SWK Mode again after a wake on CANx, a rearming is required. The rearming is done by programming the CANx transceiver into a different mode and back into the CAN WK Mode or CAN SWK Mode. To avoid lock-up when switching the SBC into SBC Sleep Mode with an already woken CANx transceiver, the SBC does an automatic rearming of the CANx transceiver when switching into Sleep Mode. So after switching into SBC Sleep Mode the CANx transceiver is either in CAN SWK Mode or CAN WK Mode depending on CANx_2 setting and SYSERR_x bit (If CAN is switched to OFF Mode it is also OFF in Sleep Mode)

Table 12 CAN Modes change when switching to SBC Sleep Mode

Programmed CAN Mode in SBC Normal Mode	CANx Modes	SYSERR_ x bit	CAN Mode in SBC Sleep Mode	CANx Modes
CAN OFF	000	0	CAN OFF	000
CAN WK Mode (no SWK)	001	0	CAN WK Mode (no SWK)	001
CAN Receive Only (no SWK)	010	0	CAN WK Mode (no SWK)	001
CAN Normal Mode (no SWK)	011	0	CAN WK Mode (no SWK)	001
CAN OFF	100	0	CAN OFF	100
CAN SWK Mode	101	0	CAN SWK Mode	101
CAN SWK Mode	101	1	CAN WK Mode (no SWK)	101
CAN Receive Only with SWK	110	0	CAN SWK Mode	101
CAN Receive Only with SWK	110	1	CAN WK Mode (no SWK)	101
CAN Normal Mode with SWK	111	0	CAN SWK Mode	101
CAN Normal Mode with SWK	111	1	CAN WK Mode (no SWK)	101

5.3.4.4 SBC Restart Mode with SWK

If SBC Restart Mode is entered the transceiver can change the CAN mode. During Restart or after Restart the following modes are possible:

- CAN OFF
- CAN WK Mode (either still wake cable or already woken up)
- CAN SWK Mode (WUF Wake from Sleep)

Table 13 CAN Modes change in case of Restart out of SBC Normal Mode

Programmed CAN Mode in SBC Normal Mode	CANx Modes	SYSERR_ x bit	CAN Mode in and after SBC Restart Mode	CANx Modes	SYSERR _x bit
CAN OFF	000	0	CAN OFF	000	0
CAN WK Mode (no SWK)	001	0	CAN WK Mode (no SWK)	001	0
CAN Receive Only (no SWK)	010	0	CAN WK Mode (no SWK)	001	0
CAN Normal Mode (no SWK)	011	0	CAN WK Mode (no SWK)	001	0
CAN OFF	100	0	CAN OFF	100	0
CAN SWK Mode	101	0	CAN WK Mode (no SWK)	101	1
CAN SWK Mode	101	1	CAN WK Mode (no SWK)	101	1
CAN Receive Only with SWK	110	0	CAN WK Mode (no SWK)	101	1
CAN Receive Only with SWK	110	1	CAN WK Mode (no SWK)	101	1
CAN Normal Mode with SWK	111	0	CAN WK Mode (no SWK)	101	1
CAN Normal Mode with SWK	111	1	CAN WK Mode (no SWK)	101	1

The various reasons for entering SBC Restart Mode and the respective status flag settings are shown in **Table 14**.

Table 14 CAN Modes change in case of Restart out of SBC Sleep Mode

CAN Mode in SBC Sleep Mode	CAN Mode in and after SBC Restart Mode	CANx Modes	SYS ERR_x	CAN_x_WU	WUP_x	WUF_x	ECNT_x bits	Reason for Restart
CAN OFF	CAN OFF	000	0	0	0	0	0	Wake on other wake source
CAN WK Mode	CAN woken up	001	0	1	1	0	0	Wake (WUP) on CAN
CAN WK Mode	CAN WK Mode	001	0	0	0	0	0	Wake on other wake source
CAN SWK Mode	CAN woken up	101	0	1	0/1[1)]	1	x	Wake (WUF) on CAN
CAN SWK Mode	CAN woken up	101	1	1	0/1[2)]	0	100000	Wake due to error counter overflow
CAN SWK selected, CAN WK active	CAN woken up	101	1	1	1	0	0	Wake (WUP) on CAN, config check was not pass
CAN SWK Mode	CAN WK Mode	101	1	0	0/1	0	x	Wake on other wake source

1) In case there is a WUF detection within $t_{SILENCE}$ then the WUP_x bit will not be set. Otherwise it will always be set together with the WUF_x bit.

2) In some cases the WUP_x bit might stay cleared even after $t_{SILENCE}$, e.g. when the error counter expires without detecting a wake up pattern

5.3.4.5 SBC Fail-Safe Mode with SWK

When SBC Fail-Safe Mode is entered the CAN transceiver is automatically set into WK Mode (wake capable) without the selective wake function.

5.3.5 Wake-up

A wake-up via CAN leads to a restart out of SBC Sleep Mode and to an interrupt in SBC Normal Mode, and in SBC Stop Mode. After the wake event the bit CAN_x_WU is set, and the details about the wake can be read out of the bits WUP_x, WUF_x, SYSERR_x and ECNT_x bits.

5.3.6 Configuration for SWK

The CAN protocol handler settings can be configured in following registers:

- **SWK_BTL1_CTRL**defines the number of time quanta in a bit time. This number depends also on the internal clock settings performed in the register **SWK_CDR_CTRL2**.
- **SWK_BTL2_CTRL**defines the sampling point position.
- The respective receiver during frame detection mode can be selected via the bit **RX_WK_SEL**.
- The clock and data recovery (see also **Chapter 5.3.8.2**) can be configured in the registers **SWK_CDR_CTRL1**, **SWK_CDR_CTRL2**, **SWK_CDR_LIMIT_HIGH_CTRL** and **SWK_CDR_LIMIT_LOW_CTRL**.

The actual configuration for selective wake is done via the Selective Wake Control Registers SWK_IDx_CTRL, SWK_MASK_IDx_CTRL, SWK_DLC_CTRL, SWK_DATAx_CTRL.

The oscillator has the option to be trimmed by the microcontroller. To measure the oscillator, the SPI bit **OSC_CAL** needs to be set to 1 and a defined pulse needs to be given to the TXDCANx pin by the microcontroller (e.g. 1µs pulse, CANx needs to be switched off before). The SBC measures the length of the pulse by counting the time with the integrated oscillator. The counter value can be read out of the register **SWK_OSC_CAL_H_STAT** and **SWK_OSC_CAL_L_STAT**. To change the oscillator the trimming function needs to be enabled by setting the bits TRIM_EN_x = 11 (and **OSC_CAL** = 1). The oscillator can then be adjusted by writing into the registers **SWK_OSC_TRIM_CTRL** and **SWK_OPT_CTRL**. To finish the trimming, the bits TRIM_EN_x need to be set back to “00”.

5.3.7 CAN Flexible Data Rate (CAN FD) Tolerant Mode

The CAN FD tolerant mode can be activated by setting the bit **CAN_FD_EN** = 1 in the register **SWK_CAN_FD_CTRL**. With this mode the internal CANx frame decoding will be stopped for CAN FD frame formats:

- The high baud rate part of a CAN FD frame will be ignored.
- No Error Handling (Bit Stuffing, CRC checking, Form Errors) will be applied to remaining CAN frame Fields (Data Field, CRC Field, …).
- No wake up is done on CAN FD frames.

The internal CAN frame decoder will be ready for new CAN frame reception when the End of frame (EOF) of a CAN FD frame is detected.The identification for a CAN FD frame is based on the EDL Bit, which is sent in the Control Field of a CAN FD frame:

- EDL Bit = 1 identifies the current frame as an CAN FD frame and will stop further decoding on it.
- EDL Bit = 0 identifies the current frame as CAN 2.0 frame and processing of the frame will be continued.

In this way it is possible to send mixed CAN frame formats without affecting the selective wake functionality by error counter increment and subsequent misleading wake up.In addition to the **CAN_FD_EN** bit also a filter setting must be provided for the CAN FD tolerant mode. This filter setting defines the minimum dominant time for a CAN FD dominant bit which will be considered as a dominant bit from the CAN FD frame decoder. This value must be aligned with the selected high baud rate of the data field in the CAN network.

To support programming via CAN during CAN FD mode a dedicated SPI bit **DIS_ERR_CNT** is available to avoid an overflow of the implemented error counter (see also **Chapter 5.3.2.4**).

The behavior of the error counter depends on the setting of the bits **DIS_ERR_CNT** and **CAN_FD_EN** and is show in below table:

Table 15 Error Counter Behavior

DIS_ERR_CNT setting	**CAN_FD_EN setting**	**Error Counter Behavior**
0	0	Error Counter counts up when a CAN FD frame or an incorrect/corrupted CAN frame is received; counts down when a CAN frame is received properly (as specified in ISO 11898-6)
1	0	Error Counter counts up when a CAN FD frame or an incorrect/corrupted CAN frame is received; counts down when a CAN frame is received properly (as specified in ISO 11898-6)

Table 15 Error Counter Behavior (cont'd)

DIS_ERR_CNT setting	CAN_FD_EN setting	Error Counter Behavior
0	1	Error Counter counts down when correct CAN (incl. CAN FD) frame is received
1	1	Error Counter is and stays cleared to avoid an overflow during programming via CAN

The **DIS_ERR_CNT** bit is automatically cleared at $t_{SILENCE}$ expiration.

5.3.8 Clock and Data Recovery

In order to compensate possible deviations on the CAN oscillator frequency caused by assembly and lifetime effects, the device features an integrated clock and data recovery (CDR).

It is recommended to always enable the CDR feature during SWK operation.

5.3.8.1 Configuring the Clock Data Recovery for SWK

The Clock and Data Recovery can be optionally enabled or disabled with the **CDR_EN** Bit in the **SWK_CDR_CTRL1** SPI Register. In case the feature is enabled, the CAN bit stream will be measured and the internal clock used for the CAN frame decoding will be updated accordingly. Before the Clock and Data Recovery can be used it must be configured properly related to the used baud rate and filtering characteristics (refer to **Chapter 5.3.8.2**).

It is strongly recommended to not enable/disable the Clock Recovery during a active CAN Communication.

To ensure this it is recommended to enable/disable it during CAN OFF.

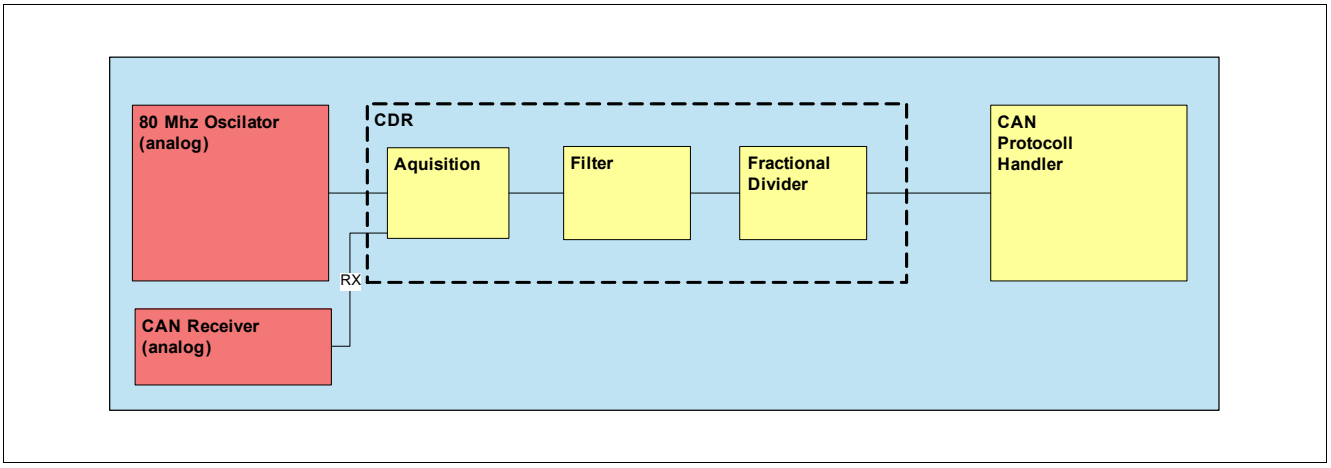


Figure 11 Clock and Data Recovery Block Diagram

5.3.8.2 Setup of Clock and Data Recovery

It is strongly recommended to enable the clock and data recovery feature only when the setup of the clock and data recovery is finished.

The following sequence should be followed for enabling the clock and data recovery feature:

- Step 1: Switch CANx to OFF and **CDR_EN** to OFF
  Write SPI Register BUS_CTRL_x (CANx = 000).
- Step 2: Configure CDR Input clock frequency
  Write SPI Register **SWK_CDR_CTRL2** (SEL_OSC_CLK[1:0]).

- Step 3: Configure Bit timing Logic
  Write SPI Register **SWK_BTL1_CTRL** and adjusting **SWK_CDR_LIMIT_HIGH_CTRL** and **SWK_CDR_LIMIT_LOW_CTRL** according to **Table 33**.
- Step 4: Enable Clock and Data Recovery
  Choose filter settings for Clock and Data recovery. Write SPI Register **SWK_CDR_CTRL1** with **CDR_EN** = 1

Additional hints for the CDR configuration and operation:

- Even if the CDR is disabled, when the baud rate is changed, the settings of **SEL_OSC_CLK** in the register **SWK_CDR_CTRL1** and **SWK_BTL1_CTRL** have to be updated accordingly.
- The **SWK_CDR_LIMIT_HIGH_CTRL** and **SWK_CDR_LIMIT_LOW_CTRL** registers have to be also updated when the baud rate or clock frequency is changed (the CDR is discarding all the acquisitions and looses all acquired information, if the limits are reached - the **SWK_BTL1_CTRL** value is reloaded as starting point for the next acquisitions).
- When updating the CDR registers, it is recommended to disable the CDR and to enable it again only after the new settings are updated.
- The **SWK_BTL2_CTRL** register represents the sampling point position. It is recommended to be used at default value: 11 0011 (~80%).

5.3.9 Electrical Characteristics

Table 16 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40°C to +150°C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60 Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CAN Partial Network Timing							
Time-out for bus inactivity	$t_{SILENCE}$	0.6	–	1.2	s	1)	P_5.3.1
Bias reaction time	t_{bias}	–	–	200	µs	1) Load R_L = 60 Ω, C_L = 100 pF, C_{GND} = 100 pF	P_5.3.2
Wake-up reaction time (WUP or WUF)	$t_{WU\_WUP/WUF}$	–	–	100	µs	1)2)3) Wake-up reaction time after a valid WUP or WUF;	P_5.3.3
Min. Bit Time	t_{Bit_min}	1	–	–	µs	1)4)	P_5.3.4
CAN FD Tolerance[5]							
SOF acceptance	n_{Bits_idle}	6	–	10	bits	6)Number of recessive bits before a new SOF shall be accepted	P_5.3.5
Dominant signals which are ignored (up to 2 MBit/s)	$t_{FD\_Glitch\_4}$	0	–	5	%	6)7)8) of arbitration bit time; to be configured via **FD_FILTER**;	P_5.3.6
Dominant signals which are ignored (up to 5 MBit/s)	$t_{FD\_Glitch\_10}$	0	–	2.5	%	6)7)9) of arbitration bit time; to be configured via **FD_FILTER**;	P_5.3.7
Signals which are detected as a dominant data bit after the FDF bit and before EOF bit (up to 2 MBit/s)	$t_{FD\_DOM\_4}$	17.5	–	–	%	6)7)8) of arbitration bit time; to be configured via **FD_FILTER**;	P_5.3.8
Signals which are detected as a dominant data bit after the FDF bit and before EOF bit (up to 5 MBit/s)	$t_{FD\_DOM\_10}$	8.75	–	–	%	6)7)9) of arbitration bit time; to be configured via **FD_FILTER**;	P_5.3.9

1) Not subject to production test, tolerance defined by internal oscillator tolerance.

2) Wake-up is signalized via INTN pin activation in SBC Stop Mode and via VCC1 ramping up with wake from SBC Sleep Mode.

3) For WUP: time starts with end of last dominant phase of WUP; for WUF: time starts with end of CRC delimiter of the WUF.
4) The minimum bit time corresponds to a maximum bit rate of 1 Mbit/s. The lower end of the bit rate depends on the protocol IC or the permanent dominant detection circuitry preventing a permanently dominant clamped bus.
5) Applies for an arbitration rate of up to 500 kbps until the FDF bit is detected.
6) Not subject to production test; specified by design.
7) Parameter applies only for the Normal Mode CAN receiver (RX_WK_sel = 0).
8) A data phase bit rate less or equal to four times of the arbitration bit rate or 2 Mbit/s, whichever is lower.
9) A data phase bit rate less or equal to ten times of the arbitration bit rate or 5 Mbit/s, whichever is lower.

6 DC/DC Regulator

6.1 Block Description

The SMPS module in the TLE9278-3BQX V33 is implemented as a cascade of a step-up regulator followed by a step-down post-regulator. The step-up regulator (DC/DC Boost converter) provides a V_S level which permits the step-down post-regulator (DC/DC Buck converter) to regulate without entering a low-drop condition.

The SMPS module is active in SBC Normal, Stop and Restart Mode. In SBC Sleep and Fail-Safe Mode, the SMPS module is disabled.

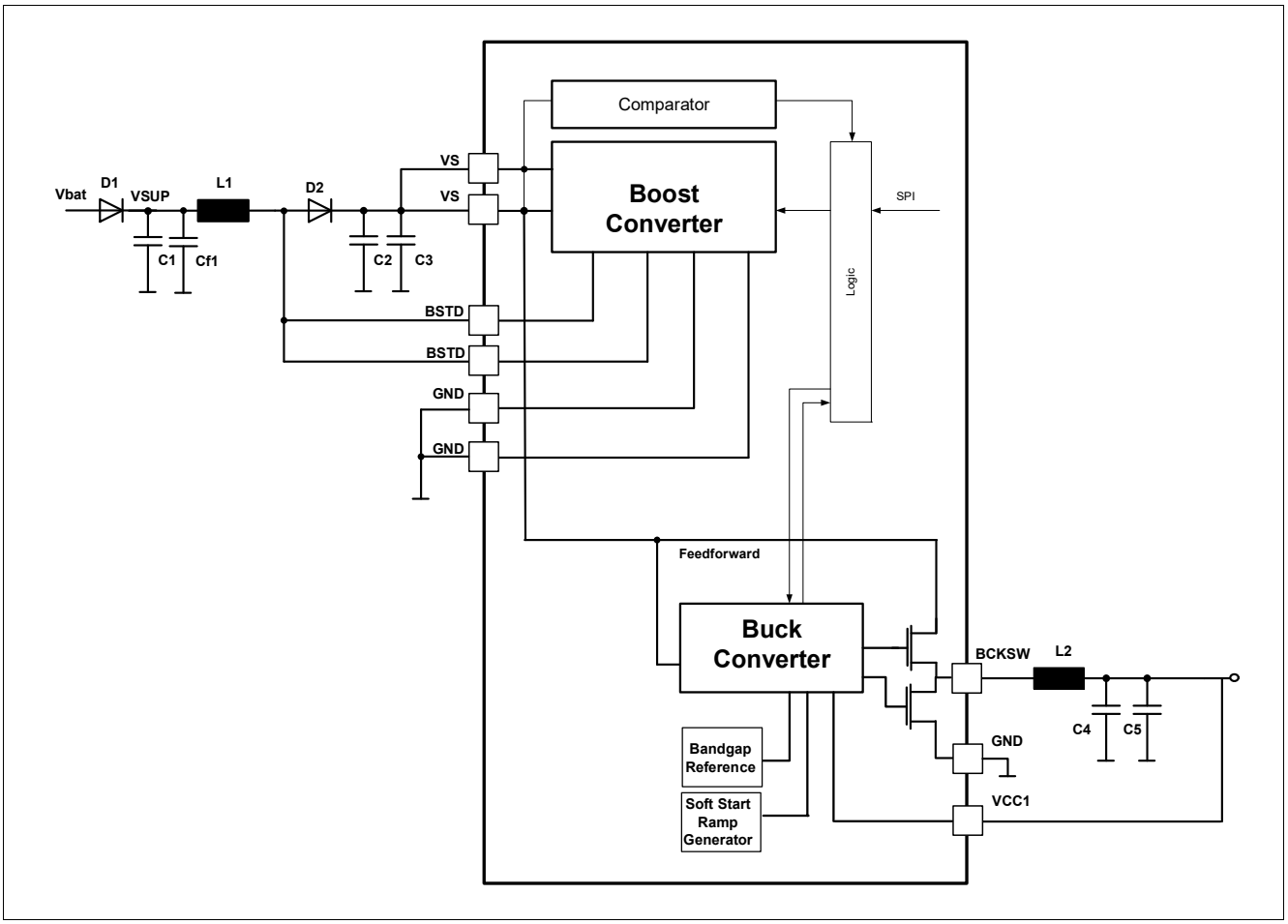


Figure 12 DC/DC Block Diagram

Functional Features

- 3.3 V SMPS (DC/DC) Buck Regulator with integrated high-side and low-side power switching transistor.
- SMPS (DC/DC) Boost Regulator for low V_{SUP} supply voltage with integrated power transistor.
- Adjustable output DC/DC Boost pre-regulator voltage via SPI.
- Fixed switching frequency for Buck and Boost Regulator in SBC Normal Mode in PWM (Pulse Width Modulation).
- PFM (Pulse Frequency Modulation) for Buck converter in SBC Stop Mode to reduce the quiescent current.
- Automatic transition PFM to PWM in SBC Stop Mode.
- Soft start-up.

- Edge Shaping for better EMC performances for Buck and Boost regulator.
- Undervoltage monitoring via VIO pin with adjustable reset level (refer to **Chapter 12.7**).
- Overvoltage detection via VIO pin activates the FO pin in case that **VIO_OV_RST** bit is set (refer to **Chapter 12.8**).
- Buck short circuit detection.
- Buck 100% Duty Cycle at low V_S operation.
- Buck overcurrent peak detection.
- Boost overcurrent peak detection.

6.1.1 Functional Description of the Buck Converter

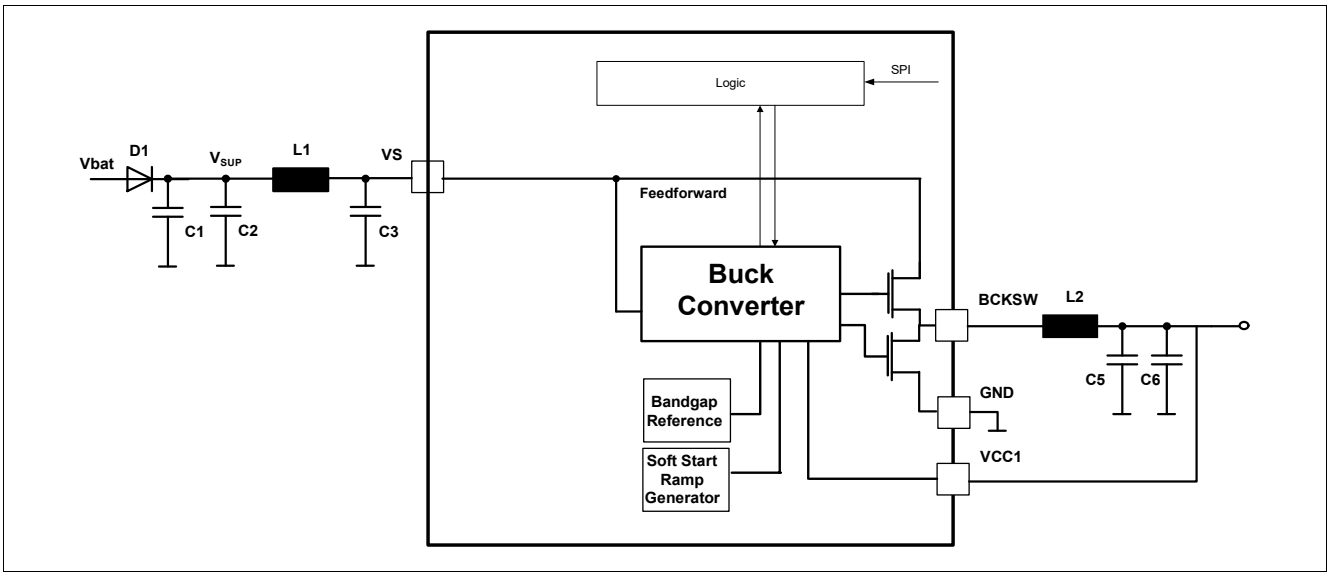


Figure 13 Buck Block Diagram

The DC/DC Buck converter is intended as post-regulator (VCC1) and it provides a step down converter function transferring energy from V_S to a lower output voltage with high efficiency (typically more than 80%). The output voltage is 3.3 V in a current range up to 750 mA. It is regulated via a digital loop with a precision of ±2%.

It requires an external inductor and capacitor filter on the output switching pin (BCKSW). The Buck regulator has integrated high-side and low-side power switching transistors. The compensation of the regulation loop is done internally and no additional external components are needed.

A typical application example and external components proposal is available in **Chapter 14.1**.

The Buck converter is active in SBC Normal, Stop and Restart Mode and it is disabled in SBC Sleep and Fail-Safe Mode.

Depending on the SBC Mode, the Buck converter works in two different modes:

- PWM Mode (Pulse Width Modulation): This mode is available in SBC Normal Mode, SBC Restart Mode and SBC Stop Mode (only for automatic or manual PFM to PWM transitions. Refer to **Chapter 6.2.2**). In PWM, the Buck converter operates with a fixed switching frequency (f_{BUK}). The duty cycle is calculated internally based on input voltage, output voltage and output current. The precision is ±2% on input supply and output current range (refer to **Figure 18** for more information). In PWM Mode, the Buck converter is capable of a 100% duty cycle in case of low V_S conditions. In order to reduce EMC, the edge shaping feature has been implemented to control the activation and deactivation of the two power switches.

- PFM Mode (Pulse Frequency Modulation): This mode is activated automatically when the SBC Stop Mode is entered. The PFM Mode is an asynchronous mode. PFM Mode does not have a controller switching frequency. The switching frequency depends on conditions of the Buck regulator such as the following: input supply voltage, output voltage, output current and external components. A typical timing diagram is shown in **Figure 14**. The Buck converter in PFM Mode has a tolerance of ±4%. The transition from PFM mode to PWM mode is described in **Chapter 6.2.2**.

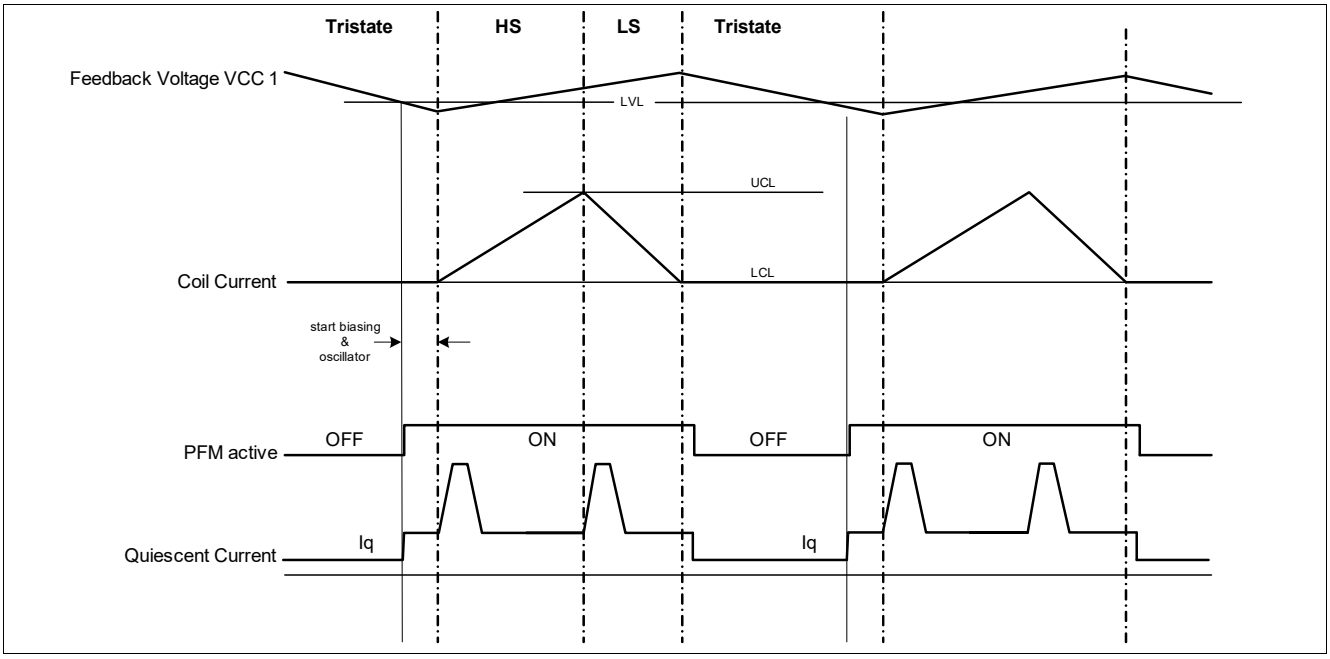


Figure 14 Typical PFM timing diagram

6.1.1.1 Startup Procedure (Soft Start)

The Startup Procedure (Soft Start) permits to achieve the Buck regulator output voltage avoiding large overshoot on the output voltage. This feature is activated during the power-up, from SBC Sleep to Restart Mode and from SBC Fail-Safe to SBC Restart Mode.

When the Buck regulator is activated, it starts in open loop with a minimum duty cycle which is maintained for a limited number of switching periods. After this first phase, the duty cycle is linearly increased by a fixed step and it is maintained for a limited number of switching periods for each duty cycle step. This procedure is repeated until the target output voltage value of the Buck regulator is reached. As soon as the Buck regulator output voltage is reached, the regulation loop is closed and it starts to operate normally using PWM Mode adjusting the duty cycle according to the Buck input and output voltages and the output current.

6.1.1.2 Buck regulator Status register

The register **SMPS_STAT** contains information about the open or short conditions on BCKSW pin. No SBC Mode or configuration changes are triggered if one bit on **SMPS_STAT** register is set.

6.1.1.3 External components

The Buck converter needs one inductor and output capacitor filter. The inductor has a fixed value of 47 µH. Secondary parameters such as saturation current must be selected based on the maximum current capability needed in the application.

The output filter capacitors are two parallel 22 µF ceramic capacitor. For additional information, refer to **Chapter 14.1**.

6.1.2 Functional Description of the Boost Converter

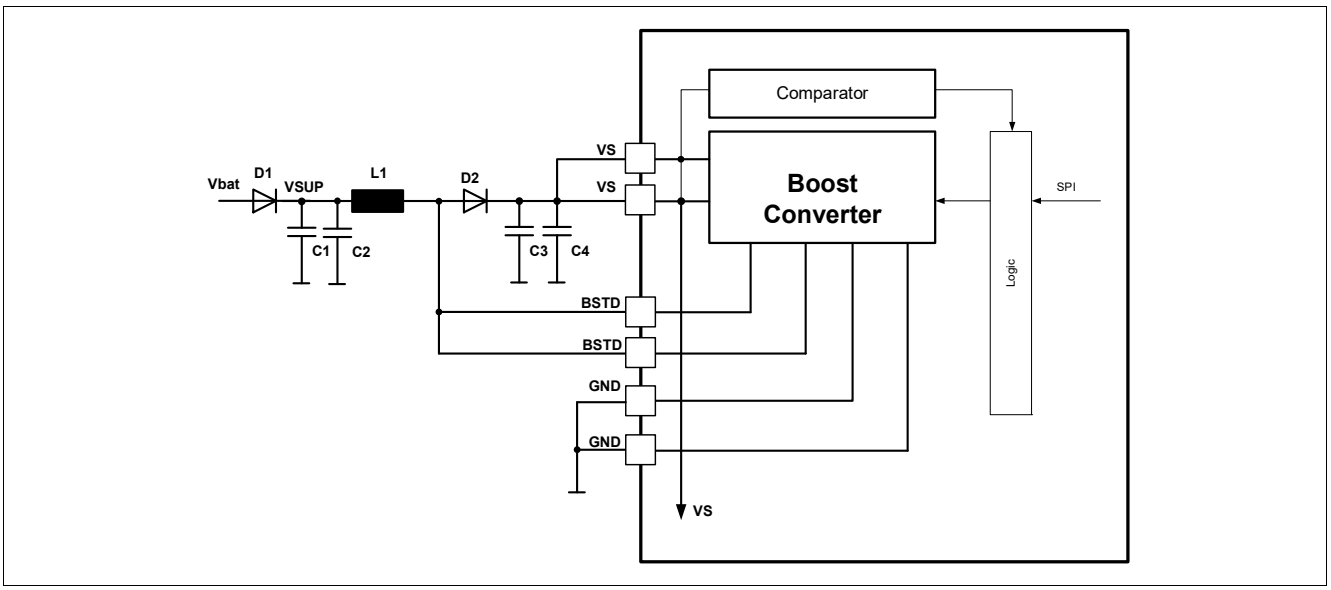


Figure 15 Boost Block Diagram

The Boost converter is intended as a pre-regulator and it provides a step up converter function. It transfers energy from an input supply V_{SUP} (battery voltage after reverse protection circuit) to a higher output voltage (V_S) with high efficiency (typically more than 80%).

The regulator integrates the power switching and the sense resistor for overcurrent detection.

The Boost regulator can be enabled in SBC Normal Mode via SPI (register **HW_CTRL_0**, bit **BOOST_EN**) and four output voltage values are selectable via **BOOST_V**. The Boost regulator can also be active in SBC Stop and Restart Mode. The selected boost output voltage will automatically define the voltage thresholds where the boost will be ON (**$V_{BST,TH1}$**, **$V_{BST,TH2}$**, **$V_{BST,TH3}$** and **$V_{BST,TH4}$**). If the Boost regulator is enabled, it switches ON automatically when V_S falls below the selected threshold voltage and switches OFF when crossing this threshold including hysteresis again. The bit **BST_ACT** on **SMPS_STAT** register indicates that the Boost has been activated.

The Boost output voltage can be changed only if **BOOST_EN** is set to 0. In case that the boost output voltage configuration changes with **BOOST_EN** set to 1, the **SPI_FAIL** bit is set and the command is ignored.

Figure 16 shows the typical timing for enabling the Boost converter.

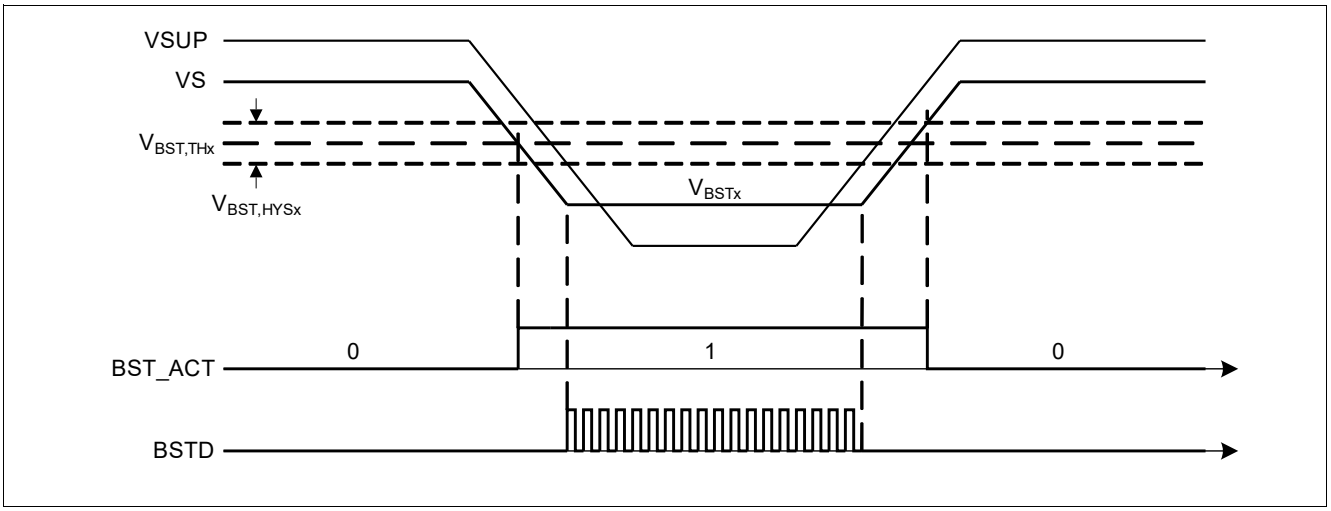


Figure 16 Boost converter activation

The Boost regulator works in PWM Mode with fixed frequency (f_{BST}) and a tolerance of ±3%.

If the Boost is enabled in Stop Mode, the quiescent current in the SBC is increased (P_4.4.31).

6.1.2.1 Boost Regulator Status register

The register **SMPS_STAT** contains information about the open or short conditions on Boost pins including loss of GND detection. No SBC mode or configuration is triggered if one bit is set on the **SMPS_STAT** register.

6.1.2.2 External Components

The Boost converter requires a number of external components such as the following: input buffer capacitor on the battery voltage, inductor, freewheeling diode and filter capacitors.

For recommend external components and corresponding values, refer to **Chapter 14.1**.

6.2 Power Scenarios

The chapter describes the features and performance of the Buck regulator according to SBC modes. The Boost module works only in SBC Normal or Stop Mode using PWM modulation (refer also to **Chapter 6.1.2**).

6.2.1 Buck behavior in SBC Normal Mode

In SBC Normal Mode the Buck works is in PWM mode with fixed switching frequency. All supervision functions for Buck converter are available in SBC Normal Mode and available depending the device configuration (**Chapter 5.1.1**). For additional details on the supervision functions, refer to **Chapter 12.7**, **Chapter 12.8**, **Chapter 12.9** and **Chapter 12.11**.

6.2.2 Buck behavior in SBC Stop Mode

The SBC Stop Mode operation is intended to reduce the total amount of quiescent current while still providing output voltage. In order to achieve this, the Buck regulator changes the modulation from PWM (Pulse Width Modulation) to PFM (Pulse Frequency Modulation) when entering SBC Stop Mode.

In SBC Stop Mode, the Buck modulation can change as follow:

- Buck module always in PFM modulation (default setting).
- Automatically change from PFM to PWM (setting **PWM_AUTO**).
- Modulation is controlled by the WK pin (setting **PWM_BY_WK**).

If the **PWM_BY_WK** and **PWM_AUTO** are set at the same time, the **PWM_AUTO** has highest priority and PWM automatic transition will be used.

If **PWM_BY_WK** and **PWM_AUTO** are at the same time set to 0, the buck module remains in PFM in SBC Stop Mode.

If in SBC Stop Mode the Buck modulation is PWM, the buck output voltage tolerance and output current capability are like SBC Normal Mode (P_6.5.13 and P_6.5.46).

6.2.2.1 Automatic Transition from PFM to PWM in SBC Stop Mode

If more current is needed, an automatic transition from PFM to PWM mode is implemented. When the Buck regulator output current exceeds the $I_{PFM-PWM,TH}$ threshold, the Buck module changes the modulation to PWM and an INTN event is generated. In addition, the **PFM_PWM** bit on **WK_STAT_0** is set.

In order to set the Buck modulation again in PFM mode, a SBC Stop Mode command has to be write to **M_S_CTRL** register. This command has to be sent when the required Buck output current is below the $I_{PFM-PWM,TH}$ threshold.

By default, the feature is disable. To enable the automatic transition from PFM to PWM, the **PWM_AUTO** bit in **HW_CTRL_0** has to be set before entering SBC Stop Mode.

When entering SBC Stop Mode, the automatic transition from PFM to PWM mode is activated after the transition time (t_{lag}), during which the Buck regulator loop changes the modulation technique. **Figure 17** shows the timing transition from SBC Normal to Stop Mode.

The transition time t_{lag} is always implemented in case of transition from PWM to PFM modulation.

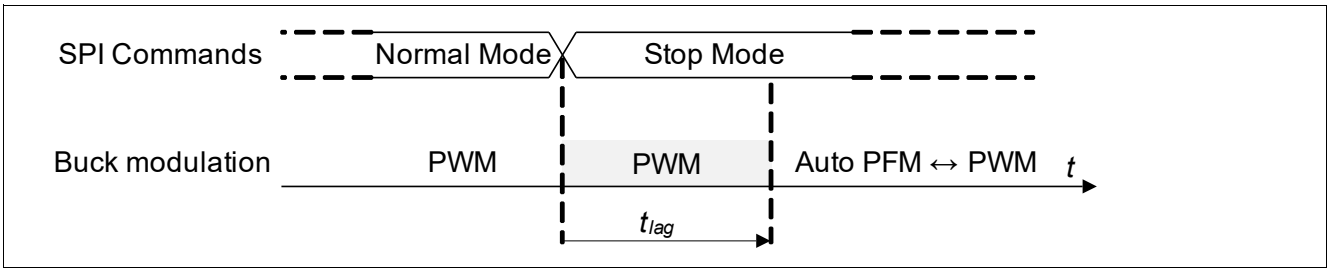


Figure 17 Transition from SBC Normal to SBC Stop Mode

The t_{lag} can be configured via SPI using the **PWM_TLAG** in **HW_CTRL_0** register.

The automatic transition from PFM to PWM can be disabled by setting the **PWM_AUTO** to 0 in the **HW_CTRL_0** register.

6.2.2.2 Manual Transition from PFM to PWM in SBC Stop Mode

The PFM to PWM transition can also be controlled by the microcontroller or an external signal by using the WK pin as a trigger signal in SBC Stop Mode.

When the **PWM_BY_WK** bit is set to 1, the Buck regulator can be switched from PFM to PWM using the WK pin.

A LOW level at the WK pin will switch the Buck converter to PFM mode, a HIGH level will switch the Buck converter to PWM Mode. In this configuration, the transition time t_{lag} is not taken into account because a defined signal from microcontroller or external source is expected.

6.2.2.3 SBC Stop to Normal Mode transition

The microcontroller sends an SPI command to switch from SBC Stop Mode to SBC Normal Mode. In this transition, the Buck regulator changes the modulation from PFM to PWM.

Once the SPI command for the SBC Normal Mode transition is received, the Buck output current is able to rise above the specified maximum Stop Mode current ($I_{PFM-PWM,TH}$).

If the transition from SBC Stop Mode to SBC Normal Mode is carried out when the Boost is enabled and operating, it will continue to operate without any changes.

6.2.3 Buck behavior in SBC Sleep or Fail Safe Mode

In SBC Sleep or Fail Safe Mode, the Buck and Boost converter are off and not operating. The lowest quiescent current is achievable.

6.2.3.1 SBC Sleep/Fail Safe Mode to SBC Normal Mode transition

In case of a wake-up event from WK pin or transceivers, the SBC will be set to SBC Restart Mode and as soon as the reset is released, into SBC Normal Mode.

In SBC Restart Mode, the Buck regulator is activated and ramping-up. The Boost regulator is activated and ramping-up again (in case the V_S is below the selected threshold) in according the configuration selected in SBC Normal Mode. As soon as the Buck output voltage exceeds the reset threshold, the RSTN pin is released.

6.3 Electrical Characteristics

Table 17 Electrical Characteristics

T_j = -40°C to +150°C; V_S = 5.5 V to 28 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Buck Regulator							
Output Voltage PWM including Line and Load regulation	$V_{CC1,out1}$	3.23	3.3	3.37	V	SBC Normal Mode (PWM) 1 mA < I_{VCC1} < 750 mA 6.5 V < V_S < 28 V Boost Disable	P_6.5.13
Output Voltage PWM including Line and Load regulation	$V_{CC1,out1}$	3.23	3.3	3.37	V	1) SBC Normal Mode (PWM) I_{VCC1} = 400 mA V_S =4 V Boost Disable	P_6.5.46
Output Voltage PFM including Line and Load regulation	$V_{CC1,out2}$	3.16	3.3	3.44	V	SBC Stop Mode (PFM) 10 µA < I_{VCC1} < $I_{PFM-PWM,TH}$ 6.5 V < V_S < 28 V Boost Disable	P_6.5.14
Output Voltage PFM including Line and Load regulation	$V_{CC1,out3}$	3.18	3.3	3.39	V	SBC Stop Mode (PFM) 10 µA < I_{VCC1} < 50 mA 6.5 V < V_S < 28 V Boost Disable	P_6.5.48
Power Stage on-resistance High-Side	$R_{DSON1,HS}$	–	–	1.3	Ω	V_S = 6.5 V I_{VS} = 100 mA	P_6.5.3
Power Stage on-resistance Low-Side	$R_{DSON1,LS}$	–	–	1.3	Ω	I_{BCKSW} = 100 mA	P_6.5.20
Overcurrent peak limitation internal high side	$I_{BCK\_LIM,TH}$	0.85	1.05	1.2	A	V_S > 6.5 V	P_6.5.40
Buck switching frequency	f_{BUK}	405	450	495	kHz	SBC Normal Mode (PWM)	P_6.5.5
Automatic transition PFM to PWM threshold	$I_{PFM-PWM,TH}$	80	110	150	mA	1) SBC Stop Mode (PFM) 6.5 V < V_S < 28 V	P_6.5.6
Transition time from PWM to PFM	t_{lag}	–	1	–	ms	1) **PWM_TLAG**=1 (on **HW_CTRL_0**)	P_6.5.15
Transition time from PWM to PFM	t_{lag}	–	100	–	µs	1) **PWM_TLAG**=0 (on **HW_CTRL_0**)	P_6.5.16
Boost Regulator							

Table 17 Electrical Characteristics (cont'd)

T_j = -40°C to +150°C; V_S = 5.5 V to 28 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Boost Voltage 1 including Line and Load regulation	V_{BST1}	6.5	6.7	6.9	V	2) SBC Normal Mode V_{SUP} = 3 V I_{VS} = 550 mA Boost enabled **BOOST_V** = 00_B	P_6.5.7
Boost Voltage 2 including Line and Load regulation	V_{BST2}	7.76	8	8.24	V	2) SBC Normal Mode V_{SUP} = 3V I_{VS} = 450 mA Boost enabled **BOOST_V** = 01_B	P_6.5.8
Boost Voltage 3 including Line and Load regulation	V_{BST3}	9.7	10	10.3	V	2) SBC Normal Mode V_{SUP} = 3 V I_{VS} = 300 mA Boost enabled **BOOST_V** = 10_B	P_6.5.28
Boost Voltage 4 including Line and Load regulation	V_{BST4}	11.64	12	12.36	V	2) SBC Normal Mode V_{SUP} = 3 V I_{VS} = 250 mA Boost enabled **BOOST_V** = 11_B	P_6.5.31
Boost Switch ON voltage	$V_{BST,TH1}$	6.50	7	7.30	V	Boost enabled, V_S falling **BOOST_V** = 00_B	P_6.5.9
Boost Switch ON voltage	$V_{BST,TH2}$	7.90	8.5	8.90	V	Boost enabled, V_S falling **BOOST_V** = 01_B	P_6.5.18
Boost Switch ON voltage	$V_{BST,TH3}$	9.80	10.5	10.80	V	Boost enabled, V_S falling **BOOST_V** = 10_B	P_6.5.34
Boost Switch ON voltage	$V_{BST,TH4}$	11.7	12.5	13.0	V	Boost enabled, V_S falling **BOOST_V** = 11_B	P_6.5.35
Boost Switch ON/OFF hysteresis	$V_{BST,HYS}$	0.35	0.5	0.70	V	Boost enabled	P_6.5.10
Overcurrent peak limitation internal switch	$I_{BST\_LIM,TH}$	1.7	2.0	2.3	A	Boost enable $V_{SUP} \geq 3$ V	P_6.5.11
Boost switching frequency	f_{BST}	405	450	495	kHz	SBC Normal Mode (PWM)	P_6.5.12

1) Not subject to production test, specified by design.

2) Values verified in characterization with Boost converter external components specified in **Chapter 14.1**. No subject to production test; specified by design. Refer to **Figure 19** for additional information.

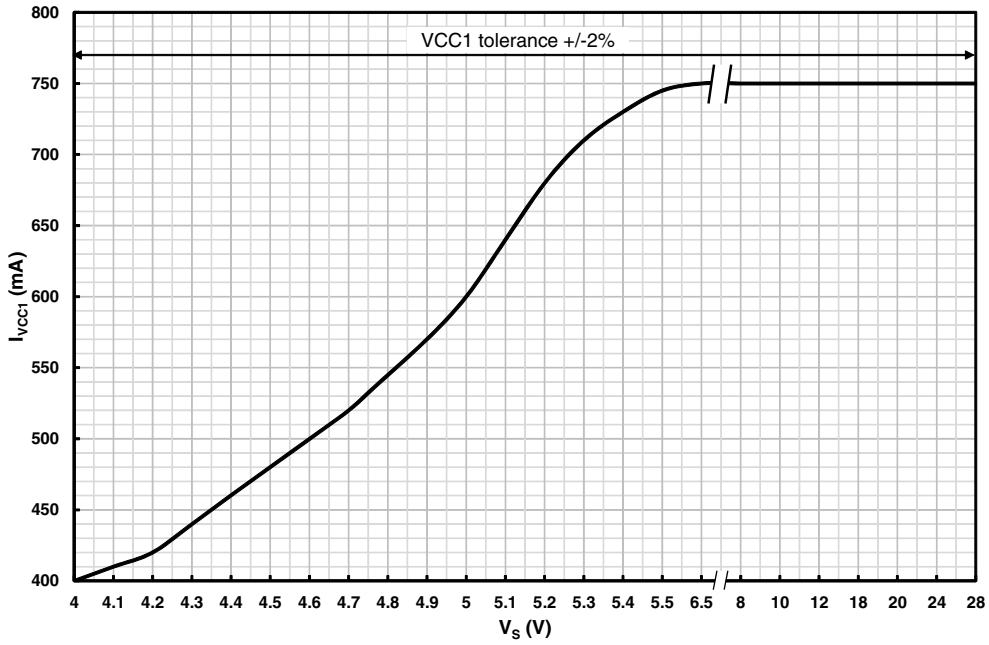


Figure 18 Maximum DCDC Buck current capability versus V_S

*Note: **Figure 18** is based on characterization results overtemperature with external components specified in **Chapter 14.1**.*

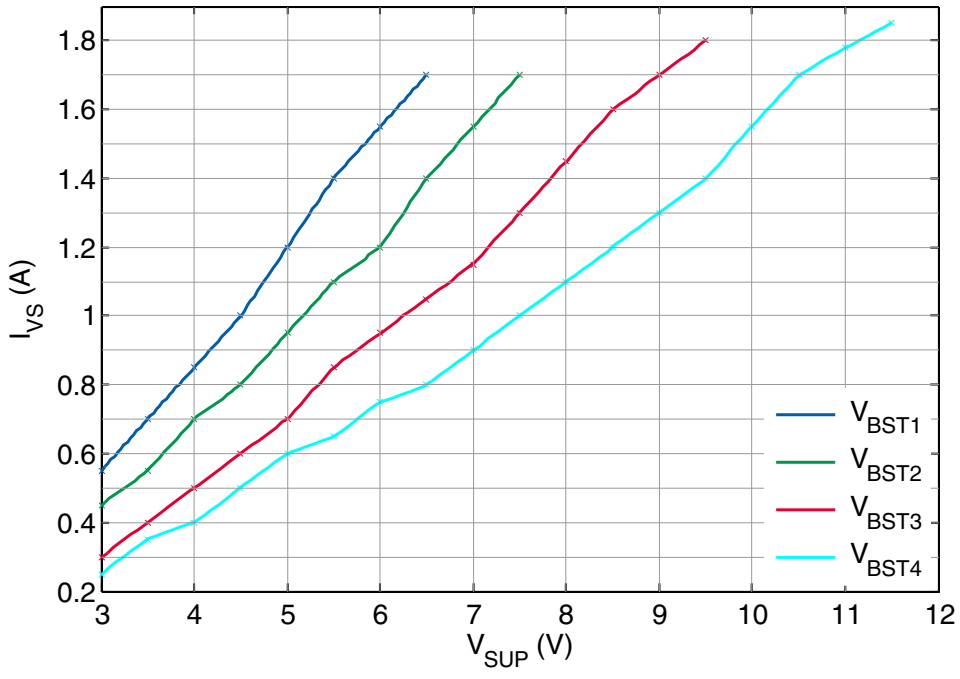


Figure 19 Maximum DCDC Boost current capability versus V_{SUP}

*Note: **Figure 19** is based on simulation results (specified by design), with Boost converter external components specified in **Chapter 14.1**.*

7 External Voltage Regulator

7.1 Block Description

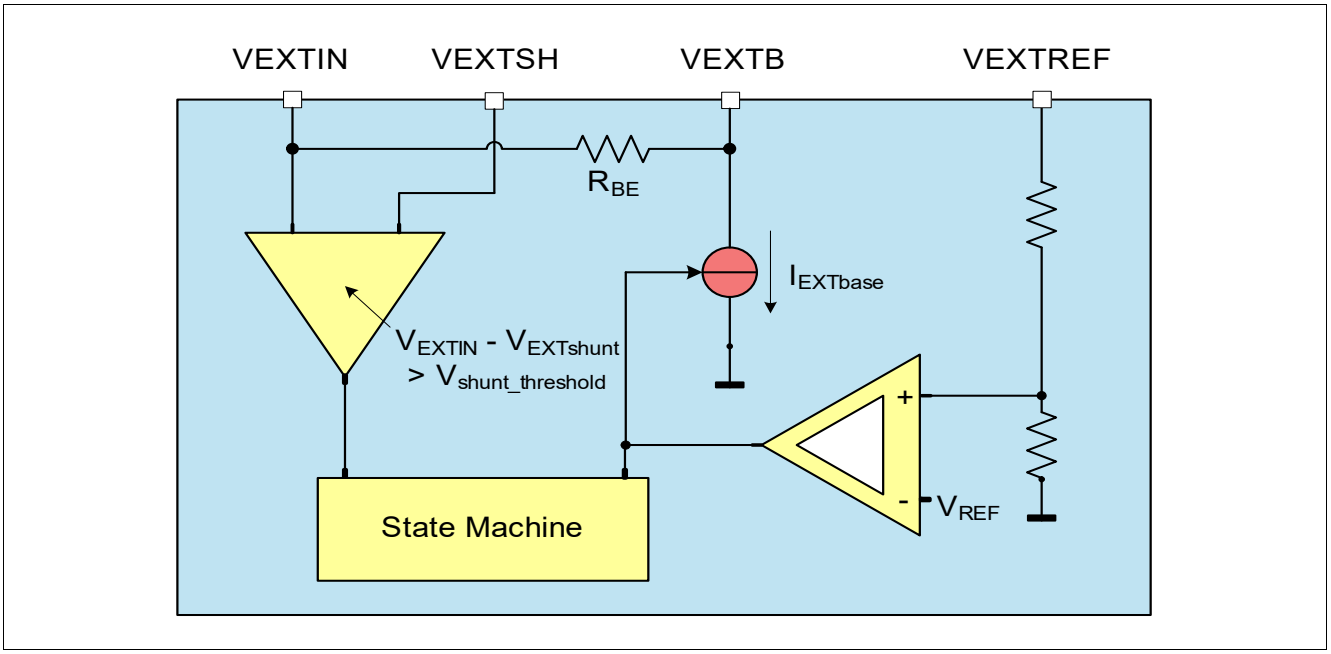


Figure 20 Functional Block Diagram

Functional Features

- Low-drop voltage regulator with external PNP transistor (up to 400 mA with 470 mΩ shunt resistor).
- Four high voltage pins are used: VEXTIN, VEXTB, VEXTSH, VEXTREF.
- Dedicated supply input VEXTIN to supply from V_S or from VCC1 (Buck regulator output voltage) depending on the application.
- Configurable output voltages via SPI: 5.0 V, 3.3 V (default), 1.8 V and 1.2 V.
- ≥ 4.7 µF ceramic capacitor at output voltage for stability, with ESR < 150 mΩ @ f = 10 kHz to achieve the voltage regulator control loop stability based on the safe phase margin (bode diagram).
- Overcurrent limitation can be configured with external shunt resistor.

7.2 General Description

The external voltage regulator is used as an independent voltage regulator. The **VEXT_VCFG** in **HW_CTRL_1** register set the VEXT output voltage. The **VEXT_ON** in the **M_S_CTRL** register in SBC Normal Mode activates the VEXT voltage regulator.

The regulator will act in the respective SBC Mode as described in **Table 18**.

The maximum current I_{EXT_max} is defined by the shunt used. To protect the VEXT against overtemperature condition, the base driver has a dedicate temperature sensor. For detailed temperature protection features, refer to **Chapter 12.11**.

The status of VEXT is reported in the **SUP_STAT_1** register (for detailed protection features refer to **Chapter 12.10**).

Table 18 External Voltage Regulator State by SBC Mode

SBC Mode	Voltage Regulator Behavior
INIT Mode	OFF
Normal Mode	Configurable
Stop Mode	Fixed
Sleep Mode	Fixed
Restart Mode	Fixed
Fail-Safe Mode	OFF

*Note: The configuration of the VEXT voltage regulator behavior must be implemented immediately when the SBC Normal Mode is reached after power-up of the device. As soon as the bit **VEXT_ON** is set for the first time, the configuration for VEXT cannot be changed anymore. The configuration cannot be changed as long as the device is supplied.*

*Note: If the VEXT output voltage is supplying external off-board loads, the application must consider the series resonance circuit built by cable inductance and decoupling capacitor at load. Sufficient damping must be provided(e.g. series resistor with capacitor directly at device or 100 Ω Resistor between PNP collector and VEXTREF with 10 µF cap on collector (see **Figure 21**).*

7.2.1 Functional Description

This regulator offers with VEXT a second supply which could be used as off-board supply e.g. for sensors due to the integrated HV pins VEXTB, VEXTSH, VEXTREF.

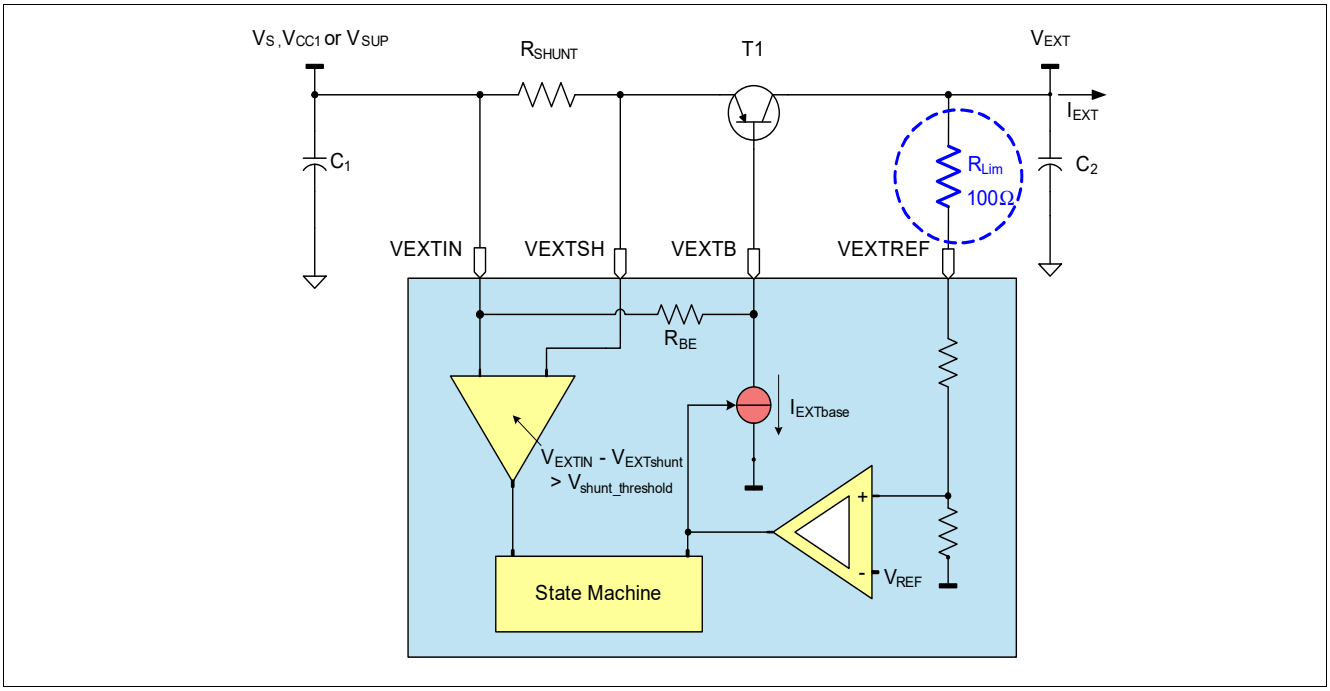


Figure 21 VEXT Hardware Setup

VEXT can be switched ON or OFF but the output voltage configuration cannot no longer be changed once activated.

An overcurrent detection function is realized with the external shunt (see **Chapter 7.4** for calculating the desired shunt value) and output current shunt voltage threshold (**$V_{shunt\_threshold}$**). When this threshold is reached, IEXT is limited and only the overcurrent detection bit **VEXT_OC** is set (no other reactions). This bit can be cleared via SPI once the overcurrent condition is no longer present. If the overcurrent detection feature is not needed, connect the VEXTSH pin to VEXT supply (VEXTIN pin).

If the VEXT is enabled, an undervoltage event is signaled with the bit **VREG_UV** in the **SUP_STAT_0** register.

7.3 External Components

The characterization is done with the BCP52-16 from Infineon (I_{EXT} < 200 mA) and with MJD253 from ON Semi.Other PNP transistors can be used. The functionality must be checked in the application.

Figure 21 shows the hardware set up used.

Table 19 Bill of Materials for VEXT with BCP52-16

Device	Vendor	Reference / Value
C2	Murata	10 µF/10V GCM31CR71A106K64L
RSHUNT	–	1 Ω
T1	Infineon	BCP52-16

Note: The SBC is not able to ensure a thermal protection of the external PNP transistor. The power handling capabilities for the application must therefore be chosen according to the selected PNP device and according to the PCB layout and the properties of the application to prevent thermal damage.

Table 20 Bill of Materials for VEXT with MJD-253

Device	Vendor	Reference / Value
C2	Murata	10 µF/10V GCM31CR71A106K64L
RSHUNT	–	470 mΩ
T1	ON-Semi	MJD253

7.4 Calculation of R_{SHUNT}

The maximum current I_{EXT_max} where the overcurrent detection bit is set (**VEXT_OC** = 1 on the **SUP_STAT_1** register), is determined by the shunt resistor R_{SHUNT} and the Output Current Shunt Voltage Threshold (**$V_{shunt\_threshold}$**).

The resistor can be calculated as following:

$$R_{SHUNT} = \frac{V_{shunt\_threshold}}{I_{EXT\_max}} \tag{7.1}$$

7.5 Unused Pins

In case the VEXT is not used in the application, connect the unused pins of VEXT as followed:

- Connect VEXTSH, VEXTIN to V_S or leave open.
- Leave VEXTB open.
- Leave VEXTREF open.
- Keep VEXT disabled.

7.6 Electrical Characteristics

Table 21 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40°C to +150°C; SBC Normal Mode; all outputs open; all voltages with respect to ground; positive current defined flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Parameters independent from Test Set-up							
External Regulator Control Drive Current Capability	$I_{EXTbase}$	40	60	80	mA	$V_{EXTbase}$ = 13.5 V	P_7.6.1
Input Current V_{EXTref}	I_{EXTref}	–	3	10	µA	V_{EXTref} = 3.3 V, 5 V, 1.8 V, 1.2 V	P_7.6.2
Input Current V_{EXT} Shunt Pin	$I_{EXTshunt}$	1	3	10	µA	$V_{EXTshunt}$ = V_S	P_7.6.3
Output Current Shunt Voltage Threshold	$V_{shunt\_threshold}$	180	245	310	mV	1)	P_7.6.4
Leakage current of $V_{EXTbase}$ when VEXT disabled	$I_{EXTbase\_lk}$	–	–	5	µA	$V_{EXTbase}$ = V_S; T_j = 25°C	P_7.6.7
Leakage current of $V_{EXTshunt}$ when VEXT disabled	$I_{EXTshunt\_lk}$	–	–	5	µA	$V_{EXTshunt}$ = V_S; T_j = 25°C	P_7.6.25
Base to emitter resistor	R_{BE}	120	150	185	kΩ	$V_{EXTbase}$ = V_S - 0.3 V; V_{EXT} OFF	P_7.6.9
Active Peak Threshold VEXT (Transition threshold between high-power and low-power mode regulator)	$I_{VEXT,Ipeak,r}$	–	50	–	µA	2) Drive current $I_{\_EXTbase}$; $I_{EXTbase}$ rising V_S =13.5 V; -40°C < T_j < 150°C	P_7.6.26
Active Peak Threshold VEXT (Transition threshold between high-power and low-power mode regulator)	$I_{VEXT,Ipeak,f}$	–	30	–	µA	2) Drive current $I_{\_EXTbase}$; $I_{EXTbase}$ falling V_S = 13.5 V; -40°C < T_j < 150°C	P_7.6.27
Parameters dependent on the Test Set-up (with external PNP device MJD-253)							
External Regulator Output Voltage including Line and Load regulation	$V_{EXT,out1}$	4.9	5	5.1	V	3) SBC Normal Mode; **VEXT_VCFG**=00_B 5.5 V < V_{INEXT} < 28 V 10 mA < I_{EXT} < 400 mA;	P_7.6.10

Table 21 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40°C to +150°C; SBC Normal Mode; all outputs open; all voltages with respect to ground; positive current defined flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
External Regulator Output Voltage including Line and Load regulation	$V_{EXT,out2}$	4.8	5	5.2	V	[3] SBC Stop, Sleep Mode; **VEXT_VCFG**=00_B 5.5 V < V_{INEXT} < 28 V 10 µA < I_{EXT} < 20 mA;	P_7.6.21
External Regulator Output Voltage including Line and Load regulation	$V_{EXT,out3}$	3.23	3.3V	3.37	V	[3] SBC Normal Mode; **VEXT_VCFG**=01_B 5.5 V < V_{INEXT} < 28 V 10 mA < I_{EXT} < 300 mA;	P_7.6.11
External Regulator Output Voltage including Line and Load regulation	$V_{EXT,out4}$	3.15	3.3V	3.45	V	[3] SBC Stop, Sleep Mode; **VEXT_VCFG**=01_B 5.5 V < V_{INEXT} < 28 V 10 µA < I_{EXT} < 20 mA;	P_7.6.12
External Regulator Output Voltage including Line and Load regulation	$V_{EXT,out5}$	1.75	1.8	1.85	V	[3] SBC Normal Mode; **VEXT_VCFG**=10_B 5.5 V < V_{INEXT} < 28 V 10 mA < I_{EXT} < 300 mA;	P_7.6.13
External Regulator Output Voltage including Line and Load regulation	$V_{EXT,out6}$	1.7	1.8	1.9	V	[3] SBC Stop, Sleep Mode; **VEXT_VCFG**=10_B 5.5 V < V_{INEXT} < 28 V 10 µA < I_{EXT} < 20 mA;	P_7.6.14
External Regulator Output Voltage including Line and Load regulation	$V_{EXT,out7}$	1.16	1.2	1.24	V	[3] SBC Normal Mode; **VEXT_VCFG**=11_B 5.5 V < V_{INEXT} < 28 V 10 mA < I_{EXT} < 300 mA;	P_7.2.22
External Regulator Output Voltage including Line and Load regulation	$V_{EXT,out8}$	1.15	1.2	1.25	V	[3] SBC Stop, Sleep Mode; **VEXT_VCFG**=11_B 5.5 V < V_{INEXT} < 28 V 10 µA < I_{EXT} < 20 mA;	P_7.6.23

1) Threshold at which the current limitation starts to operate.

2) Not subject to production test, specified by design.

3) Tolerance includes load regulation and line regulation.

8 High Speed CAN Transceiver

8.1 Block Description

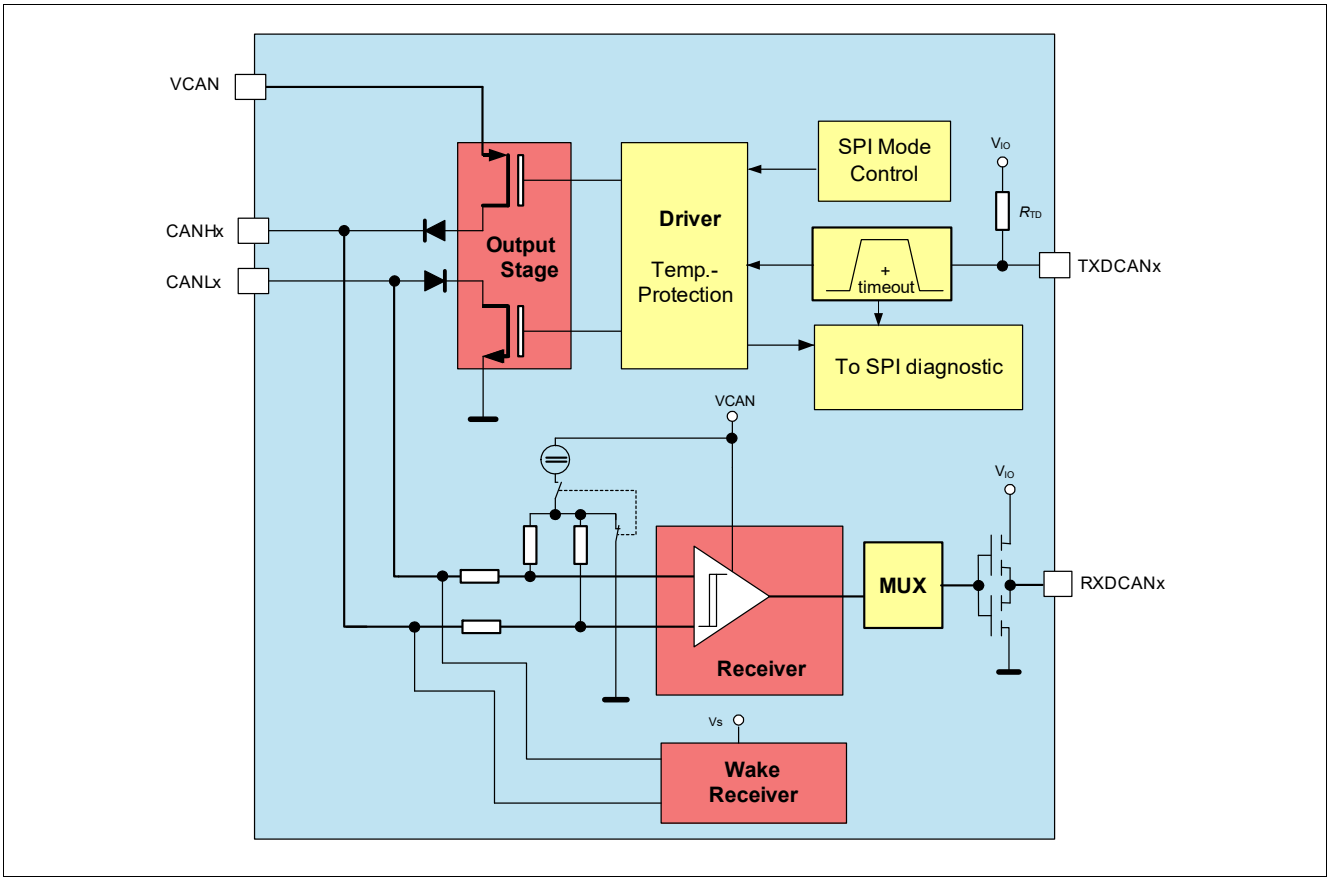


Figure 22 Functional Block Diagram

8.2 Functional Description

The Controller Area Network (CAN) transceiver part of the SBC provides high-speed (HS) differential mode data transmission (up to 5 Mb) and reception in automotive and industrial applications. It works as an interface between the CAN protocol controller and the physical bus lines compatible with ISO 11898-2, 11898-5 and ISO11898-6 as well as SAE J2284.

The CAN transceiver offers low power modes to reduce current consumption. This supports networks with partially powered down nodes. To support software diagnostic functions, a CAN Receive-only Mode is implemented.

It is designed to provide excellent passive behavior when the transceiver is switched off (mixed networks, clamp15/30 applications).

A wake-up from the CAN wake capable mode is possible via a message on the bus. Thus, the microcontroller can be powered down or idled and will be woken up by the CAN bus activities.

The CAN transceiver is designed to withstand the severe conditions of automotive applications and to support 12 V applications.

The different transceiver modes can be controlled via the SPI CANx bits.

Figure 23 shows the possible transceiver mode transitions when changing the SBC mode.

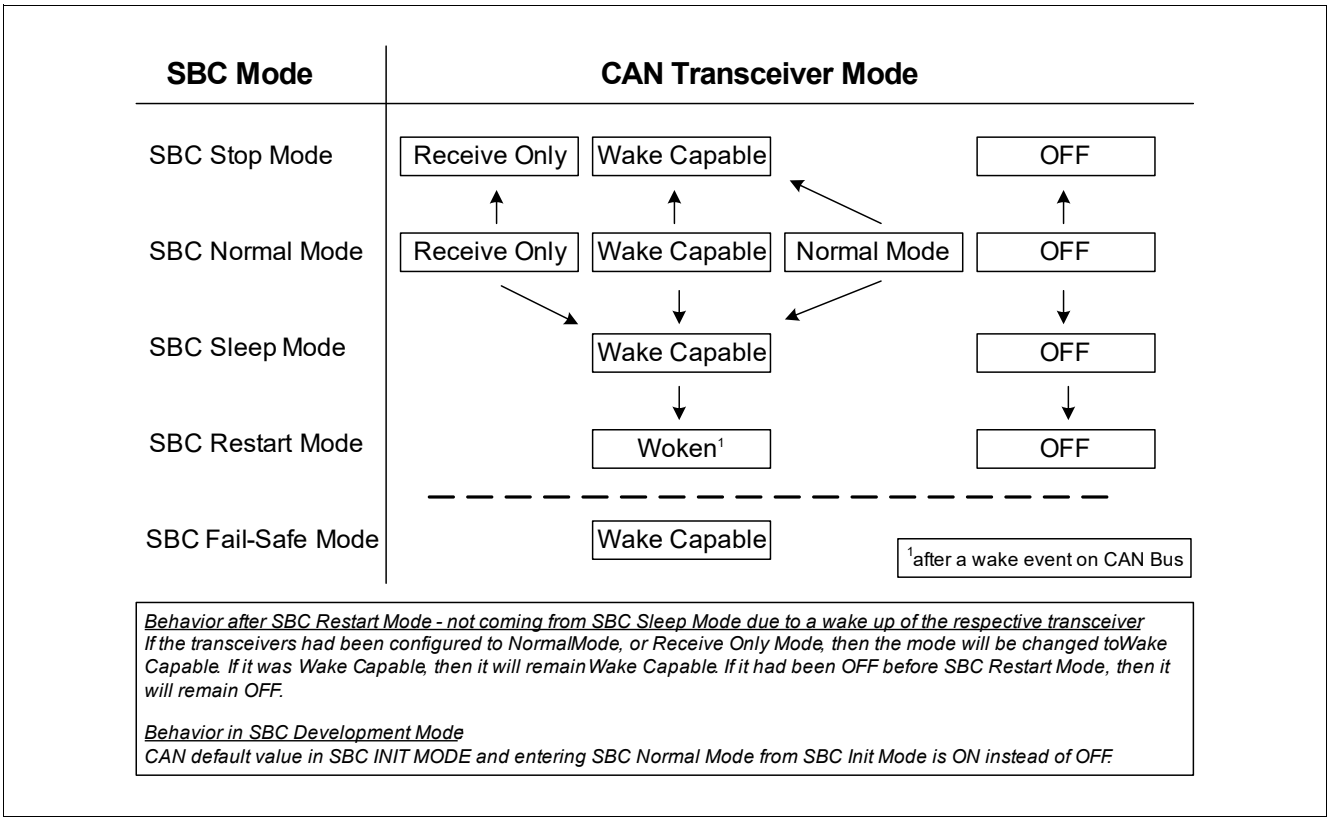


Figure 23 CAN Mode Control Diagram

CAN FD Support

CAN FD stands for 'CAN with Flexible Data Rate'. It is based on the well established CAN protocol as specified in ISO 11898-1. CAN FD still uses the CAN bus arbitration method. The benefit is that the bit rate can be increased by switching to a shorter bit time at the end of the arbitration process and then returning to the longer bit time at the CRC delimiter before the receivers transmit their acknowledge bits. See also **Figure 24**. In addition, the effective data rate is increased by allowing longer data fields. CAN FD allows the transmission of up to 64 data bytes compared to the 8 data bytes from the standard CAN.

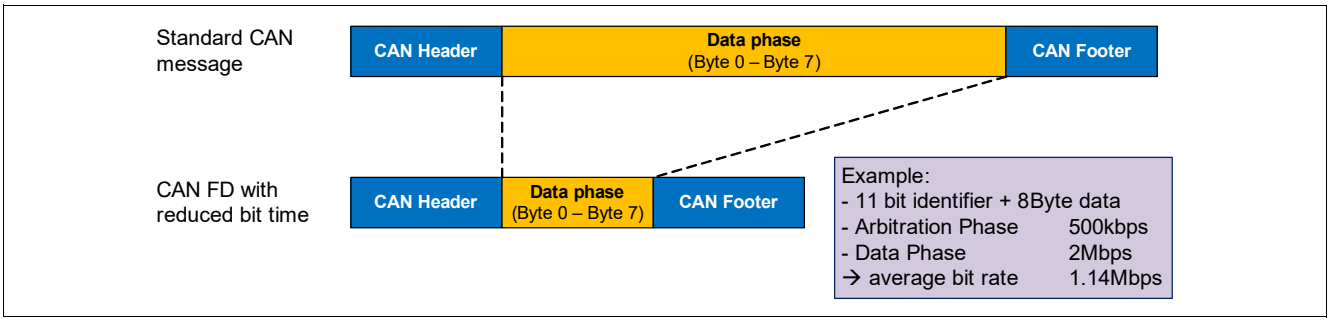


Figure 24 Bit Rate Increase with CAN FD vs. Standard CAN

CAN FD has to be supported by both the physical layer and the CAN controller. If the CAN controller cannot support CAN FD, then the respective CAN node must at least tolerate CAN FD communication. This CAN FD tolerant mode is implemented in the physical layer.

8.2.1 CAN OFF Mode

The CAN OFF Mode is the default mode after power-up of the SBC. It is available in all SBC Modes and is intended to completely stop CAN activities or when CAN communication is not needed. The CANH/L bus interface acts as a high impedance input with a very small leakage current. In CAN OFF Mode, a wake-up event on the bus will be ignored.

8.2.2 CAN Normal Mode

The CAN Transceiver is enabled via SPI in SBC Normal Mode. CAN Normal Mode is designed for normal data transmission/reception within the HS-CAN network. The mode is only available in SBC Normal Mode or SBC Init Mode if the SBC Development Mode is used. The bus biasing is set to VCAN/2.

Transmission

The signal from the microcontroller is applied to the TXDCANx input of the SBC. The bus driver switches the CANH/L output stages to transfer this input signal to the CAN bus lines.

Enabling sequence

The CAN transceiver requires an enabling time $t_{CAN,EN}$ before a message can be sent on the bus. This means that the TXDCANx signal can only be pulled LOW after the enabling time. If this is not ensured, then the TXDCANx needs to be set back to HIGH (=recessive) until the enabling time is completed. Only the next dominant bit will be transmitted on the bus. **Figure 25** shows different scenarios and explanations for CAN enabling.

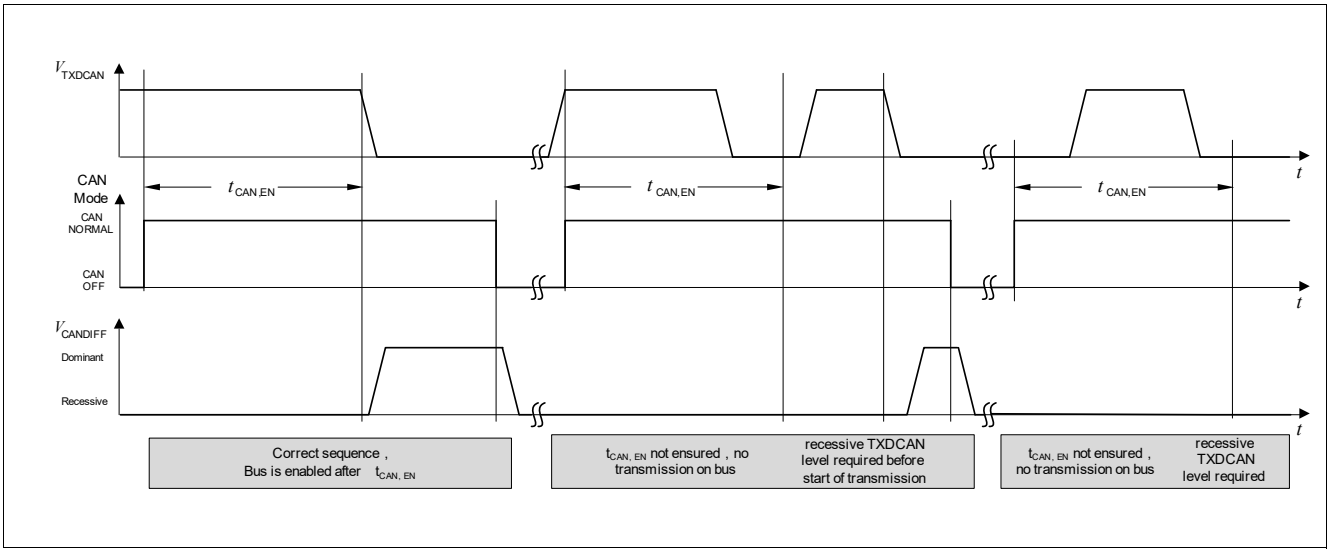


Figure 25 CAN Transceiver Enabling Sequence

Reduced Electromagnetic Emission

To reduce electromagnetic emissions (EME), the bus driver controls CANH/L slopes symmetrically.

The slope control can be disabled using the CAN_x_Flash bits to achieve bite rate higher than 5 Mb.

Reception

Analog CAN bus signals are converted into digital signals at RXDCANx via the differential input receiver.

8.2.3 CAN Receive Only Mode

In CAN Receive Only Mode (RXD only), the driver stage is de-activated but reception is still operational. This mode is available in SBC Normal and Stop Mode. The bus biasing is set to VCAN/2.

8.2.4 CAN Wake Capable Mode

This mode can be used in SBC Stop, Sleep, Restart and Normal Mode and it is used to monitor bus activities. It is automatically accessed in SBC Fail-Safe Mode. A valid wake-up pattern (WUP) on the bus results in a change of behavior of the SBC, as described in **Table 22**. As a signalization to the microcontroller, the RXDCANx pin is set LOW and will stay LOW until the CANx transceiver is changed to any other mode. After a wake-up event, the transceiver can be switched to CAN Normal Mode for communication using SPI command.

As shown in **Figure 26**, a wake-up pattern is signaled on the bus by two consecutive dominant bus levels for at least t_{Wake1} (filter time t > t_{Wake1}), each separated by a recessive bus level of less than t_{Wake2}.

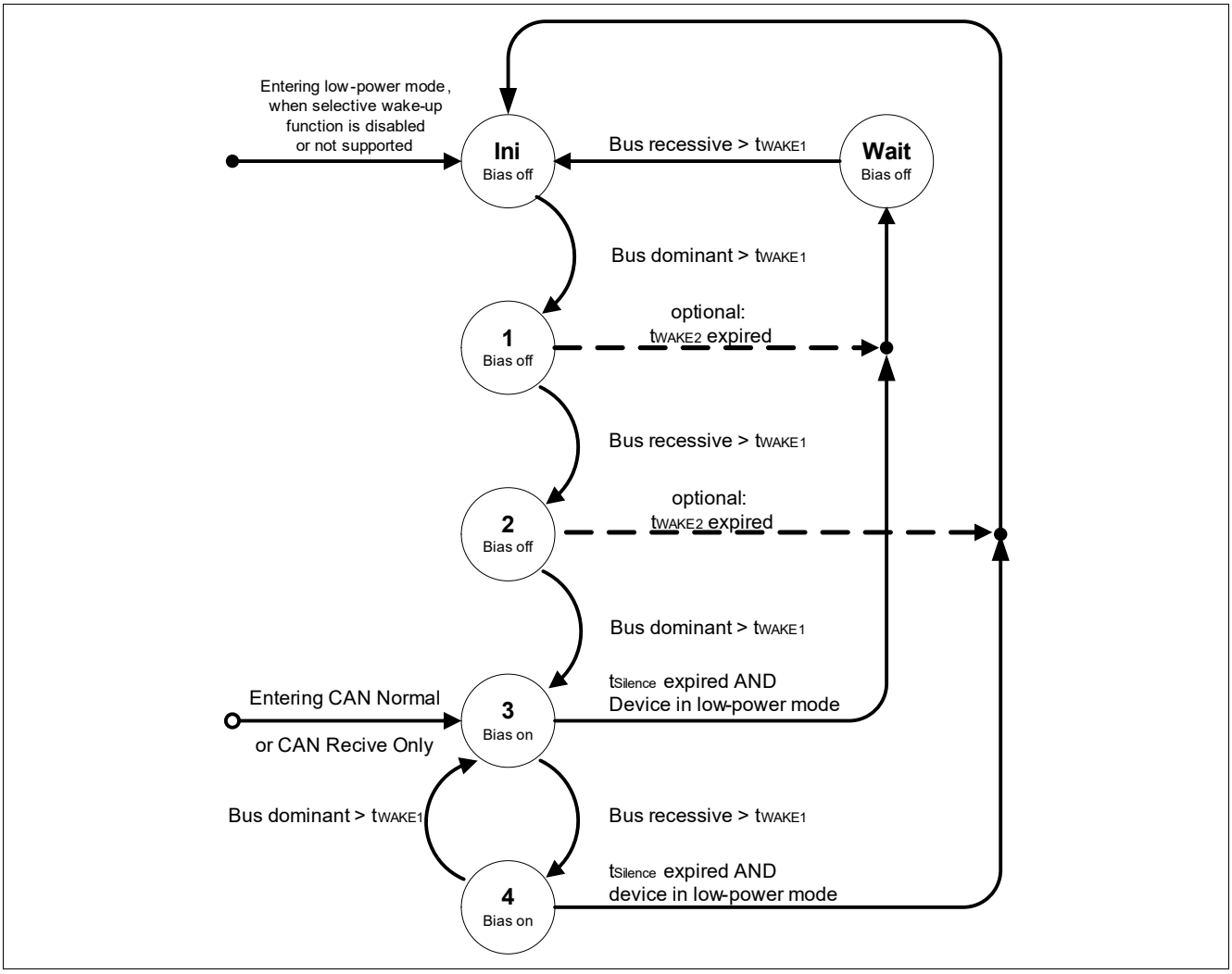


Figure 26 WUP detection following the definition in ISO 11898-5

Rearming the Transceiver for Wake Capability

After a bus wake-up event, the transceiver is woken. However, the CANx transceiver mode bits will still show wake capable (=‘01’) so that the RXDCAN signal will be pulled low. There are two possibilities how the CAN transceiver’s wake capable mode is enabled again after a wake event:

- The CAN transceiver mode must be toggled, i.e. switched from Wake Capable Mode to CAN Normal Mode, CAN Receive Only Mode or CAN Off, before switching to CAN Wake Capable Mode again.
- Rearming is done automatically when the SBC is changed to SBC Stop, Sleep, or SBC Fail-Safe Mode to ensure wake-up capability.

Note: It is not necessary to clear the CAN wake-up bit CAN_x_WU to become wake capable again. It is sufficient to toggle the CAN mode.

Wake-Up in SBC Stop and Normal Mode

In SBC Stop Mode, if a wake-up is detected, it is always signaled by the INTN output and in the **WK_STAT_0**, **WK_STAT_2** SPI registers. It is also signaled by RXDCANx pulled to low. The same applies for the SBC Normal Mode. The microcontroller should set the device from SBC Stop Mode to SBC Normal Mode; there is no automatic transition to SBC Normal Mode.

For functional safety reasons, the watchdog will be automatically enabled in SBC Stop Mode after a bus wake event in case it was disabled before (if bit **WD_EN_WK_ BUS** was configured to HIGH before).

Wake-Up in SBC Sleep Mode

Wake-up is possible via a CAN message (filter time t > t_{Wake1}). The wake-up automatically transfers the SBC into the SBC Restart Mode and from there to Normal Mode the corresponding RXDCANx pin in set to LOW. The microcontroller is able to detect the low signal on RXDCANx and to read the wake source out of the **WK_STAT_0** or **WK_STAT_2** register via SPI. No interrupt is generated when coming out of SBC Sleep Mode. The microcontroller can now for example switch the CAN transceiver into CAN Normal Mode via SPI to start communication.

Table 22 Action due to CAN Bus Wake-Up

SBC Mode	SBC Mode after Wake	VCC1	INTN	RXD
Normal Mode	Normal Mode	ON	LOW	LOW
Stop Mode	Stop Mode	ON	LOW	LOW
Sleep Mode	Restart Mode	Ramping Up	HIGH	LOW
Restart Mode	Restart Mode	ON	HIGH	LOW
Fail-Safe Mode	Restart Mode	Ramping up	HIGH	LOW

8.2.5 TXD Time-out Feature

If the TXDCANx signal is dominant for a time *t* > $t_{TXD\_CAN\_TO}$, in CAN Normal Mode, the TXD time-out function deactivates the transmission of the signal at the bus. This is implemented to prevent the bus from being blocked permanently due to an error. The transmitter is disabled and the transceiver is switched to Receive Only Mode. The failure is stored in the SPI flag CAN_x_FAIL. The CAN transmitter stage is activated again after the dominant time-out condition is removed and the transceiver is automatically switched back to CAN Normal Mode.The transceiver configuration stays unchanged.

8.2.6 Bus Dominant Clamping

If the HS-CAN bus signal is dominant for a time *t* > $t_{BUS\_CAN\_TO}$, regardless of the CAN transceiver mode a bus dominant clamping is detected and the SPI bit CAN_x_FAIL is set. The transceiver configuration stays unchanged.

8.2.7 Undervoltage Detection

The voltage at the CAN supply pin is monitored in CAN Normal Mode and CAN Receiver Only Mode . In case of VCAN undervoltage, the bit **VCAN_UV** is set and the SBC disables the transmitter stage. If the undervoltage condition is not present anymore (VCAN > $V_{CAN\_UV,f}$), the transceiver is automatically switched back to CAN Normal Mode. The transceiver configuration stays unchanged.

8.3 Electrical Characteristics

Table 23 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40°C to +150°C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60 Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CAN Supply Voltage							
CAN Supply undervoltage detection threshold	$V_{CAN\_UV,f}$	4.5	–	4.75	V	CAN Normal Mode; VCAN falling;	P_8.3.1
CAN Bus Receiver							
Differential Receiver Threshold Voltage, recessive to dominant edge	V_{diff,rd_N}	–	0.80	0.90	V	$V_{diff} = V_{CANH} - V_{CANL}$; -12 V ≤ VCM(CAN) ≤ +12 V; CAN Normal Mode	P_8.3.2
Dominant state differential input voltage range	$V_{diff\_D\_range}$	0.9	–	8.0	V	1) $V_{diff} = V_{CANH} - V_{CANL}$; -12 V ≤ VCM(CAN) ≤ +12 V; CAN Normal Mode	P_8.3.60
Differential Receiver Threshold Voltage, dominant to recessive edge	V_{diff,dr_N}	0.50	0.60	–	V	$V_{diff} = V_{CANH} - V_{CANL}$; -12 V ≤ VCM(CAN) ≤ +12 V; CAN Normal Mode	P_8.3.3
Recessive state differential input voltage range	$V_{diff\_R\_range}$	-3.0	–	0.5	V	1) $V_{diff} = V_{CANH} - V_{CANL}$; -12 V ≤ VCM(CAN) ≤ +12 V; CAN Normal Mode	P_8.3.61
Common Mode Range	CMR	-12	–	12	V	1)	P_8.3.4
CANH, CANL Input Resistance	R_i	20	40	50	kΩ	CAN Normal / Wake capable Mode; -2 V ≤ VCANH/L ≤ +7 V Recessive state	P_8.3.5
Differential Input Resistance	R_{diff}	40	80	100	kΩ	CAN Normal / Wake capable Mode; -2 V ≤ VCANH/L ≤ +7 V Recessive state	P_8.3.6
Input Resistance Deviation between CANH and CANL	DR_i	-3	–	3	%	1) Recessive state VCANH = VCANL =5 V	P_8.3.7
Input Capacitance CANH, CANL versus GND	C_{in}	–	20	40	pF	2) V_{TXD} = 5 V	P_8.3.8
Differential Input Capacitance	C_{diff}	–	10	20	pF	2) V_{TXD} = 5 V	P_8.3.9

Table 23 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40°C to +150°C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60 Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Wake-up Receiver Threshold Voltage, recessive to dominant edge	V_{diff, rd_W}	–	0.8	1.15	V	-12 V ≤ VCM(CAN) ≤ +12 V; CAN Wake Capable Mode	P_8.3.10
Wake-up Receiver Dominant state differential input voltage range	V_{diff,D_range_W}	1.15	–	8.0	V	[1] -12 V ≤ VCM(CAN) ≤ +12 V; CAN Wake Capable Mode	P_8.3.62
Wake-up Receiver Threshold Voltage, dominant to recessive edge	V_{diff, dr_W}	0.4	0.7	–	V	-12 V ≤ VCM(CAN) ≤ +12 V; CAN Wake Capable Mode	P_8.3.11
Wake-up Receiver Recessive state differential input voltage range	V_{diff,R_range_W}	-3.0	–	0.4	V	[1] -12 V ≤ VCM(CAN) ≤ +12 V; CAN Wake Capable Mode	P_8.3.63
CAN Bus Transmitter							
CANH/CANL Recessive Output Voltage (CAN Normal Mode)	V_{CANL/H_NM}	2.0	–	3.0	V	CAN Normal Mode; $V_{TXD} = V_{IO}$; no load	P_8.3.12
CANH/CANL Recessive Output Voltage (CAN Wake Capable Mode)	V_{CANL/H_LP}	-0.1	–	0.1	V	CAN Wake Capable Mode; $V_{TXD} = V_{IO}$; no load	P_8.3.13
CANH, CANL Recessive Output Voltage Difference $V_{diff} = V_{CANH} - V_{CANL}$	$V_{diff\_r\_N}$	-500	–	50	mV	CAN Normal Mode $V_{TXD} = V_{IO}$; no load	P_8.3.14
CANH, CANL Recessive Output Voltage Difference $V_{diff} = V_{CANH} - V_{CANL}$	$V_{diff\_r\_W}$	-100	–	100	mV	CAN Wake Capable Mode; $V_{TXD} = V_{IO}$; no load	P_8.3.15
CANL Dominant Output Voltage	V_{CANL}	0.5	–	2.25	V	CAN Normal Mode; V_{TXD} = 0 V; 50 Ω ≤ R_L ≤ 65 Ω	P_8.3.16
CANH Dominant Output Voltage	V_{CANH}	2.75	–	4.5	V	CAN Normal Mode; V_{TXD} = 0 V; 50 Ω ≤ R_L ≤ 65 Ω	P_8.3.17
CANH, CANL Dominant Output Voltage Difference $V_{diff} = V_{CANH} - V_{CANL}$	$V_{diff\_d\_N}$	1.5	2.0	2.5	V	CAN Normal Mode; V_{TXD} = 0 V; 50 Ω ≤ R_L ≤ 65 Ω	P_8.3.18

Table 23 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40°C to +150°C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60 Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CANH, CANL Dominant Output Voltage Difference $V_{diff} = V_{CANH} - V_{CANL}$ on extended bus load range	$V_{diff\_d\_N}$	1.5	–	5.0	V	[1] CAN Normal Mode; V_{TXD} = 0 V; R_L = 2240 Ω	P_8.3.58
CANH, CANL output voltage difference slope, recessive to dominant	$V_{diff\_slope\_rd}$	–	–	70	V/us	[1] 30% to 70% of measured differential bus voltage, C_L = 100 pF, R_L = 60 Ω	P_8.3.47
CANH, CANL output voltage difference slope, dominant to recessive	$V_{diff\_slope\_dr}$	–	–	70	V/us	[1] 70% to 30% of measured differential bus voltage, C_L = 100 pF, R_L = 60 Ω	P_8.3.48
CANH Short Circuit Current	I_{CANHsc}	-100	-80	-50	mA	CAN Normal Mode; $V_{CANHshort}$ = -3 V	P_8.3.20
CANL Short Circuit Current	I_{CANLsc}	50	80	100	mA	CAN Normal Mode $V_{CANLshort}$ = 18 V	P_8.3.21
Leakage Current (unpowered device)	$I_{CANH,lk}$ $I_{CANL,lk}$	–	5	7.5	µA	$V_S = V_{CAN}$ = 0 V; 0 V < $V_{CANH,L}$ ≤ 5 V; [3] R_{test} = 0 / 47 kΩ	P_8.3.22
Receiver Output RXD							
HIGH level Output Voltage	$V_{RXD,H}$	0.8 × V_{IO}	–	–	V	CAN Normal Mode $I_{RXD(CAN)}$ = -2 mA;	P_8.3.23
LOW Level Output Voltage	$V_{RXD,L}$	–	–	0.2 × V_{IO}	V	CAN Normal Mode $I_{RXD(CAN)}$ = 2 mA;	P_8.3.24
Transmission Input TXD							
HIGH Level Input Voltage Threshold	$V_{TXD,H}$	–	–	0.7 × V_{IO}	V	CAN Normal Mode recessive state	P_8.3.25
LOW Level Input Voltage Threshold	$V_{TXD,L}$	0.3 × V_{IO}	–	–	V	CAN Normal Mode dominant state	P_8.3.26
TXD Input Hysteresis	$V_{TXD,hys}$	–	0.12 × V_{IO}	–	mV	[1]	P_8.3.27
TXD Pull-up Resistance	R_{TXD}	20	40	80	kΩ	–	P_8.3.28
CAN Transceiver Enabling Time	$t_{CAN,EN}$	8	13	18	µs	[8] CSN = HIGH to first valid transmitted TXD dominant	P_8.3.29

Table 23 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40°C to +150°C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60 Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Dynamic CAN-Transceiver Characteristics							
Driver Symmetry $V_{SYM} = V_{CANH} + V_{CANL}$	V_{SYM}	4.5	–	5.5	V	[1)4)] CAN Normal Mode; V_{TXD} = 0 V / 5 V; V_{CAN}= 5 V; C_{SPLIT} = 4.7 nF; 50 Ω ≤ R_L ≤ 60 Ω	P_8.3.19
Min. Dominant Time for Bus Wake-up	t_{Wake1}	0.5	1.2	1.8	µs	-12 V ≤ VCM(CAN) ≤ +12 V; CAN Wake capable Mode	P_8.3.30
Wake-up Time-out, Recessive Bus	t_{Wake2}	0.5	–	10	ms	[8)] CAN Wake capable Mode	P_8.3.31
WUP Wake-up Reaction Time	t_{WU_WUP}	–	–	100	µs	[5)6)8)] Wake-up reaction time after a valid WUP on CAN bus;	P_8.3.32
ISO: Loop Delay (recessive to dominant)	$t_{loop,f}$	–	150	255	ns	CAN Normal Mode C_L = 100 pF; R_L = 60 Ω; C_{RXD} = 15 pF (see **Figure 27**)	P_8.3.33
ISO: Loop Delay (dominant to recessive)	$t_{loop,r}$	–	150	255	ns	CAN Normal Mode C_L = 100 pF; R_L = 60 Ω; C_{RXD} = 15 pF (see **Figure 27**)	P_8.3.34
Propagation Delay TXD LOW to bus dominant	$t_{d(L),T}$	–	50	–	ns	CAN Normal Mode C_L = 100 pF; R_L = 60 Ω; (see **Figure 27**)	P_8.3.35
Propagation Delay TXD HIGH to bus recessive	$t_{d(H),T}$	–	50	–	ns	CAN Normal Mode C_L = 100 pF; R_L = 60 Ω; (see **Figure 27**)	P_8.3.36
Propagation Delay bus dominant to RXD LOW	$t_{d(L),R}$	–	100	–	ns	CAN Normal Mode C_L = 100 pF; R_L = 60 Ω; C_{RXD} = 15 pF (see **Figure 27**)	P_8.3.37

Table 23 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40°C to +150°C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60 Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Propagation Delay bus recessive to RXD HIGH	$t_{d(H),R}$	–	100	–	ns	CAN Normal Mode C_L = 100 pF; R_L = 60 Ω ; C_{RXD} = 15 pF (see **Figure 27**)	P_8.3.38
Received Recessive bit width CAN FD up to 2 Mbps	$t_{bit(RXD)}$	400	–	550	ns	CAN Normal Mode C_L = 100 pF R_L = 60 Ω C_{RXD} = 15 pF $t_{bit(TXD)}$ = 500 ns Parameter definition in according to **Figure 28**.	P_8.3.45
Transmitted Recessive bit width CAN FD up to 2 Mbps	$t_{bit(BUS)}$	435	–	530	ns	CAN Normal Mode C_L = 100 pF R_L = 60 Ω C_{RXD} = 15 pF $t_{bit(TXD)}$ = 500 ns Parameter definition in according to **Figure 28**.	P_8.3.52
Received Recessive bit width CAN FD up to 5 Mbps	$t_{bit(RXD)}$	120	–	220	ns	CAN Normal Mode C_L = 100 pF R_L = 60 Ω C_{RXD} = 15 pF $t_{bit(TXD)}$ = 200 ns Parameter definition in according to **Figure 28**.	P_8.3.46
Transmitted Recessive bit width CAN FD up to 5 Mbps	$t_{bit(BUS)}$	155	–	210	ns	CAN Normal Mode C_L = 100 pF R_L = 60 Ω C_{RXD} = 15 pF $t_{bit(TXD)}$ = 200ns Parameter definition in according to **Figure 28**.	P_8.3.53

Table 23 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40°C to +150°C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60 Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Receiver timing symmetry[7] CAN FD up to 2 Mbps	Δt_{Rec}	-65	–	40	ns	[7] CAN Normal Mode C_L = 100 pF R_L = 60 Ω C_{RXD} = 15 pF $t_{bit(TXD)}$ = 500 ns Parameter definition according to **Figure 28**.	P_8.3.39
Receiver timing symmetry CAN FD up to 5 Mbps	Δt_{Rec}	-45	–	15	ns	[7] CAN Normal Mode C_L = 100 pF R_L = 60 Ω C_{RXD} = 15 pF $t_{bit(TXD)}$ = 200 ns Parameter definition according to **Figure 28**.	P_8.3.43
TXD Permanent Dominant Time-out	$t_{TXD\_CAN\_TO}$	–	2	–	ms	[8] CAN Normal Mode	P_8.3.40
BUS Permanent Dominant Time-out	$t_{BUS\_CAN\_TO}$	–	2	–	ms	[8] CAN Normal Mode	P_8.3.41
Time-out for bus inactivity	$t_{SILENCE}$	0.6	–	1.2	s	[8]	P_8.3.44

1) Not subject to production test, specified by design.
2) Not subject to production test, specified by design, S2P - Method; f = 10 MHz.
3) R_{test} between V_S/V_{CAN} and 0 V (GND).
4) **V_{SYM}** shall be observed during dominant and recessive state and also during the transition from dominant to recessive and vice versa while TxD is simulated by a square signal (50% duty cycle) a frequency of 1 MHz.
5) Wake-up is signalized via INTN pin activation in SBC Stop Mode and via VCC1 ramping up with wake from SBC Sleep Mode.
6) Time starts with end of last dominant phase of WUP.
7) $\Delta t_{Rec} = t_{bit(RXD)} - t_{bit(BUS)}$
8) Not subject to production test, tolerance defined by internal oscillator tolerance.

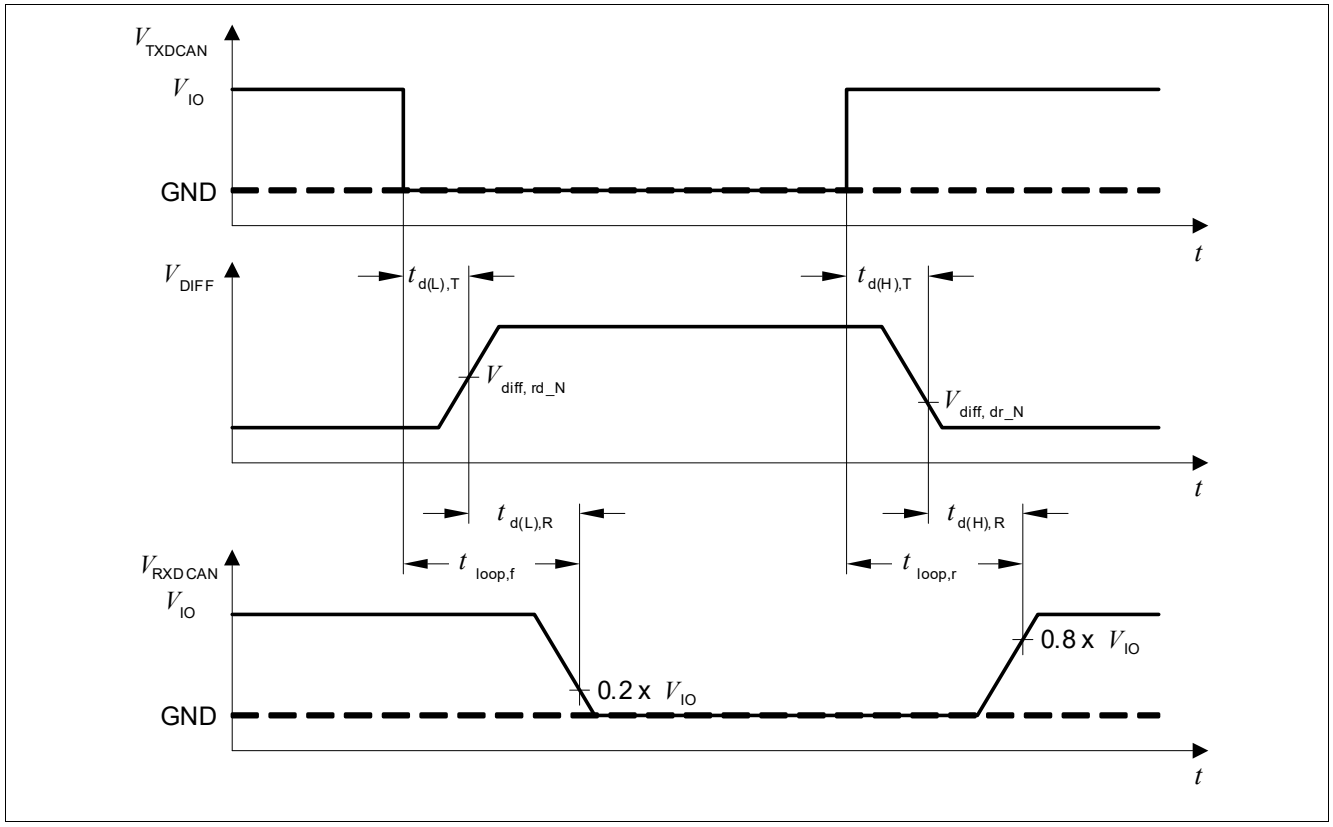


Figure 27 Timing Diagrams for Dynamic Characteristics

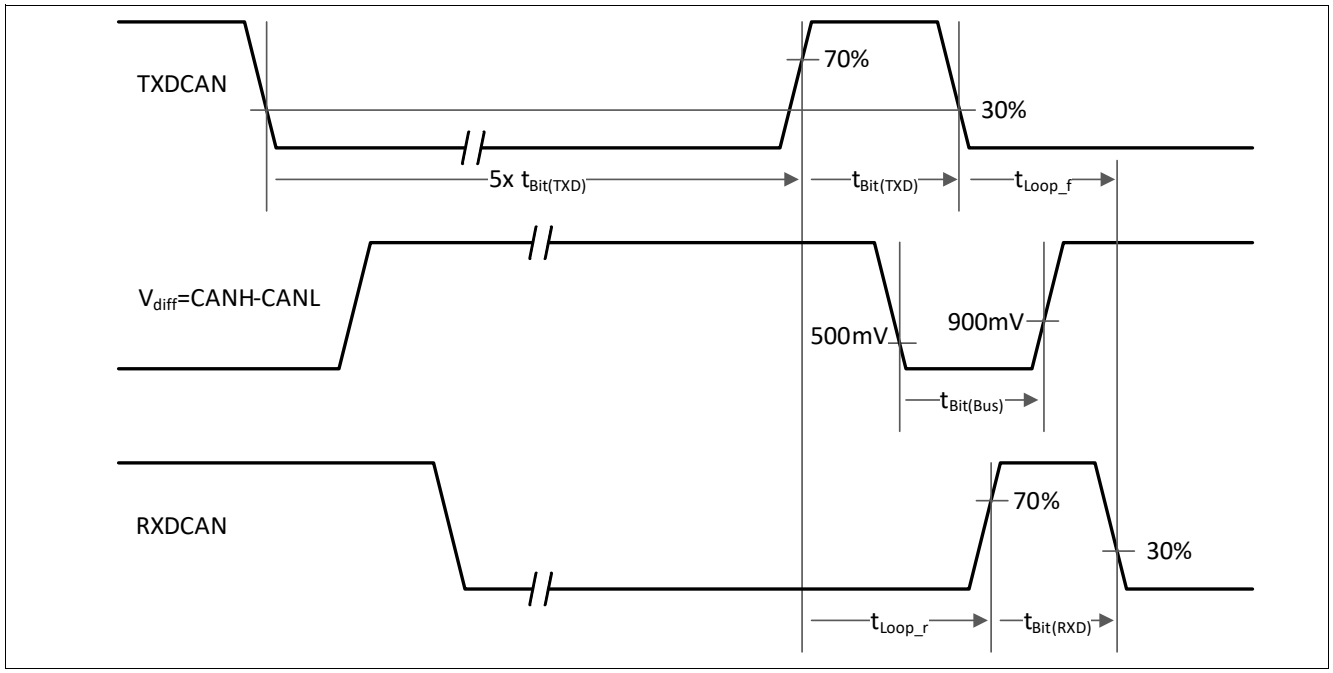


Figure 28 From ISO 11898-2: t_{Loop}, $t_{Bit(TXD)}$, $t_{Bit(RXD)}$ Definition

9 Wake Input

9.1 Features

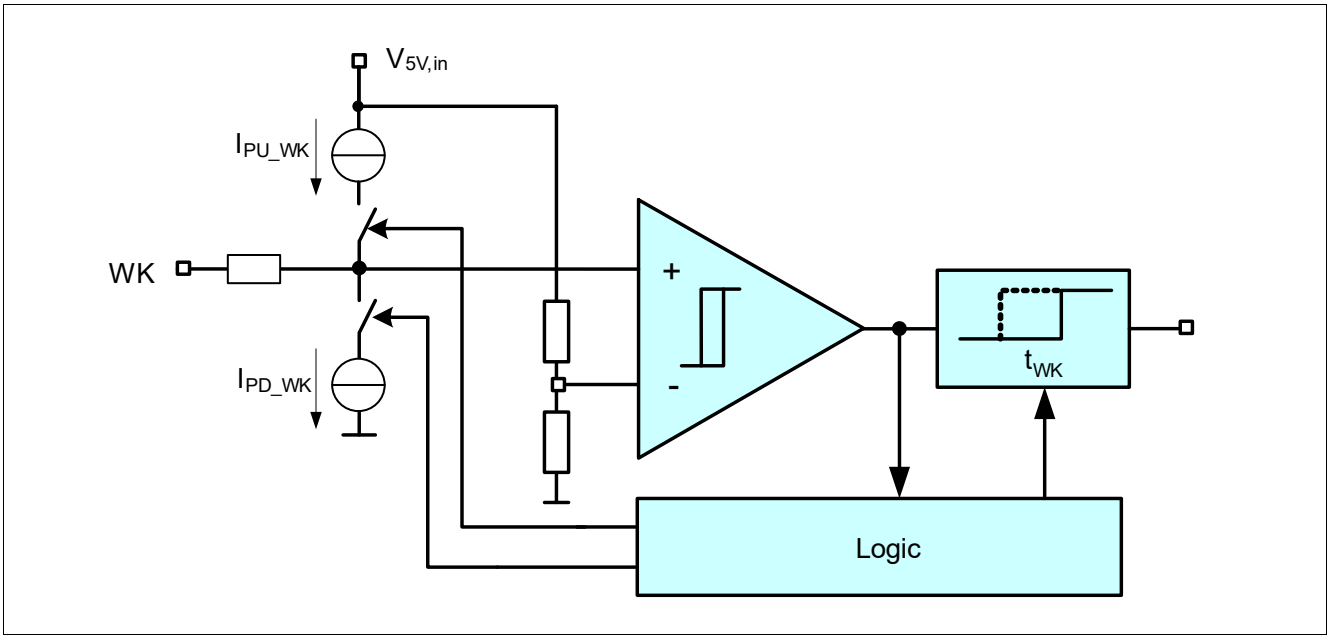


Figure 29 Wake Input Block Diagram

Features

- One HIGH-voltage inputs with V_{WKth} threshold voltage.
- Wake-up capability for power saving modes.
- Switch feature for DC/DC Mode (PFM/PWM) in SBC Stop Mode.
- Sensitive for level changes LOW to HIGH and HIGH to LOW.
- Pull-up and Pull-down current, selectable via SPI.
- In SBC Normal and Stop Mode, the WK pin level can be read via SPI.

9.2 Functional Description

The SBC can wake up following a voltage level change at the wake input. The WK input pin is sensitive to level changes. This means that both transitions, HIGH to LOW and LOW to HIGH, result in SBC signalling (see also **Figure 30**). The signal is created in one of the following ways:

- By triggering the interrupt in SBC Normal and SBC Stop Mode.
- By waking up the device in SBC Sleep and SBC Fail-Safe Mode.

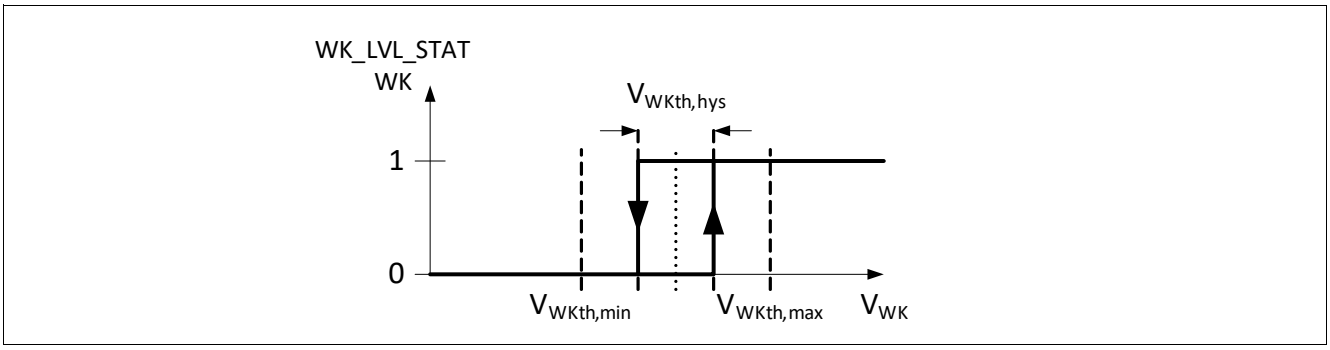


Figure 30 Wake Input Threshold Levels and Hysteresis

The wake-up capability, using WK pin, can be enabled or disabled via SPI command.

When the WK is enabled (**WK_EN** set to 1 on **WK_CTRL_1** register), the device wakes up from Sleep Mode with a HIGH to LOW or LOW to HIGH transition on the WK pin. In SBC Stop and Normal Mode, an Interrupt will be generated after t_{FWK} (filter time). In SBC Fail-Safe Mode, the WK is automatically selected as wake-up source and the device will always go to SBC Restart Mode with a HIGH to LOW or LOW to HIGH transition. The wake source for WK pin can be read in the register **WK_STAT_0** at the bit **WK_WU**.The state of the WK pin (LOW or HIGH) can always be read in SBC Normal and Stop Mode at the bit **WK** on register **WK_LVL_STAT**.

The WK pin can also be configured as a selection pin for PFM / PWM mode in SBC Stop Mode using the bit **PWM_BY_WK** of register **HW_CTRL_0**. In this case a LOW level at the WK pin will switch the Buck converter to PFM mode, a HIGH level will switch the Buck converter to PWM Mode maintaining the SBC in SBC Stop Mode. The filter time is not taken into account because a defined signal is expected (refer to **Chapter 6.2.2.2**).

In case that the **PWM_BY_WK** is used, it is still possible to use the WK pin to wake-up from SBC Sleep Mode to SBC Normal Mode.

Figure 31 shows a typical wake-up timing:

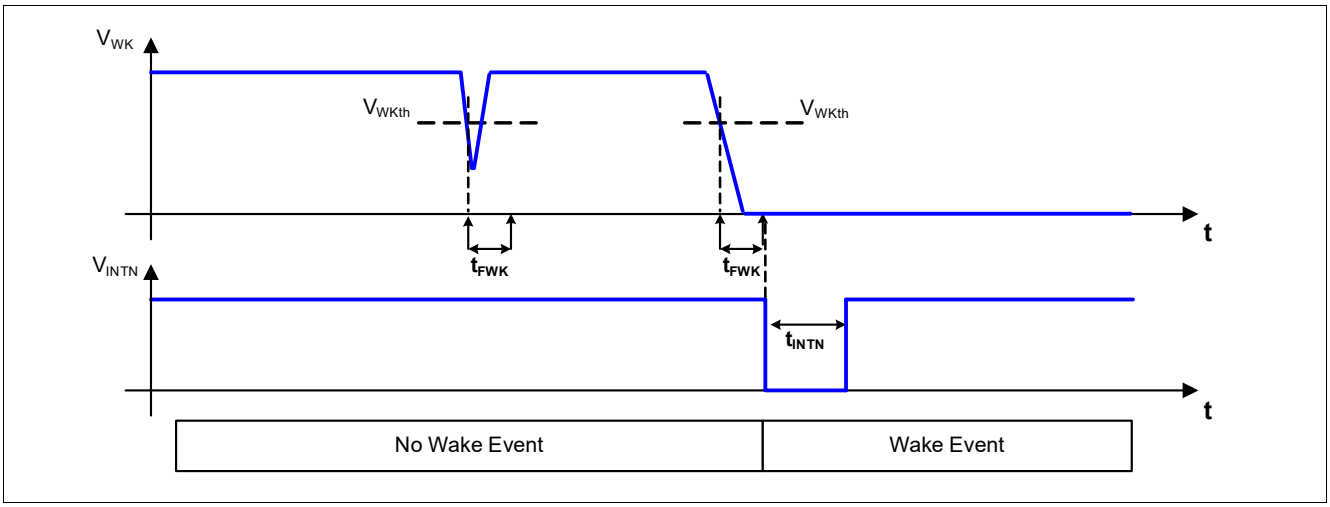


Figure 31 Wake-up Filter Timing for Static Sense

9.2.1 Wake Input Configuration

To ensure a defined and stable voltage level at the internal comparator input, it is possible to configure an integrated current source via the SPI register **WK_PUPD_CTRL**.

Table 24 shows the possible pull-up and pull-down current configuration.

Table 24 Pull-Up / Pull-Down Resistor

WK_PUPD_1	WK_PUPD_0	Output Current	Note
0	0	no current source	WK is floating if left open (default setting)
0	1	pull-down current	WK input internally pulled to GND
1	0	pull-up current	WK input internally pulled to 5V
1	1	automatic switching	If a HIGH level is detected, the pull-up current is activated If low level is detected, the pull down current is activated.

Note: If there is no pull-up or pull-down configured on the WK input, then the respective input should be tied to GND or V_S on board to avoid unintended floating and waking of the pin.

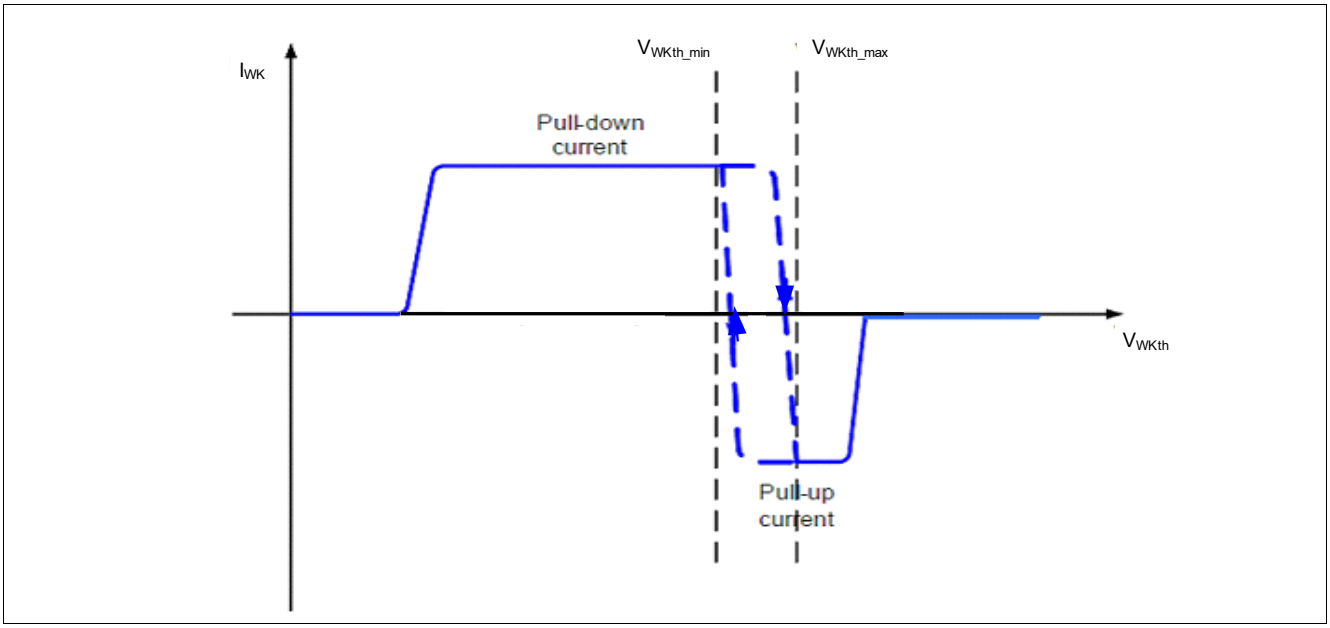


Figure 32 Illustration for Pull-Up / Down Current Sources with Automatic Switching Configuration

9.3 Electrical Characteristics

Table 25 Electrical Characteristics

T_j = -40°C to +150°CT_j = -40°C to +150°C; V_S = 5.5 V to 28 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
WK Input Pin characteristics							
Wake-up/monitoring threshold voltage	V_{WKth}	2	3	4	V	Falling and rising edge included	P_9.3.1
Threshold hysteresis	$V_{WKNth,hys}$	0.1	–	0.7	V	2)	P_9.3.2
WK pin Pull-up Current	I_{PU_WK}	-20	-10	-3	µA	V_{WK_IN} = 4 V	P_9.3.3
WK pin Pull-down Current	I_{PD_WK}	3	10	20	µA	V_{WK_IN} = 2 V	P_9.3.4
Input leakage current	$I_{LK,I}$	-2	–	2	µA	0 V < V_{WK_IN} < V_S+0.3 V 1)	P_9.3.5
Timing							
Wake-up filter time	t_{FWK}	12	16	20	µs	2)	P_9.3.6

1) With pull-up, pull down current disabled.

2) Not subject to production test; specified by design.

10 Interrupt Function

10.1 Block and Functional Description

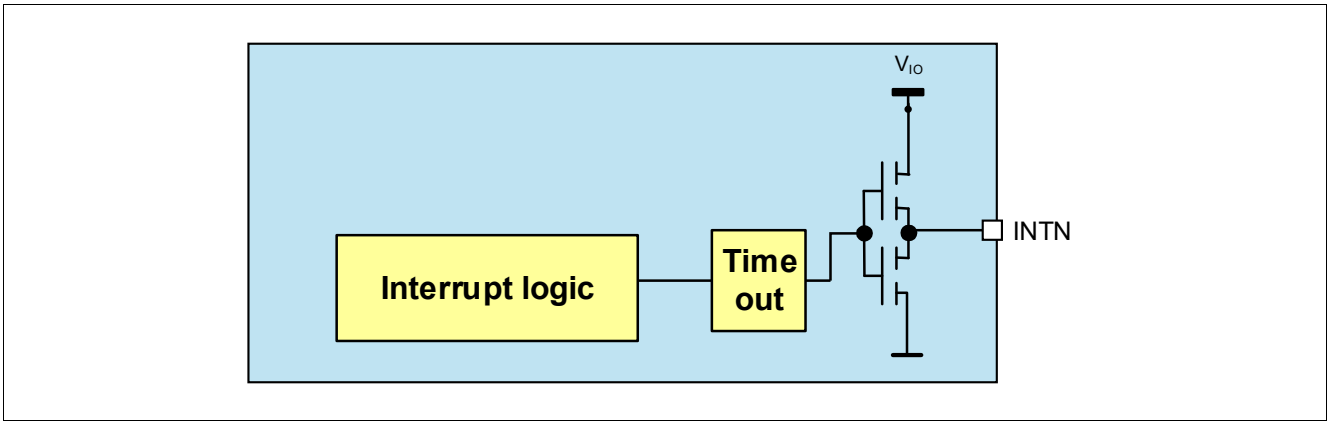


Figure 33 Interrupt Block Diagram

The interrupt is used to signal wake-up events in real time to the microcontroller. The interrupt block is designed as a push/pull output stage as shown in **Figure 33**. An interrupt is triggered and the INTN pin is pulled low (active low) for t_{INTN} in SBC Normal and Stop Mode and it is released again once t_{INTN} is expired. The minimum HIGH-time of INTN between two consecutive interrupts is t_{INTD}. An interrupt does not automatically cause a SBC mode change.

The following wake-up events will be signalized via INTN:

- All wake-up events stored in the wake status SPI register **WK_STAT_0** and **WK_STAT_2**.
- If the bit CANTO_x is set and if it was not masked out.
- The VBAT (at pin VBSENSE) monitoring threshold is triggered.
- An interrupt is only triggered if the respective function is also enabled as a wake source.
- Automatic transition from PFM to PWM mode in SBC Stop Mode.

The register **WK_LVL_STAT** is not generating interrupt events.

In addition to this behavior, an INTN will be triggered when the SBC is sent to SBC Stop Mode and not all bits were cleared in the **WK_STAT_0** and **WK_STAT_2**registers.

The SPI status registers are updated at every falling edge of the INTN pulse. All interrupt events are stored in the respective register (except the register **WK_LVL_STAT**) until the register is read and cleared via an SPI command. The interrupt behavior is shown in **Figure 34**.

Interrupt Function

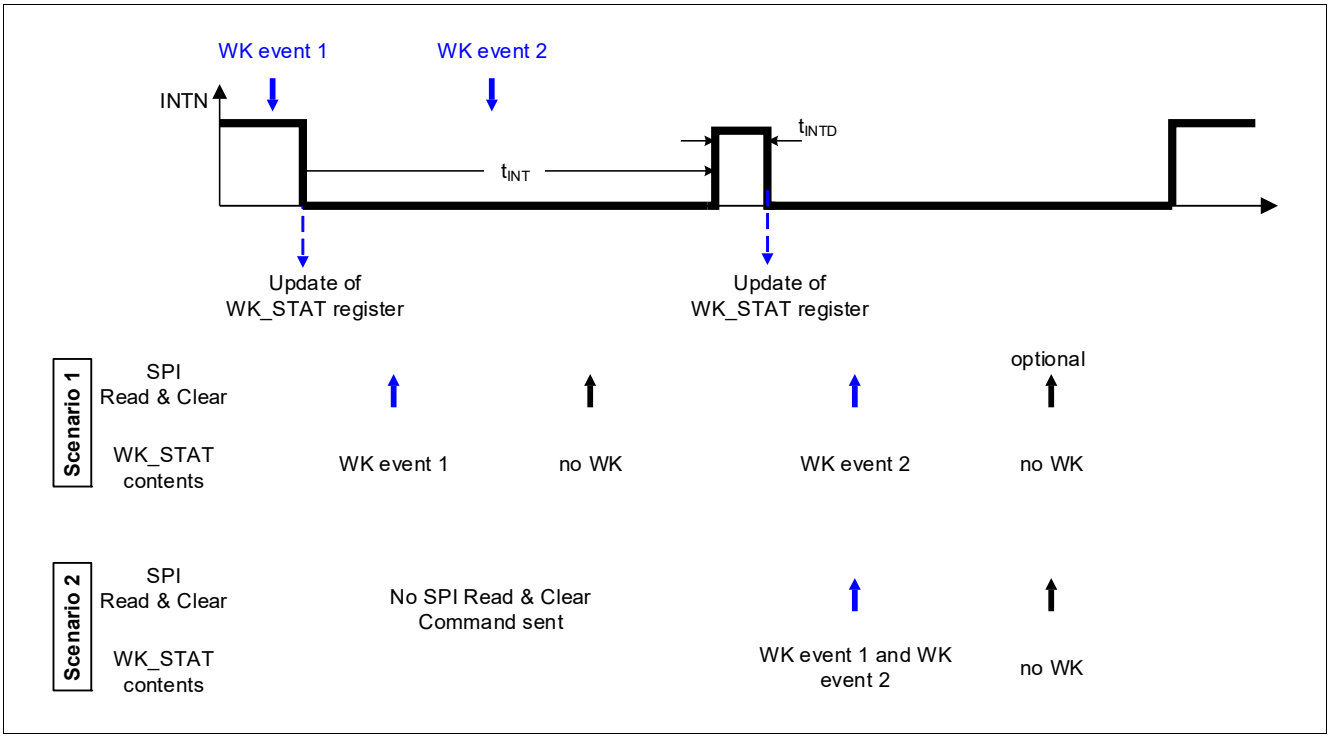


Figure 34 Interrupt Signaling Behavior

10.2 Electrical Characteristics

Table 26 Interrupt Output

V_S = 6 V to 28 V; T_j = -40°C to +150°C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Interrupt output; Pin INTN							
INTN HIGH Output Voltage	$V_{INTN,H}$	0.8 × V_{IO}	–	–	V	I_{INTN} = -2 mA; INTN = OFF	P_10.2.1
INTN LOW Output Voltage	$V_{INTN,L}$	–	–	0.2 × V_{IO}	V	I_{INTN} = 2 mA; INTN = ON	P_10.2.2
INTN Pulse Width	t_{INTN}	80	100	120	µs	1)	P_10.2.3
INTN Pulse Minimum Delay Time	t_{INTD}	80	100	120	µs	1) Between consecutive pulses	P_10.2.4
Configuration Select; Pin INTN							
Config Pull-down Resistance	R_{CFG}	–	250	–	kΩ	V_{INTN} = 5 V	P_10.2.5
Config Select Filter Time	t_{CFG_F}	6	8	10	µs	1)	P_10.2.6

1) Not subject to production test; specified by design.

11 Fail Output

11.1 Functional Description

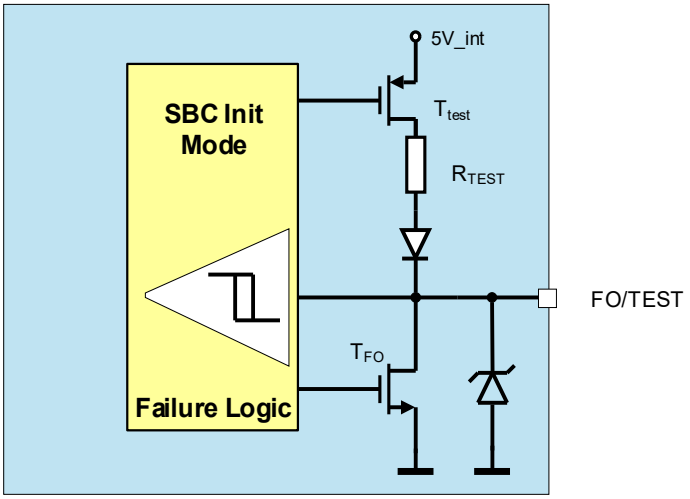


Figure 35 Fail Output Block Diagram

The Fail Output consists of a failure logic block and one LOW-side switch. In case of a failure, the FO output is activated and the SPI bit **FO_ON_STATE**, in the register **DEV_STAT**, is set.

The Failure Output is activated due to the following failure conditions.

Failure Conditions

- After one or two Watchdog Trigger failures depending on the configuration.
- Thermal Shutdown **TSD2**.
- VIO short to GND.
- VIO overvoltage in case that **VIO_OV_RST** bit is set.
- After four consecutive VIO undervoltage detection.

Configurations

Four different configurations can be selected. The selection is done using the pin INTN and the SPI bit **CFG2**.

Table 27 Reasons for Fail

Config	Event	Fail-Safe Mode Entered	SPI CFG2 bit	INTN pin
1	1 × watchdog failure	no	1	External pull-up
2	1 × watchdog failure	yes	1	No ext. pull-up

Fail Output

Table 27 Reasons for Fail (cont'd)

Config	Event	Fail-Safe Mode Entered	SPI CFG2 bit	INTN pin
3	2 × watchdog failure	no	0	External pull-up
4	2 × watchdog failure	yes	0	No ext. pull-up

In order to deactivate the Fail Output, the failure conditions (e.g. TSD2) must not be present anymore and the bit **FO_ON_STATE** needs to be cleared via SPI command.

In case of Watchdog fail, the deactivation of the Fail Output is only allowed after a successful WD trigger, i.e. the **FO_ON_STATE** bit must be cleared.

Note: The Fail Output pin is triggered for any of the above described failure and not only for failures leading to the SBC Fail-Safe Mode.

11.2 Electrical Characteristics

Table 28 Interrupt Output

V_S = 6 V to 28 V; T_j = -40°C to +150°C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Fail Output; Pin FO/TEST							
FO LOW output voltage (active)	$V_{FO,L}$	–	0.6	1	V	I_{FO} = 5 mA	P_11.2.1
FO HIGH output leakage current (inactive)	$I_{FO,H}$	0	–	2	µA	V_{FO} = 28 V	P_11.2.2
FO/TEST HIGH-input voltage threshold	$V_{TEST,H}$	–	–	3.5	V	–	P_11.2.3
FO/TEST LOW-input voltage threshold	$V_{TEST,L}$	1.5	–	–	V	–	P_11.2.4
FO/Pull-up Resistance at pin TEST	R_{TEST}	2.5	5	10	kΩ	1) V_{TEST} = 0 V	P_11.2.6
FO/TEST Input Filter Time	t_{TEST}	52	64	81	µs	1)	P_11.2.7

1) Not subject to production test; specified by design.

12 Supervision Functions

12.1 Reset Function

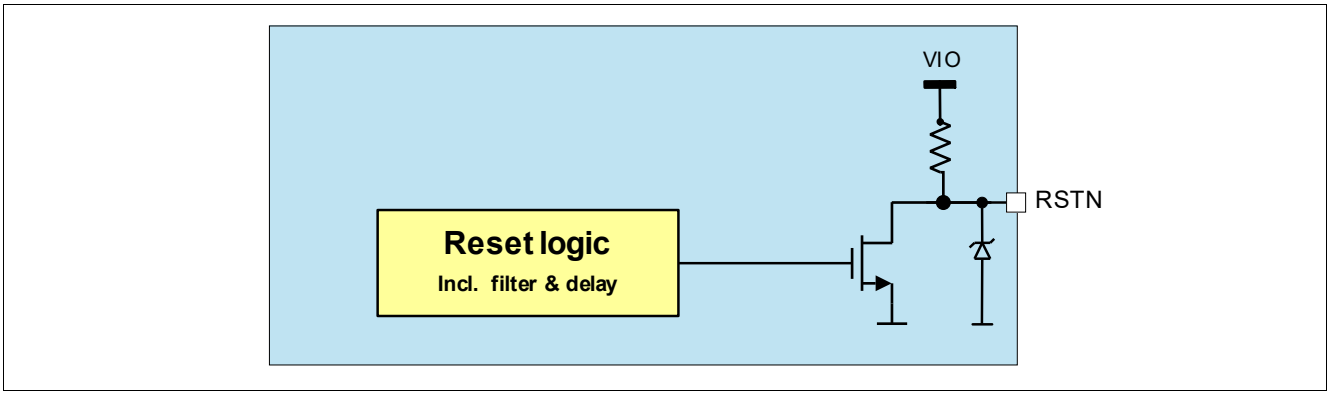


Figure 36 Reset Block Diagram

12.1.1 Reset Output Description

The reset output pin RSTN provides a reset information to the microcontroller, e.g. when the VIO voltage falls below the undervoltage threshold $V_{RT1/2/3/4}$. In case of a reset event due to an undervoltage on V_{IO}, the reset output RSTN is pulled to LOW after the filter time t_{RF} and stays LOW as long as the reset event is present plus a reset delay time t_{RD1}. When connecting the SBC to battery voltage, the reset signal remains LOW initially. When the output voltage V_{IO} has reached the default reset threshold $V_{RT1,f}$, the reset output RSTN is released to HIGH after the reset delay time t_{RD1}. A reset can also occur due to a Watchdog trigger failure. The reset threshold can be adjusted via SPI; the default reset threshold is $V_{RT1,f}$. The RSTN pin has an integrated pull-up resistor. In case reset is triggered, RSTN will pull LOW for $V_S \geq V_{POR,f}$.

The RSTN trigger timing regarding the VIO undervoltage and watchdog trigger is shown in **Figure 37**.

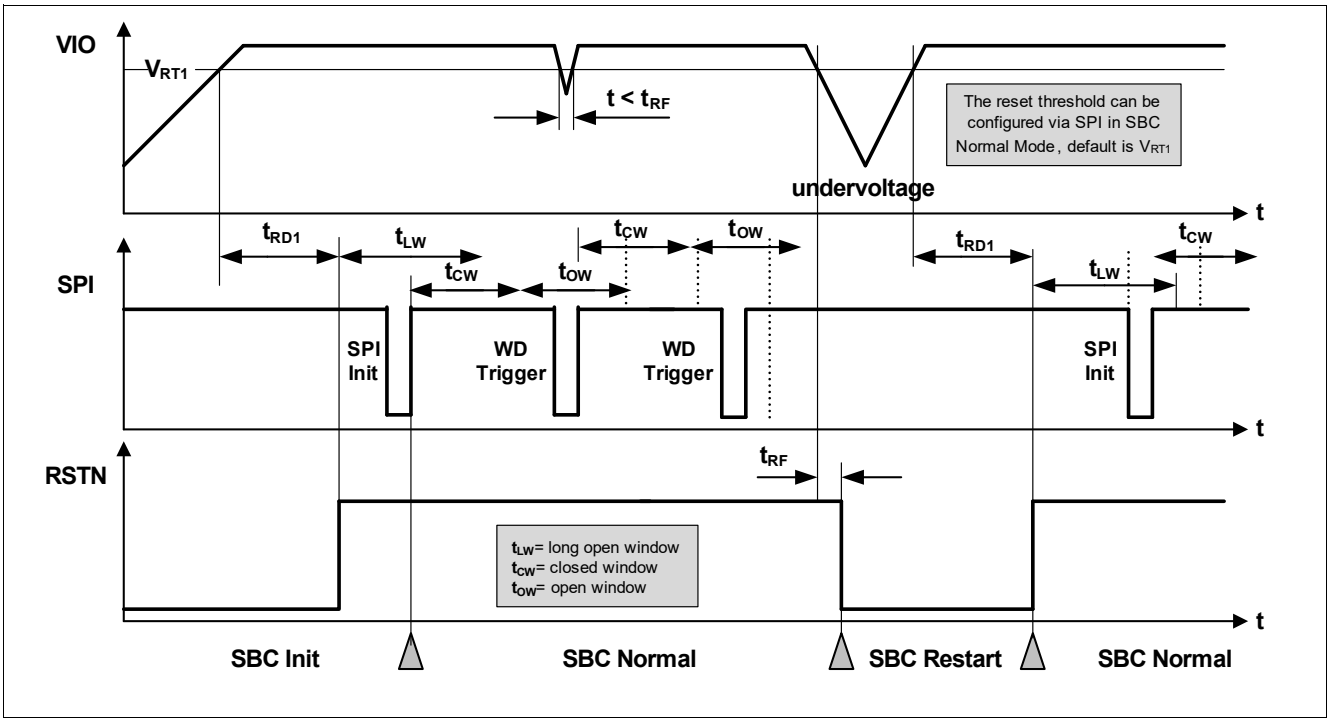


Figure 37 Reset Timing Diagram

12.1.2 Soft Reset Description

In SBC Normal and Stop Mode, It is also possible to trigger a Soft Reset via an SPI command in order to bring the SBC into a defined state in case of failures. In this case the microcontroller must send an SPI command and set the **MODE** bits to '11' in the **M_S_CTRL** register. As soon as this command becomes valid, the SBC is set back to SBC Init Mode and all SPI registers are set to their default values (see SPI **Chapter 13.5** and **Chapter 13.6**).

As soon as the SBC is in SBC Init Mode due to a software reset, it is possible to change the device configuration according to the FO/Test, INTN pins and **CFG2** bit value. For more information, refer to **Chapter 5.1.1**.

Two different soft reset configurations are possible via the SPI bit **SOFT_RESET_ RSTN**:

- The reset output (RSTN) is triggered when the soft reset is executed (default setting, the same reset delay time t_{RD1} applies).
- The reset output (RSTN) is not triggered when the soft reset is executed.

Note: The device must be in SBC Normal Mode or SBC Stop Mode when sending this command. Otherwise, the command will be ignored.

12.2 Watchdog

The watchdog is used to monitor the software execution of the microcontroller and to trigger a reset if the microcontroller stops serving the watchdog due to a lock up in the software.

Two different types of watchdog functions are implemented and can be selected via the bit **WD_WIN** on the **WD_CTRL** register:

- Time-Out Watchdog (default value).
- Window Watchdog.

The respective watchdog function can be selected and programmed in SBC Normal Mode. The configuration remains unchanged in SBC Stop Mode.

Refer to **Table 29** to match the SBC Modes with the respective Watchdog Modes.

Table 29 Watchdog Functionality by SBC Modes

SBC Mode	Watchdog Mode	Remarks
INIT Mode	Start with Long Open Window	Watchdog starts with Long Open Window after RSTN is released.
Normal Mode	WD Programmable	Window Watchdog, Time-Out watchdog or switched OFF for SBC Stop Mode.
Stop Mode	Watchdog is fixed or OFF	
Sleep Mode	OFF	SBC will start with Long Open Window when entering Normal Mode.
Restart Mode	OFF	SBC will start with Long Open Window when entering Normal Mode.
Fail-Safe Mode	OFF	SBC will start with Long Open Window when entering Normal Mode.

Watchdog timing is programmed via an SPI command. As soon as the Watchdog is programmed, the timer starts with the new setting and the Watchdog must be served.

The Watchdog is triggered by sending a valid SPI command with write access to **WD_CTRL** register. The trigger SPI command is executed when the Chip Select input (CSN) becomes HIGH.

When coming from SBC Init, Restart or in certain cases Stop Mode, the watchdog timer starts with a long open window.

The long open window (t_{LW}) allows the microcontroller to run its initialization sequences and then to trigger the Watchdog via the SPI.

The watchdog timer period can be selected via the watchdog timing bit field (**WD_TIMER** on **WD_CTRL** register) and it is in the range of 10 ms up to 1000 ms. The timer setting is valid for both watchdog types.

The following Watchdog timer periods are available:

- WD Setting 1: 10 ms
- WD Setting 2: 20 ms
- WD Setting 3: 50 ms
- WD Setting 4: 100 ms
- WD Setting 5: 200 ms (reset value)
- WD Setting 6: 500 ms
- WD Setting 7: 1000 ms

In case of a watchdog reset, SBC Restart Mode is started or SBC Fail-Safe Mode is entered according to the configuration and **WD_FAIL** bits are set.

Once the RSTN goes HIGH again, the watchdog immediately starts with a long open window and the SBC enters automatically in SBC Normal Mode.

In SBC Development Mode, no reset is generated due to watchdog failure; the watchdog is OFF.

In case of 3 consecutive resets due to WD fail, it is possible in config 1/3 not to generate additional resets by setting the **MAX_3_RST** bit on **WD_CTRL** register.

12.2.1 Time-Out Watchdog

The time-out watchdog is an easier and less secure watchdog than a window watchdog as the watchdog trigger can become active at any time within the configured watchdog timer period.

A correct watchdog service immediately results in starting a new watchdog timer period. Taking the tolerances of the internal oscillator into account leads to the safe trigger area defined in **Figure 38**.

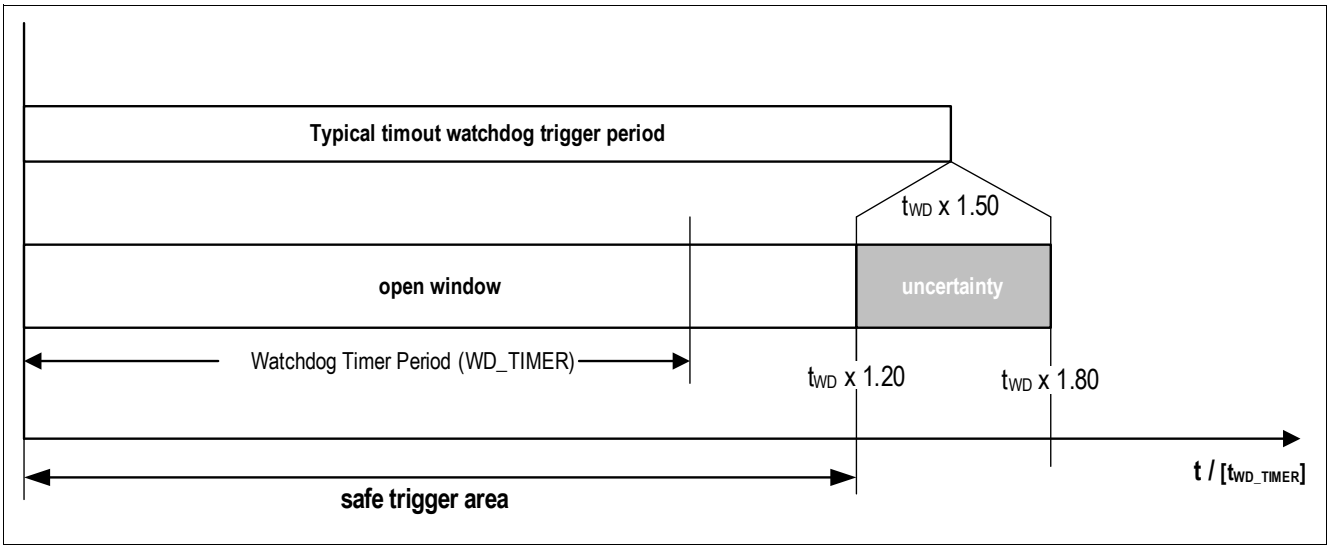


Figure 38 Time-Out Watchdog Definitions

If the time-out watchdog period elapses, a watchdog reset is created by setting the reset output RSTN LOW and the SBC switches to SBC Restart or SBC Fails-Safe Mode.

12.2.2 Window Watchdog

Compared to the time-out watchdog, the characteristic of the window watchdog is that the watchdog timer period is divided between a closed and an open window. The watchdog must be triggered inside the open window.

A correct watchdog trigger results in starting the window watchdog period by a closed window followed by an open window.

The watchdog timer period is at the same time the typical trigger time and defines the middle of the open window.

Taking the oscillator tolerances into account leads to a safe trigger area of:

$t_{WD} \times 0.72 <$ safe trigger area $< t_{WD} \times 1.20$.

The typical closed window is defined to a width of 60% of the selected window watchdog timer period. Taking the tolerances of the internal oscillator into account leads to the timings as defined in **Figure 39**.

A correct Watchdog service immediately results in starting the next closed window.

Should the trigger signal meet the closed window or should the watchdog timer period elapse, a watchdog reset is created by setting the reset output RSTN LOW and the SBC switches to SBC Restart or Fail-Safe Mode.

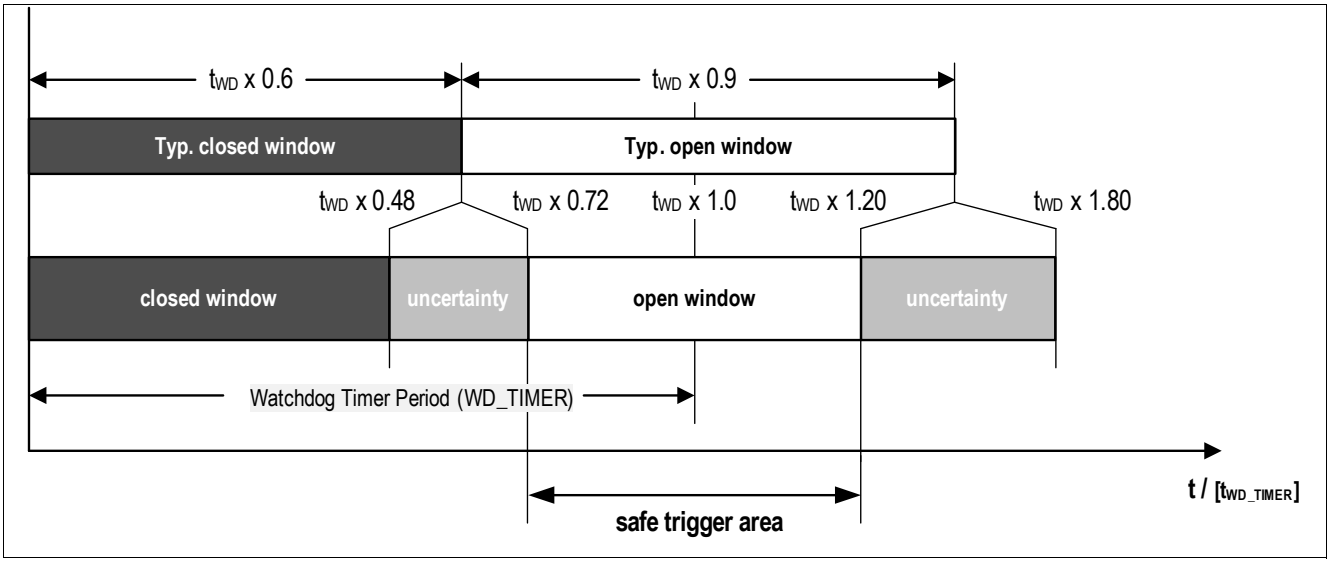


Figure 39 Window Watchdog Definitions

12.2.3 Checksum

A checksum bit is part of the SPI command to trigger the watchdog and to set the watchdog setting. The sum of the 8 bits in the register **WD_CTRL** needs to be even. This is realized by either setting the bit **CHECKSUM** to “0” or “1”. If the checksum is wrong, the SPI command is ignored (watchdog not triggered, settings not changed) and the bit **SPI_FAIL** is set.

The checksum is calculated by taking all 8 data bits into account.

(12.1)

$$CHKSUM = Bit15 \oplus \ldots \oplus Bit8$$

12.2.4 Watchdog during Stop Mode

The watchdog can be disabled via SPI in Stop Mode.

For safety reasons, there is a special sequence to be ensured in order to disable the watchdog as described in **Figure 40**. Two dedicated SPI bits (**WD_STM_EN_0** and **WD_STM_EN_1**) in the registers **WD_CTRL** and **WK_CTRL_0**.

If this sequence is not fulfilled, then the bit **WD_STM_EN_1** will be cleared and the sequence has to be started again. As soon as the SBC is set to SBC Normal Mode, then the bits **WD_STM_EN_1** and **WD_STM_EN_0** are cleared and this sequence must be followed again to switch OFF the watchdog.

The watchdog can be enabled by triggering the watchdog in SBC Stop Mode or by switching back to SBC Normal Mode via SPI. In both cases, the watchdog will start with a long open window and the bits **WD_STM_EN_1** and **WD_STM_EN_0** are cleared. After the long open window, the watchdog has to be served as configured in the **WD_CTRL** register.

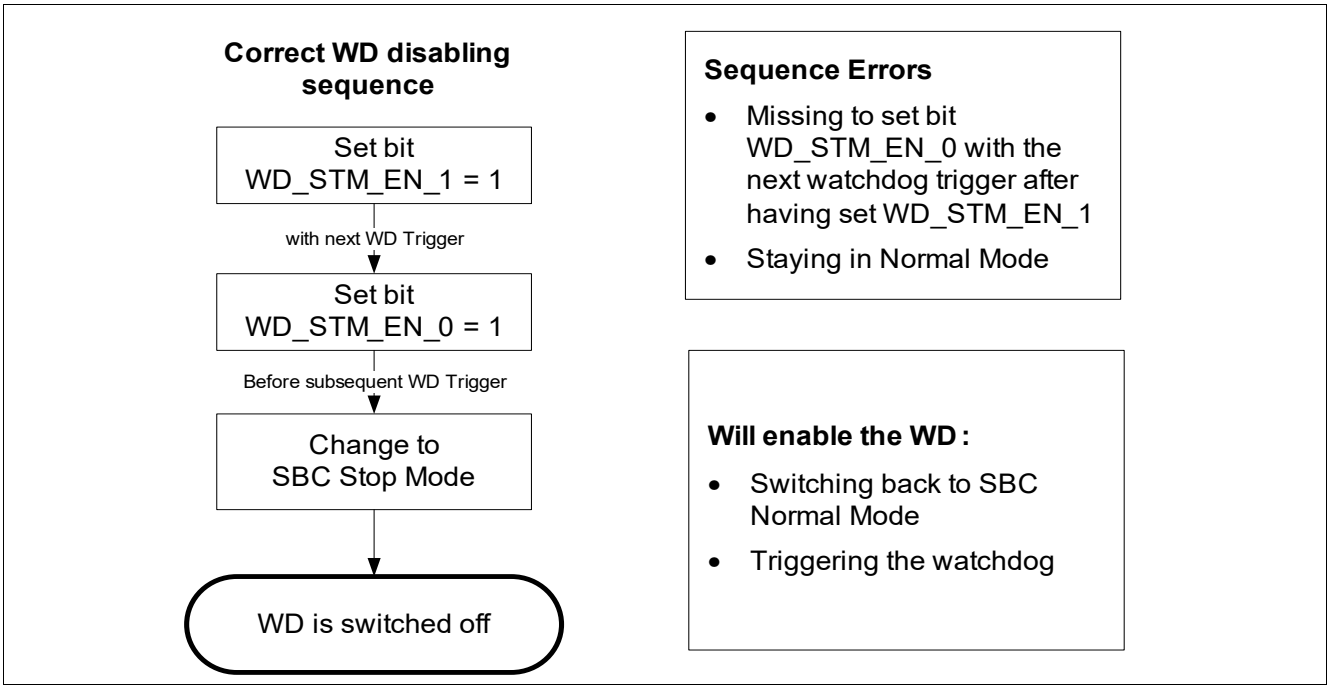


Figure 40 Watchdog Disabling Sequence

*Note: The bit **WD_STM_EN_0** will be cleared automatically when the sequence is started and it was "1" before.*

12.2.4.1 Watchdog Start in SBC Stop Mode due to BUS Wake

In SBC Stop Mode the watchdog can be disabled. In addition a feature can be enabled to start the watchdog with any BUS wake during Stop Mode. The feature is enabled by setting the bit **WD_EN_WK_ BUS**. The bit can only be changed in SBC Normal Mode and needs to be programmed before entering SBC Stop Mode: it is not reset by the SBC. The sequence described in **Chapter 12.2.4** needs to be followed to disable the WD.

With the function enabled, the watchdog will start again with any wake on CANx. The wake on CANx will generate an interrupt and the RXDCANx is pulled to low. The watchdog starts a with long open window. The watchdog can be triggered in SBC Stop Mode or the SBC can be switched to SBC Normal Mode. To disable the watchdog again, the SBC needs to be switched to Normal Mode and the sequence needs to be sent again.

The sequence is shown in **Figure 41**.

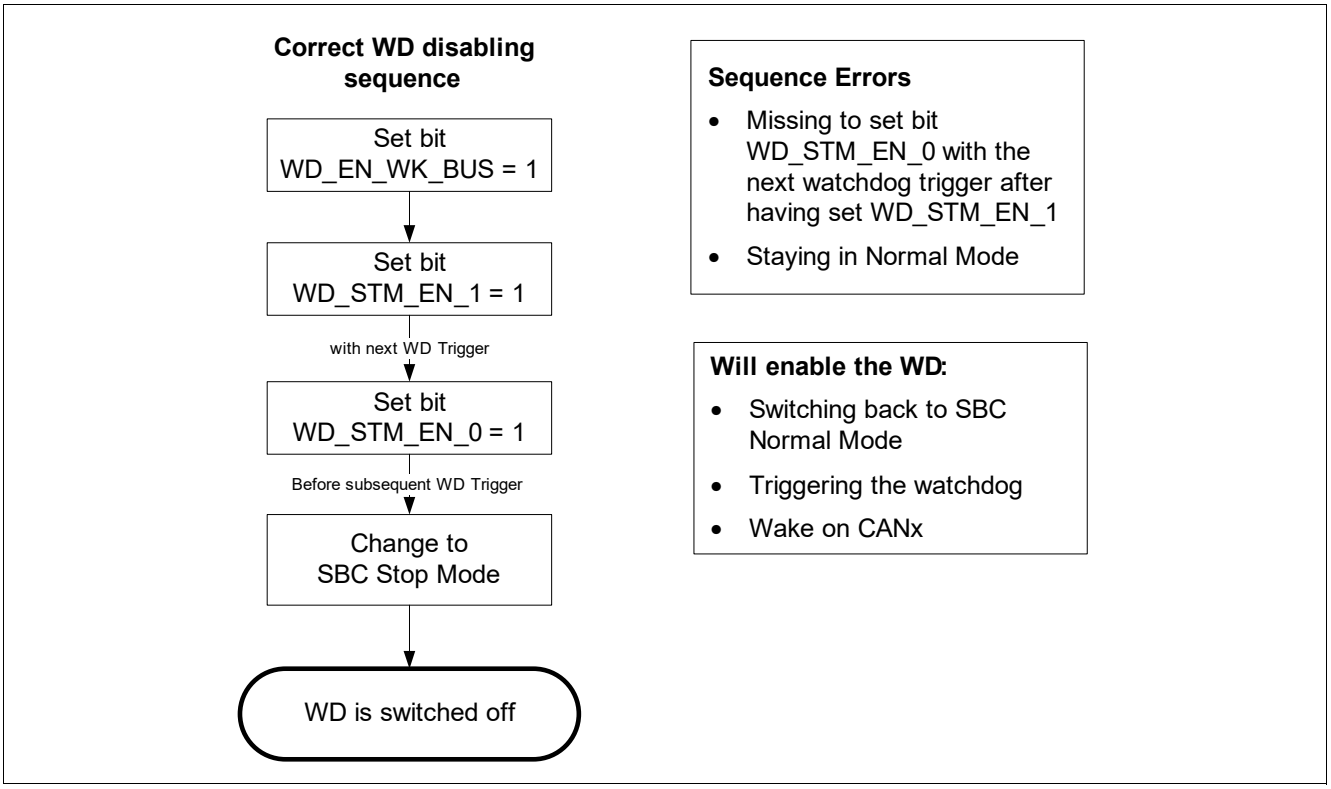


Figure 41 Watchdog Disabling Sequence (with wake via BUS)

12.3 V_S Power ON Reset

When powering up, the device detects the V_S Power ON Reset when V_S > **$V_{POR,f}$**, and the **POR** is set to indicate that all SPI registers are set to POR default setting. The Buck regulator starts up. The RSTN output is kept LOW and is only released when VIO has exceeded **$V_{RT1,r}$** and after **t_{RD1}** has elapsed.

If V_S<**$V_{POR,f}$**, an internal reset is generated and the SBC is switched OFF. The SBC will restart in SBC INIT Mode when V_S>**$V_{POR,r}$** rising. Timing behavior is shown in **Figure 42**.

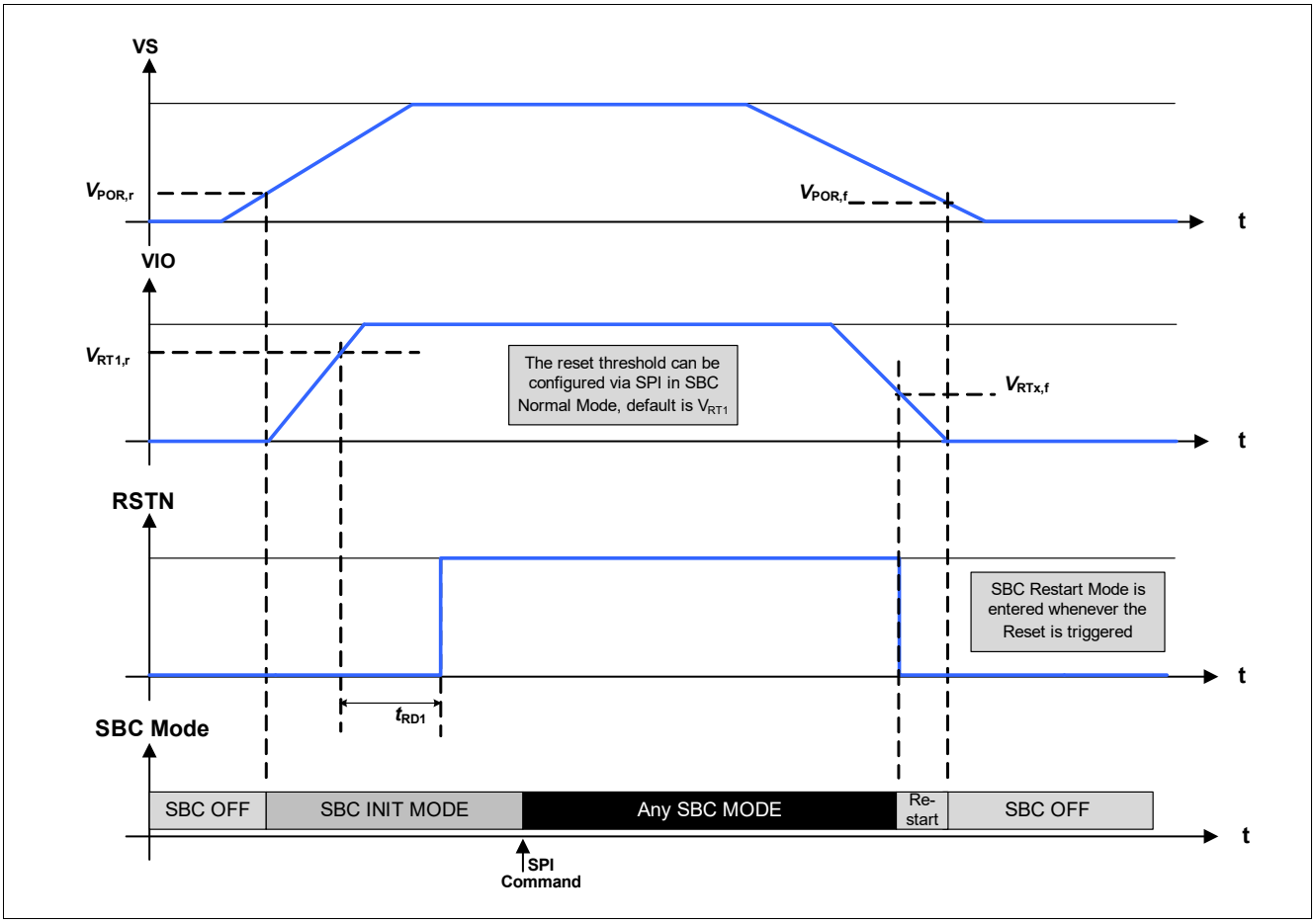


Figure 42 Ramp up / down example of Supply Voltage

12.4 Measurement Interface

The measurement interface is sensing the voltage on WK and VBSENSE pin, converting to digital using a 8 bit SAR high input voltage analog to digital converter and store the value in **ADC_STAT**.

The input selection (between WK pin or VBSENSE pin) is made by **ADC_SEL** bit on **HW_CTRL_1** register.

The feature is available only in SBC Normal Mode. In SBC Stop, Sleep and Fail Safe Mode, the feature is automatically disabled to reduce current consumption. **Figure 43** shows the block diagram.

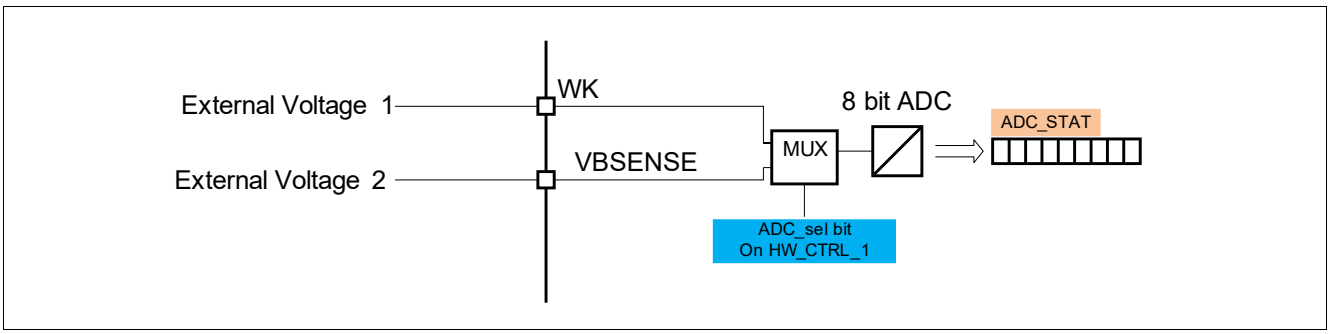


Figure 43 Measure Interface: basic concept implementation.

12.5 Fast Battery Voltage Monitoring

A battery monitoring feature is implemented in the TLE9278-3BQX V33 in order to provide a fast signalization path to the microcontroller in case of low battery voltage condition.
The block diagram is shown in **Figure 44**. The functionality is as follows:

- The battery voltage is monitored on the dedicated pin VBSENSE (see also the application diagram in **Chapter 14.1**).
- If the voltage falls below the selected threshold, an interrupt is triggered at the INTN pin and the bit **VBAT_UV_ LATCH** in the register **WK_STAT_2** is set.
- The bit can be cleared via an SPI if the voltage is above the thresholds again.
- The bit **VBAT_UV_ STATE** in the register **WK_LVL_STAT** is showing the actual level of the comparator output, i.e. if the battery voltage is below or above the selected monitoring threshold.
- The monitoring threshold can be selected via SPI bit with **VBSENSE_CFG** in the **WK_CTRL_0** register. The feature can be enable in SBC Normal, Stop and Restart Mode using **VBSENSE_EN** bit on the **WK_CTRL_0** register. Four thresholds are available: $V_{BSENSE0,f}$...$V_{BSENSE3,f}$.
- The Fast Battery voltage monitoring feature is filtered with the time $t_{F\_VBSENSE}$.

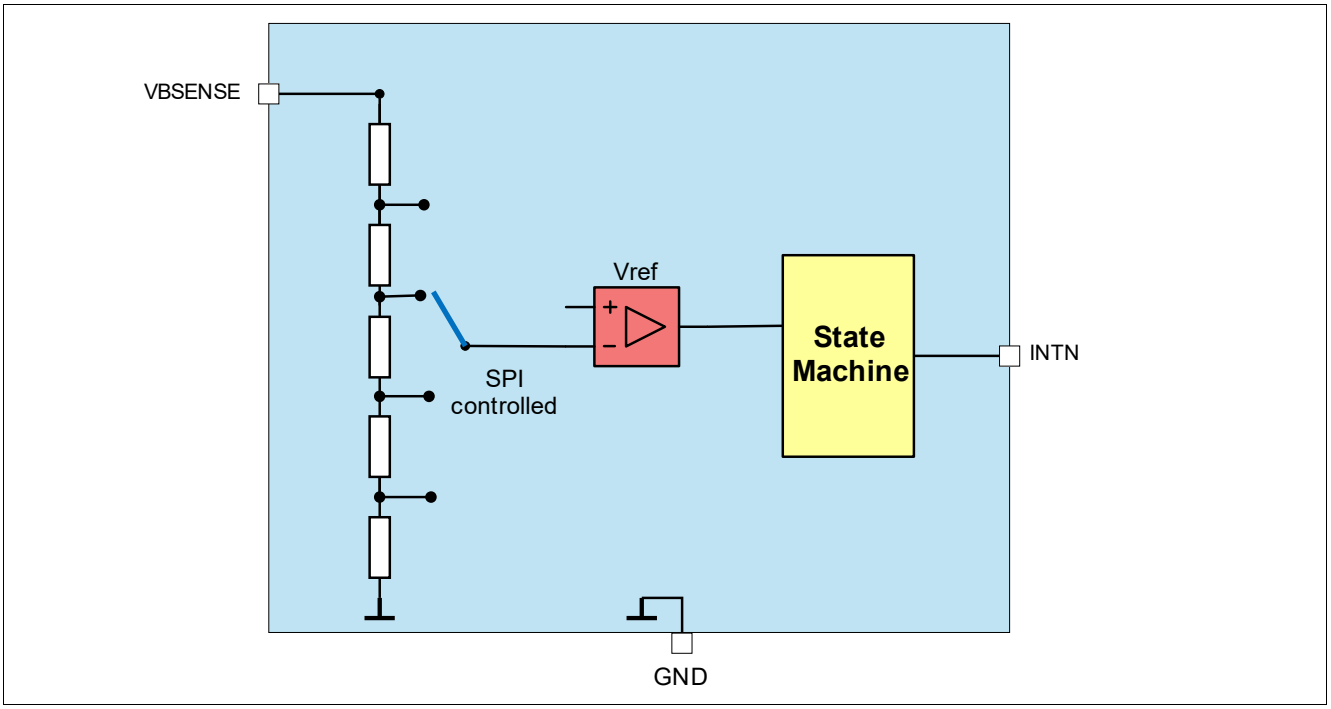


Figure 44 Fast Battery Voltage Monitoring Block Diagram

12.6 VBSENSE Boost deactivation

In case of low battery voltage conditions, where the Boost module can operate out of nominal functional range, it is possible to disable the boost and supply the VS pin only with the output boost capacitor.

The **BST_VB_UV_ OFF** bit enable this feature.

As soon as the battery voltage is crossing the $Boost_{OFF,th}$ threshold, the boost is disabled and **VB_UV_BST** is set.

The Boost is automatically enabled when the VBSENSE is crossing $Boost_{ON,th}$ threshold.

The **VB_UV_BST** bit has to be cleared manually.

12.7 VIO Undervoltage and Undervoltage Prewarning

A first-level voltage detection threshold is implemented as a prewarning for microcontroller. The prewarning event is signaled with the bit **VIO_WARN**. No other actions are taken.

As described in **Chapter 12.1** and shown in **Figure 45**, when the VIO voltage reaches the undervoltage threshold (V_{RTx}), a reset will be triggered (RSTN pulled 'LOW'), the bit **VIO_UV** is set and the SBC will enter SBC Restart Mode.

*Note: The **VIO_WARN** and **VIO_UV** bits are not set in SBC Sleep Mode as VIO = 0 V in this case.*

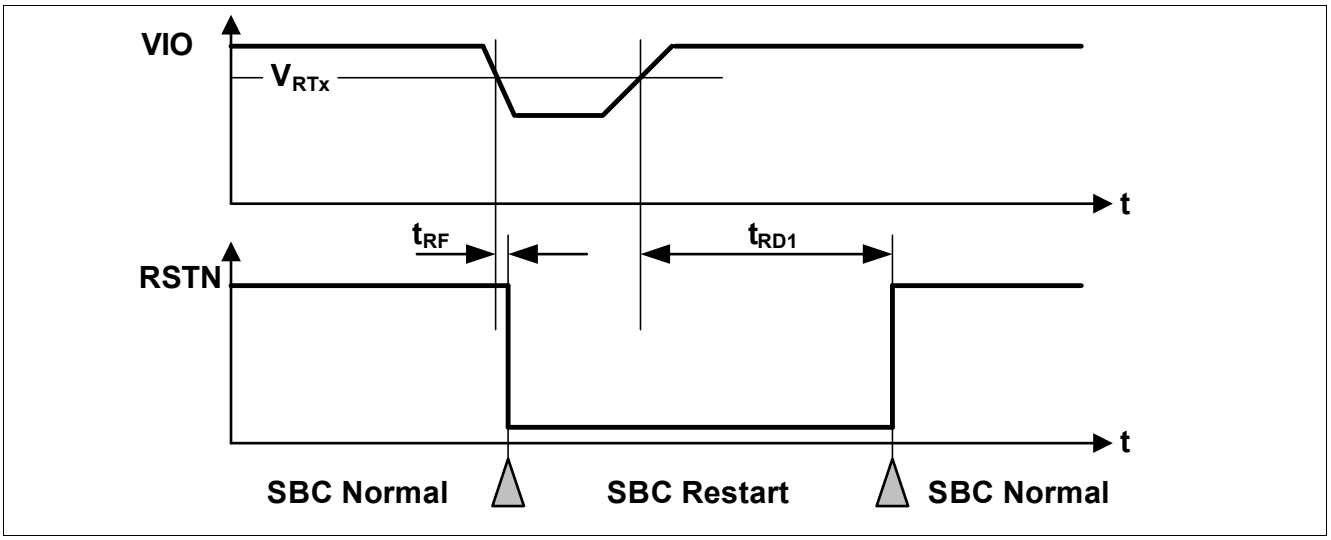


Figure 45 VIO Undervoltage Timing Diagram

An additional safety mechanism is implemented to avoid repetitive VIO undervoltage resets:

- A counter is increased for every consecutive VIO undervoltage event.
- The counter is active in SBC Init, Normal and Stop Mode and as V_S > **$V_{S,UV}$**.
- A 4th consecutive VIO undervoltage events will lead to SBC Fail-Safe Mode entry and to setting the bit **VIO_UV_FS**.
- The counter is cleared when:
  - SBC Fail-Safe Mode is entered.
  - The bit **VIO_UV** is cleared.
  - A Soft Reset is triggered.

*Note: It is recommended to clear the **VIO_UV** bit once it was set and detected.*

12.8 VIO Overvoltage

For fail safe reasons, a configurable VIO overvoltage detection feature is implemented.

In case the **$V_{IO,OV,r}$** threshold is crossed, the SBC triggers following measures depending on the configuration:

- The bit **VIO_OV** is always set.
- If the bit **VIO_OV_RST** is set in config 1/3, then SBC Restart Mode is entered. The FO output is activated. After the reset delay time (**t_{RD1}**), the SBC Restart Mode is exited and SBC Normal Mode is resumed even if the VIO overvoltage event is still present (see also **Figure 46**). The **VIO_OV_RST** bit is cleared automatically.
- If the bit **VIO_OV_RST** is set in config 2/4, then SBC Fail-Safe Mode is entered and FO output is activated.

If the **VIO_OV_RST** bit is not set, one overvoltage event on VIO pin will set the **VIO_OV** bit but no reset is generated and FO remains OFF. The SBC doesn't change the SBC mode.

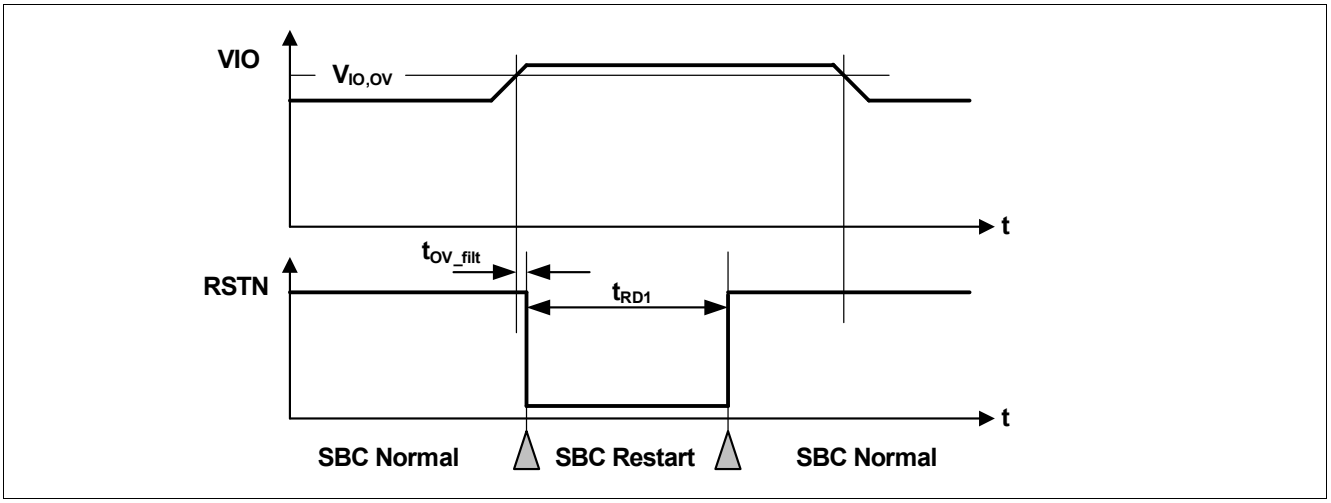


Figure 46 VIO Overvoltage Timing Diagram

12.9 VIO Short Circuit

The following protection feature is implemented for VIO:

- When VIO stays below the undervoltage threshold VRTx for more than $t_{VIO,SC}$, the SBC enters SBC Fail-Safe Mode and turns off VCC1. This feature is available only if $V_S > V_{S,UV}$. In addition the SPI status bit **VIO_SC** is set. The SBC can exited SBC Fail Safe Mode via a wake-up event on CANx and/or WK pin.

12.10 VEXT Undervoltage

Following protection feature is implemented for VEXT:

- If VEXT drops below the $V_{EXT,UV}$ threshold, the SPI bit **VREG_UV** is set and can only be cleared via SPI.

*Note: The **VREG_UV** flag is not set during turn-on or turn-off of VEXT.*

12.11 Thermal Protection

The thermal protection mechanism is designed in such a way that the individual modules (VCC1, CANx, Boost and VEXT) can remain active on as long as possible in case of high temperature. The following thermal protection features are available and signaled via SPI:

- Thermal Prewarning T_{jPW}
- Overtemperature Protection:
  - Overtemperature shut down with 2 levels of priority (**TSD1** for peripherals and **TSD2** for microcontroller supply).
  - The **TSD1** status bit is a combination of CANx, Boost and VEXT thermal shutdown.
  - The **TSD2** status bit is related to VCC1.
  - If the VEXT base driver sensor detected that T_{jTSD1} has been reached, it is switched OFF as an initial protection measure. The control bits (**VEXT_ON** bits on **M_S_CTRL** register) are reset and the bits **VEXT_OT** and **TSD1** are set. The other output stages are not affected if their T_{jTSD1} threshold is not reached. When the overtemperature event is not present anymore, the VEXT must be switched ON by setting the **VEXT_ON** bit.

- If one of the CANx output stages reaches the **T_{jTSD1}** temperature threshold, then the transmitter is switched OFF individually as first-level protection measure. The respective control bits are not reset and the **TSD1** and CAN_x_FAIL bits are set. The CANx drivers are automatically switched on again when the overtemperature condition is no longer present. The user has to reset the **BUS_STAT_0** and **BUS_STAT_2** registers via SPI.
- If VCC1 reaches the **T_{jTSD2}** temperature threshold, the SBC is sent to SBC Fail-Safe Mode. The SBC stays in SBC Fail-Safe Mode for at least **t_{TSD2}** (typ.1s) after the **TSD2** event is not present anymore. The **VCC1_OT** is set.The default wake sources CANx and WK are enabled together with the Fail Safe output.
- Boost Switched OFF in case of **TSD1** along with the **BOOST_OT** bit. The Boost has to activate again setting the **BOOST_EN** after the thermal shutdown event.
- Once the respective bits (**TSD1**, **TSD2**) are set, they can be cleared via SPI if the condition is not present anymore.

12.11.1 Temperature Prewarning

As a next level of thermal protection a temperature prewarning is implemented if the main supply VCC1 reaches the thermal prewarning temperature threshold **T_{jPW}**. Then the status bit **TPW** is set. This bit can only be cleared via SPI once the overtemperature is not present anymore. The thermal prewarning is only active if the VCC1 is in PWM mode.

12.12 Electrical Characteristics

Table 30 Electrical Specification

V_S = 5.5 V to 28 V; T_j = -40°C to +150°C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VIO Monitoring, Reset Generator with VIO = VCC1 = 3.3 V; Pin RSTN							
Undervoltage Prewarning Threshold Voltage	$V_{PW,f}$	3.0	3.1	3.2	V	VIO falling, **VIO_WARN** bit is set	P_12.10.57
Undervoltage Prewarning Threshold Voltage	$V_{PW,r}$	3.10	3.2	3.27	V	VIO rising	P_12.10.58
Reset Threshold Voltage RT1,f	$V_{RT1,f}$	2.95	3.05	3.15	V	Default setting; VIO falling	P_12.10.34
Reset Threshold Voltage RT1,r	$V_{RT1,r}$	3.0	3.1	3.2	V	Default setting; VIO rising	P_12.10.35
Reset Threshold Voltage RT2,f	$V_{RT2,f}$	2.5	2.6	2.7	V	SPI option; VIO falling	P_12.10.36
Reset Threshold Voltage RT2,r	$V_{RT2,r}$	2.55	2.65	2.75	V	SPI option; VIO rising	P_12.10.37
Reset Threshold Voltage RT3,f	$V_{RT3,f}$	2.2	2.3	2.4	V	SPI option; $V_S \geq 4$ V; VIO falling	P_12.10.38
Reset Threshold Voltage RT3,r	$V_{RT3,r}$	2.25	2.35	2.45	V	SPI option; $V_S \geq 4$ V; VIO rising	P_12.10.39
Reset Threshold Voltage RT4,f	V_{RT34f}	2.0	2.1	2.2	V	SPI option; $V_S \geq 4$ V; VIO falling	P_12.10.55
Reset Threshold Voltage RT4,r	$V_{RT4,r}$	2.05	2.15	2.25	V	SPI option; $V_S \geq 4$ V; VIO rising	P_12.10.56
VIO Monitoring, Overvoltage detection							
VIO Overvoltage Detection Threshold	$V_{IO,OV,r}$	3.5	3.63	3.75	V	[1] Rising VIO PCFG = GND	P_12.10.41
VIO Overvoltage Detection Threshold	$V_{IO,OV,f}$	3.45	3.56	3.7	V	[1] Falling VIO PCFG = GND	P_12.10.45
VIO Overvoltage filter time	$t_{VIO,OV}$	12	15	21	µs	[1]	P_12.10.60

Table 30 Electrical Specification (cont'd)

V_S = 5.5 V to 28 V; T_j = -40°C to +150°C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VIO Monitoring, Reference Supply Undervoltage detection							
VS Undervoltage Detection Threshold	$V_{S,UV}$	3.7	4	4.4	V	Supply UV supervision for VIO PCFG = open; includes rising and falling threshold	P_12.10.43
VIO Short to GND Filter Time	$t_{VIO,SC}$	3.2	4	4.8	ms	1)	P_12.10.10
Electrical Characteristics RSTN							
Reset LOW Output Voltage	$V_{RSTN,LOW}$	–	0.2	0.4	V	I_{RSTN} = 1 mA for V_{IO}≥ 1 V	P_12.10.12
Reset HIGH Output Voltage	$V_{RSTN,HIGH}$	0.7 × V_{IO}	–	V_{IO} + 0.3 V	V	I_{RSTN} = -20 µA	P_12.10.13
Reset Pull-up Resistor	R_{RSTN}	10	20	40	kΩ	V_{RSTN} = 0 V	P_12.10.14
Reset Filter Time	t_{RF}	4	10	26	µs	1) V_{IO} < $V_{RT1×}$ to RSTN = L	P_12.10.15
Reset Delay Time	t_{RD1}	1.5	2	2.5	ms	1)2)	P_12.10.16
VEXT Monitoring							
V_{EXT} Undervoltage Detection	$V_{EXT,UV}$	4.5	4.6	4.75	V	5 V option **VEXT_VCFG**=00_B falling	P_12.10.17
V_{EXT} Undervoltage Detection	$V_{EXT,UV}$	2.65	2.85	3.00	V	3.3 V option **VEXT_VCFG**=01_B falling	P_12.10.46
V_{EXT} Undervoltage Detection	$V_{EXT,UV}$	1.45	1.52	1.6	V	1.8 V option **VEXT_VCFG**=10_B falling	P_12.10.61
V_{EXT} Undervoltage Detection	$V_{EXT,UV}$	0.94	1.03	1.1	V	1.2 V option **VEXT_VCFG**=11_B falling	P_12.10.62
V_{EXT} Undervoltage detection hysteresis	$V_{EXT,UV, hys}$	20	100	250	mV	1)	P_12.10.63
Watchdog Generator							
Long Open Window	t_{LW}	160	200	240	ms	1)	P_12.10.18
Internal Oscillator	f_{CLKSBC}	0.8	1.0	1.2	MHz		P_12.10.19
Minimum Waiting Time during SBC Fail-Safe Mode							
Min. waiting time in Fail-Safe	$t_{FS,min}$	80	100	120	ms	1)3)	P_12.10.20
Power-ON Reset, Over-/Undervoltage Protection							
V_s Power ON reset rising	$V_{POR,r}$	4.5	–	5	V	V_s increasing	P_12.10.21

Table 30 Electrical Specification (cont'd)

V_S = 5.5 V to 28 V; T_j = -40°C to +150°C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
V_S Power ON reset falling	$V_{POR,f}$	–	–	3	V	V_S decreasing	P_12.10.22
Battery Voltage Monitoring							
VBSENSE Monitoring Threshold 0	$V_{BSENSE0,f}$	7.5	8.0	8.5	V	VBSENSE decreasing	P_12.10.24
VBSENSE Monitoring Threshold 1	$V_{BSENSE1,f}$	5.7	6.0	6.3	V	VBSENSE decreasing	P_12.10.25
VBSENSE Monitoring Threshold 2	$V_{BSENSE2,f}$	4.2	4.5	4.8	V	VBSENSE decreasing	P_12.10.26
VBSENSE Monitoring Threshold 3	$V_{BSENSE3,f}$	3.2	3.5	3.8	V	VBSENSE decreasing	P_12.10.27
VBSENSE Monitoring Threshold Hysteresis	$V_{BSENSE,hys}$	50	100	200	mV	1)	P_12.10.28
VBSENSE Monitoring Filter Time	$t_{F\_VBSENSE}$	13	16	21	µs	1)	P_12.10.48
VBSENSE Boost deactivation threshold	$Boost_{OFF,th}$	1.5	1.75	2	V	VBSENSE falling	P_12.10.49
VBSENSE Boost activation threshold	$Boost_{ON,th}$	2.5	2.75	3	V	VBSENSE rising	P_12.10.80
Overtemperature Shutdown							
Thermal Prewarning ON Temperature	T_{jPW}	125	145	165	°C	1)	P_12.10.29
Thermal Shutdown TSD1	T_{jTSD1}	165	185	200	°C	1)	P_12.10.30
Thermal Shutdown TSD2	T_{jTSD2}	165	185	200	°C	1)	P_12.10.31
Thermal Shutdown Hysteresis	T_{HYS}	–	20	–	°C	1)	P_12.10.81
Deactivation time after thermal shutdown TSD2	t_{TSD2}	0.8	1	1.2	s	1)	P_12.10.32
Measurement Interface							
Resolution	–		8		Bits	Input voltage full scale = 0V ..39 V	P_12.10.70
Guarantee offset error	–	-1	–	+1	LSB	Input voltage full scale = 0V ..39 V	P_12.10.71
Gain error	–	-1.5	–	1.5	%FSR	Full scale range	P_12.10.72
Differential non-linearity (DNL)	–	-1.5	–	1.5	LSB	Input voltage full scale = 0 V..39 V	P_12.10.73
Integral non-linearity (INL)	–	-1.5	–	1.5	LSB	Input voltage full scale = 0 V..39 V	P_12.10.74

1) Not subject to production test; specified by design.

2) The reset delay time will start when VIO crosses above the selected VRTx threshold.
3) This time applies for all failure entries except a device thermal shutdown (TSD2 has a 1 s waiting time t_{TSD2}).

13 Serial Peripheral Interface

13.1 SPI Protocol Description

The 16-bit wide Control Input Word is read via the data input SDI, which is synchronized with the clock input CLK provided by the microcontroller. The output word appears synchronously at the data output SDO (see **Figure 47**).The transmission cycle begins when the chip is selected by the input CSN (Chip Select Not), LOW active. After the CSN input returns from LOW to HIGH, the word that has been read is interpreted according to the content. The SDO output switches to tristate status (HIGH impedance) at this point, thereby releasing the SDO bus for other use.The state of SDI is shifted into the input register with every falling edge on CLK. The state of SDO is shifted out of the output register after every rising edge on CLK. The SPI of the SBC is not daisy-chain capable.

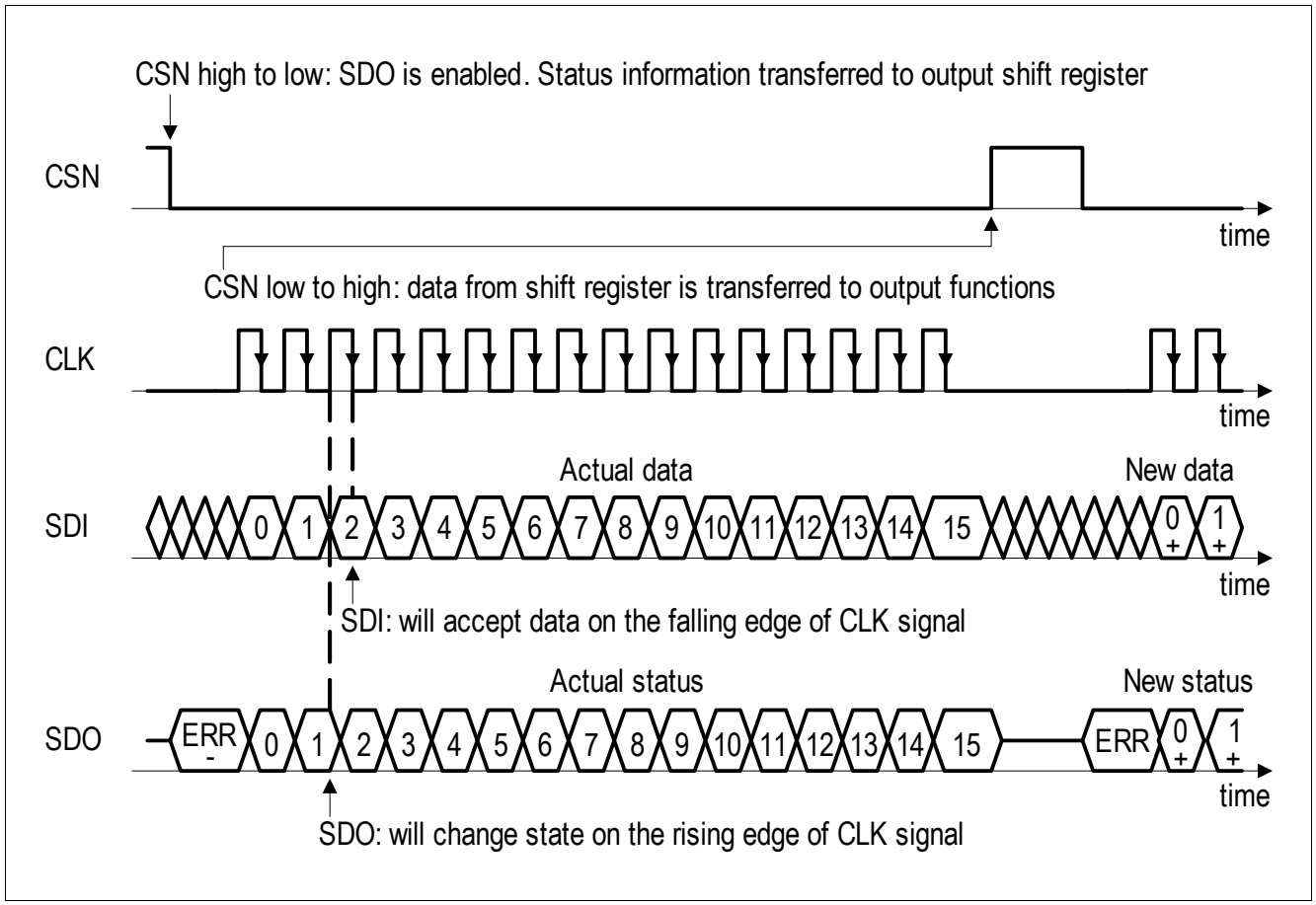


Figure 47 SPI Data Transfer Timing (note the reversed order of LSB and MSB shown in this figure compared to the register description)

13.2 Failure Signalization in the SPI Data Output

When the microcontroller sends a wrong SPI command to the SBC, the SBC ignores the information. Wrong SPI commands are either invalid SBC mode commands or commands which are prohibited by the state machine to avoid undesired device or system states (see below). In this case the diagnosis bit '**SPI_FAIL**' is set and the SPI Write command is ignored (mostly no partial interpretation). This bit can only be reset by actively clearing it via a SPI command.

Invalid SPI Commands leading to SPI_FAIL are listed below:

- Illegal state transitions: going from SBC Stop to SBC Sleep Mode. In this case the SBC additionally enters the SBC Restart Mode.
  Trying to go to SBC Stop or SBC Sleep mode from SBC Init Mode. In this case SBC Normal Mode is entered.
- Uneven parity in the data bit of the **WD_CTRL** register. In this case either the watchdog trigger is ignored or the new watchdog settings are ignored.
- In SBC Stop Mode: attempting to change any SPI settings , e.g. changing the watchdog configuration during SBC Stop Mode.
  the SPI command is ignored in this case.
  The following are allowed in SBC Stop Mode: WD trigger, returning to SBC Normal Mode , triggering a SBC Soft Reset, set to SBC Stop Mode (to return from PWM to PFM following an automatic Buck mode transition) and Read & Clear status register commands are valid SPI commands in SBC Stop Mode.
- When entering SBC Stop Mode and **WK_STAT_0** and **WK_STAT_2** are not cleared; **SPI_FAIL** will not be set but the INTN pin will be triggered.
- When changing from SBC Stop to Normal Mode, any attempt to change the bits on the **M_S_CTRL** register will be ignored (SBC remains in SBC Stop Mode). Only **VIO_OV_RST** and **VIO_RT** set the **SPI_FAIL** bit.
- SBC Sleep Mode: attempt to go to Sleep Mode when all bits in the **BUS_CTRL_0**, **BUS_CTRL_2**, **BUS_CTRL_3** and **WK_CTRL_1** registers are cleared (i.e. no wake sources are activated). In this case the **SPI_FAIL** bit is set and the SBC enters SBC Restart Mode.
  Even though the SBC Sleep Mode command is not entered in this case, the rest of the command (e.g modifying VEXT) is executed and the values stay unchanged during SBC Restart Mode.
  Note: at least one wake source must be activated in order to avoid a deadlock situation in SBC Sleep Mode, i.e. the SBC would not be able to wake up anymore.
  No failure handling occurs for the attempt to go to SBC Stop Mode when all bits in the registers **BUS_CTRL_0**, **BUS_CTRL_2**, **BUS_CTRL_3** and **WK_CTRL_1** are cleared because the microcontroller can leave this mode via SPI.
- After the first VEXT on command, the **VEXT_VCFG** bits can no longer be changed. if the microcontroller tries to modify the **VEXT_VCFG** bits, then the rest of the command is executed but **VEXT_VCFG** will remain unchanged.
- The Boost output voltage can be changed only if **BOOST_EN** is set to 0. If the Boost output voltage is changed with **BOOST_EN**=1, the **SPI_FAIL** bit is set and the SPI command is ignored.
- SDI stuck at HIGH or LOW, e.g. SDI received all '0' or all '1'.

Signalization of the ERR flag in the SPI data output (see Figure 47):

The ERR flag presents an additional diagnosis possibility for the SPI communication. The ERR flag is being set for the following conditions:

- In case the number of received SPI clocks is not 0 or 16.
- In case RSTN is LOW and SPI frames are being sent at the same time.

Note: In order to read the SPI ERR flag property, CLK must be low when CSN is triggered, i.e. the ERR bit is not valid if the CLK is high on a falling edge of CSN.

The number of received SPI clocks is not 0 or 16:

The number of received input clocks is supervised to be 0 or 16 clock cycles and the input word is discarded in case of a mismatch (0 clock cycle to enable ERR signalization). The error logic also recognizes if CLK was high during the CSN edges. Both errors, 0 bit and 16 bit CLK mismatch or CLK high during CSN edges are flagged in the following SPI output by a “HIGH” at the data output (SDO pin, bit ERR) before the first rising edge of the clock is received. The error logic also recognizes if CLK was HIGH during CSN edges. The entire SPI command is ignored in these cases.

RSTN is LOW and SPI frames are being sent at the same time:

The ERR flag will be set when the RSTN pin is triggered (during SBC Restart Mode) and SPI frames are being sent to the SBC at the same time. The behavior of the ERR flag signaled at the next SPI command when the condition below are present:

- If the command begins when RSTN is HIGH and ends when RSTN is LOW.
- If an SPI command is sent while RSTN is LOW.
- If an SPI command begins when RSTN is LOW and ends when RSTN is HIGH.

And the SDO output will behave as follows:

- When RSTN is LOW, SDO is always HIGH.
- When SPI command begins with RSTN is LOW and ends when RSTN is HIGH, then the SDO should be ignored because wrong data will be sent.

Note: It is possible to quickly check for the ERR flag without sending any data bits. i.e. only the CSN is pulled low and SDO is observed - no SPI clocks are sent in this case.

Note: The ERR flag could also be set after the SBC has entered SBC Fail-Safe Mode because SPI communication stops immediately.

13.3 SPI Programming

For TLE9278, 7 bits are used for the address selection (6...0). Bit 7 is used to control the SPI Access, i.e. to decide between Read Only (if set to '0') and Read_Clear (if set to '1') for the status bits, and between Write (if set to '1') and Read Only (if set to '0') for configuration bits. For the actual configuration and status information, 8 data bits (15...8) are used.

Writing, clearing and reading is done byte wise. SPI configuration and status bits are not cleared automatically and must be cleared by the microcontroller, e.g. if the TSD2 was set due to overtemperature. The configuration bits will be partially automatically cleared by the SBC (refer to the description of the individual registers for detailed information). During SBC Restart, Sleep or Fail-Safe mode, the SPI communication is ignored by the SBC, i.e. it is not interpreted.

There are two types of SPI registers:

- Control registers: Those are the registers to configure the SBC, e.g. SBC mode, watchdog trigger, etc.
- Status registers: Those are the registers where the status of the SBC is signalled, e.g. wake-up events, warnings, failures, etc.

For the status registers, the requested information is given in the same SPI command in DO.
For the control registers, also the status of the respective bit is shown in the same SPI command, but if the setting is changed this is only shown with the next SPI command (it is only valid after CSN HIGH) of the same register.

The SBC status information from the SPI status registers, is transmitted in a compressed way with each SPI response on SDO in the so called Status Information Field register (see also **Figure 48**).

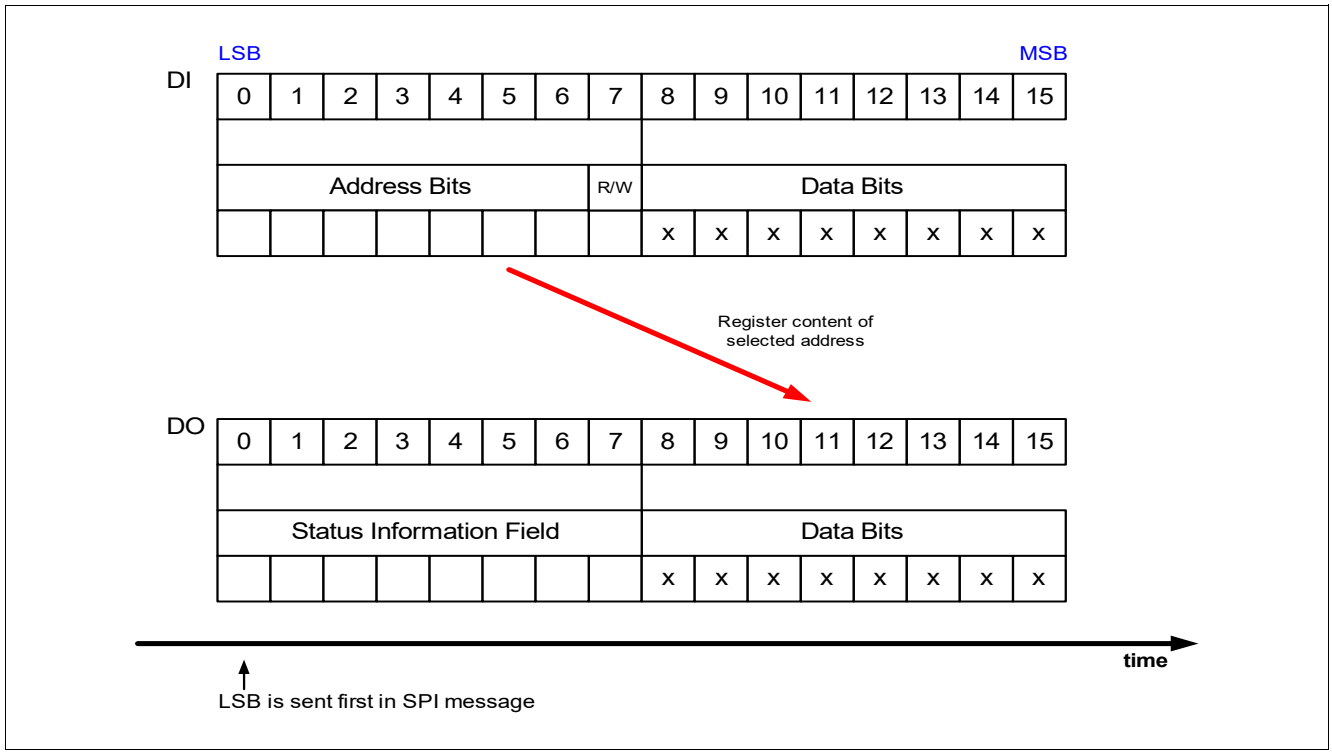


Figure 48 SPI Operation Mode

The purpose of this register is to quickly signal the information to the microcontroller if there was a change in one of the SPI status registers. In this way, the microcontroller does not need to read constantly all the SPI status registers but only those registers, which were changed. Each bit in the Status Information Field

represents a SPI status register or a combinational OR of two status registers (see **Table 31**). As soon as one bit is set in one of the status registers, the respective bit in the Status Information Field register is set. The register **WK_LVL_STAT** is not included in the status information field. This is listed in **Table 31**:

Table 31 Status Information Field

Status Information Bit	Symbol Address Bit	Status Register
0	100 0001	**SUP_STAT_0** & **SUP_STAT_1** (Combinational OR): Supply Status (VCC1 and VEXT), POR
1	100 0010	**THERM_STAT**: Thermal Protection Status
2	100 0011	**DEV_STAT**: Device Status - Mode before Wake, WD Fail, SPI Fail, Failure
3	100 0100	**BUS_STAT_0**: Bus Failure Status: CAN0, VCAN
4	100 0101	**BUS_STAT_2** & **BUS_STAT_3** (Combinational OR): Bus Failure Status: CAN1, CAN2 and CAN3
5	100 0110	**WK_STAT_0**: Wake Source Status for CAN0, WK, Timer and PFM-to-PWM transition
6	100 1001	**WK_STAT_2**: Wake Source Status for CAN1, CAN2, CAN3, and VBAT_UV
7	100 1100	**SMPS_STAT**: SMPS Status

For example if bit 2 in the Status Information Field is set to 1, one or more bits of the register **DEV_STAT** is set to 1. Then this register needs to be read in a second SPI command. The bit in the Status Information Field will be set to 0 when all bits in the register **DEV_STAT** are set back to 0.

13.4 SPI Bit Mapping

13.4.1 SPI Mapping Structure

Figure 49 and **Figure 49** show the mapping of the SPI bits and the respective registers.

Depending on bit 7, the bits are only read or also written. The Control Registers ‘000 0001’ to ‘011 1111’ are READ/WRITE Registers.

The new setting of the bit after write can be seen with the next read / write command. An exception are the registers ‘011 101x’, which are Read Only registers needed for the oscillator re-configuration.

The registers ‘100 0000’ to ‘111 1110’ are Status Registers and can be read or read with clearing the bit (if possible) depending on bit 7. To clear a Data Byte of one of the Status Registers, bit 7 must be set to 1. The register **WK_LVL_STAT** is an exception as it shows the actual voltage level at the respective pin (LOW/HIGH) and thus can not be cleared.

When changing to a different SBC Mode, certain configurations and status bits will be modified by the SBC:

- The SBC Mode bits are updated to the actual status, e.g. when returning to SBC Normal Mode.
- In SBC Sleep Mode the CANx control bits will be modified in CANx wake capable if they were ON before. FO will stay activated if it was triggered before.
- In general, the configurations is only possible in SBC Normal Mode. Diagnosis are also active in SBC Stop Mode (e.g. UV, OT). VEXT can be also active in Low power mode (Stop/Sleep).
- Depending on the respective configuration, CANx transceivers will be either OFF, woken or still wake capable.

13.4.2 SPI Register Banking

The CAN Selective Wake configuration registers consume a lot of address space but do not need to be accessed very often.
Therefore, the CAN Selective Wake configuration for the CAN modules is managed by banking. The respective bank is selected via the **CAN_SWK** bits in **BUS_CTRL_3**. All registers with the attribute “banked”, as shown in **Chapter 13.4.3**, will then be accessible for the selected CAN module.

The Status Registers for the CAN Selective wake are not banked to allow a quick diagnosis.

13.4.3 SPI Mapping Tables

Register Short Name	banked	7	6...0
		Access Control	Address A6...A0
CONTROL REGISTERS			
M_S_CTRL	no	read/write	0000001
HW_CTRL_0	no	read/write	0000010
WD_CTRL	no	read/write	0000011
BUS_CTRL_0	no	read/write	0000100
WK_CTRL_0	no	read/write	0000110
WK_CTRL_1	no	read/write	0000111
WK_PD_CTRL	no	read/write	0001000
BUS_CTRL_2	no	read/write	0001010
BUS_CTRL_3	no	read/write	0001011
TIMER_CTRL	no	read/write	0001100
HW_CTRL_1	no	read/write	0001110
SYS_STAT_CTRL	no	read/write	0011110
SELECTIVE WAKE REGISTERS			
SWK_CTRL	yes	read/write	0100000
SWK_BTL1_CTRL	yes	read/write	0100001
SWK_BTL2_CTRL	yes	read/write	0100010
SWK_ID3_CTRL	yes	read/write	0100011
SWK_ID2_CTRL	yes	read/write	0100100
SWK_ID1_CTRL	yes	read/write	0100101
SWK_ID0_CTRL	yes	read/write	0100110
SWK_MASK_ID3_CTRL	yes	read/write	0100111
SWK_MASK_ID2_CTRL	yes	read/write	0101000
SWK_MASK_ID1_CTRL	yes	read/write	0101001
SWK_MASK_ID0_CTRL	yes	read/write	0101010
SWK_DLC_CTRL	yes	read/write	0101011
SWK_DATA7_CTRL	yes	read/write	0101100
SWK_DATA6_CTRL	yes	read/write	0101101
SWK_DATA5_CTRL	yes	read/write	0101110
SWK_DATA4_CTRL	yes	read/write	0101111
SWK_DATA3_CTRL	yes	read/write	0110000
SWK_DATA2_CTRL	yes	read/write	0110001
SWK_DATA1_CTRL	yes	read/write	0110010
SWK_DATA0_CTRL	yes	read/write	0110011
SWK_CAN_FD_CTRL	yes	read/write	0110100
SWK TRIM &CONFIG. REGISTERS			
SWK_OSC_TRIM_CTRL	no	read/write	0111000
SWK_OPT_CTRL	no	read/write	0111001
SWK_OSC_CAL_H_STAT	no	read	0111010
SWK_OSC_CAL_L_STAT	no	read	0111011
SWK_CDR_CTRL1	yes	read/write	0111100
SWK_CDR_CTRL2	yes	read/write	0111101
SWK_CDR_LIMIT_HIGH_CTRL	yes	read/write	0111110
SWK_CDR_LIMIT_LOW_CTRL	yes	read/write	0111111
STATUS REGISTERS			
SUP_STAT_1	no	read/clear	1000000
SUP_STAT_0	no	read/clear	1000001
THERM_STAT	no	read/clear	1000010
DEV_STAT	no	read/clear	1000011
BUS_STAT_0	no	read/clear	1000100
WK_STAT_0	no	read/clear	1000110
WK_LVL_STAT	no	read	1001000
WK_STAT_2	no	read/clear	1001001
BUS_STAT_2	no	read/clear	1001010
BUS_STAT_3	no	read/clear	1001011
SMPS_STAT	no	read/clear	1001100
ADC_STAT	no	read/clear	1011000
SELECTIVE WAKE STATUS REGISTERS			
SWK_STAT_3	no	read	1100100
SWK_ECNT_STAT_3	no	read	1100101
SWK_CDR_STAT_3_1	no	read	1100110
SWK_CDR_STAT_3_0	no	read	1100111
SWK_STAT_2	no	read	1101000
SWK_ECNT_STAT_2	no	read	1101001
SWK_CDR_STAT_2_1	no	read	1101010
SWK_CDR_STAT_2_0	no	read	1101011
SWK_STAT_1	no	read	1101100
SWK_ECNT_STAT_1	no	read	1101101
SWK_CDR_STAT_1_1	no	read	1101110
SWK_CDR_STAT_1_0	no	read	1101111
SWK_STAT_0	no	read	1110000
SWK_ECNT_STAT_0	no	read	1110001
SWK_CDR_STAT_0_1	no	read	1110010
SWK_CDR_STAT_0_2	no	read	1110011
FAMILY AND PRODUCT REGISTERS			
FAM_PROD_STAT	no	read	1111110

Figure 49 SPI Register Mapping

Register Short Name	15	14	13	12	11	10	9	8	banked	7	6...0
	Data Bit 15...8									Read-Only (1)	Address A6...A0
	D7	D6	D5	D4	D3	D2	D1	D0			
CONTROL REGISTERS											
M_S_CTRL	MODE_1	MODE_0	VEXT_ON	reserved	reserved	VIO_OV_RST	VIO_RT_1	VIO_RT_0	no	read/write	0000001
HW_CTRL_0	reserved	PWM_TLAG	FO_ON	PWM_BY_WK	PWM_AUTO	reserved	BOOST_EN	CFG2	no	read/write	0000010
WD_CTRL	CHECKSUM	WD_STM_EN_0	WD_WIN	WD_EN_WK_BUS	MAX_3_RST	WD_TIMER_2	WD_TIMER_1	WD_TIMER_0	no	read/write	0000011
BUS_CTRL_0	reserved	reserved	reserved	reserved	reserved	CAN0_2	CAN0_1	CAN0_0	no	read/write	0000100
WK_CTRL_0	reserved	TIMER_WK_EN	VBSENSE_CFG_1	VBSENSE_CFG_0	reserved	WD_STM_EN_1	reserved	VBSENSE_EN	no	read/write	0000110
WK_CTRL_1	reserved	reserved	reserved	reserved	reserved	reserved	reserved	WK_EN	no	read/write	0000111
WK_PUPD_CTRL	reserved	reserved	reserved	reserved	reserved	reserved	WK_PUPD_1	WK_PUPD_0	no	read/write	0001000
BUS_CTRL_2	CAN_2_FLASH	CAN_1_FLASH	CAN2_2	CAN2_1	CAN2_0	CAN1_2	CAN1_1	CAN1_0	no	read/write	0001010
BUS_CTRL_3	CAN_SWK_1	CAN_SWK_0	reserved	CAN_0_FLASH	CAN_3_FLASH	CAN3_2	CAN3_1	CAN3_0	no	read/write	0001011
TIMER_CTRL_0	reserved	reserved	reserved	reserved	reserved	TIMER_PER_2	TIMER_PER_1	TIMER_PER_0	no	read/write	0001100
HW_CTRL_1	reserved	SOFT_RESET_RST	BST_VB_UV_OFF	reserved	BOOST_V_1	BOOST_V_0	VEXT_VCFG_1	VEXT_VCFG_0	no	read/write	0001110
SYS_STAT_CTRL	SYS_STAT_7	SYS_STAT_6	SYS_STAT_5	SYS_STAT_4	SYS_STAT_3	SYS_STAT_2	SYS_STAT_1	SYS_STAT_0	no	read/write	0011110
SELECTIVE WAKE REGISTERS											
SWK_CTRL	OSC_CAL	TRIM_EN_1	TRIM_EN_0	CANTO_MASK	reserved	reserved	reserved	CFG_VAL	yes	read/write	0100000
SWK_BTL1_CTRL	TBIT_7	TBIT_6	TBIT_5	TBIT_4	TBIT_3	TBIT_2	TBIT_1	TBIT_0	yes	read/write	0100001
SWK_BTL2_CTRL	reserved	reserved	SP_5	SP_4	SP_3	SP_2	SP_1	SP_0	yes	read/write	0100010
SWK_ID3_CTRL	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21	yes	read/write	0100011
SWK_ID2_CTRL	ID20	ID19	ID18	ID17	ID16	ID15	ID14	ID13	yes	read/write	0100100
SWK_ID1_CTRL	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	yes	read/write	0100101
SWK_ID0_CTRL	reserved	ID4	ID3	ID2	ID1	ID0	RTR	IDE	yes	read/write	0100110
SWK_MASK_ID3_CTRL	MASK_ID28	MASK_ID27	MASK_ID26	MASK_ID25	MASK_ID24	MASK_ID23	MASK_ID22	MASK_ID21	yes	read/write	0100111
SWK_MASK_ID2_CTRL	MASK_ID20	MASK_ID19	MASK_ID18	MASK_ID17	MASK_ID16	MASK_ID15	MASK_ID14	MASK_ID13	yes	read/write	0101000
SWK_MASK_ID1_CTRL	MASK_ID12	MASK_ID11	MASK_ID10	MASK_ID9	MASK_ID8	MASK_ID7	MASK_ID6	MASK_ID5	yes	read/write	0101001
SWK_MASK_ID0_CTRL	reserved	MASK_ID4	MASK_ID3	MASK_ID2	MASK_ID1	MASK_ID0	reserved	reserved	yes	read/write	0101010
SWK_DLC_CTRL	reserved	reserved	reserved	reserved	DLC_3	DLC_2	DLC_1	DLC_0	yes	read/write	0101011
SWK_DATA7_CTRL	DATA7_7	DATA7_6	DATA7_5	DATA7_4	DATA7_3	DATA7_2	DATA7_1	DATA7_0	yes	read/write	0101100
SWK_DATA6_CTRL	DATA6_7	DATA6_6	DATA6_5	DATA6_4	DATA6_3	DATA6_2	DATA6_1	DATA6_0	yes	read/write	0101101
SWK_DATA5_CTRL	DATA5_7	DATA5_6	DATA5_5	DATA5_4	DATA5_3	DATA5_2	DATA5_1	DATA5_0	yes	read/write	0101110
SWK_DATA4_CTRL	DATA4_7	DATA4_6	DATA4_5	DATA4_4	DATA4_3	DATA4_2	DATA4_1	DATA4_0	yes	read/write	0101111
SWK_DATA3_CTRL	DATA3_7	DATA3_6	DATA3_5	DATA3_4	DATA3_3	DATA3_2	DATA3_1	DATA3_0	yes	read/write	0110000
SWK_DATA2_CTRL	DATA2_7	DATA2_6	DATA2_5	DATA2_4	DATA2_3	DATA2_2	DATA2_1	DATA2_0	yes	read/write	0110001
SWK_DATA1_CTRL	DATA1_7	DATA1_6	DATA1_5	DATA1_4	DATA1_3	DATA1_2	DATA1_1	DATA1_0	yes	read/write	0110010
SWK_DATA0_CTRL	DATA0_7	DATA0_6	DATA0_5	DATA0_4	DATA0_3	DATA0_2	DATA0_1	DATA0_0	yes	read/write	0110011
SWK_CAN_FD_CTRL	reserved	reserved	DIS_ERR_CNT	reserved	FD_FILTER_2	FD_FILTER_1	FD_FILTER_0	CAN_FD_EN	yes	read/write	0110100
SELECTIVE WAKE TRIM&CONFIGURATIONS REGISTERS											
SWK_OSC_TRIM_CTRL	TRIM_OSC_7	TRIM_OSC_6	TRIM_OSC_5	TRIM_OSC_4	TRIM_OSC_3	TRIM_OSC_2	TRIM_OSC_1	TRIM_OSC_0	no	read/write	0111000
SWK_OPT_CTRL	RX_WK_SEL	reserved	reserved	TRIM_OSC_12	TRIM_OSC_11	TRIM_OSC_10	TRIM_OSC_9	TRIM_OSC_8	no	read/write	0111001
SWK_OSC_CAL_H_STAT	OSC_CAL_H_7	OSC_CAL_H_6	OSC_CAL_H_5	OSC_CAL_H_4	OSC_CAL_H_3	OSC_CAL_H_2	OSC_CAL_H_1	OSC_CAL_H_0	no	read	0111010
SWK_OSC_CAL_L_STAT	OSC_CAL_L_7	OSC_CAL_L_6	OSC_CAL_L_5	OSC_CAL_L_4	OSC_CAL_L_3	OSC_CAL_L_2	OSC_CAL_L_1	OSC_CAL_L_0	no	read	0111011
SWK_CDR_CTRL1	reserved	reserved	reserved	reserved	SELFILT_1	SELFILT_0	reserved	CDR_EN	yes	read/write	0111100
SWK_CDR_CTRL2	reserved	reserved	reserved	reserved	reserved	reserved	SEL_OSC_CLK_1	SEL_OSC_CLK_0	yes	read/write	0111101
SWK_CDR_LIMIT_HIGH_CTRL	CDR_LIM_H_7	CDR_LIM_H_6	CDR_LIM_H_5	CDR_LIM_H_4	CDR_LIM_H_3	CDR_LIM_H_2	CDR_LIM_H_1	CDR_LIM_H_0	yes	read/write	0111110
SWK_CDR_LIMIT_LOW_CTRL	CDR_LIM_L_7	CDR_LIM_L_6	CDR_LIM_L_5	CDR_LIM_L_4	CDR_LIM_L_3	CDR_LIM_L_2	CDR_LIM_L_1	CDR_LIM_L_0	yes	read/write	0111111
STATUS REGISTERS											
SUP_STAT_1	BVB_UV_BST	VS_UV	reserved	VEXT_OC	VREG_UV	VEXT_OT	VIO_OV	VIO_WARN	no	read/clear	1000000
SUP_STAT_0	POR	reserved	reserved	reserved	reserved	VIO_SC	VIO_UV_FS	VIO_UV	no	read/clear	1000001
THERM_STAT	reserved	VCC1_OT	BOOST_OT	reserved	reserved	TSD2	TSD1	TPW	no	read/clear	1000010
DEV_STAT	DEV_STAT_1	DEV_STAT_0	reserved	reserved	WD_FAIL_1	WD_FAIL_0	SPI_FAIL	FO_ON_STATE	no	read/clear	1000011
BUS_STAT_0	reserved	reserved	reserved	CANTO_0	SYSERR_0	CAN_0_FAIL_1	CAN_0_FAIL_0	VCAN_UV	no	read/clear	1000100
WK_STAT_0	PFM_PWM	reserved	CAN_0_WU	TIMER_WU	reserved	reserved	reserved	WK_WU	no	read/clear	1000110
WK_LVL_STAT	TEST	CFG1_STATE	CFG2_STATE	PCFG_STATE	VBAT_UV_STATE	reserved	reserved	WK	no	read	1001000
WK_STAT_2	VBAT_UV_LATCH	reserved	reserved	reserved	reserved	CAN_3_WU	CAN_2_WU	CAN_1_WU	no	read/clear	1001001
BUS_STAT_2	CANTO_2	SYSERR_2	CAN_2_FAIL_1	CAN_2_FAIL_0	CANTO_1	SYSERR_1	CAN_1_FAIL_1	CAN_1_FAIL_0	no	read/clear	1001010
BUS_STAT_3	reserved	reserved	reserved	reserved	CANTO_3	SYSERR_3	CAN_3_FAIL_1	CAN_3_FAIL_0	no	read/clear	1001011
SMPS_STAT	BST_ACT	BST_SH	BST_OP	reserved	reserved	BCK_SH	BCK_OP	reserved	no	read/clear	1001100
SELECTIVE WAKE STATUS REGISTERS											
SWK_STAT_3	reserved	SYNC_3	reserved	reserved	CANSIL_3	SWK_SET_3	WUP_3	WUF_3	no	read	1100100
SWK_ECNT_STAT_3	reserved	reserved	ECNT_3_5	ECNT_3_4	ECNT_3_3	ECNT_3_2	ECNT_3_1	ECNT_3_0	no	read	1100101
SWK_CDR_STAT_3_1	N_AVG_3_11	N_AVG_3_10	N_AVG_3_9	N_AVG_3_8	N_AVG_3_7	N_AVG_3_6	N_AVG_3_5	N_AVG_3_4	no	read	1100110
SWK_CDR_STAT_3_0	N_AVG_3_3	N_AVG_3_2	N_AVG_3_1	N_AVG_3_0	reserved	reserved	reserved	reserved	no	read	1100111
SWK_STAT_2	reserved	SYNC_2	reserved	reserved	CANSIL_2	SWK_SET_2	WUP_2	WUF_2	no	read	1101000
SWK_ECNT_STAT_2	reserved	reserved	ECNT_2_5	ECNT_2_4	ECNT_2_3	ECNT_2_2	ECNT_2_1	ECNT_2_0	no	read	1101001
SWK_CDR_STAT_2_1	N_AVG_2_11	N_AVG_2_10	N_AVG_2_9	N_AVG_2_8	N_AVG_2_7	N_AVG_2_6	N_AVG_2_5	N_AVG_2_4	no	read	1101010
SWK_CDR_STAT_2_0	N_AVG_2_3	N_AVG_2_2	N_AVG_2_1	N_AVG_2_0	reserved	reserved	reserved	reserved	no	read	1101011
SWK_STAT_1	reserved	SYNC_1	reserved	reserved	CANSIL_1	SWK_SET_1	WUP_1	WUF_1	no	read	1101100
SWK_ECNT_STAT_1	reserved	reserved	ECNT_1_5	ECNT_1_4	ECNT_1_3	ECNT_1_2	ECNT_1_1	ECNT_1_0	no	read	1101101
SWK_CDR_STAT_1_1	N_AVG_1_11	N_AVG_1_10	N_AVG_1_9	N_AVG_1_8	N_AVG_1_7	N_AVG_1_6	N_AVG_1_5	N_AVG_1_4	no	read	1101110
SWK_CDR_STAT_1_0	N_AVG_1_3	N_AVG_1_2	N_AVG_1__1	N_AVG_1_0	reserved	reserved	reserved	reserved	no	read	1101111
SWK_STAT_0	reserved	SYNC_0	reserved	reserved	CANSIL_0	SWK_SET_0	WUP_0	WUF_0	no	read	1110000
SWK_ECNT_STAT_0	reserved	reserved	ECNT_0_5	ECNT_0_4	ECNT_0_3	ECNT_0_2	ECNT_0_1	ECNT_0__0	no	read	1110001
SWK_CDR_STAT_0_1	N_AVG_0_11	N_AVG_0_1_0	N_AVG_0_9	N_AVG_0_8	N_AVG_0_7	N_AVG_0_6	N_AVG_0_5	N_AVG_0_4	no	read	1110010
SWK_CDR_STAT_0_0	N_AVG_0_3	N_AVG_0_2	N_AVG_0_1	N_AVG_0_0	reserved	reserved	reserved	reserved	no	read	1110011
FAMILY AND PRODUCT REGISTERS											
FAM_PROD_STAT	FAM_3	FAM_2	FAM_1	FAM_0	PROD_3	PROD_2	PROD_1	PROD_0	no	read	1111110

Figure 50 Detailed SPI Bit Mapping

*Note: The CAN Selective Wake configuration for the 4 CAN modules is managed by banking. The relevant bank is selected via CAN_SWK[1:0] in **BUS_CTRL_3**.*

13.5 SPI Control Registers

Read / Write Operation (see **Chapter 13.3**):

- The ‘POR / Soft Reset Value’ defines the register content after POR or SBC Software Reset.
- The ‘Restart Value’ defines the register content after SBC Restart; ‘x’ means the bit is unchanged.
- ‘y’ in ‘Restart Value’ means the bit can be changed by SBC.
- One 16-bit SPI command consist of two bytes:
  - the 7-bit address and one additional bit for the register access mode and
  - following the data byte
  The numbering of following bit definitions refers to the data byte and correspond to the bits D0...D7 and to the SPI bits 8...15.
- There are three different bit types:
  - ‘**r**’ = READ; read only bits (or reserved bits).
  - ‘**rw**’ = READ/WRITE; readable and writable bits.
  - ‘**rwh**’ = READ/WRITE/HARDWARE; as **rw** with the possibility that the hardware can change the bits.
- Reading a register is done byte wise by setting the SPI bit 7 to “0” (= Read Only).
- Writing to a register is done byte wise by setting the SPI bit 7 to “1”.
- SPI control bits are not cleared or changed automatically. This must be done by the microcontroller via SPI programming.

The registers are addressed wordwise.

13.5.1 General Control Registers

Mode- and Supply Control

M_S_CTRL
Mode- and Supply Control (Address 000 0001$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 00x0 00xx$_B$

7	6	5	4	3	2	1	0
MODE		VEXT_ON	Reserved		VIO_OV_RST	VIO_RT	
rwh		rw	r		rwh	rw	

Field	Bits	Type	Description
MODE	7:6	rwh	**SBC Mode Control** 00_B SBC Normal Mode 01_B SBC Sleep Mode 10_B SBC Stop Mode 11_B SBC Reset: Soft Reset is executed (configuration of RSTN triggering in bit **SOFT_RESET_ RSTN**)
VEXT_ON	5	rw	**VEXT Mode Control** 0_B VEXT OFF 1_B VEXT is enabled
Reserved	4:3	r	**Reserved, always reads as 0**
VIO_OV_RST	2	rwh	**VIO Overvoltage Reset / Fail-Safe enable** 0_B **VIO_OV** is set in case of VIO_OV; no SBC Restart or Fail-Safe is entered for VIO_OV 1_B **VIO_OV** is set in case of VIO_OV; depending on the device configuration SBC Restart or SBC Fail-Safe Mode is entered (see **Chapter 5.1.1**);
VIO_RT	1:0	rw	**VIO Reset Threshold Control** 00_B Vrt1 selected (highest threshold) 01_B Vrt2 selected 10_B Vrt3 selected 11_B Vrt4 selected

Notes

1. *It is not possible to change from SBC Stop to Sleep Mode via an SPI Command. See also the State Machine Chapter.*
2. *After entering SBC Restart Mode, the MODE bits will be automatically set to SBC Normal Mode.*
3. *The SPI output will always show the previously written state with a Write Command (what has been programmed before).*

Hardware Control 0

HW_CTRL_0
Hardware Control 0 (Address 000 0010$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0x0x xxxx$_B$

7	6	5	4	3	2	1	0
Reserved	**PWM_TLAG**	**FO_ON**	**PWM_BY_WK**	**PWM_AUTO**	**Reserved**	**BOOST_EN**	**CFG2**
r	rw	rwh	rwh	rw	r	rwh	rw

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
PWM_TLAG	6	rw	**PWM Lag time** This bit permits to set the time between the PWM to PFM transition. 0_B 100µs 1_B 1ms
FO_ON	5	rwh	**Failure Output activation** This bit is used to activate the Fail Output by software. 0_B FO not activated by software, FO can be activated by defined failure 1_B FO activated by software.
PWM_BY_WK	4	rwh	**PWM of Buck converter enabled by WK pin** 0_B Buck converter uses PFM in SBC Stop Mode 1_B Buck converter can be switched between PFM and PWM by the WK pin in SBC Stop Mode.
PWM_AUTO	3	rw	**Automatic transition PFM-PWM in SBC Stop Mode** This bit is used to activate the automatic transition PFM to PWM. 0_B Buck converter always uses PFM in SBC Stop Mode (default) 1_B Buck converter uses automatic transition PFM to PWM in case large current needed in SBC Stop Mode. To come back in PFM, write a SBC Stop Mode command to **M_S_CTRL**.
Reserved	2	r	**Reserved, always reads as 0**
BOOST_EN	1	rwh	**Boost converter enable** 0_B Boost Off 1_B Boost enabled, automatic switch ON for LOW V_S Voltage
CFG2	0	rw	**Configuration Select 2** 0_B Fail Output (FO) enabled after 2nd watchdog trigger fail Config 3/4 1_B Fail Output (FO) enabled after 1st watchdog trigger fail Config 1/2

Notes

1. *The FO_ON bit is cleared by the SBC after SBC Restart Mode. Clearing the bit via SPI or via SBC Restart Mode will not disable the FO output, if the failure condition is still present. See also **Chapter 11** for FO activation and deactivation. Setting the FO output via an SPI should be used for testing purposes only.*
2. *The selection between Config 1/3 respectively Config 2/4 is done by the pin INTN. The INTN pin defines if the SBC enters to SBC Fail-Safe Mode with VCC1 OFF in case of a watchdog failure.*

Watchdog Control

WD_CTRL
Watchdog Control (Address 000 0011$_B$)
POR / Soft Reset Value: 0001 0100$_B$; Restart Value: x0xx x100$_B$

7	6	5	4	3	2	1	0
CHECKSUM	WD_STM_EN_0	WD_WIN	WD_EN_WK_BUS	MAX_3_RST	WD_TIMER		
rw	rwh	rw	rw	rw	rwh		

Field	Bits	Type	Description
CHECKSUM	7	rw	**Watchdog Setting Checksum Bit** The sum of bits 7:0 needs to have even parity 0_B Counts as 0 for checksum calculation 1_B Counts as 1 for checksum calculation
WD_STM_EN_0	6	rwh	**Watchdog Deactivation during SBC Stop Mode, bit 0 (Chapter 12.2.4)** 0_B Watchdog is active in Stop Mode 1_B Watchdog is deactivated in Stop Mode
WD_WIN	5	rw	**Watchdog Type Selection** 0_B Watchdog works as a Time-Out watchdog 1_B Watchdog works as a Window watchdog
WD_EN_WK_BUS	4	rw	**Watchdog Enable after Bus (CANx) Wake in SBC Stop Mode** 0_B Watchdog will not start after a CANx wake 1_B Watchdog starts with a long open window after CANx Wake
MAX_3_RST	3	rw	**Limit number of resets due to a Watchdog failure** 0_B Always generate a reset in case of WD fail 1_B After 3 consecutive resets due to WD fail, no further reset is generated (only valid in config 1/3)
WD_TIMER	2:0	rwh	**Watchdog Timer Period** 000_B 10ms 001_B 20ms 010_B 50ms 011_B 100ms 100_B 200ms 101_B 500ms 110_B 1000ms 111_B reserved

Notes

1. *See **Chapter 12.2.3** for calculating the checksum.*
2. *See also **Chapter 12.2.4** for more information on disabling the watchdog in SBC Stop Mode.*
3. *See **Chapter 12.2.4** for more information on the effect of the bit WD_EN_WK_BUS.*

Bus Control 0

BUS_CTRL_0
Bus Control 0 (Address 000 0100_B)
POR / Soft Reset Value: 0000 0000_B; Restart Value: 0000 $0xyy_B$

7	6	5	4	3	2	1	0
Reserved					CAN0		
r					rwh		

Field	Bits	Type	Description
Reserved	7:3	r	**Reserved, always reads as 0**
CAN0	2:0	rwh	**HS-CAN_0 Module Modes** 000_B CAN OFF 001_B CAN is wake capable (no SWK) 010_B CAN Receive Only Mode (no SWK) 011_B CAN Normal Mode (no SWK) 100_B CAN OFF 101_B CAN is wake capable with SWK 110_B CAN Receive Only Mode with SWK 111_B CAN Normal Mode with SWK

Notes

1. *See **Figure 23** for detailed state changes of the CAN Transceiver for different SBC modes.*
2. *The bit CAN0_2 is not modified by the SBC but can only be changed by the user. Therefore, the access type is 'rw' compared to bits CAN0_0 and CAN0_1.*
3. *In case SYSERR_0 = 0 and the CAN transceiver is configured to 'x11' while going to SBC Sleep Mode, it will be automatically set to wake capable ('x01'). The SPI bits will be changed to wake capable. If configured to 'x10' and SBC Sleep Mode is entered, then the transceiver is set to wake capable, while it will stay in Receive Only Mode when it had been configured to 'x10' when going to SBC Stop Mode. If it had been configured to wake capable or OFF then the mode will remain unchanged.The Receive Only Mode has to be selected by the user before entering SBC Stop Mode. Refer to **Chapter 5.3.4** for detailed information on the Selective Wake mode changes.*
4. *Failure Handling Mechanism: When the SBC enters SBC Fail-Safe Mode due to a failure (e.g. TSD2, WD-Failure), then the bus and wake registers are modified by the SBC in order to ensure that the device can be woken again. Refer to the respective register descriptions.*

Internal Wake Input Control 0

WK_CTRL_0
Internal Wake Input Control 0 (Address 000 0110$_B$)
POR / Soft Reset Value: 0000 0001$_B$; Restart Value: 0xxx 000x$_B$

7	6	5	4	3	2	1	0
Reserved	**TIMER1_WK_EN**	**VBSENSE_CFG**		**Reserved**	**WD_STM_EN_1**	**Reserved**	**VBSENSE_EN**
r	rw	rw		r	rwh	r	rw

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
TIMER1_WK_EN	6	rw	**Wake Source Control (for cyclic wake)** 0_B Cyclic wake disabled 1_B Cyclic wake enabled as a wake source
VBSENSE_CFG	5:4	rw	**Battery Voltage Monitoring Threshold Selection** 00_B VBSENSE0 threshold selected (highest threshold) 01_B VBSENSE1 threshold selected 10_B VBSENSE2 threshold selected 11_B VBSENSE3 threshold selected
Reserved	3	r	**Reserved, always reads as 0**
WD_STM_EN_1	2	rwh	**Watchdog Deactivation during Stop Mode, bit 1 (Chapter 12.2.4)** 0_B Watchdog is active in Stop Mode 1_B Watchdog is deactivated in Stop Mode
Reserved	1	r	**Reserved, always reads as 0**
VBSENSE_EN	0	rw	**Enable the fast battery voltage monitoring** 0_B Fast Vbatt Monitoring disabled 1_B Fast Vbatt Monitoring enabled

*Note: See also **Chapter 12.2.4** for more information on disabling the watchdog in SBC Stop Mode.*

External Wake Source Control 1

WK_CTRL_1
External Wake Source Control 1 (Address 000 0111_B)
POR / Soft Reset Value: 0000 0001_B; Restart Value: 0000 $000x_B$

7	6	5	4	3	2	1	0
Reserved							**WK_EN**
r							rwh

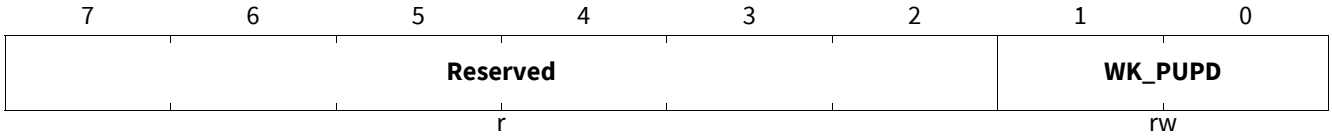
Field	Bits	Type	Description
Reserved	7:1	r	**Reserved, always reads as 0**
WK_EN	0	rwh	**WK Wake Source Control** 0_B WK wake disabled 1_B WK is enabled as a wake source

Notes

1. *Failure Handling Mechanism: When the device enters SBC Fail-Safe Mode due to a failure (e.g. TSD2, WD-Failure), the **WK_CTRL_1** is modified to the value '0000 0001' in order to ensure that the device can be woken again.*

Wake Input Level Control

WK_PUPD_CTRL
Wake Input Level Control (Address 000 1000_B)
POR / Soft Reset Value: 0000 0000_B; Restart Value: 0000 $00xx_B$



Field	Bits	Type	Description
Reserved	7:2	r	**Reserved, always reads as 0**
WK_PUPD	1:0	rw	**WK Pull-Up / Pull-Down Configuration** 00_B No pull-up / pull-down selected 01_B Pull-down resistor selected 10_B Pull-up resistor selected 11_B Automatic switching to pull-up or pull-down

Bus Control 2

BUS_CTRL_2
Bus Control 2 (Address 000 1010$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxy yxyy$_B$

7	6	5	4	3	2	1	0
CAN_2_Flash	CAN_1_Flash	CAN2			CAN1		
rw	rw	rwh			rwh		

Field	Bits	Type	Description
CAN_2_Flash	7	rw	**CAN2 Flash Mode activation** 0_B Flash Mode disabled: CAN communication up to 5MBaud 1_B Flash Mode enabled: CAN communication for higher than 5MBaud (higher emission on CAN bus - no slew rate control)
CAN_1_Flash	6	rw	**CAN1 Flash Mode activation** 0_B Flash Mode disabled: CAN communication up to 5MBaud 1_B Flash Mode enabled: CAN communication for higher than 5MBaud (higher emission on CAN bus - no slew rate control)
CAN2	5:3	rwh	**HS-CAN_2 Module Modes** 000_B CAN OFF 001_B CAN is wake capable (no SWK) 010_B CAN Receive Only Mode (no SWK) 011_B CAN Normal Mode (no SWK) 100_B CAN OFF 101_B CAN is wake capable with SWK 110_B CAN Receive Only Mode with SWK 111_B CAN Normal Mode with SWK
CAN1	2:0	rwh	**HS-CAN_1 Module Modes** 000_B CAN OFF 001_B CAN is wake capable (no SWK) 010_B CAN Receive Only Mode (no SWK) 011_B CAN Normal Mode (no SWK) 100_B CAN OFF 101_B CAN is wake capable with SWK 110_B CAN Receive Only Mode with SWK 111_B CAN Normal Mode with SWK

Notes

1. *See **Figure 23** for detailed state changes of the CAN Transceiver for different SBC modes.*
2. *The bit CANx_2 is not modified by the SBC but can only be changed by the user. Therefore, the access type is 'rw' compared to bits CANx_0 and CANx_1.*
3. *In case SYSERR_x = 0 and the CAN transceiver is configured to 'x11' while going to SBC Sleep Mode, it will be automatically set to wake capable ('x01'). The SPI bits will be changed to wake capable. If configured to 'x10' and SBC Sleep Mode is entered, then the transceiver is set to wake capable, while it will stay in Receive Only Mode when it had been configured to 'x10' when going to SBC Stop Mode. If it had been configured to wake capable or OFF then the mode will remain unchanged.The Receive Only Mode has to be selected by the user*

*before entering SBC Stop Mode. Refer to **Chapter 5.3.4** for detailed information on the Selective Wake mode changes.*

4. *Failure Handling Mechanism: When the device enters SBC Fail-Safe Mode due to a failure (e.g. TSD2, WD-Failure), then the bus and wake registers are modified by the SBC in order to ensure that the device can be woken again. Refer to the respective register descriptions.*

Timer_0 Control and Selection

TIMER_CTRL_0
Timer_0 Control and Selection (Address 000 1100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 0000$_B$

7	6	5	4	3	2	1	0
Reserved					**TIMER_0_PER**		
r					rwh		

Field	Bits	Type	Description
Reserved	7:3	r	**Reserved, always reads as 0**
TIMER_0_PER	2:0	rwh	**Cyclic Wake Period Configuration** 000_B 10ms 001_B 20ms 010_B 50ms 011_B 100ms 100_B 200ms 101_B 1s 110_B 2s 111_B reserved

Serial Peripheral Interface

Hardware Control 1

HW_CTRL_1
Hardware Control 1 (Address 000 1110_B)
POR / Soft Reset Value: 0000 $00yy_B$; Restart Value: 0x0x $xxxx_B$

7	6	5	4	3	2	1	0
ADC_SEL	SOFT_RESET_RSTN	BST_VB_UV_OFF	Reserved	BOOST_V		VEXT_VCFG	
rw	rw	rw	r	rw		rwh	

Field	Bits	Type	Description
ADC_SEL	7	rw	**8 bit ADC input channel selector** 0_B WK pin is selected 1_B VBSENSE pin is selected
SOFT_RESET_RSTN	6	rw	**Soft Reset Configuration** 0_B RSTN will be triggered (pulled low) during a Soft Reset (default) 1_B No RSTN triggering during a Soft Reset
BST_VB_UV_OFF	5	rw	**Boost switch-off control on VBSENSE low voltage condition** 0_B Boost automatic switch-off disable 1_B Boost automatic switch-off enable
Reserved	4	r	**Reserved, always reads as 0**
BOOST_V	3:2	rw	**BOOST Output voltage configuration** 00_B 6.7V output (default) 01_B 8V output 10_B 10V output 11_B 12V output
VEXT_VCFG	1:0	rwh	**VEXT Output voltage configuration** 00_B 5.0V output 01_B 3.3V output (default) 10_B 1.8V output 11_B 1.2V output

Notes

1. *After triggering a SBC Software Reset the bits **VEXT_VCFG** remain unchanged, as shown by the 'y' in the POR/Soft Reset Value.*
2. *The **VEXT_VCFG** can not be accessed if the PCFG pin is connected to GND. Always read '01'.*

Bus Control 3

BUS_CTRL_3
Bus Control 3 (Address 000 1011$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xx0x xxyy$_B$

7	6	5	4	3	2	1	0
CAN_SWK		Reserved	CAN_0_Flash	CAN_3_Flash	CAN3		
rw		r	rw	rw	rwh		

Field	Bits	Type	Description
CAN_SWK	7:6	rw	**Banking Control for CAN Selective Wake Configurations** 00_B CAN0 Module 01_B CAN1 Module 10_B CAN2 Module 11_B CAN3 Module
Reserved	5	r	**Reserved, always reads as 0**
CAN_0_Flash	4	rw	**CAN0 Flash Mode activation** 0_B Flash Mode disabled: CAN communication up to 5MBaud 1_B Flash Mode enabled: CAN communication for higher than 5MBaud (higher emission on CAN bus - no slew rate control)
CAN_3_Flash	3	rw	**CAN3 Flash Mode activation** 0_B Flash Mode disabled: CAN communication up to 5MBaud 1_B Flash Mode enabled: CAN communication for higher than 5MBaud (higher emission on CAN bus - no slew rate control)
CAN3	2:0	rwh	**HS-CAN_3 Module Modes** 000_B CAN OFF 001_B CAN is wake capable (no SWK) 010_B CAN Receive Only Mode (no SWK) 011_B CAN Normal Mode (no SWK) 100_B CAN OFF 101_B CAN is wake capable with SWK 110_B CAN Receive Only Mode with SWK 111_B CAN Normal Mode with SWK

Notes

1. *SPI Register Banking for CAN Selective Wake configuration is managed with the bits CAN_SWK[1:0]. See also **Chapter 13.4.2**.*
2. *See **Figure 23** for detailed state changes of CAN Transceiver for different SBC modes.*
3. *The bit CAN3_2 is not modified by the SBC but can only be changed by the user. Therefore, the access type is 'rw' compared to bits CAN3_0 and CAN3_1.*
4. *In case SYSERR_3 = 0 and the CAN transceiver is configured to 'x11' while going to SBC Sleep Mode, it will be automatically set to wake capable ('x01'). The SPI bits will be changed to wake capable. If configured to 'x10' and SBC Sleep Mode is entered, then the transceiver is set to wake capable, while it will stay in Receive Only Mode when it had been configured to 'x10' when going to SBC Stop Mode. If it had been configured to wake capable or OFF then the mode will remain unchanged.The Receive Only Mode has to be selected by the user*

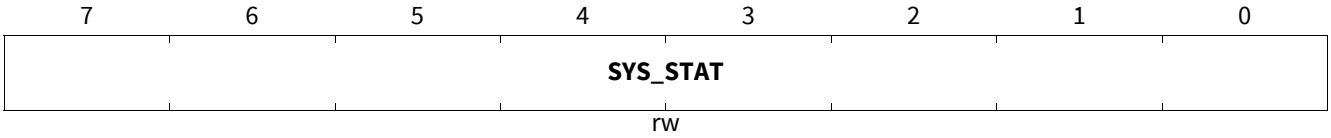
*before entering SBC Stop Mode. Refer to **Chapter 5.3.4** for detailed information on the Selective Wake mode changes.*

5. *Failure Handling Mechanism: When the device enters Fail-Safe Mode due to a failure (e.g. TSD2, WD-Failure), then the bus and wake registers are modified by the SBC in order to ensure that the device can be woken again. Refer to the respective register descriptions.*

Serial Peripheral Interface

System Status Control

SYS_STATUS_CTRL
System Status Control (Address 001 1110_B)
POR Value: 0000 0000_B; Restart Value/Soft Reset Value: xxxx $xxxx_B$



Field	Bits	Type	Description
SYS_STAT	7:0	rw	**System Status Control Byte (bit0=LSB; bit7=MSB)** Dedicated byte for system configuration, access only by microcontroller

Notes

1. *The **SYS_STATUS_CTRL** register is an exception for the default values, i.e. it will keep its configured value even after a Software Reset.*
2. *This byte is intended for storing system configurations of the ECU by the microcontroller and is only accessible in SBC Normal Mode. The byte is not accessible by the SBC and is also not cleared after SBC Fail-Safe or Restart Mode. It allows the microcontroller to quickly store the system configuration without losing the data.*

13.5.2 Selective Wake Control Registers

CAN Selective Wake Control

SWK_CTRL
CAN Selective Wake Control (Address 010 0000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxx0$_B$

7	6	5	4	3	2	1	0
OSC_CAL	**TRIM_EN**		**CANTO_MASK**	**Reserved**			**CFG_VAL**
rw	rw		rw	r			rwh

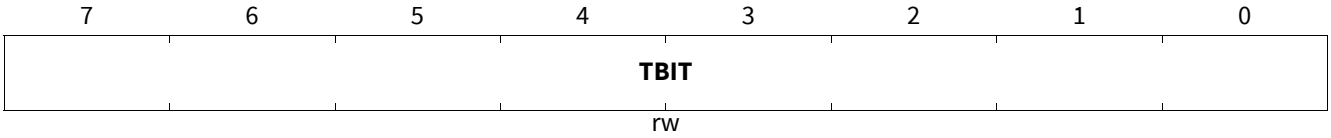
Field	Bits	Type	Description
OSC_CAL	7	rw	**Oscillator Calibration Mode** 0_B Oscillator Calibration is disabled 1_B Oscillator Calibration is enabled
TRIM_EN	6:5	rw	**(Un)locking mechanism of oscillator recalibration** 00_B locked 01_B locked 10_B locked 11_B unlocked
CANTO_MASK	4	rw	**CAN Time Out Masking** 0_B CAN time-out is masked - no interrupt (on pin INTN) is triggered 1_B CAN time-out is signaled on INTN
Reserved	3:1	r	**Reserved, always reads as 0**
CFG_VAL	0	rwh	**SWK Configuration valid** 0_B Configuration is not valid (SWK not possible) 1_B SWK configuration valid, written by up to enable SWK

Notes

1. *TRIM_EN unlocks the oscillation calibration mode. Only the bit combination '11' is the valid unlock. The pin TXDCANx is used for oscillator synchronisation (trimming).*
2. *The microcontroller needs to validate the SWK configuration and set CFG_VAL to '1'. The SBC will only enable SWK if CFG_VAL is set to '1'. The bit will be cleared automatically by the SBC after a wake up or POR or if a SWK configuration data is changed by the microcontroller.*
3. *CANTO_x bit will only be updated inside BUS_STAT_x while CANx_2 is set. Therefore, an interrupt is only signaled upon occurrence of CANTO_x while CANx_2 (SWK is enabled) is set in SBC Normal and Stop Mode.*
4. *TRIM_EN also unlocks the writing to the SWK_OPT_CTRL register in order to enable the alternate low-power Receiver. Only the bit combination '11' unlocks the calibrations / configurations.*
5. *In case, the microcontroller writes a command to a CAN configuration register during SBC stop-mode, the SWK configuration gets invalid.*

SWK Bit Timing Logic Control 1

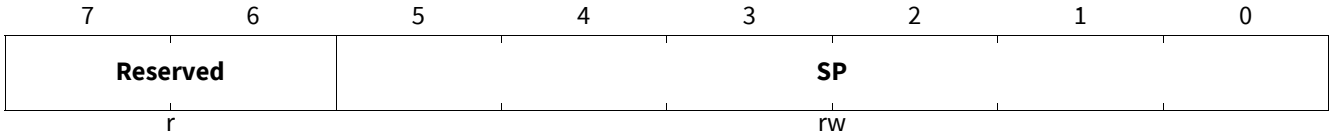
SWK_BTL1_CTRL
SWK Bit Timing Logic Control 1 (Address 010 0001$_B$)
POR / Soft Reset Value: 1010 0000$_B$; Restart Value: xxxx xxxx$_B$



Field	Bits	Type	Description
TBIT	7:0	rw	**Number of Time Quanta in a Bit Time** Represents the number of time quanta in a bit time. Quanta is depending on **SEL_OSC_CLK**<1:0> from the **SWK_CDR_CTRL2** register.

SWK Bit Timing Control 2

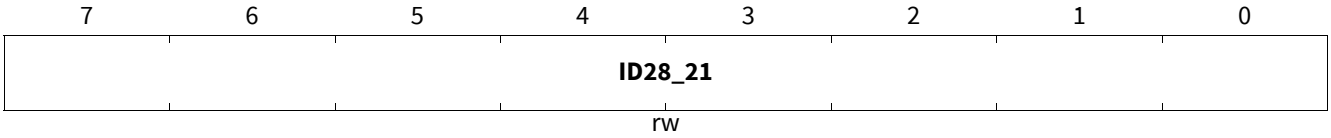
SWK_BTL2_CTRL
SWK Bit Timing Control 2 (Address 010 0010$_B$)
POR / Soft Reset Value: 0011 0011$_B$; Restart Value: xxxx xxxx$_B$



Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
SP	5:0	rw	**Sampling Point Position** $_B$ Represents the sampling point position (fractional number < 1). Example: 0011 0011 = 0.796875 (~80%)

SWK WUF Identifier bits 28...21

SWK_ID3_CTRL
SWK WUF Identifier bits 28...21 (Address 010 0011$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

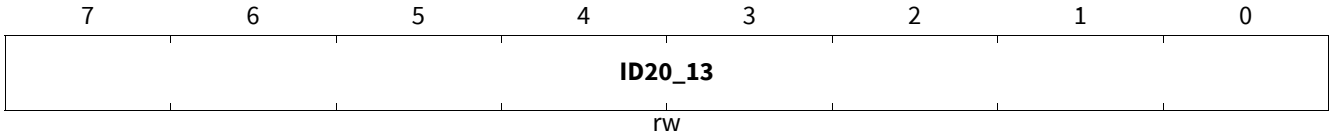


Field	Bits	Type	Description
ID28_21	7:0	rw	**WUF Identifier Bits 28...21**

Note: Please note the configuration of the standard identifier and extended identifier. The standard identifier is configured with the bits ID18...ID28.

SWK WUF Identifier bits 20...13

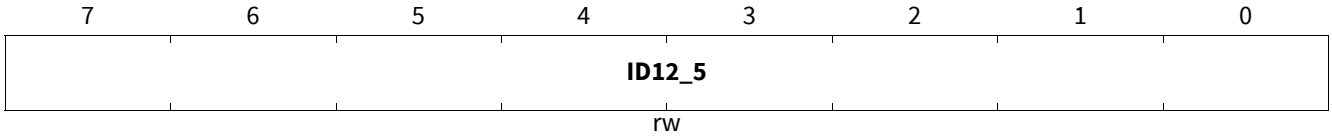
SWK_ID2_CTRL
SWK WUF Identifier bits 20...13 (Address 010 0100_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$



Field	Bits	Type	Description
ID20_13	7:0	rw	**WUF Identifier Bits 20...13**

SWK WUF Identifier bits 12...5

SWK_ID1_CTRL
SWK WUF Identifier bits 12...5 (Address 010 0101_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$



Field	Bits	Type	Description
ID12_5	7:0	rw	**WUF Identifier Bits 12...5**

SWK WUF Identifier bits 4...0

SWK_ID0_CTRL
SWK WUF Identifier bits 4...0 (Address 010 0110$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

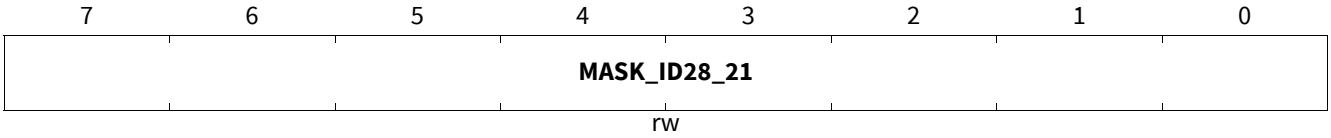
7	6	5	4	3	2	1	0
Reserved	**ID4_0**					**RTR**	**IDE**
r	rw					rw	rw

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
ID4_0	6:2	rw	**WUF Identifier Bits 4..0**
RTR	1	rw	**Remote Transmission Request Field (acc. ISO 11898-1)** 0_B Normal Data Frame 1_B Remote Transmission Request
IDE	0	rw	**Identifier Extension Bit** 0_B Standard Identifier Length (11 bit) 1_B Extended Identifier Length (29 bit)

Note: The setting RTR = 1 is not allowed for wake-up frames according to the ISO11898-6.

SWK WUF Identifier Mask bits 28...21

SWK_MASK_ID3_CTRL
SWK WUF Identifier Mask bits 28...21 (Address 010 0111_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$

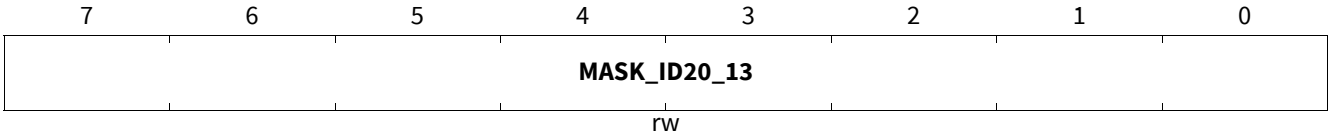


Field	Bits	Type	Description
MASK_ID28_21	7:0	rw	**WUF Identifier Mask Bits 28...21** 0_B Unmasked - bit is ignored 1_B Masked - bit is compared in CAN frame

Note: WUF bits are masked by setting the respective MASK bit to '1'.

SWK WUF Identifier Mask bits 20...13

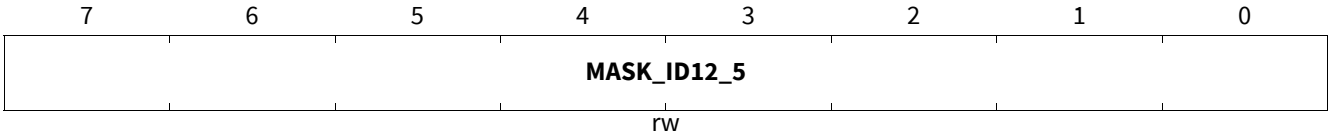
SWK_MASK_ID2_CTRL
SWK WUF Identifier Mask bits 20...13 (Address 010 1000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$



Field	Bits	Type	Description
MASK_ID20_13	7:0	rw	**WUF Identifier Mask Bits 20...13** 0_B Unmasked - bit is ignored 1_B Masked - bit is compared in CAN frame

SWK WUF Identifier Mask bits 12...5

SWK_MASK_ID1_CTRL
SWK WUF Identifier Mask bits 12...5 (Address 010 1001_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$



Field	Bits	Type	Description
MASK_ID12_5	7:0	rw	**WUF Identifier Mask Bits 12...5** 0_B Unmasked - bit is ignored 1_B Masked - bit is compared in CAN frame

SWK WUF Identifier bits 4...0

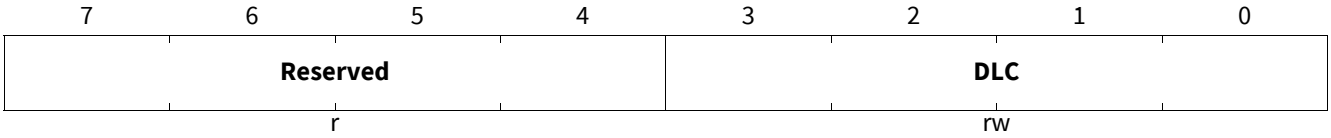
SWK_MASK_ID0_CTRL
SWK WUF Identifier bits 4...0 (Address 010 1010$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xx00$_B$

7	6	5	4	3	2	1	0
Reserved	**MASK_ID4_0**					**Reserved**	
r	rw					r	

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
MASK_ID4_0	6:2	rw	**WUF Identifier MASK Bits 4..0** 0_B Unmasked - bit is ignored 1_B Masked - bit is compared in CAN frame
Reserved	1:0	r	**Reserved, always reads as 0**

SWK Frame Data Length Code Control

SWK_DLC_CTRL
SWK Frame Data Length Code Control (Address 010 1011_B)
POR / Soft Reset Value: 0000 0000_B; Restart Value: xxxx $xxxx_B$

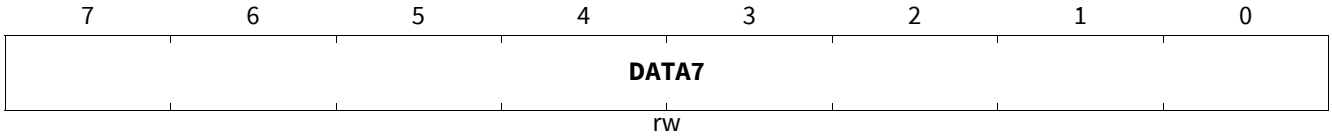


Field	Bits	Type	Description
Reserved	7:4	r	**Reserved, always reads as 0**
DLC	3:0	rw	**Payload length in number of bytes** 0000_B Frame Data Length = 0 or cleared 0001_B Frame Data Length = 1 0010_B Frame Data Length = 2 0011_B Frame Data Length = 3 0100_B Frame Data Length = 4 0101_B Frame Data Length = 5 0110_B Frame Data Length = 6 0111_B Frame Data Length = 7 from 1000_B to 1111_B Frame Data Length = 8

*Note: The number of bytes in the data field has to be indicated by the DLC. This DLC consists of four bits. The admissible number of data bytes for a data frame is in a range from zero to eight. DLCs in the range of zero to seven indicates data fields of length of zero to seven bytes. DLCs in the range from eight to fifteen indicate data fields of length of eight byte.The configured DLC value has to match bit by bit with the DLC in the received wake-up frame (refer also to **Chapter 5.3.2.3**).*

SWK Data7 Register

SWK_DATA7_CTRL
SWK Data7 Register (Address 010 1100_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$

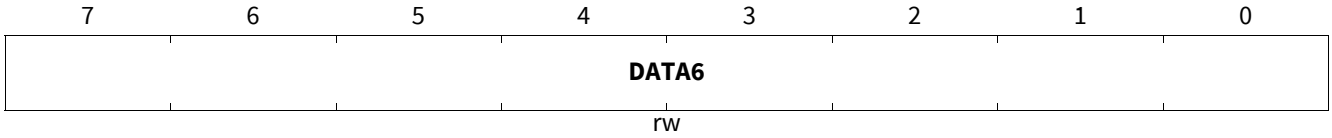


Field	Bits	Type	Description
DATA7	7:0	rw	**Data7 byte content(bit0=LSB; bit7=MSB)**

Serial Peripheral Interface

SWK Data6 Register

SWK_DATA6_CTRL
SWK Data6 Register (Address 010 1101_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$

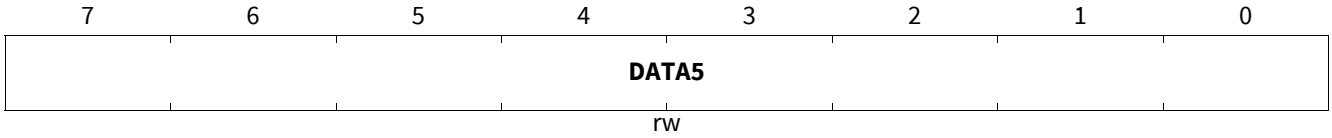


Field	Bits	Type	Description
DATA6	7:0	rw	**Data6 byte content (bit0=LSB; bit7=MSB)**

Serial Peripheral Interface

SWK Data5 Register

SWK_DATA5_CTRL
SWK Data5 Register (Address 010 1110$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

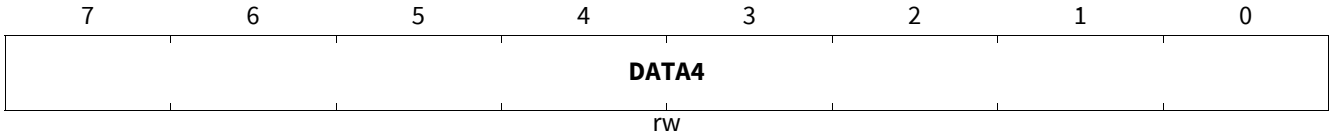


Field	Bits	Type	Description
DATA5	7:0	rw	**Data5 byte content (bit0=LSB; bit7=MSB)**

Serial Peripheral Interface

SWK Data4 Register

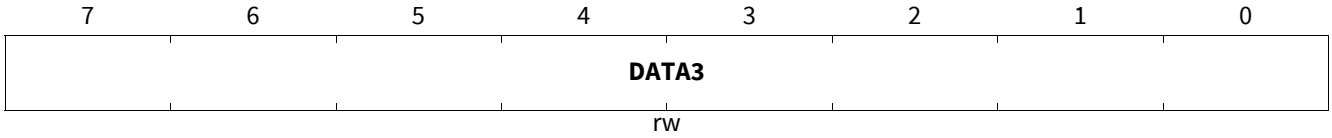
SWK_DATA4_CTRL
SWK Data4 Register (Address 010 1111_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$



Field	Bits	Type	Description
DATA4	7:0	rw	**Data4 byte content (bit0=LSB; bit7=MSB)**

SWK Data3 Register

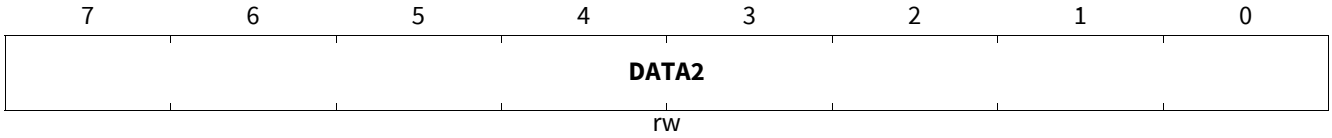
SWK_DATA3_CTRL
SWK Data3 Register (Address 011 0000_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$



Field	Bits	Type	Description
DATA3	7:0	rw	**Data3 byte content (bit0=LSB; bit7=MSB)**

SWK Data2 Register

SWK_DATA2_CTRL
SWK Data2 Register (Address 011 0001$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

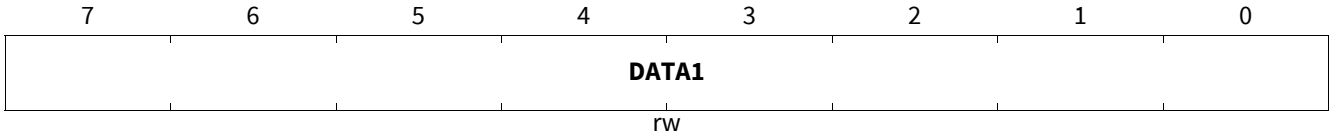


Field	Bits	Type	Description
DATA2	7:0	rw	**Data2 byte content (bit0=LSB; bit7=MSB)**

Serial Peripheral Interface

SWK Data1 Register

SWK_DATA1_CTRL
SWK Data1 Register (Address 011 0010$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

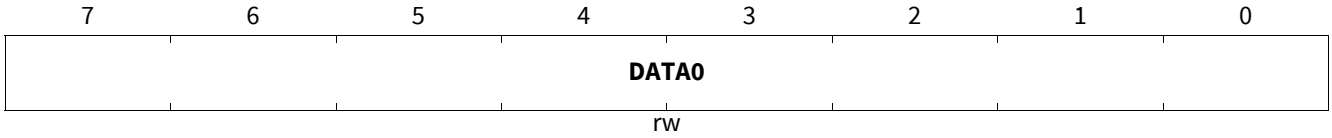


Field	Bits	Type	Description
DATA1	7:0	rw	**Data1 byte content (bit0=LSB; bit7=MSB)**

Serial Peripheral Interface

SWK Data0 Register

SWK_DATA0_CTRL
SWK Data0 Register (Address 011 0011$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$



Field	Bits	Type	Description
DATA0	7:0	rw	**Data0 byte content (bit0=LSB; bit7=MSB)**

CAN FD Configuration Control Register

SWK_CAN_FD_CTRL
CAN FD Configuration Control Register (Address 011 0100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

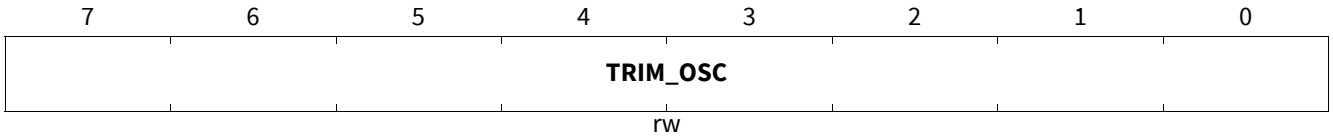
7	6	5	4	3	2	1	0
Reserved		DIS_ERR_CNT	Reserved	FD_FILTER			CAN_FD_EN
r		rwh	r	rw			rw

Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
DIS_ERR_CNT	5	rwh	**Error Counter Disable Function** 0_B Error Counter is enabled during SWK 1_B Error counter is disabled during SWK only if CAN_FD_EN = ‘1’
Reserved	4	r	**Reserved, always reads as 0**
FD_FILTER	3:1	rw	**CAN FD Dominant Filter Time** 000_B 50 ns 001_B 100 ns 010_B 150 ns 011_B 200 ns 100_B 250 ns 101_B 300 ns 110_B 350 ns 111_B 775 ns
CAN_FD_EN	0	rw	**Enable CAN FD Tolerant Mode** 0_B CAN FD Tolerant Mode disabled 1_B CAN FD Tolerant Mode enabled

13.5.3 Selective Wake Trimming and Calibration Control Registers

SWK Oscillator Trimming Register

SWK_OSC_TRIM_CTRL
SWK Oscillator Trimming Register (Address 011 1000$_B$)
POR / Soft Reset Value: xxxx xxxx$_B$; Restart Value: xxxx xxxx$_B$



Field	Bits	Type	Description
TRIM_OSC	7:0	rw	**Oscillator trimming (bit0=LSB; bit7=MSB); (only writable if TRIM_EN = '11')**

Note: TRIM_OSC[0:4] represent the 32-steps fine trimming range with a monotonous behavior from slower to faster frequency. The step width is ~0.25 MHz.
TRIM_OSC[5:7] changes the oscillator temperature coefficient. It is strongly recommended not to chance these values.
Due to CDR functionality, it is not required to change these values.

Serial Peripheral Interface

Selective Wake Options Register

SWK_OPT_CTRL
Selective Wake Options Register (Address 011 1001$_B$)
POR / Soft Reset Value: 000x xxxx$_B$; Restart Value: x00x xxxx$_B$

7	6	5	4	3	2	1	0
RX_WK_SEL	**Reserved**		**TRIM_OSC**				
rw	r		rw				

Field	Bits	Type	Description
RX_WK_SEL	7	rw	**SWK Receiver selection (only accessible if TRIM_EN = '11')** 0_B Standard Receiver selected during SWK 1_B Wake Receiver selected during SWK
Reserved	6:5	r	**Reserved, always reads as 0**
TRIM_OSC	4:0	rw	**Oscillator trimming (bit8=LSB; bit12=MSB);** **(only writable if TRIM_EN = '11')**

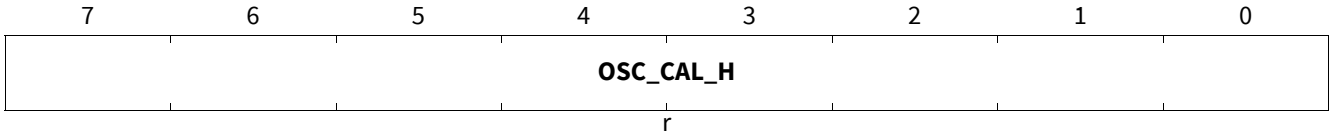
Notes

1. *The bit RX_WK_SEL is used to switch between different receivers. Therefore the same registers are described below again except for the RX_WK_SEL bit. The bit might be not needed in case one receiver is used for Normal Mode and SWK detection.*
2. *TRIM_OSC[8:12] represent the 32-steps coarse trimming range, which is not monotonous. It is not recommended to change these values.*
3. *If only the RX_WK_SEL bit needs to be changed, read the TRIM_OSC [8:12] bits and keep these values for the next write command on SWK_OPT_CRTL.*

Serial Peripheral Interface

SWK Oscillator Calibration High Register

SWK_OSC_CAL_H_STAT
SWK Oscillator Calibration High Register (Address 011 1010$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

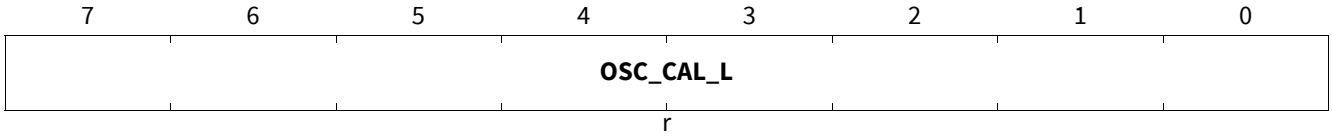


Field	Bits	Type	Description
OSC_CAL_H	7:0	r	**Oscillator Calibration High Register**

Serial Peripheral Interface

SWK Oscillator Calibration Low Register

SWK_OSC_CAL_L_STAT
SWK Oscillator Calibration Low Register (Address 011 1011$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$



Field	Bits	Type	Description
OSC_CAL_L	7:0	r	**Oscillator Calibration Low Register**

CDR Control 1 Register

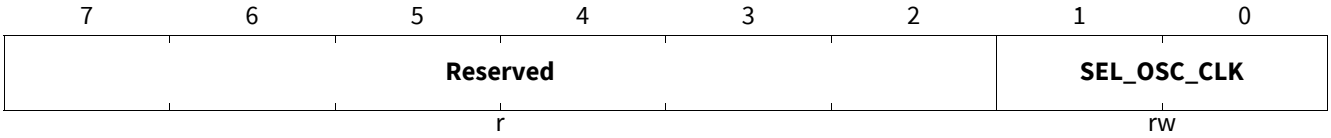
SWK_CDR_CTRL1
CDR Control 1 Register (Address 011 1100$_B$)
POR / Soft Reset Value: 0000 0100$_B$; Restart Value: 0000 xxxx$_B$

7	6	5	4	3	2	1	0
Reserved				SEL_FILT		Reserved	CDR_EN
r				rw		r	rw

Field	Bits	Type	Description
Reserved	7:4	r	**Reserved, always reads as 0**
SEL_FILT	3:2	rw	**Select Time Constant of Filter** 00_B Time constant 8 01_B Time constant 16 (default) 10_B Time constant 32 11_B adapt distance between falling edges 2, 3 bit: Time constant 32 distance between f. edges 4, 5, 6, 7, 8 bit: Time constant 16 distance between falling edges 9, 10 bit: Time constant 8
Reserved	1	r	**Reserved, always reads as 0**
CDR_EN	0	rw	**Enable CDR** 0_B CDR disabled 1_B CDR enabled

CDR Control 2 Register

SWK_CDR_CTRL2
CDR Control 2 Register (Address 011 1101$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 00xx$_B$



Field	Bits	Type	Description
Reserved	7:2	r	**Reserved, always reads as 0**
SEL_OSC_CLK	1:0	rw	**Input Frequency for CDR module** See **Table 32** and **Table 33**

Table 32 Frequency Settings of Internal Clock for the CDR

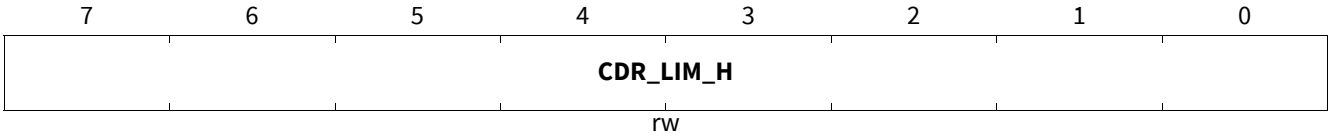
SEL_OSC_CLK[1:0]	int. Clock for CDR
00	80 MHz
01	40 MHz
10	20 MHz
11	10 MHz

Table 33 Recommended CDR Settings for Different Baud Rates

SEL_OSC_CLK [1:0]	Baudrate	SWK_BTL1_CTRL Value	SWK_CDR_LIMIT_HIGH _CTRL Value	SWK_CDR_LIMIT_LOW_ CTRL Value
00	500k	1010 0000	1010 1000	1001 1000
01	500k	0101 0000	0101 0100	0100 1100
10	500k	CDR Setting not recommended for this baudrate due to insufficient precision		
11	500k	CDR Setting not recommended for this baudrate due to insufficient precision		
00	250k	CDR Setting not to be used due to excessive time quanta (counter overflow)		
01	250k	1010 0000	1010 1000	1001 1000
10	250k	0101 0000	0101 0100	0100 1100
11	250k	CDR Setting not recommended for this baudrate due to insufficient precision		
00	125k	CDR Setting not to be used due to excessive time quanta (counter overflow)		
01	125k	CDR Setting not to be used due to excessive time quanta (counter overflow)		
10	125k	1010 0000	1010 1000	1001 1000
11	125k	0101 0000	0101 0100	0100 1100

SWK CDR Upper Limit Control

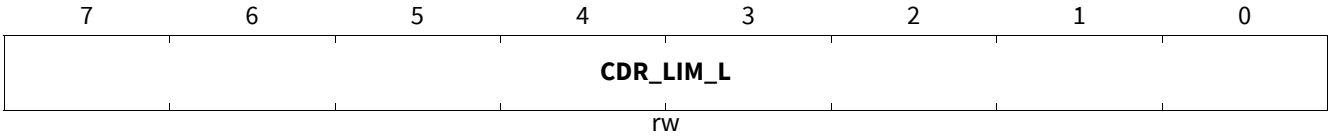
SWK_CDR_LIMIT_HIGH_CTRL
SWK CDR Upper Limit Control (Address 011 1110$_B$)
POR / Soft Reset Value: 1010 1000$_B$; Restart Value: xxxx xxxx$_B$



Field	Bits	Type	Description
CDR_LIM_H	7:0	rw	**Upper Bit Time Detection Range of Clock and Data Recovery** **SWK_BTL1_CTRL** values > + 5% will be clamped

SWK CDR Lower Limit Control

SWK_CDR_LIMIT_LOW_CTRL
SWK CDR Lower Limit Control (Address 011 1111$_B$)
POR / Soft Reset Value: 1001 1000$_B$; Restart Value: xxxx xxxx$_B$



Field	Bits	Type	Description
CDR_LIM_L	7:0	rw	**Lower Bit Time Detection Range of Clock and Data Recovery** **SWK_BTL1_CTRL** values < - 5% will be clamped

13.6 SPI Status Information Registers

Read/Clear Operation (see **Chapter 13.3**):

- One 16-bit SPI command consist of two bytes:
  - the 7-bit address and one additional bit for the register access mode and
  - following the data byte will be ignored when accessing a status register
  The numbering of following bit definitions refers to the data byte and correspond to the bits D0...D7 and to the SPI bits 8...15.
- There are three different bit types:
  - ‘r’ = READ: read only bits (or reserved bits)
  - ‘rc’ = READ/CLEAR: readable and clearable bits
  - ‘rh’ = READ/HARDWARE: readable and the possibility that the hardware can change the bits
- Reading a register is done byte wise by setting the SPI bit 7 to “0” (= Read Only)
- Clearing a register is done byte wise by setting the SPI bit 7 to “1”
- SPI status registers are in general not cleared or changed automatically (an exception are the **WD_FAIL** bits). This must be done by the microcontroller via SPI command

The registers are addressed wordwise.

13.6.1 General Status Registers

Supply Voltage Fail Status 1

SUP_STAT_1
Supply Voltage Fail Status 1 (Address 100 0000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xx0x xxxx$_B$

7	6	5	4	3	2	1	0
VB_UV_BST	**VS_UV**	**Reserved**	**VEXT_OC**	**VREG_UV**	**VEXT_OT**	**VIO_OV**	**VIO_WARN**
rc	rc	r	rc	rc	rc	rc	rc

Field	Bits	Type	Description
VB_UV_BST	7	rc	**VBSENSE low voltage detection** 0_B No VBSENSE low voltage detected 1_B VBSENSE low voltage detected
VS_UV	6	rc	**VS Undervoltage Detection ($V_{S,UV}$)** 0_B No V_S undervoltage detected 1_B V_S undervoltage detected
Reserved	5	r	**Reserved, always reads as 0**
VEXT_OC	4	rc	**VEXT Overcurrent Detection** 0_B No OC 1_B OC detected
VREG_UV	3	rc	**The status is related to VEXT** 0_B No VEXT UV detection 1_B VEXT UV Fail detected
VEXT_OT	2	rc	**VEXT Overtemperature Detection** 0_B No overtemperature 1_B VEXT overtemperature detected
VIO_OV	1	rc	**VIO Overvoltage Detection ($V_{IO,OV,r}$)** 0_B No VIO overvoltage warning 1_B VIO overvoltage detected
VIO_WARN	0	rc	**VIO Undervoltage Prewarning ($V_{PW,f}$)** 0_B No VIO undervoltage prewarning 1_B VIO undervoltage prewarning detected

Notes

1. *The VIO undervoltage prewarning threshold $V_{PW,f}$ is a fixed threshold and independent of the VIO undervoltage reset thresholds.*
2. *VIO_WARN bit setting: It is never updated in SBC Restart Mode. In SBC Init Mode it is only updated after RSTN was released for the first time. It is always updated in SBC Normal and Stop Mode. It is never updated in SBC Sleep Mode and it is always updated in any SBC modes in a VIO_SC condition (after VIO_UV = 1 longer than $t_{VIO,SC}$).*

Supply Voltage Fail Status 0

SUP_STAT_0
Supply Voltage Fail Status 0 (Address 100 0001$_B$)
POR / Soft Reset Value: y000 0000$_B$; Restart Value: x000 0xxx$_B$

7	6	5	4	3	2	1	0
POR	**Reserved**				**VIO_SC**	**VIO_UV_FS**	**VIO_UV**
rc	r				rc	rc	rc

Field	Bits	Type	Description
POR	7	rc	**Power-On Reset Detection** 0_B No POR 1_B POR occurred
Reserved	6:3	r	**Reserved, always reads as 0**
VIO_SC	2	rc	**VIO Short to GND Detection** 0_B No short 1_B VIO short to GND detected
VIO_UV_FS	1	rc	**VIO UV-Detection (due to VRTx reset)** 0_B No Fail-Safe Mode entry due to 4th consecutive VIO_UV 1_B Fail-Safe Mode entry due to 4th consecutive VIO_UV
VIO_UV	0	rc	**VIO UV-Detection (due to VRTx reset)** 0_B No VIO_UV detection 1_B VIO UV-Fail detected

Notes

1. *The MSB of the POR/Soft Reset value is marked as 'y': the default value of the POR bit is set after Power-on reset (POR value = 1000 0000). However it will be cleared after a SBC Software Reset command (Soft Reset value = 0000 0000).*
2. *During SBC Sleep Mode, the bits VIO_SC, VIO_OV and VIO_UV will not be set because the regulator suppling VIO is off.*
3. *The VIO_UV bit is never updated in SBC Restart Mode. In SBC Init Mode, it is only updated after RSTN was released for the first time. It is always updated in SBC Normal and Stop Mode, and it is always updated in any SBC modes in a VIO_SC condition (after VIO_UV = 1 longer than $t_{VIO,SC}$).*

Serial Peripheral Interface

Thermal Protection Status

THERM_STAT
Thermal Protection Status (Address 100 0010$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0xx0 0xxx$_B$

7	6	5	4	3	2	1	0
Reserved	**VCC1_OT**	**BOOST_OT**	**Reserved**		**TSD2**	**TSD1**	**TPW**
r	rc	rc	r		rc	rc	rc

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
VCC1_OT	6	rc	**VCC1 Overtemperature detection** 0_B No VCC1 overtemperature 1_B VCC1 overtemperature detected
BOOST_OT	5	rc	**Boost Overtemperature detection** 0_B No Boost overtemperature 1_B Boost overtemperature detected
Reserved	4:3	r	**Reserved, always reads as 0**
TSD2	2	rc	**TSD2 Thermal Shut-Down Detection** 0_B No TSD2 event 1_B TSD2 OT detected - leading to SBC Fail-Safe Mode
TSD1	1	rc	**TSD1 Thermal Shut-Down Detection** 0_B No TSD1 fail 1_B TSD1 OT detected
TPW	0	rc	**Thermal Pre Warning** 0_B No Thermal Pre warning 1_B Thermal Pre warning detected

Note: TPW, TSD1 and TSD2 are not reset automatically, even if the overtemperature pre warning or TSD1/2 conditions are not longer present.

Serial Peripheral Interface

Device Information Status

DEV_STAT
Device Information Status (Address 100 0011$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xx00 xxxx$_B$

7	6	5	4	3	2	1	0
DEV_STAT		Reserved		WD_FAIL		SPI_FAIL	FO_ON_STATE
rc		r		rh		rc	rc

Field	Bits	Type	Description
DEV_STAT	7:6	rc	**Device Status before Restart Mode** 00_B Cleared (Register must be actively cleared) 01_B Restart due to failure described in **Table 8** and **Table 9**. 10_B Sleep Mode 11_B Reserved
Reserved	5:4	r	**Reserved, always reads as 0**
WD_FAIL	3:2	rh	**Number of WD-Failure Events (1/2 WD failures depending on INTN)** 00_B No WD Fail 01_B 1x WD Fail, FOx activation- Config 1/2 10_B 2x WD Fail, FOx activation- Config 3/4 11_B Reserved (never reached)
SPI_FAIL	1	rc	**SPI Fail Information** 0_B No SPI fail 1_B Invalid SPI command detected
FO_ON_STATE	0	rc	**Activation of Fail Output FO** 0_B No Failure 1_B Failure occurred, FO is activated

Notes

1. *The **WD_FAIL** bits are configured as a counter and are the only status bits, which are cleared automatically by the SBC. They are cleared after a successful watchdog trigger and when the watchdog is stopped (also in SBC Sleep and Fail-Safe Mode unless it was reached due to a watchdog failure). See also **Chapter 11.1**.*
2. *The SPI_FAIL bit is cleared only by SPI command.*
3. *With Config 2/4, the WD_Fail counter is frozen in case of WD trigger failure until a successful WD trigger occurs.*

Bus Communication Status 0

BUS_STAT_0
Bus Communication Status 0 (Address 100 0100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 000x xxxx$_B$

7	6	5	4	3	2	1	0
Reserved			CANTO_0	SYSERR_0	CAN_0_FAIL		VCAN_UV
r			rc	rc	rc		rc

Field	Bits	Type	Description
Reserved	7:5	r	**Reserved, always reads as 0**
CANTO_0	4	rc	**CAN_0 Time Out Detection** 0_B Normal operation 1_B CAN Time Out detected
SYSERR_0	3	rc	**CAN_0 SWK System Error** 0_B Selective Wake Mode is possible 1_B System Error detected, SWK enabling not possible
CAN_0_FAIL	2:1	rc	**CAN_0 Failure Status** 00_B No error 01_B CAN TSD shutdown 10_B CAN_TXD_DOM: TXD dominant time out for more than 2ms 11_B CAN_BUS_DOM: BUS dominant time out for more than 2ms
VCAN_UV	0	rc	**Undervoltage CAN Bus Supply** 0_B Normal operation 1_B CAN Supply undervoltage detected. Transmitter disabled

Notes

1. *CAN0 Recovery Conditions:*
   1.) TXD Time Out: TXDCAN0 goes HIGH or transmitter is switched off or the transceiver is wake capable;
   2.) Bus dominant time out: Bus will become recessive or transceiver is set to wake capable or switched off.
   3.) Supply undervoltage: as soon as the threshold is crossed again, i.e. VCAN > VCAN_UV
   4.) In all cases (also for TSD shutdown): to enable the Bus transmission again, TXDCAN0 needs to be HIGH for a certain time (transmitter enable time).
2. *The VCAN_UV comparator is enabled if the mode bit CANx_1 = '1', i.e. in CAN Normal or CAN Receive Only Mode.*
3. *CANTO_x is set only if CANx_2 = 1 (=SWK Mode enabled). It is set as soon as CANSIL_x is set and stays set even in CANSIL_x is reset. An interrupt is issued in SBC Stop and SBC Normal Mode as soon as CANTO_x is set and the interrupt is not masked out, i.e. CANTO_x must be set to 1.*
4. *The SYSERR_x flag is set in case of a configuration error and in case of an error counter overflow (n>32). It is only updated if SWK is enabled (CANx_2 = '1'). See also **Chapter 5.3.3**.*
5. *CANTO_x is set asynchronously to the INTN pulse. In order to prevent undesired clearing of CANTO_x and thus possibly missing this interrupt, the bit will be prevented from clearing (i.e. cannot be cleared) until the next falling edge of INTN.*

Wake-up Source and Information Status 0

WK_STAT_0
Wake-up Source and Information Status 0 (Address 100 0110_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $x0xx\ 000x_B$

7	6	5	4	3	2	1	0
PFM_PWM	**Reserved**	**CAN_0_WU**	**TIMER_0_WU**	**Reserved**			**WK_WU**
rc	r	rc	rc	r			rc

Field	Bits	Type	Description
PFM_PWM	7	rc	**PFM_PWM automatic transition detected** 0_B No automatic PFM_PWM transition detected 1_B Automatic PFM_PWM transition detected
Reserved	6	r	**Reserved, always reads as 0**
CAN_0_WU	5	rc	**Wake up via CAN_0 Bus** 0_B No Wake up 1_B Wake up
TIMER_0_WU	4	rc	**Wake up via cyclic wake** 0_B No Wake up 1_B Wake up
Reserved	3:1	r	**Reserved, always reads as 0**
WK_WU	0	rc	**Wake up via WK** 0_B No Wake up 1_B Wake up

Note: The respective wake source bit will also be set when the device is woken from SBC Fail-Safe Mode.

WK Input Level

WK_LVL_STAT
WK Input Level (Address 100 1000_B)
POR / Soft Reset Value: xx0x $000x_B$; Restart Value: xxxx $x00x_B$

7	6	5	4	3	2	1	0
TEST	CFG1_STATE	CFG2_STATE	PCFG_STATE	VBAT_UV_STATE	Reserved		WK
r	r	r	r	r	r		r

Field	Bits	Type	Description
TEST	7	r	**Status of SBC Development Mode** 0_B LOW Level (=0), Normal User Operation, SBC Development Mode is disabled 1_B HIGH Level (=1), SBC Development Mode is enabled, no reset triggered due to wrong Watchdog trigger
CFG1_STATE	6	r	**Status of INTN Pin** This bit shows the level of the INTN pin regarding the device configuration 0_B LOW Level; Fail-Safe Mode entered due to WD failure (1 or 2 failure) depending on CFG2 bit) Config 2/4 1_B HIGH Level; Fail-Safe Mode not entered, due to WD failure, Config 1/3
CFG2_STATE	5	r	**Status of CFG2 bit on HW_CTRL_0 register** This bit shows the setting in bit CFG2 0_B LOW Level (=0), Fail Outputs (FOx) are active after 2nd watchdog trigger fail Config 3/4 1_B HIGH Level (=1); Fail Outputs (FOx) are active after 1st watchdog trigger fail Config 1/2
PCFG_STATE	4	r	**Status of PCFG Pin** 0_B LOW Level; (connected to GND) 1_B HIGH Level; (left OPEN)
VBAT_UV_STATE	3	r	**VBSENSE Undervoltage Detection Status** 0_B No VBSENSE undervoltage detected 1_B VBSENSE undervoltage detected
Reserved	2:1	r	**Reserved, always reads as 0**
WK	0	r	**Status of WK** 0_B LOW Level (=0) 1_B HIGH Level (=1)

Wake-up Source and Information Status 2

WK_STAT_2
Wake-up Source and Information Status 2 (Address 100 1001_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $x000\ 0xxx_B$

7	6	5	4	3	2	1	0
VBAT_UV_LATCH	Reserved				CAN_3_WU	CAN_2_WU	CAN_1_WU
rc	r				rc	rc	rc

Field	Bits	Type	Description
VBAT_UV_LATCH	7	rc	**VBSENSE Undervoltage Detection** 0_B No VBSENSE undervoltage detected 1_B VBSENSE undervoltage detected (latched status)
Reserved	6:3	r	**Reserved, always reads as 0**
CAN_3_WU	2	rc	**Wake up via CAN_3 Bus** 0_B No wake up 1_B Wake up
CAN_2_WU	1	rc	**Wake up via CAN_2 Bus** 0_B No wake up 1_B Wake up
CAN_1_WU	0	rc	**Wake up via CAN_1 Bus** 0_B No wake up 1_B Wake up

Note: The respective wake source bit will also be set when the device is woken from SBC Fail-Safe Mode.

Bus Communication Status 2

BUS_STAT_2
Bus Communication Status 2 (Address 100 1010$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
CANTO_2	SYSERR_2	CAN_2_FAIL		CANTO_1	SYSERR_1	CAN_1_FAIL	
rc	rc	rc		rc	rc	rc	

Field	Bits	Type	Description
CANTO_2	7	rc	**CAN_2 Time Out Detection** 0_B Normal operation 1_B CAN Time Out detected
SYSERR_2	6	rc	**CAN_2 SWK System Error** 0_B Selective Wake Mode is possible 1_B System Error detected, SWK enabling not possible
CAN_2_FAIL	5:4	rc	**CAN_2 Failure Status** 00_B No error 01_B CAN TSD shutdown 10_B CAN_TXD_DOM: TXD dominant time out for more than 2ms 11_B CAN_BUS_DOM: BUS dominant time out for more than 2ms
CANTO_1	3	rc	**CAN_1 Time Out Detection** 0_B Normal operation 1_B CAN Time Out detected
SYSERR_1	2	rc	**CAN_1 SWK System Error** 0_B Selective Wake Mode is possible 1_B System Error detected, SWK enabling not possible
CAN_1_FAIL	1:0	rc	**CAN_1 Failure Status** 00_B No error 01_B CAN TSD shutdown 10_B CAN_TXD_DOM: TXD dominant time out for more than 2ms 11_B CAN_BUS_DOM: BUS dominant time out for more than 2ms

Notes

1. *CAN Recovery Conditions:*
   1.) TXD Time Out: TXDCANx goes HIGH or transmitter is switched off or the transceiver is wake capable.
   2.) Bus dominant time out: Bus will become recessive or transceiver is set to wake capable or switched off.
   3.) Supply undervoltage: as soon as the threshold is crossed again, i.e. VCAN > VCAN_UV.
   4.) In all cases (also for TSD shutdown): to enable the Bus transmission again, TXDCANx needs to be HIGH for a certain time (transmitter enable time).
2. *CANTO_x is set only if CANx_2 = 1 (=SWK Mode enabled). It is set as soon as CANSIL_x is set and remains set even in CANSIL_x is reset. An interrupt is issued in SBC Stop and SBC Normal Mode as soon as CANTO_x is set and the interrupt is not masked out, i.e. CANTO_x must be set to 1.*
3. *The SYSERR_x Flag is set in case of a configuration error and in case of an error counter overflow (n>32). It is only updated if SWK is enabled (CANx_2 = '1'). See also **Chapter 5.3.3**.*

4. *CANTO_x is set asynchronously to the INTN pulse. In order to prevent undesired clearing of CANTO_x and thus possibly missing this interrupt, the bit will be prevented from clearing (i.e. cannot be cleared) until the next falling edge of INTN.*

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Bus Communication Status 3

BUS_STAT_3
Bus Communication Status 3 (Address 100 1011$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 xxxx$_B$

7	6	5	4	3	2	1	0
Reserved				CANTO_3	SYSERR_3	CAN_3_FAIL	
r				rc	rc	rc	

Field	Bits	Type	Description
Reserved	7:4	r	**Reserved, always reads as 0**
CANTO_3	3	rc	**CAN_3 Time Out Detection** 0_B Normal operation 1_B CAN Time Out detected
SYSERR_3	2	rc	**CAN_3 SWK System Error** 0_B Selective Wake Mode is possible 1_B System Error detected, SWK enabling not possible
CAN_3_FAIL	1:0	rc	**CAN_3 Failure Status** 00_B No error 01_B CAN TSD shutdown 10_B CAN_TXD_DOM: TXD dominant time out for more than 2ms 11_B CAN_BUS_DOM: BUS dominant time out for more than 2ms

Notes

1. *CAN Recovery Conditions:*
   1.) TXD Time Out: TXDCAN3 goes HIGH or transmitter is switched off or the transceiver is wake capable.
   2.) Bus dominant time out: Bus will become recessive or transceiver is set to wake capable or switched off.
   3.) Supply undervoltage: as soon as the threshold is crossed again, i.e. VCAN > VCAN_UV.
   4.) In all cases (also for TSD shutdown): to enable the Bus transmission again, TXDCAN3 needs to be HIGH for a certain time (transmitter enable time).
2. *CANTO_x is set only if CANx_2 = 1 (=SWK Mode enabled). It is set as soon as CANSIL_x is set and will stay set even in CANSIL_x it is reset. An interrupt is issued in SBC Stop and SBC Normal Mode as soon as CANTO_x is set and the interrupt is not masked out, i.e. CANTO_x must be set to 1.*
3. *The SYSERR_x Flag is set in case of a configuration error and in case of an error counter overflow (n>32). It is only updated if SWK is enabled (CANx_2 = '1'). See also **Chapter 5.3.3**.*
4. *CANTO_x is set asynchronously to the INTN pulse. In order to prevent undesired clearing of CANTO_x and thus possibly missing this interrupt, the bit will be prevented from clearing (i.e. cannot be cleared) until the next falling edge of INTN.*

SMPS state

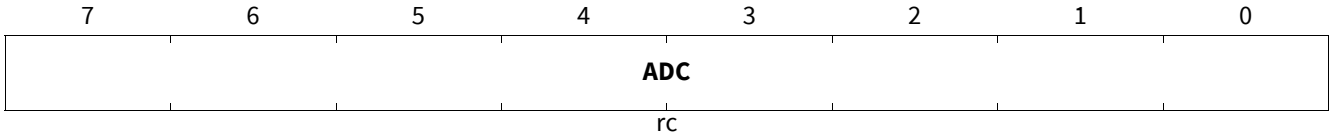
SMPS_STAT
SMPS state (Address 100 1100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxx0 0xx0$_B$

7	6	5	4	3	2	1	0
BST_ACT	**BST_SH**	**BST_OP**	**Reserved**		**BCK_SH**	**BCK_OP**	**Reserved**
rc	rc	rc	r		rc	rc	r

Field	Bits	Type	Description
BST_ACT	7	rc	**Boost Regulator Active** 0_B Boost not active 1_B Boost active
BST_SH	6	rc	**BSTD short detection** 0_B No short detected on BSTD pin 1_B BSTD short to supply
BST_OP	5	rc	**BSTD open detection** 0_B No open detected on BSTD pin 1_B BSTD loss of diode detected or loss of Boost GND
Reserved	4:3	r	**Reserved, always reads as 0**
BCK_SH	2	rc	**BCKSW pin short detection** 0_B No BCKSW short detected 1_B Short to GND or short to V_S detected on BCKSW pin
BCK_OP	1	rc	**BCKSW pin open detection** 0_B No BCKSW open detected 1_B BCKSW loss of freewheeling or BCKSW loss of GND
Reserved	0	r	**Reserved, always reads as 0**

ADC state

ADC_STAT
ADC state (Address 101 1000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$



Field	Bits	Type	Description
ADC	7:0	rc	**ADC output**

13.6.2 Selective Wake Status Registers

Selective Wake Status CAN_3

SWK_STAT_3
Selective Wake Status CAN_3 (Address 110 0100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

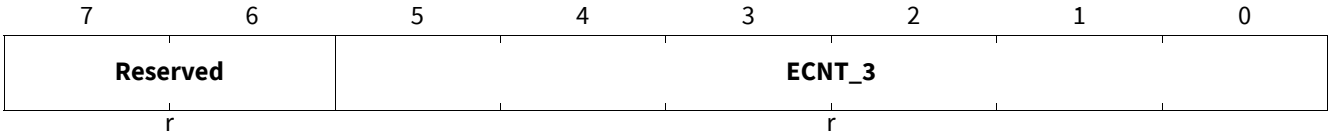
7	6	5 4	3	2	1	0
Reserved	**SYNC_3**	**Reserved**	**CANSIL_3**	**SWK_SET_3**	**WUP_3**	**WUF_3**
r	r	r	r	r	r	r

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
SYNC_3	6	r	**CAN_3 Synchronisation (at least one CAN frame without fail must have been received)** 0_B SWK function not working or not synchronous to CAN bus 1_B Valid CAN frame received, SWK function is synchronous to CAN_3 bus
Reserved	5:4	r	**Reserved, always reads as 0**
CANSIL_3	3	r	**CAN_3 Silent Time during SWK operation** 0_B tsilence not exceeded 1_B set if tsilence is exceeded.
SWK_SET_3	2	r	**CAN_3 Selective Wake Activity** 0_B Selective Wake is not active 1_B Selective Wake is activated
WUP_3	1	r	**CAN_3 Wake-up Pattern Detection** 0_B No WUP 1_B WUP detected
WUF_3	0	r	**CAN_3 SWK Wake-up Frame Detection (acc. ISO 11898-6)** 0_B No WUF 1_B WUF detected

Note: SWK_SET_x is set to flag that the selective wake functionality is activated (SYSERR_x = 0, CFG_VAL = 1, CANx_2 = 1). The selective wake function is activated via a CAN mode change, except if CANx = '100'.

SWK Error Counter Status CAN_3

SWK_ECNT_STAT_3
SWK Error Counter Status CAN_3 (Address 110 0101_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$

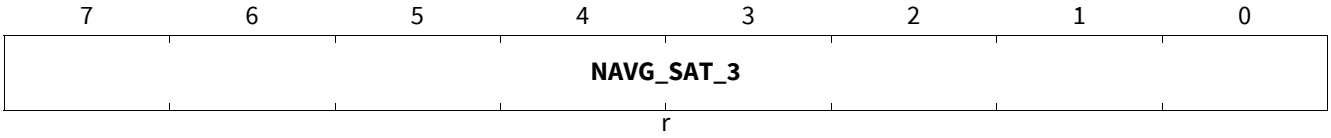


Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
ECNT_3	5:0	r	**SWK CAN_3 Frame Error Counter** $00\ 0000_B$ No Frame Error $01\ 1111_B$ 31 Frame Errors have been counted $10\ 0000_B$ Error counter overflow - SWK function will be disabled

Note: If a frame has been received that is valid according to ISO 11898-1 and the counter is not zero, then the counter shall be decremented. If the counter has reached a value of 32, the following actions shall be performed: Selective Wake function shall be disabled, SYSERR_x shall be set and the CAN wake capable function shall be enabled, which leads to a wake with the next WUP.

CDR Status CAN_3_1

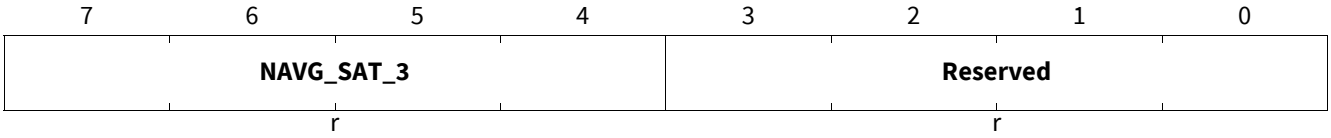
SWK_CDR_STAT_3_1
CDR Status CAN_3_1 (Address 110 0110_B)
POR / Soft Reset Value: $1010\ 0000_B$; Restart Value: xxxx $xxxx_B$



Field	Bits	Type	Description
NAVG_SAT_3	7:0	r	**Output Value from Filter Block** N_AVG is representing the integer part of the number of selected input clock frequency per CAN bus bit. N_AVG[11:4] e.g.160.75

CDR Status CAN_3_0

SWK_CDR_STAT_3_0
CDR Status CAN_3_0 (Address 110 0111_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$



Field	Bits	Type	Description
NAVG_SAT_3	7:4	r	**Output Value from Filter Block** N_AVG is representing the fractional part of the number of selected input clock frequency per CAN bus bit. N_AVG[3:0] e.g.160.75
Reserved	3:0	r	**Reserved, always reads as 0**

Selective Wake Status CAN_2

SWK_STAT_2
Selective Wake Status CAN_2 (Address 110 1000_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$

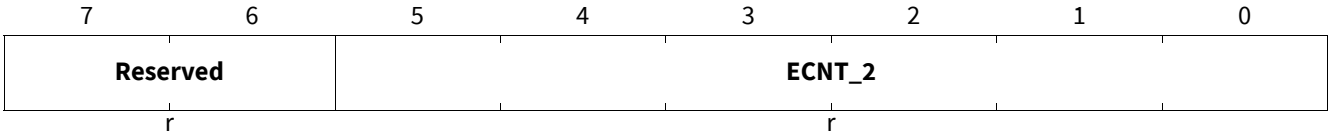
7	6	5 4	3	2	1	0
Reserved	**SYNC_2**	**Reserved**	**CANSIL_2**	**SWK_SET_2**	**WUP_2**	**WUF_2**
r	r	r	r	r	r	r

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
SYNC_2	6	r	**CAN_2 Synchronisation (at least one CAN frame without fail must have been received)** 0_B SWK function not working or not synchronous to CAN bus 1_B Valid CAN frame received, SWK function is synchronous to CAN_2 bus
Reserved	5:4	r	**Reserved, always reads as 0**
CANSIL_2	3	r	**CAN_2 Silent Time during SWK operation** 0_B tsilence not exceeded 1_B set if tsilence is exceeded.
SWK_SET_2	2	r	**CAN_2 Selective Wake Activity** 0_B Selective Wake is not active 1_B Selective Wake is activated
WUP_2	1	r	**CAN_2 Wake-up Pattern Detection** 0_B No WUP 1_B WUP detected
WUF_2	0	r	**CAN_2 SWK Wake-up Frame Detection (acc. ISO 11898-6)** 0_B No WUF 1_B WUF detected

Note: SWK_SET_x is set to flag that the selective wake functionality is activated (SYSERR_x = 0, CFG_VAL = 1, CANx_2 = 1). The selective wake function is activated via a CAN mode change, except if CANx = '100'.

SWK Error Counter Status CAN_2

SWK_ECNT_STAT_2
SWK Error Counter Status CAN_2 (Address 110 1001_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$

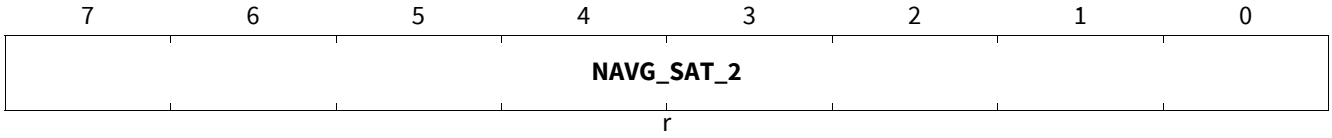


Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
ECNT_2	5:0	r	**SWK CAN_2 Frame Error Counter** $00\ 0000_B$ No Frame Error $01\ 1111_B$ 31 Frame Errors have been counted $10\ 0000_B$ Error counter overflow - SWK function will be disabled

Note: If a frame has been received that is valid according to ISO 11898-1 and the counter is not zero, then the counter shall be decremented. If the counter has reached a value of 32, the following actions shall be performed: Selective Wake function shall be disabled, SYSERR_x shall be set and the CAN wake capable function shall be enabled, which leads to a wake with the next WUP.

CDR Status CAN_2_1

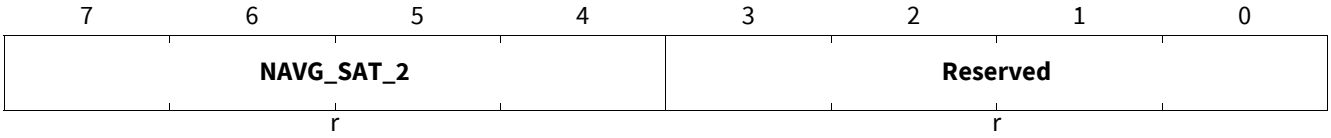
SWK_CDR_STAT_2_1
CDR Status CAN_2_1 (Address 110 1010_B)
POR / Soft Reset Value: $1010\ 0000_B$; Restart Value: xxxx $xxxx_B$



Field	Bits	Type	Description
NAVG_SAT_2	7:0	r	**Output Value from Filter Block** N_AVG is representing the integer part of the number of selected input clock frequency per CAN bus bit. N_AVG[11:4] e.g.160.75

CDR Status CAN_2_0

SWK_CDR_STAT_2_0
CDR Status CAN_2_0 (Address 110 1011_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$



Field	Bits	Type	Description
NAVG_SAT_2	7:4	r	**Output Value from Filter Block** N_AVG is representing the fractional part of the number of selected input clock frequency per CAN bus bit. N_AVG[3:0] e.g.160.75
Reserved	3:0	r	**Reserved, always reads as 0**

Selective Wake Status CAN_1

SWK_STAT_1
Selective Wake Status CAN_1 (Address 110 1100_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$

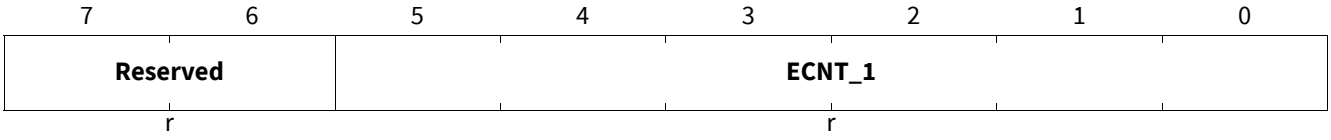
7	6	5	4	3	2	1	0
Reserved	**SYNC_1**	**Reserved**		**CANSIL_1**	**SWK_SET_1**	**WUP_1**	**WUF_1**
r	r	r		r	r	r	r

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
SYNC_1	6	r	**CAN_1 Synchronisation (at least one CAN frame without fail must have been received)** 0_B SWK function not working or not synchronous to CAN bus 1_B Valid CAN frame received, SWK function is synchronous to CAN_1 bus
Reserved	5:4	r	**Reserved, always reads as 0**
CANSIL_1	3	r	**CAN_1 Silent Time during SWK operation** 0_B tsilence not exceeded 1_B set if tsilence is exceeded.
SWK_SET_1	2	r	**CAN_1 Selective Wake Activity** 0_B Selective Wake is not active 1_B Selective Wake is activated
WUP_1	1	r	**CAN_1 Wake-up Pattern Detection** 0_B No WUP 1_B WUP detected
WUF_1	0	r	**CAN_1 SWK Wake-up Frame Detection (acc. ISO 11898-6)** 0_B No WUF 1_B WUF detected

Note: SWK_SET_x is set to flag that the selective wake functionality is activated (SYSERR_x = 0, CFG_VAL = 1, CANx_2 = 1). The selective wake function is activated via a CAN mode change, except if CANx = '100'.

SWK Error Counter Status CAN_1

SWK_ECNT_STAT_1
SWK Error Counter Status CAN_1 (Address 110 1101_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$

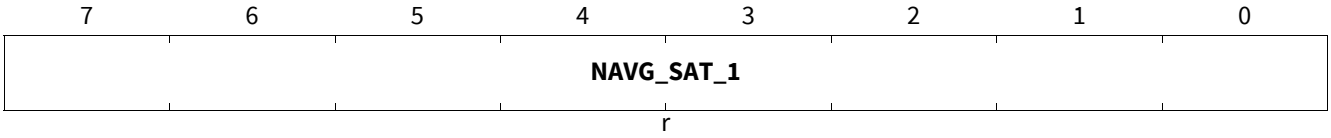


Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
ECNT_1	5:0	r	**SWK CAN_1 Frame Error Counter** $00\ 0000_B$ No Frame Error $01\ 1111_B$ 31 Frame Errors have been counted $10\ 0000_B$ Error counter overflow - SWK function will be disabled

Note: If a frame has been received that is valid according to ISO 11898-1 and the counter is not zero, then the counter shall be decremented. If the counter has reached a value of 32, the following actions shall be performed: Selective Wake function shall be disabled, SYSERR_x shall be set and the CAN wake capable function shall be enabled, which leads to a wake with the next WUP.

CDR Status CAN_1_1

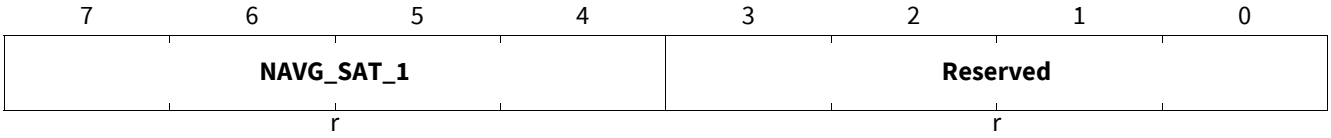
SWK_CDR_STAT_1_1
CDR Status CAN_1_1 (Address 110 1110_B)
POR / Soft Reset Value: $1010\ 0000_B$; Restart Value: xxxx $xxxx_B$



Field	Bits	Type	Description
NAVG_SAT_1	7:0	r	**Output Value from Filter Block** N_AVG is representing the integer part of the number of selected input clock frequency per CAN bus bit. N_AVG[11:4] e.g.160.75

CDR Status CAN_1_0

SWK_CDR_STAT_1_0
CDR Status CAN_1_0 (Address 110 1111_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$



Field	Bits	Type	Description
NAVG_SAT_1	7:4	r	**Output Value from Filter Block** N_AVG is representing the fractional part of the number of selected input clock frequency per CAN bus bit. N_AVG[3:0] e.g.160.75
Reserved	3:0	r	**Reserved, always reads as 0**

Selective Wake Status CAN_0

SWK_STAT_0
Selective Wake Status CAN_0 (Address 111 0000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

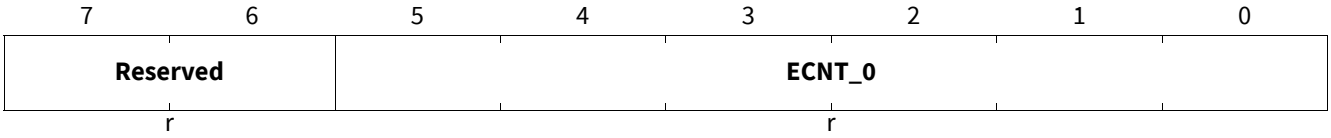
7	6	5	4	3	2	1	0
Reserved	**SYNC_0**	**Reserved**		**CANSIL_0**	**SWK_SET_0**	**WUP_0**	**WUF_0**
r	r	r		r	r	r	r

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
SYNC_0	6	r	**CAN_0 Synchronisation (at least one CAN frame without fail must have been received)** 0_B SWK function not working or not synchronous to CAN bus 1_B Valid CAN frame received, SWK function is synchronous to CAN_0 bus
Reserved	5:4	r	**Reserved, always reads as 0**
CANSIL_0	3	r	**CAN_0 Silent Time during SWK operation** 0_B tsilence not exceeded 1_B set if tsilence is exceeded.
SWK_SET_0	2	r	**CAN_0 Selective Wake Activity** 0_B Selective Wake is not active 1_B Selective Wake is activated
WUP_0	1	r	**CAN_0 Wake-up Pattern Detection** 0_B No WUP 1_B WUP detected
WUF_0	0	r	**CAN_0 SWK Wake-up Frame Detection (acc. ISO 11898-6)** 0_B No WUF 1_B WUF detected

Note: SWK_SET_x is set to flag that the selective wake functionality is activated (SYSERR_x = 0, CFG_VAL = 1, CANx_2 = 1). The selective wake function is activated via a CAN mode change, except if CANx = '100'.

SWK Error Counter Status CAN_0

SWK_ECNT_STAT_0
SWK Error Counter Status CAN_0 (Address 111 0001_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$

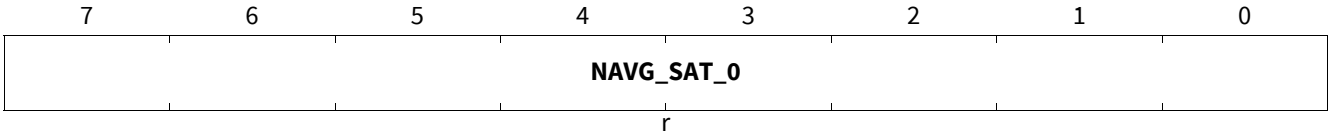


Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
ECNT_0	5:0	r	**SWK CAN_0 Frame Error Counter** $00\ 0000_B$ No Frame Error $01\ 1111_B$ 31 Frame Errors have been counted $10\ 0000_B$ Error counter overflow - SWK function will be disabled

Note: If a frame has been received that is valid according to ISO 11898-1 and the counter is not zero, then the counter shall be decremented. If the counter has reached a value of 32, the following actions shall be performed: Selective Wake function shall be disabled, SYSERR_x shall be set and the CAN wake capable function shall be enabled, which leads to a wake with the next WUP.

CDR Status CAN_0_1

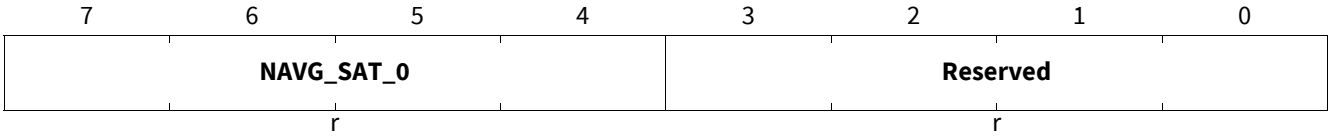
SWK_CDR_STAT_0_1
CDR Status CAN_0_1 (Address 111 0010_B)
POR / Soft Reset Value: $1010\ 0000_B$; Restart Value: xxxx $xxxx_B$



Field	Bits	Type	Description
NAVG_SAT_0	7:0	r	**Output Value from Filter Block** N_AVG is representing the integer part of the number of selected input clock frequency per CAN bus bit. N_AVG[11:4] e.g.160.75

CDR Status CAN_0_0

SWK_CDR_STAT_0_0
CDR Status CAN_0_0 (Address 111 0011_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$

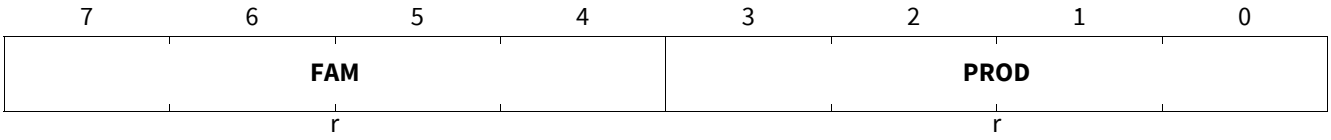


Field	Bits	Type	Description
NAVG_SAT_0	7:4	r	**Output Value from Filter Block** N_AVG is representing the fractional part of the number of selected input clock frequency per CAN bus bit. N_AVG[3:0] e.g.160.75
Reserved	3:0	r	**Reserved, always reads as 0**

13.6.3 Family and Product Information Register

Family and Product Identification Register

FAM_PROD_STAT
Family and Product Identification Register (Address 111 1110_B)
POR / Soft Reset Value: 0100 yyyy $_B$; Restart Value: 0100 yyyy$_B$



Field	Bits	Type	Description
FAM	7:4	r	**SBC Family Identifier (bit4=LSB; bit7=MSB)** 0 0 01_BDriver SBC Family 0 0 10_BDC/DC-SBC Family 0 0 11_BMid-Range SBC Family 0 1 00_BMulti-CAN Power+ SBC Family 0 1 01_BLITE SBC Family 0 1 00_BMid-Range+ SBC Family
PROD	3:0	r	**SBC Product Identifier (bit0=LSB; bit3=MSB)** 0 0 0 0_BTLE9278-3BQX 0 0 0 1_BTLE9278-3BQX V33 0 0 1 0_BTLE9278BQX 0 0 1 1_BTLE9278BQX V33

Notes

1. *The actual default register value after POR, Soft Reset or Restart of PROD depends on the respective product. Therefore the value 'y' is specified.*

13.7 Electrical Characteristics

Table 34 Electrical Characteristics: Power Stage

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SPI frequency							
Maximum SPI frequency	$f_{SPI,max}$	–	–	4.0	MHz	1)	P_13.7.1
SPI Interface; Logic Inputs SDI, CLK and CSN							
H-input Voltage Threshold	V_{IH}	–	–	0.7 × V_{IO}	V	–	P_13.7.2
L-input Voltage Threshold	V_{IL}	0.3 × V_{IO}	–	–	V	–	P_13.7.3
Hysteresis of input Voltage	V_{IHY}	–	0.2 × V_{IO}	–	V	–1)	P_13.7.4
Pull-up Resistance at pin CSN	R_{ICSN}	20	40	80	kΩ	V_{CSN} = 0.7 × V_{IO}	P_13.7.5
Pull-down Resistance at pin SDI and CLK	$R_{ICLK/SDI}$	20	40	80	kΩ	$V_{SDI/CLK}$ = 0.2 × V_{IO}	P_13.7.6
Input Capacitance at pin CSN, SDI or CLK	C_I	–	10	–	pF	1)	P_13.7.7
Logic Output SDO							
H-output Voltage Level	V_{SDOH}	V_{IO} - 0.4	V_{IO} - 0.2	–	V	I_{DOH} = -1.6 mA	P_13.7.8
L-output Voltage Level	V_{SDOL}	–	0.2	0.4	V	I_{DOL} = 1.6 mA	P_13.7.9
Tri-state Leakage Current	I_{SDOLK}	-10	–	10	µA	V_{CSN} = V_{IO}; 0 V < V_{DO} < V_{IO}	P_13.7.10
'Tri-state Input Capacitance	C_{SDO}	–	10	15	pF	1)	P_13.7.11
Data Input Timing1)							
Clock Period	t_{pCLK}	250	–	–	ns	–	P_13.7.12
Clock HIGH Time	t_{CLKH}	125	–	–	ns	–	P_13.7.13
Clock LOW Time	t_{CLKL}	125	–	–	ns	–	P_13.7.14
Clock LOW before CSN LOW	t_{bef}	125	–	–	ns	–	P_13.7.15
CSN Setup Time	t_{lead}	250	–	–	ns	–	P_13.7.16
CLK Setup Time	t_{lag}	250	–	–	ns	–	P_13.7.17
Clock LOW after CSN HIGH	t_{beh}	125	–	–	ns	–	P_13.7.18
SDI Setup Time	t_{DISU}	100	–	–	ns	–	P_13.7.19
SDI Hold Time	t_{DIHO}	50	–	–	ns	–	P_13.7.20
Input Signal Rise Time at pin SDI, CLK and CSN	t_{rIN}	–	–	50	ns	–	P_13.7.21
Input Signal Fall Time at pin SDI, CLK and CSN	t_{fIN}	–	–	50	ns	–	P_13.7.22

Table 34 Electrical Characteristics: Power Stage

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Delay Time for Mode Changes[2]	$t_{Del,Mode}$	–	–	5	µs	–	P_13.7.23
CSN HIGH Time	$t_{CSN(high)}$	3	–	–	µs	–	P_13.7.24
Data Output Timing[1]							
SDO Rise Time	t_{rSDO}	–	30	80	ns	C_L = 100 pF	P_13.7.25
SDO Fall Time	t_{fSDO}	–	30	80	ns	C_L = 100 pF	P_13.7.26
SDO Enable Time	t_{ENSDO}	–	–	50	ns	LOW impedance	P_13.7.27
SDO Disable Time	t_{DISSDO}	–	–	50	ns	HIGH impedance	P_13.7.28
SDO Valid Time	t_{VASDO}	–	–	50	ns	C_L = 100 pF	P_13.7.29

1) Not subject to production test; specified by design.

2) Applies to all mode changes triggered via SPI commands.

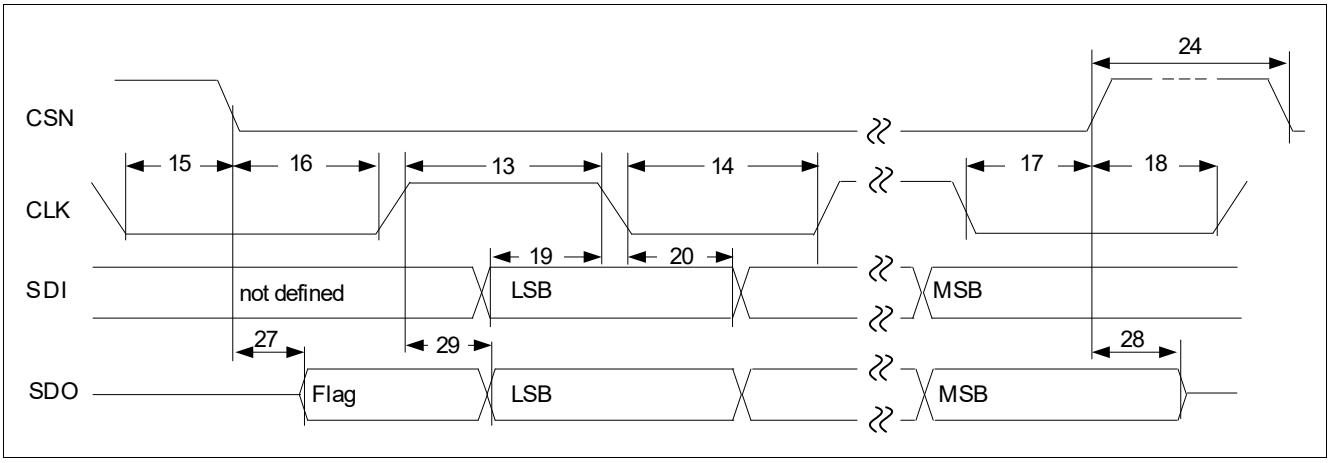


Figure 51 SPI Timing Diagram

Note: Numbers in drawing correlate with the last 2 digits of the Number field in the Electrical Characteristics table.

14 Application Information

14.1 Application Diagram

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

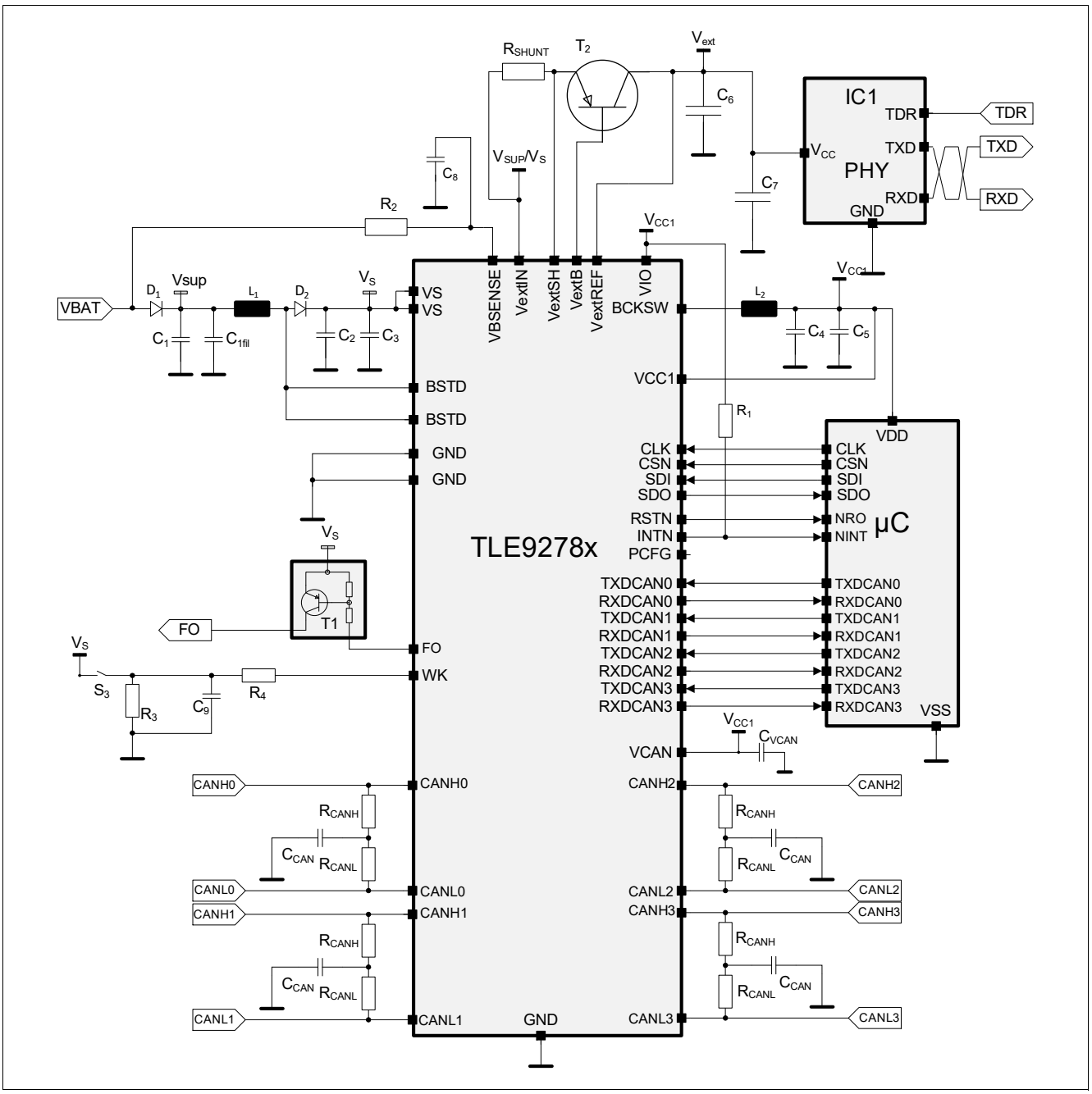


Figure 52 TLE9278-3BQX V33 Application Diagram

Table 35 Bill of Material

Ref.	Typical Value	Purpose / Comment
Capacitances		
C1	47 µF ± 20% Electrolytic	Buffering capacitor to cut off battery spikes, depending on the application. The voltage rating depends on the application.
C1fil	100 nF ± 20%, 50 V ceramic	Input filter battery capacitor for optimum EMC behavior.
C2	100 µF ± 20%, 50 V, Electrolytic	Output Boost capacitor. ESR ≤ 1Ω over the temperature range.
C3	1..10 µF ± 20%, 50 V Ceramic	Input Buck capacitor. Low ESR.
C4, C5	22 µF ± 20%, 16V Ceramic	Output Buck capacitor, for optimum current capability and dynamic behavior. Low ESR.
C_6	10 µF ± 20%, 16 V ceramic	[1] V_{EXT} Output capacitor. Low ESR.
C_7	470 pF ± 20%, 16 V ceramic	V_{EXT} Filter capacitor (only needed if used for off-board supply).
C_8	22 nF ± 20%, 16 V ceramic	V_{BSENSE} blocking capacitor. Low ESR.
C_9	22 nF ± 20%, 16 V ceramic	Spikes filtering, as required by application. Mandatory protection for off-board connection.
C_{VCAN}	1 µF ± 20%, 16 V ceramic	Input filter CAN supply. The capacitor must be placed close to the VCAN pin. For optimum EMC and CAN FD performances, the capacitor has to be ≥ 4.7 µF
C_{CANx}	47 nF / OEM dependent	Split termination stability.
Resistances		
R_{SHUNT}	1 Ω ± 1%	Sense shunt for VEXT current limitation (configured to typ. 235 mA with 1 Ω shunt).
R_1	10 kΩ..22 kΩ ± 5%	Selection of hardware configuration 1/3, i.e. in case of WD failure SBC Restart Mode is entered. If not connected, then the hardware configuration 2/4 is selected.
R_2	10 kΩ ± 5% [2]	Limit the VBSENSE pin input current.
R3	10 kΩ ± 5%	Wetting current of the switch, as required by application.
R4	10 kΩ ± 5%	Limit the WK pin input current, e.g. for ISO pulses.
R_{CANHx}	60 Ω / OEM dependent	CAN bus termination.
R_{CANL}	60 Ω / OEM dependent	CAN bus termination.
Inductors		
L_1	22 µH..47 µH ± 20%	[3] Boost regulator coil. The saturation current depends on the application.
L_2	47 µH ± 20%	[3] Buck regulator coil. The saturation current depends on the application.
Active Components		

Table 35 Bill of Material (cont'd)

Ref.	Typical Value	Purpose / Comment
D1	e.g.SS34HE3/9AT (Vishay) or similar	Reverse polarity protection.
D2	e.g. SL04-GS08 (Vishay) or SS34HE3/9AT	Boost regulator power diode. Forward current depends on the application.
T_2	BCP 52-16, Infineon	Power element of VEXT, current limit to be configured via shunt R_{SHUNT}.
	MJD253, ON Semi	Alternative power element of VEXT.
µC	e.g. XC2xxx	Microcontroller.

1) For optimized EMC performance, one additional filter capacitor ≤ 10 nF ± 20% 16 V ceramic is required.
2) For ISO7637-2 pulse robustness, a higher value might be needed.
3) The saturation current must be define according to the maximum current capability by the application.

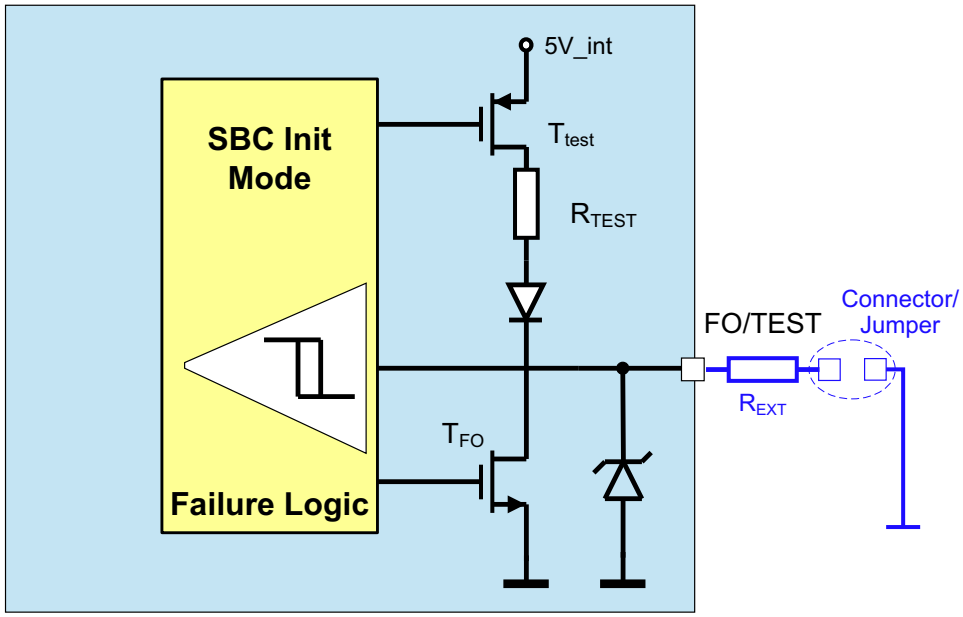


Figure 53 Hint for Increasing the Robustness of pin FO/TEST during Debugging or Programming

14.2 ESD Tests

Tests for ESD robustness according to IEC61000-4-2 “GUN test” (150 pF, 330 Ω) have been performed. The results and test condition are available in a test report. The values for the tests are listed below.

Table 36 ESD “GUN Test”[1)2)]

Performed Test	Result	Unit	Remarks
ESD at pin VS, VBSENSE, VEXTIN, VEXTREF, WK, CANHx, CANLx versus GND	> 6	kV	positive pulse
ESD at pin VS, VBSENSE, VEXTIN, VEXTREF, WK, CANHx, CANLx versus GND	< -6	kV	negative pulse

1) ESD susceptibility “ESD GUN” according to EMC 1.3 Test Specification, Section 4.3 (IEC 61000-4-2). Tested by external test house (IBEE Zwickau, EMC Test report No. 09-12-18).

2) ESD Test “GUN Test” is specified with external components for pins VS, VBSENSE, VEXTIN, VEXTREF and WK. See the application diagrams in **Chapter 14.1** for more information.

EMC and ESD susceptibility tests according to SAE J2962-2 (V. 2014-01-23) have been performed. Tested by external test house (Jakob Mooser GmbH, Test report No. 434/2016).

14.3 Thermal Behavior of Package

The figure below shows the thermal resistance (Rth_JA) of the device vs. the cooling area on the bottom of the PCB for Ta = 85°C. Every line reflects a different PCB and thermal via design.

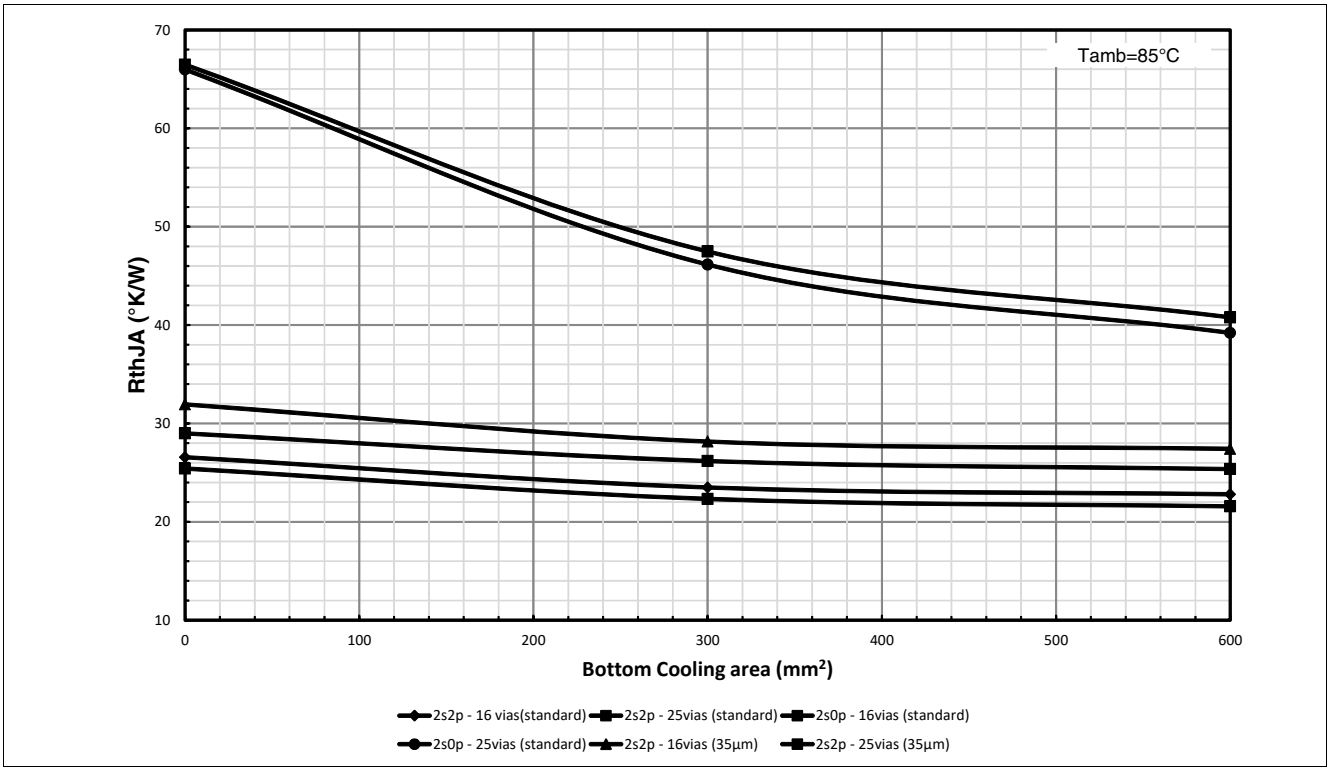


Figure 54 Thermal Resistance (Rth_JA) vs. Cooling Area

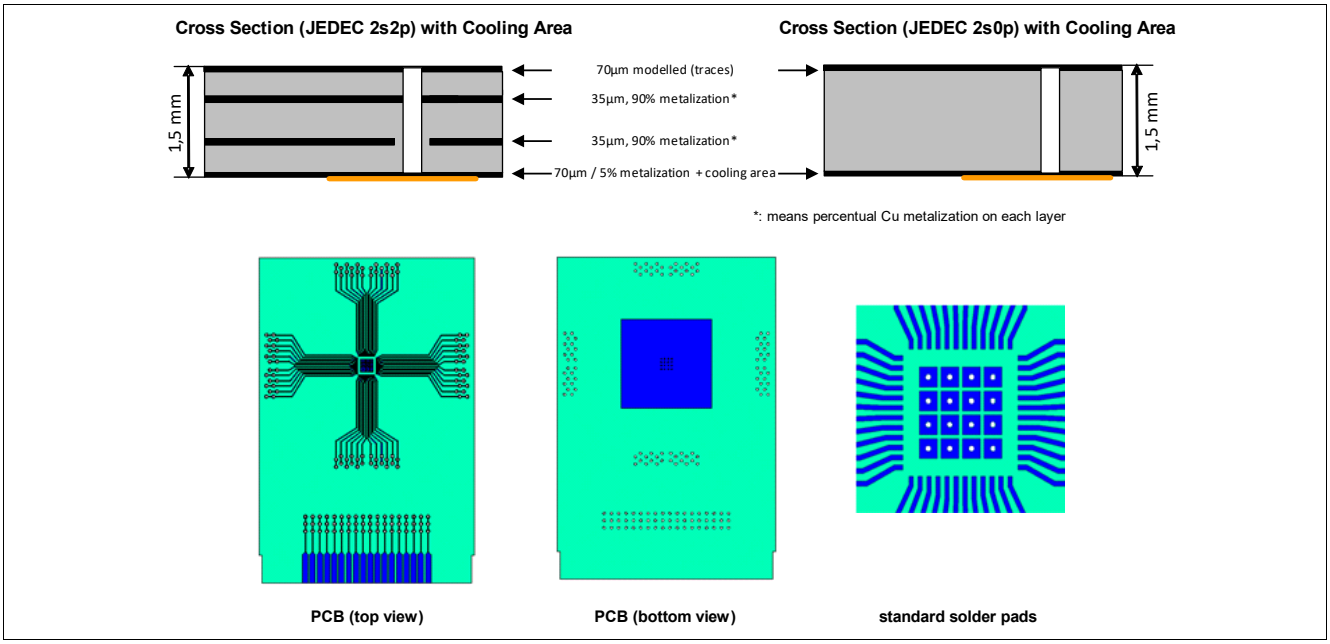


Figure 55 Board Setup

The Board setup is defined according to JESD 51-2,-5,-7.

Board: 76.2 × 114.3 × 1.5 mm^3 with 2 inner copper layers (35 µm thick), with thermal via array under the exposed pad contacting the first inner copper layer and the cooling area on the bottom layer (70 µm).

15 Package Outlines

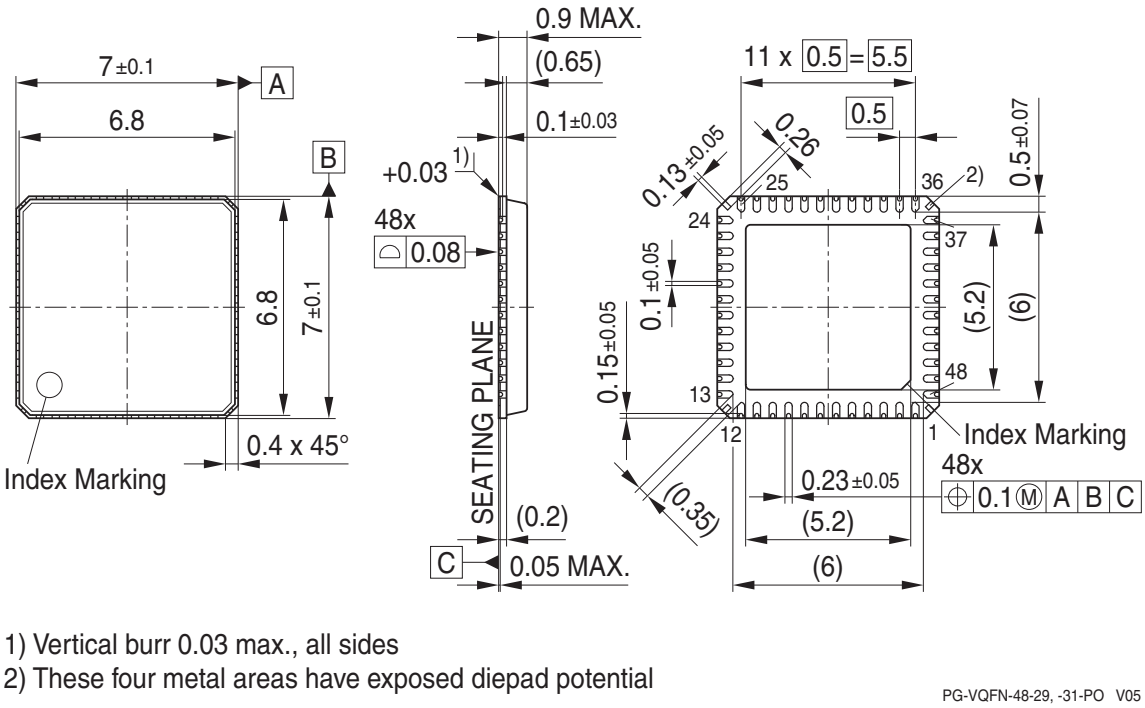


Figure 56 PG-VQFN-48[1)]

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

16 Revision History

Revision	Date	Changes
1.5	2019-09-27	Datasheet updated: • General – corrected typo “ISO 11989-1” to “11898-1” – changed “SBC Software Development Mode” to “SBC Development Mode” • Updated description of the leave procedure in **SBC Development Mode** (FO/TEST pin condition) • **Figure 12** and **Figure 15**: added dot between VS and Boost Converter • Updated **Table 23** – added P_8.3.47 and P_8.3.48 (no product change) – tightened P_8.3.18 – tightened P_8.3.8 and P_8.3.9 by additional footnote • Corrected Bit 6 Address (Status Information Field) in **Table 31** • Added footnote for R_2 in **Table 35** (Bill of Material) • Added **Figure 53**
1.4	2019-01-23	Initial Release.

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