OptiMOS™3 Power-Transistor

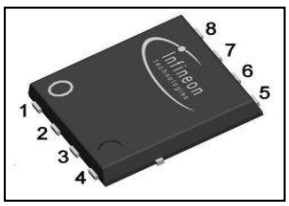
Features

- Fast switching MOSFET for SMPS
- Optimized technology for DC/DC converters
- Qualified according to JEDEC[1] for target applications
- N-channel; Logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% Avalanche tested
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product Summary

V_{DS}	40	V
$R_{DS(on),max}$	5.0	mΩ
I_D	85	A

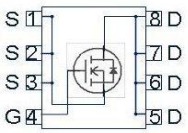
PG-TDSON-8



RoHS

Halogen-Free

Type	Package	Marking
BSC050N04LS G	PG-TDSON-8	050N04LS



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS}=10 V, T_C=25 °C	85	A
		V_{GS}=10 V, T_C=100 °C	54	
		V_{GS}=4.5 V, T_C=25 °C	71	
		V_{GS}=4.5 V, T_C=100 °C	45	
		V_{GS}=10 V, T_A=25 °C, R_{thJA}=50 K/W[2]	18	
Pulsed drain current[3]	$I_{D,pulse}$	T_C=25 °C	340	
Avalanche current, single pulse[4]	I_{AS}	T_C=25 °C	50	
Avalanche energy, single pulse	E_{AS}	I_D=50 A, R_{GS}=25 Ω	35	mJ
Gate source voltage	V_{GS}		±20	V

[1] J-STD20 and JESD22

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	T_C=25 °C	57	W
		T_A=25 °C, R_{thJA}=50 K/W[2)]	2.5	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}	bottom	-	-	2.2	K/W
		top			20	
Device on PCB	R_{thJA}	6 cm^2 cooling area[2)]	-	-	50	

Electrical characteristics, at T_j=25 °C, unless otherwise specified

Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=27 µA	1.2	-	2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=40 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=40 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=50 A	-	5.8	7.2	mΩ
		V_{GS}=10 V, I_D=50 A	-	4.2	5	
Gate resistance	R_G		-	1.5	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=50 A	50	100	-	S

[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3)] See figure 3 for more detailed information

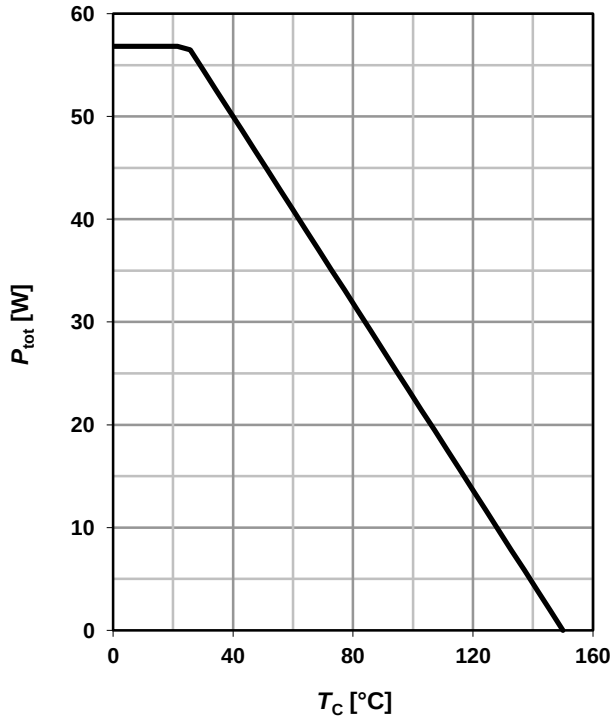
[4)] See figure 13 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz	-	2800	3700	pF
Output capacitance	C_{oss}		-	630	840	
Reverse transfer capacitance	C_{rss}		-	33	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=20 V, V_{GS}=10 V, I_D=30 A, R_G=1.6 Ω	-	6.4	-	ns
Rise time	t_r		-	3.8	-	
Turn-off delay time	$t_{d(off)}$		-	26	-	
Fall time	t_f		-	4.2	-	
Gate Charge Characteristics[5)]						
Gate to source charge	Q_{gs}	V_{DD}=20 V, I_D=30 A, V_{GS}=0 to 10 V	-	9.0	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	4.5	-	
Gate to drain charge	Q_{gd}		-	3.8	-	
Switching charge	Q_{sw}		-	8.2	-	
Gate charge total	Q_g		-	36	47	
Gate plateau voltage	$V_{plateau}$		-	3.2	-	V
Gate charge total	Q_g	V_{DD}=20 V, I_D=30 A, V_{GS}=0 to 4.5 V	-	17	23	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 10 V	-	34	-	
Output charge	Q_{oss}	V_{DD}=20 V, V_{GS}=0 V	-	24	-	
Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	47	A
Diode pulse current	$I_{S,pulse}$		-	-	340	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=50 A, T_j=25 °C	-	0.87	1.2	V
Reverse recovery charge	Q_{rr}	V_R=20 V, I_F=I_S, di_F/dt=400 A/µs	-	27	-	nC

[5)] See figure 16 for gate charge parameter definition

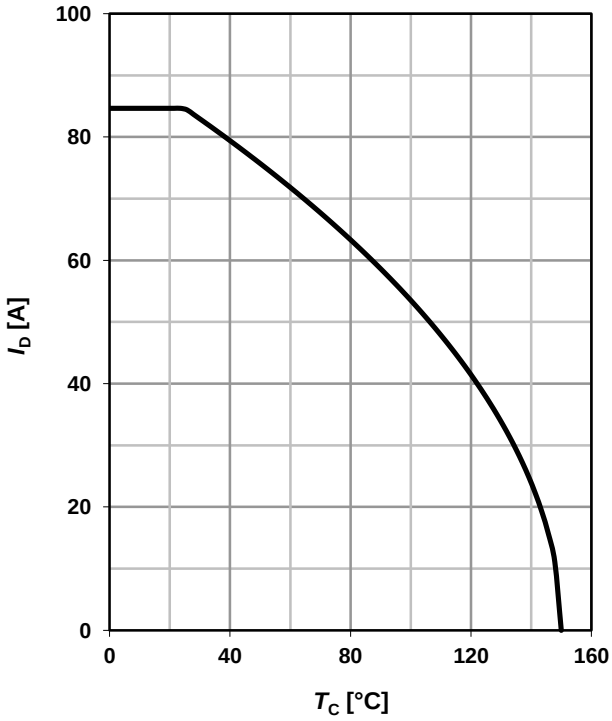
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

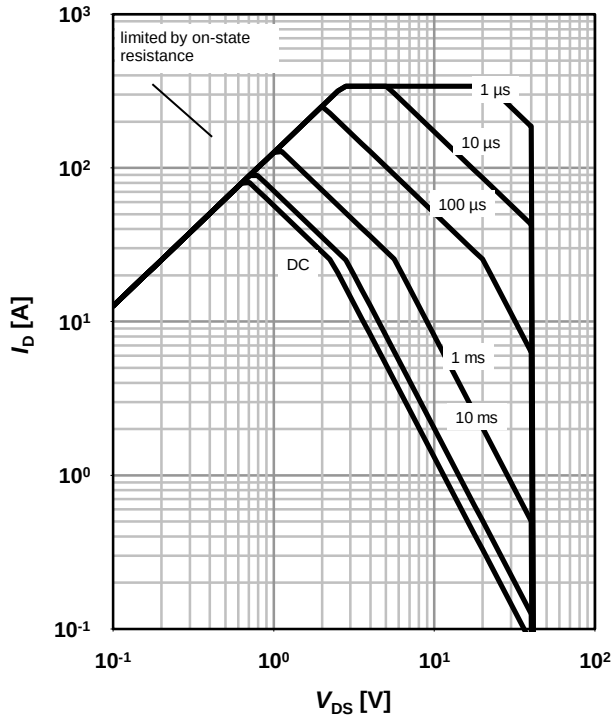
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

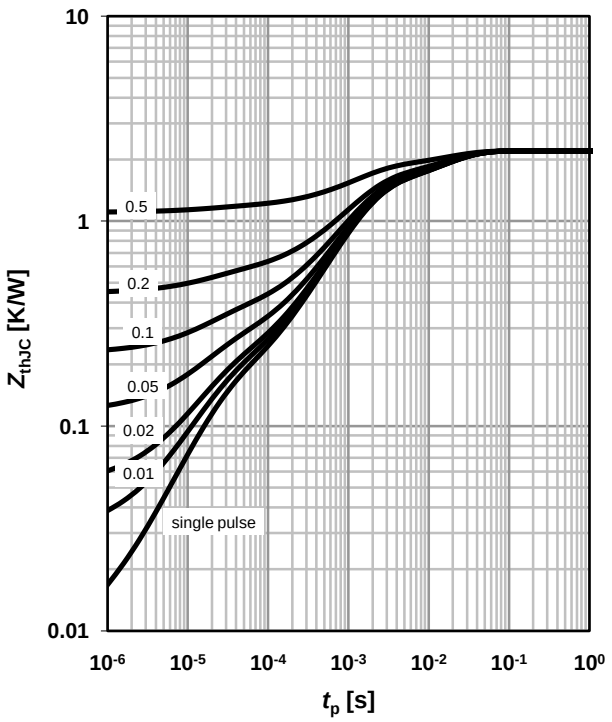
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

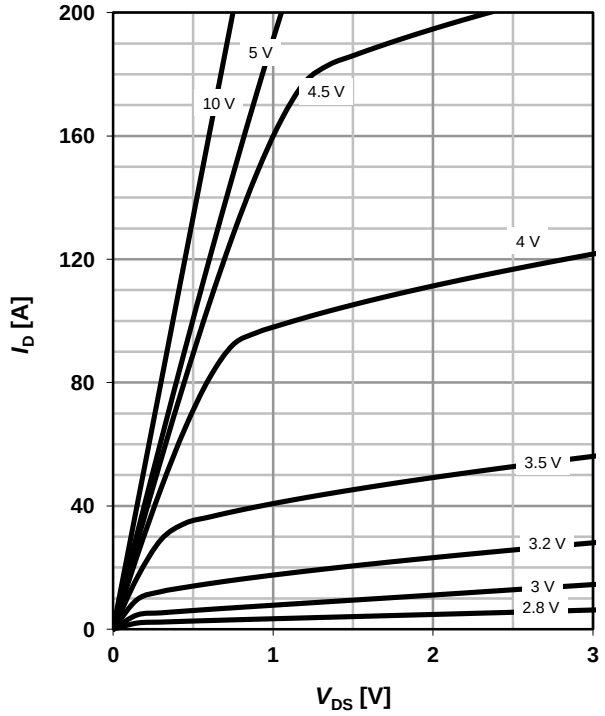
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

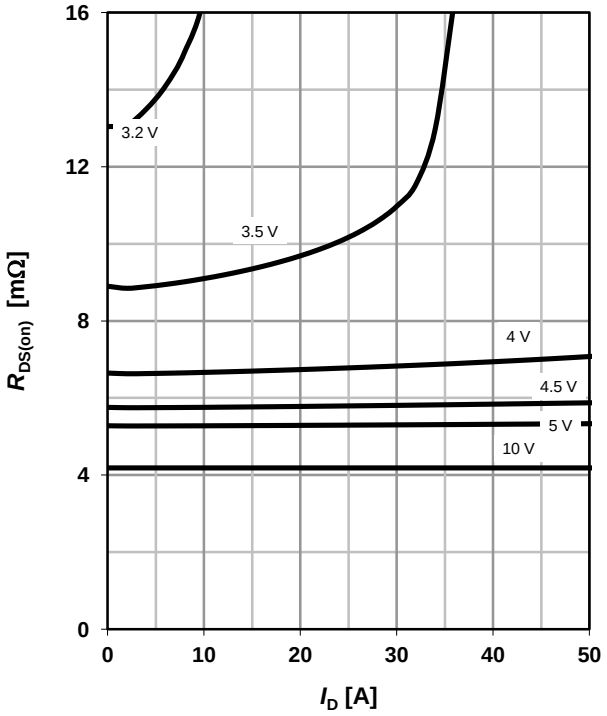
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D)$; $T_j=25$ °C

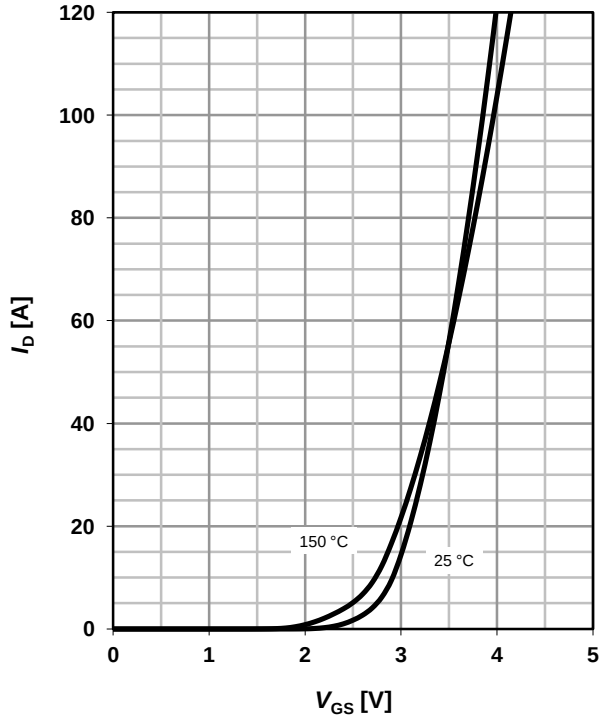
parameter: V_{GS}



7 Typ. transfer characteristics

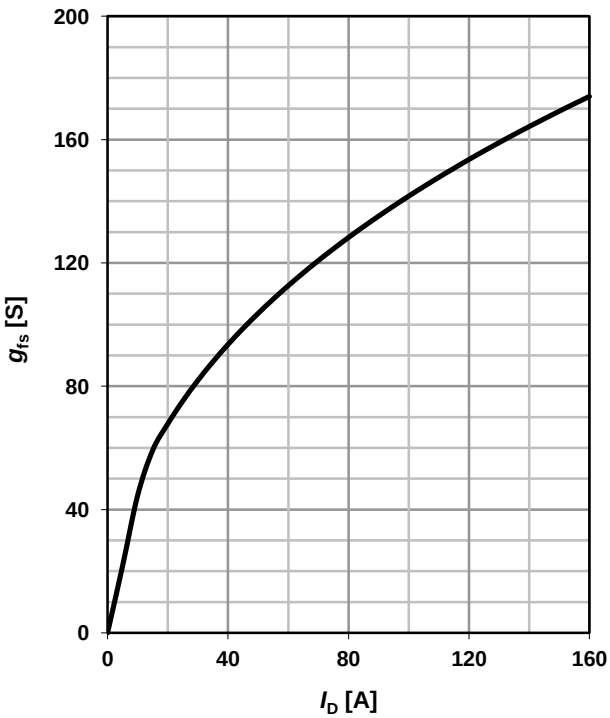
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



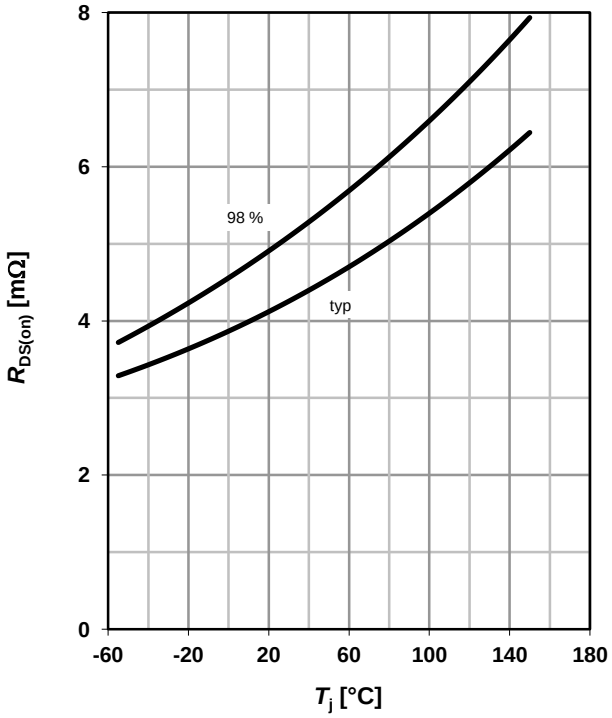
8 Typ. forward transconductance

$g_{fs}=f(I_D)$; $T_j=25$ °C



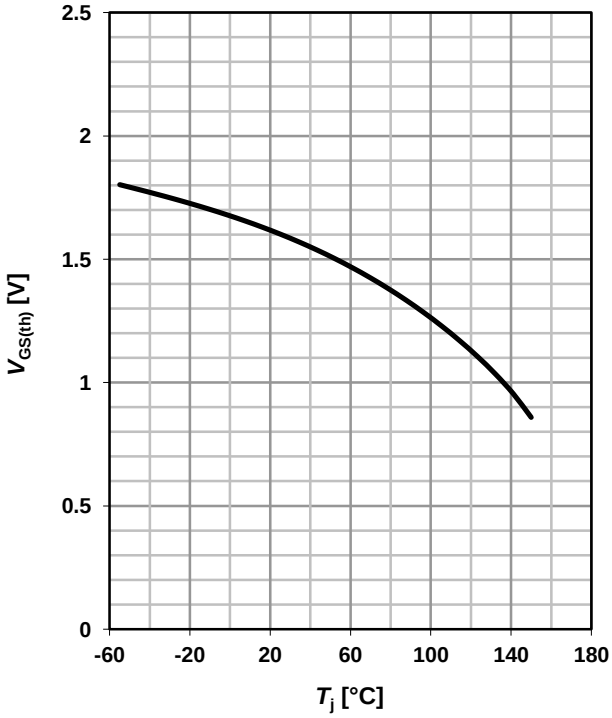
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=50 A; V_{GS}=10 V



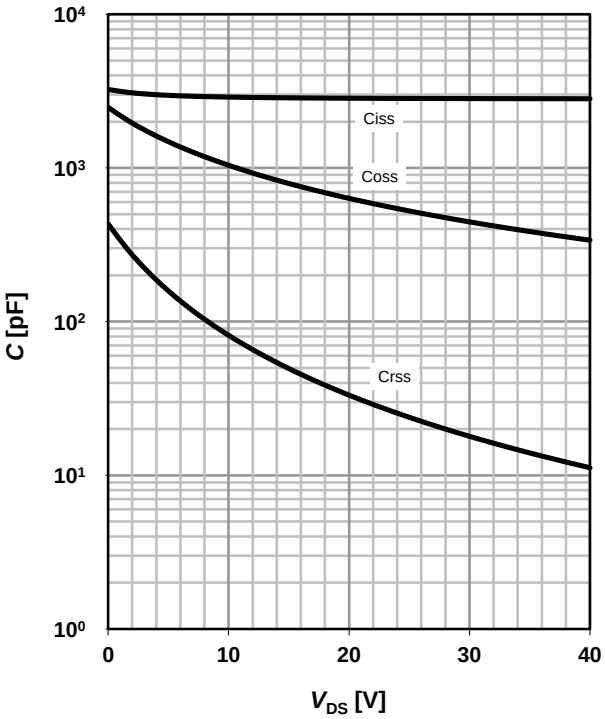
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=27 µA



11 Typ. capacitances

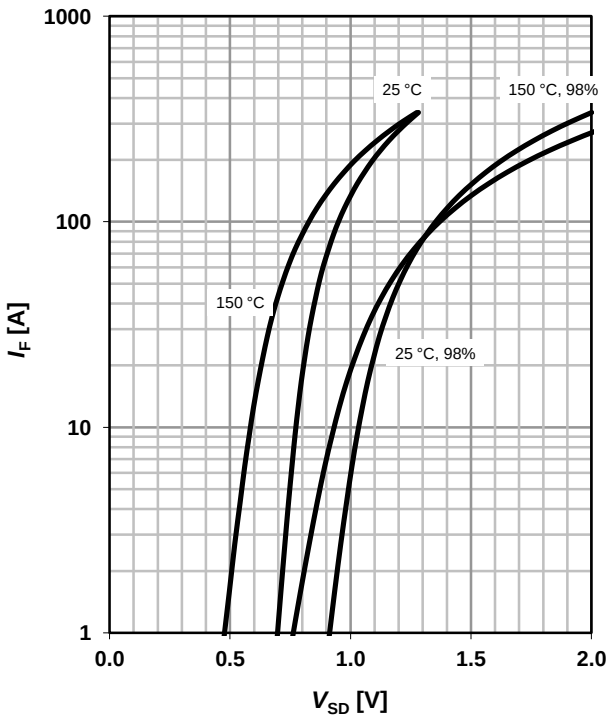
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

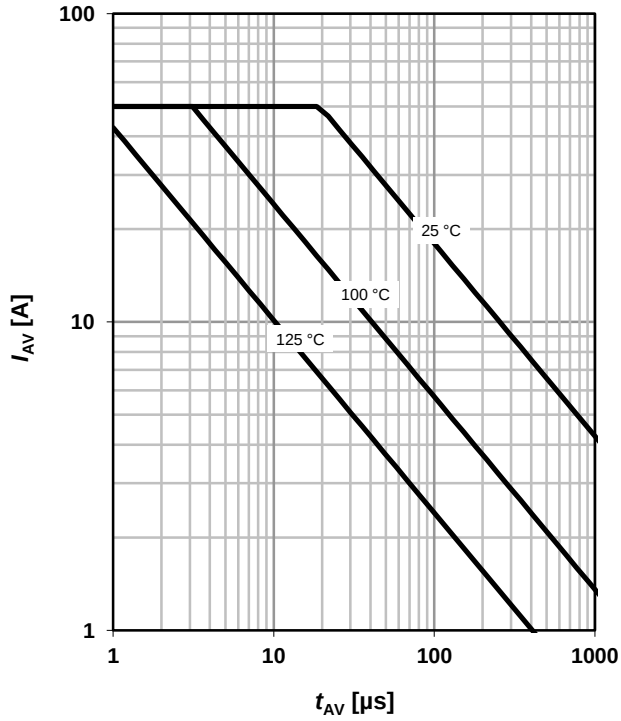
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

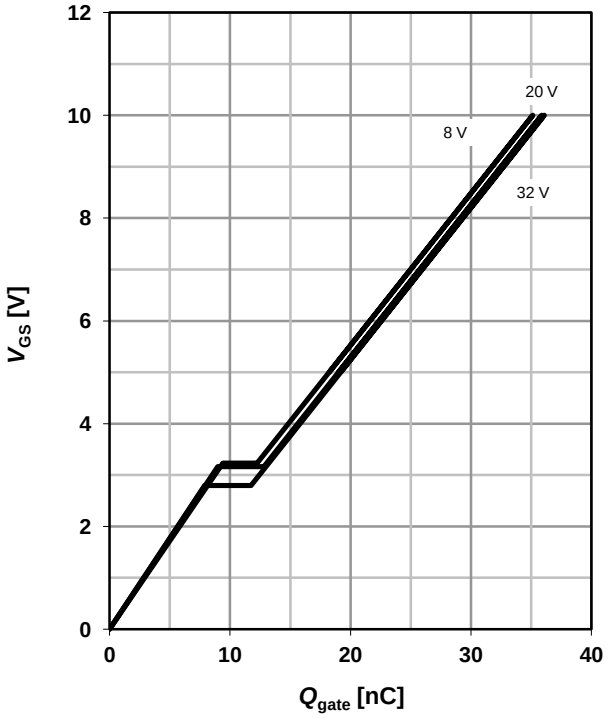
parameter: $T_{j(start)}$



14 Typ. gate charge

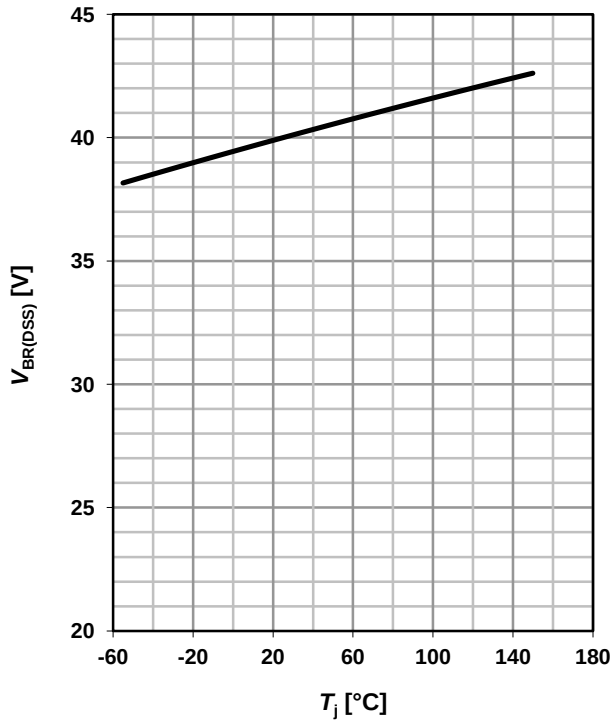
V_{GS}=f(Q_{gate}); I_D=30 A pulsed

parameter: V_{DD}

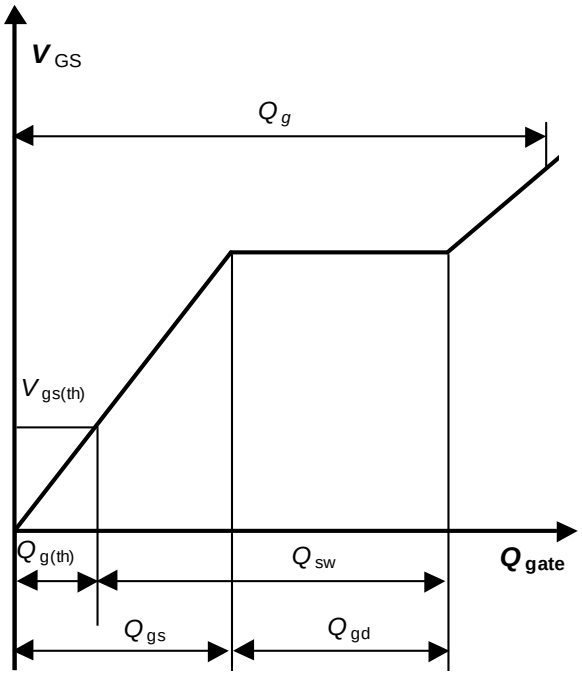


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=1 mA

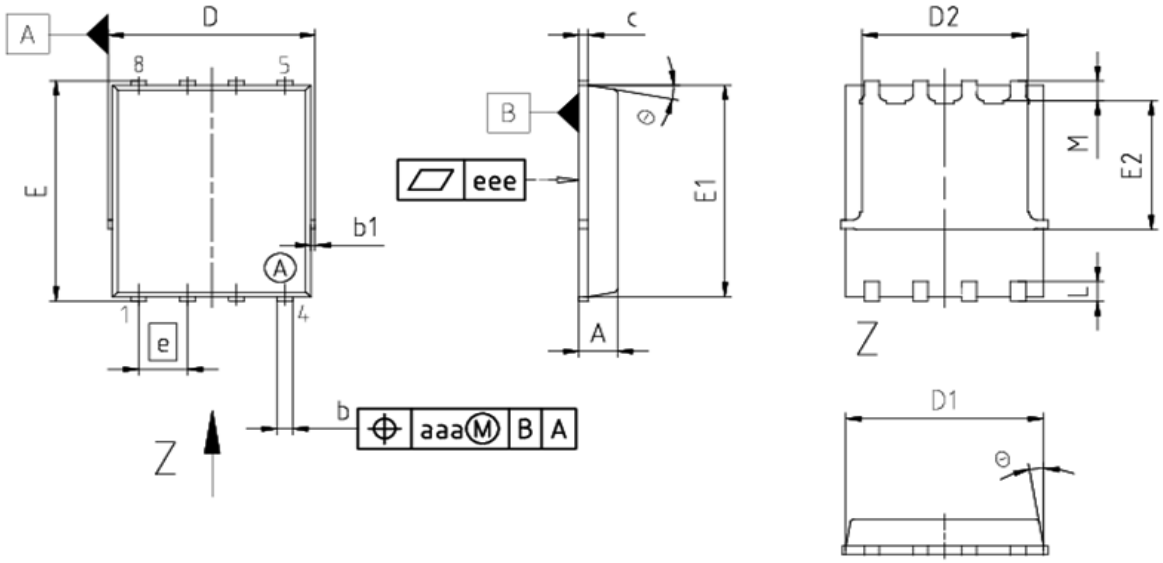


16 Gate charge waveforms



Package Outline **PG-TDSON-8-5**

PG-TDSON-8-5: Outline



DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
b	0.31	0.54
b1	0.02	0.22
c	0.15	0.35
D	5.15	5.49
D1	4.95	5.35
D2	3.70	4.40
E	5.95	6.35
E1	5.70	6.10
E2	3.40	3.80
e	1.27	
N	8	
L	0.45	0.71
M	0.45	0.75
Θ	8.5°	12°
aaa	0.25	
eee	0.08	

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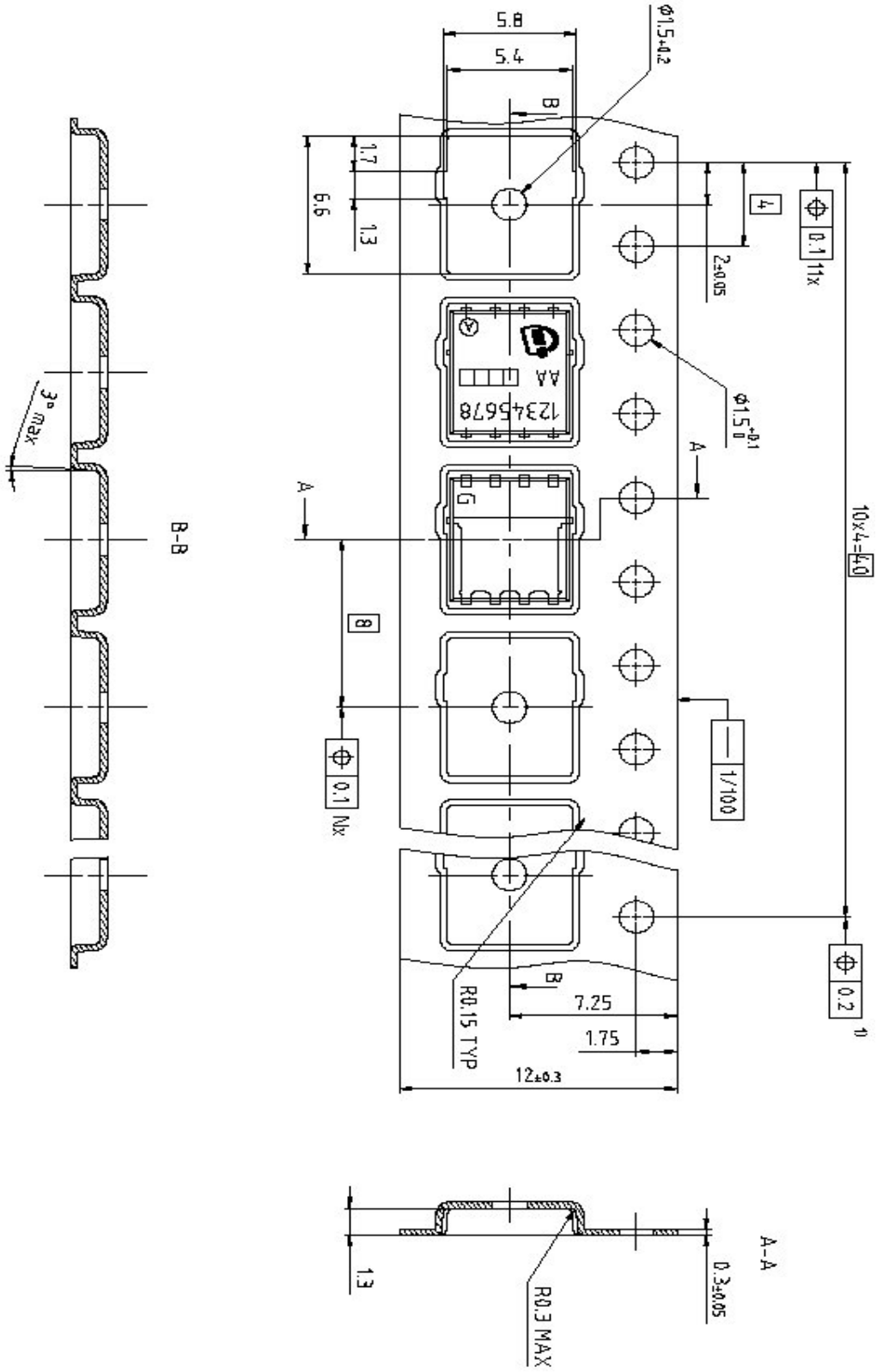
SCALE 0 2 0 2 4mm
EUROPEAN PROJECTION
ISSUE DATE 10-04-2013
REVISION 04

Footprint
Dimensions in mm

Package Outline

PG-TDSON-8: Tape



Dimensions in mm

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