The following document contains information on Cypress products. The document has the series name, product name, and ordering part numbering with the prefix “MB”. However, Cypress will offer these products to new and existing customers with the series name, product name, and ordering part number with the prefix “CY”.

How to Check the Ordering Part Number

1. Go to www.cypress.com/pcn.
2. Enter the keyword (for example, ordering part number) in the **SEARCH PCNS** field and click **Apply**.
3. Click the corresponding title from the search results.
4. Download the Affected Parts List file, which has details of all changes

For More Information

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About Cypress

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MB88155

Spread Spectrum Clock Generator

MB88155 is a clock generator for EMI (Electro Magnetic Interference) reduction. The peak of unnecessary radiation noise (EMI) can be attenuated by making the oscillation frequency slightly modulate periodically with the internal modulator. For modulation, the MB88155 supports both center-spreading and down-spreading. It has a non-modulated clock output pin (REFOUT) as well as a modulated clock output pin (CKOUT) .

Features

- Input frequency : 12.5 MHz to 50 MHz (Multiplied by 1)
  12.5 MHz to 20 MHz (Multiplied by 4)
- Output frequency : CKOUT 12.5 MHz to 80 MHz
  REFOUT The same as input frequency (not multiplied)
- Modulation rate : ± 0.5%, ± 1.0% (center spread) , − 1.0%, − 2.0% (Down spread)
- Equipped with oscillation circuit : range of oscillation 12.5 MHz to 40 MHz (Fundamental oscillation)
  40 MHz to 48 MHz (3rd overtone)
- Modulation clock output Duty : 40% to 60%
- Modulation clock cycle − cycle jitter : MB88155-1xx 12.5 MHz to 20 MHz less than 150 ps
  MB88155-1xx 20 MHz to 50 MHz less than 100 ps
  MB88155-400 less than 200 ps
- Low current consumption by CMOS process : 5 mA (24 MHz : Typ-sample, no load)
- Power supply voltage : 3.3 V ± 0.3 V
- Operating temperature : − 40 °C to + 85 °C
- Package : 8-pin plastic TSSOP

Contents

1. Product Lineup

The MB88155 is available in different models : 2 models different in multiplier (× 1 and × 4) , 2 in modulation type (center-spreading and down-spreading) , 2 in input frequency range at a multiplier of 1 (12.5 MHz to 25 MHz and 25 MHz to 50 MHz) , and 1 in input frequency range at a multiplier of 4 (12.5 MHz to 20 MHz) .
The MB88155 is also available in two versions : modulation-on/off selectable version (with ENS pin) and power-down function built-in version (with XPD pin) .

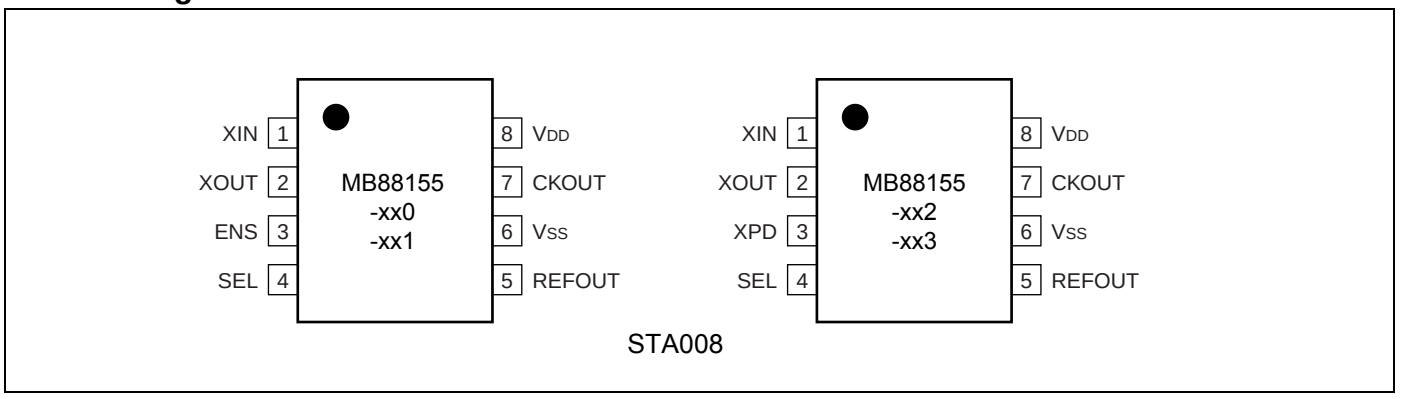
MB88155-M T F

- Input frequency range, With/without ENS/XPD → Multiplied by 1
  - 0 : 12.5 MHz to 25.0 MHz, With ENS, Without XPD
  - 1 : 25.0 MHz to 50.0 MHz, With ENS, Without XPD
  - 2 : 12.5 MHz to 25.0 MHz, Without ENS, With XPD
  - 3 : 25.0 MHz to 50.0 MHz, Without ENS, With XPD
- Multiplied by 4
  - 0 : 12.5 MHz to 20.0 MHz, With ENS, Without XPD
- Spread type → 0 : Down spread, 1 : Center spread
- Multiplication rate setting → 1 : Multiplied by 1, 4 : Multiplied by 4

Line-up of MB88155

Product	Input Frequency	Multiplication Rate	Output Frequency	Modulation Type	Modulation Enable pin	Power Down Pin
MB88155-100	12.5 MHz to 25 MHz	Multiplied by 1	The same as input frequency	Down spread	Yes	No
MB88155-102	12.5 MHz to 25 MHz				No	Yes
MB88155-103	25 MHz to 50 MHz					
MB88155-110	12.5 MHz to 25 MHz			Center spread	Yes	No
MB88155-111	25 MHz to 50 MHz					
MB88155-112	12.5 MHz to 25 MHz				No	Yes
MB88155-400	12.5 MHz to 20 MHz	Multiplied by 4	50 MHz to 80 MHz	Down spread	Yes	No

2. Pin Assignment

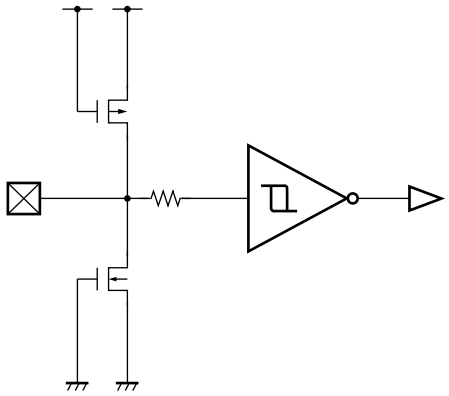
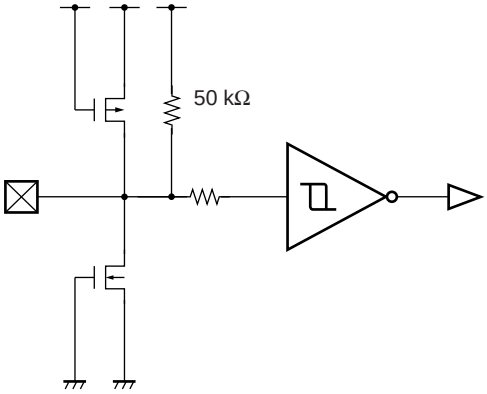
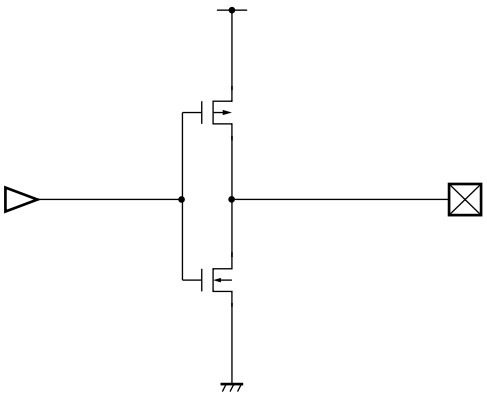


STA008

3. Pin Description

Pin Name	I/O	Pin No.	Description
XIN	I	1	Connection pin of resonator/clock input pin
XOUT	O	2	Connection pin of resonator
ENS/XPD	I	3	Modulation enable pin/power down pin
SEL	I	4	Modulation rate setting pin Down spread, SEL = “L” : Modulation rate − 1.0% Down spread, SEL = “H” : Modulation rate − 2.0% Down spread, SEL = “L” : Modulation rate ± 0.5% Down spread, SEL = “H” : Modulation rate ± 1.0%
REFOUT	O	5	Non-modulated clock output pin This pin becomes to“L” at power-down.
V_{SS}	—	6	GND Pin
CKOUT	O	7	Modulated clock output pin This pin becomes to“L” at power-down.
V_{DD}	—	8	Power supply voltage pin

4. I/O Circuit Type

Pin	Circuit Type	Remarks
SEL, XPD		CMOS hysteresis input
ENS		CMOS hysteresis input with pull-up resistor of 50 kΩ (Typ)
REFOUT		■ CMOS output ■ I_{OL} = 3 mA ■ “L” output at power-down

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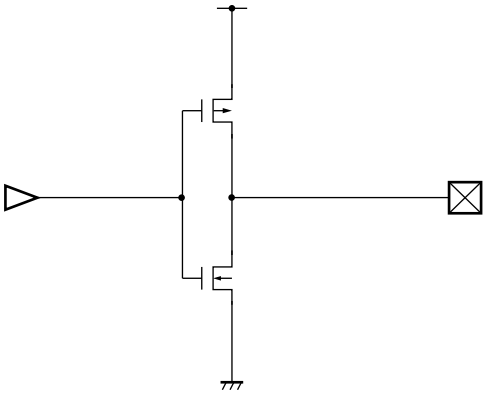
Pin	Circuit Type	Remarks
CKOUT		■ CMOS output ■ I_{OL} = 4 mA ■ “L” output at power-down

Note : For XIN pin and XOUT pin, refer to “Oscillation Circuit”.

5. Handling Devices

5.1 Preventing Latch-up

A latch-up can occur if, on this device, (a) a voltage higher than V_{DD} or a voltage lower than V_{SS} is applied to an input or output pin or (b) a voltage higher than the rating is applied between V_{DD} and V_{SS}. The latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use this device, be very careful not to exceed the maximum rating.

5.2 Handling Unused Pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, using a pull-up or pull-down resistor.

Unused output pin should be opened.

5.3 The Attention when the External Clock is Used

Input the clock to XIN pin, and XOUT pin should be opened when you use the external clock.
Please pay attention so that an overshoot and an undershoot do not occur to an input clock of XIN pin.

5.4 Power Supply Pins

Please design connecting the power supply pin of this device by as low impedance as possible from the current supply source.

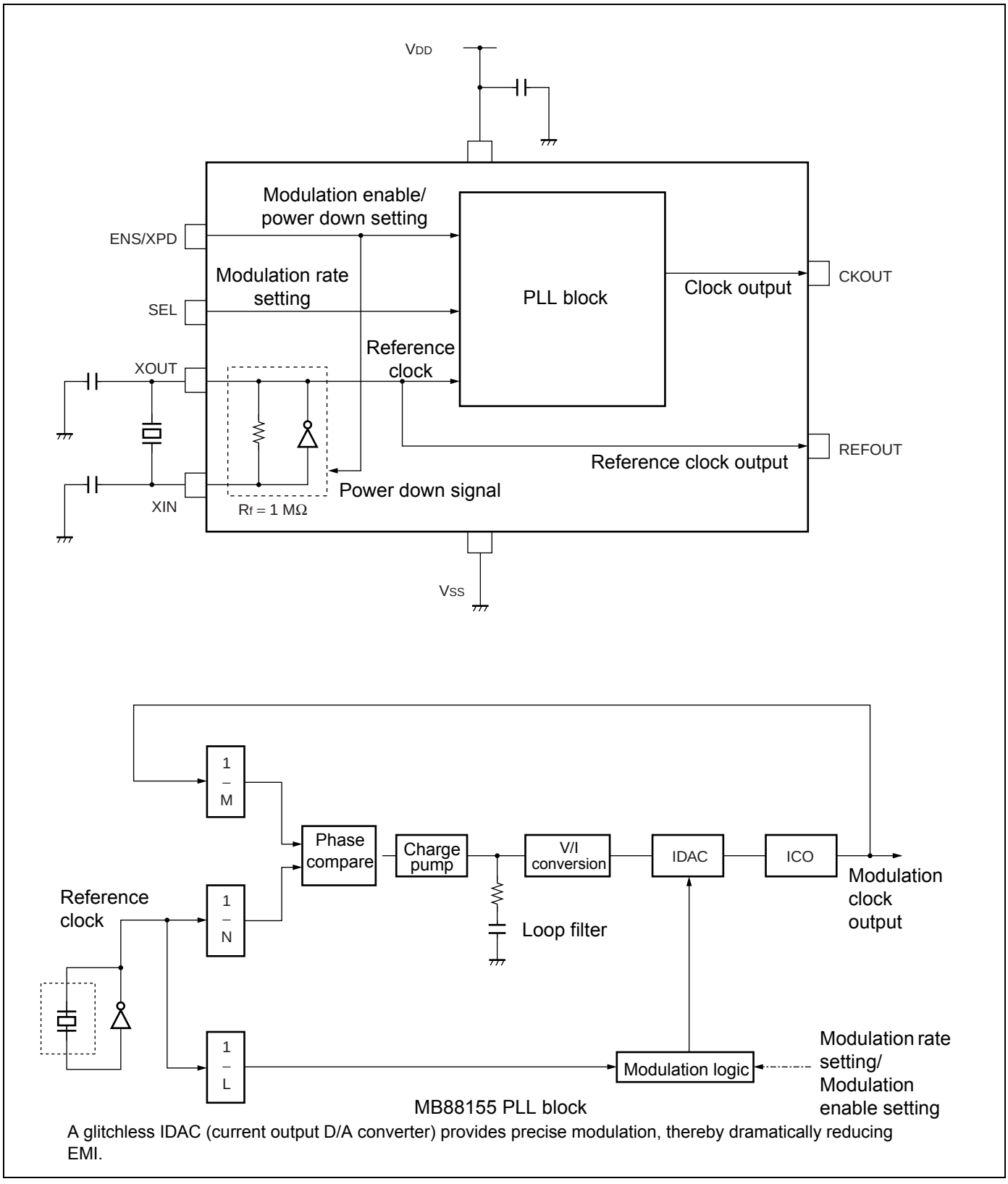
We recommend connecting electrolytic capacitor (about 10 μF) and the ceramic capacitor (about 0.01 μF) in parallel between V_{SS} and V_{DD} near the device, as a bypass capacitor.

5.5 Oscillation Circuit

Noise near the XIN and XOUT pins may cause the device to malfunction. Design printed circuit boards so that electric wiring of XIN or XOUT pin and the resonator do not intersect other wiring.

Design the printed circuit board that surrounds the XIN and XOUT pins with ground.

6. Block Diagram



MB88155 PLL block

A glitchless IDAC (current output D/A converter) provides precise modulation, thereby dramatically reducing EMI.

7. Pin Setting

The modulation clock requires stabilization wait time after the PIN setting is changed. For the modulation clock stabilization wait time, assure the maximum value for “Lock-up time” in the AC Characteristics list in “ Electrical Characteristics”.

ENS Modulation Enable Setting

ENS	Modulation	
L	No modulation	MB88155-xx0, xx1
H	Modulation	

Note : Spectrum does not diffuse when “L” is set to ENS pin.
MB88155-xx2, xx3 do not have ENS pin.

XPD Power Down

XPD	Status	
L	Power down status	MB88155-xx2, xx3
H	Operating status	

Note : When setting “L” to XPD pin, it becomes power down mode (low power consumption mode) .
Both CKOUT and REFOUT of output pins are fixed to “L” output during power down.
MB88155-xx0, xx1 do not have XPD pin.

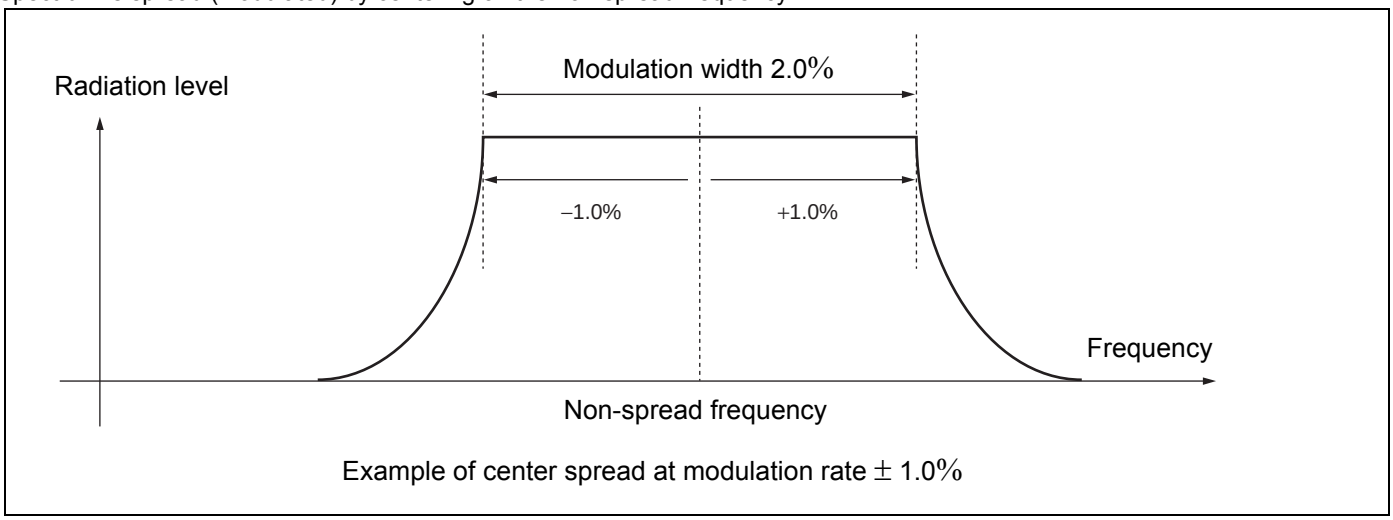
SEL Modulation Rate Setting

SEL	Frequency	
L	± 0.5%	MB88155-x1x
	– 1.0%	MB88155-x0x
H	± 1.0%	MB88155-x1x
	– 2.0%	MB88155-x0x

Note : The modulation rate can be changed at the level of the pin.

■ Center Spread

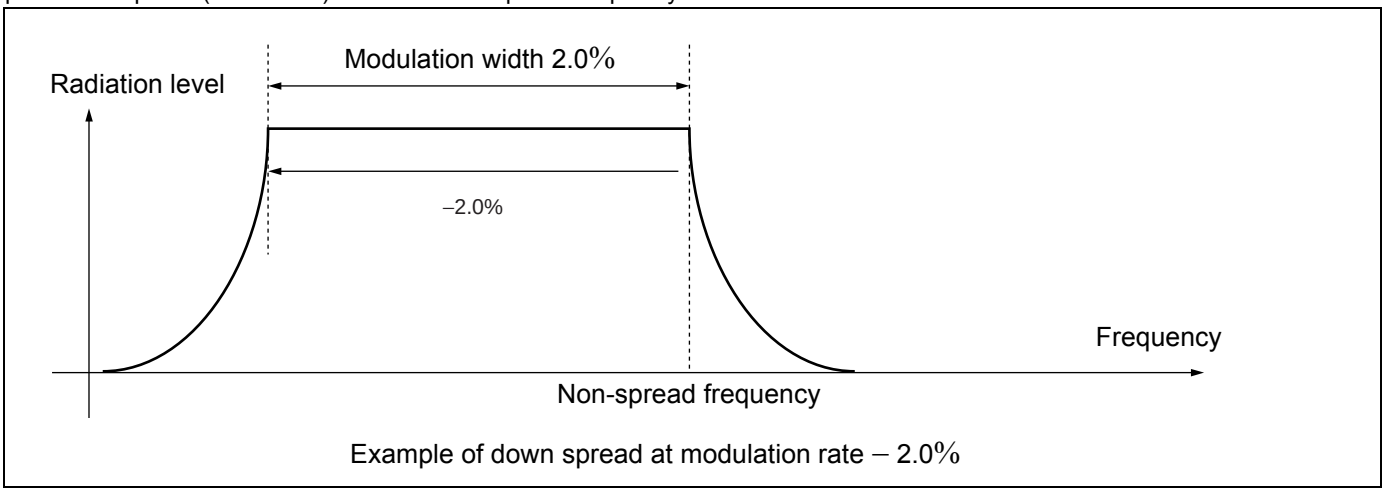
Spectrum is spread (modulated) by centering on the non-spread frequency.



Example of center spread at modulation rate ± 1.0%

■ Down Spread

Spectrum is spread (modulated) below the non-spread frequency.



Example of down spread at modulation rate – 2.0%

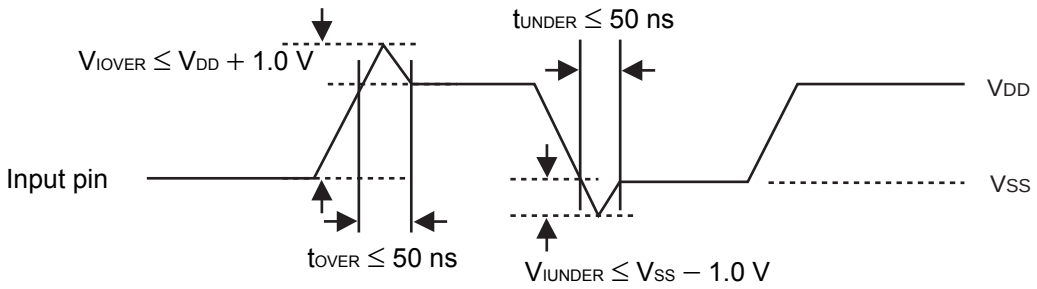
8. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	− 0.5	+ 4.0	V
Input voltage*	V_I	V_{SS} − 0.5	V_{DD} + 0.5	V
Output voltage*	V_O	V_{SS} − 0.5	V_{DD} + 0.5	V
Storage temperature	T_{ST}	− 55	+ 125	°C
Operation junction temperature	T_J	− 40	+ 125	°C
Output current	I_O	− 14	+ 14	mA
Overshoot	V_{IOVER}	—	V_{DD} + 1.0 ($t_{OVER} \leq$ 50 ns)	V
Undershoot	V_{IUNDER}	V_{SS} − 1.0 ($t_{UNDER} \leq$ 50 ns)	—	V

* : The parameter is based on V_{SS} = 0.0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Overshoot/Undershoot



9. Recommended Operating Conditions

(V_{SS} = 0.0 V)

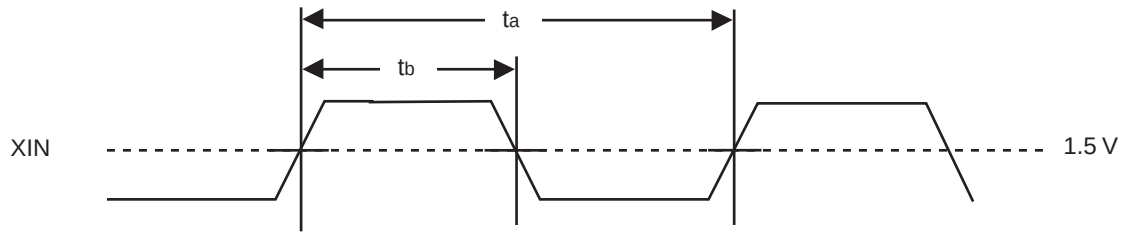
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply voltage	V_{DD}	V_{DD}	—	3.0	3.3	3.6	V
"H" level input voltage	V_{IH}	XIN, SEL, ENS, XPD	—	V_{DD} × 0.8	—	V_{DD} + 0.3	V
"L" level input voltage	V_{IL}	XIN, SEL, ENS, XPD	—	V_{SS}	—	V_{DD} × 0.2	V
Input clock duty cycle	t_{DCI}	XIN	12.5 MHz to 50 MHz	40	50	60	%
Operating temperature	Ta	—	—	− 40	—	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Cypress representatives beforehand.

Input clock duty cycle ($t_{DCI} = t_b/t_a$)



10. Electrical Characteristics

■ DC Characteristics

(Ta = − 40 °C to + 85 °C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply current	I_{CC}	V_{DD}	24 MHz output No load capacitance	—	5.0	7.0	mA
			At power-down	—	10	—	μA
Output voltage	V_{OHC}	CKOUT	"H" level output I_{OH} = − 4 mA	V_{DD} – 0.5	—	V_{DD}	V
	V_{OHR}	REFOUT	"H" level output I_{OH} = − 3 mA				
	V_{OLC}	CKOUT	"L" level output I_{OL} = 4 mA	V_{SS}	—	0.4	V
	V_{OLR}	REFOUT	"L" level output I_{OL} = 3 mA				
Output impedance	Z_{OC}	CKOUT	12.5 MHz to 80 MHz	—	45	—	Ω
	Z_{OR}	REFOUT	12.5 MHz to 50 MHz	—	70	—	
Input capacitance	C_{IN}	XIN, SEL, ENS/XPD	Ta = + 25 °C V_{DD} = V_I = 0.0 V f = 1 MHz	—	—	16	pF
Input pull-up resistor	R_{PU}	ENS	V_{IL} = 0.0 V	25	50	200	kΩ
Load capacitance	C_L	REFOUT	12.5 MHz to 50 MHz	—	—	15	pF
		CKOUT	12.5 MHz to 50 MHz	—	—	15	
			50 MHz to 80 MHz	—	—	7	

■ AC Characteristics

(Ta = − 40 °C to + 85 °C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Oscillation frequency	f_x	XIN, XOUT	Fundamental oscillation	12.5	—	40	MHz
			3rd overtone	40	—	48	
Input frequency	f_{in}	XIN	MB88155 – 1x0, 1x2	12.5	—	25	MHz
			MB88155 – 1x1, 1x3	25	—	50	
			MB88155 – 400	12.5	—	20	
Output frequency	f_{OUT}	REFOUT	MB88155 – 1x0, 1x2	12.5	—	25	MHz
			MB88155 – 1x1, 1x3	25	—	50	
			MB88155 – 400	12.5	—	20	
		CKOUT	MB88155 – 1x0, 1x2	12.5	—	25	
			MB88155 – 1x1, 1x3	25	—	50	
			MB88155 – 400	50	—	80	
Output slew rate	SRc	CKOUT	Load capacitance 15 pF, 0.4 V to 2.4 V	0.4	—	4.0	V/ns
	SR_R	REFOUT	Load capacitance 15 pF, 0.4 V to 2.4 V	0.3	—	2.0	
Output clock duty cycle	t_{DCC}	CKOUT	1.5 V reference level	40	—	60	%
	t_{DCR}	REFOUT	1.5 V reference level	t_{DCI} – 10*1	—	t_{DCI} + 10*1	
Modulation frequency	f_{MOD}	CKOUT	Input frequency at 24 MHz	—	32.4	—	kHz
Lock-up time*2	t_{LK}	CKOUT	—	—	2	5	ms
Cycle-cycle jitter	t_{JC}	CKOUT	MB88155 – 1xx Input frequency 12.5 MHz to 20 MHz, No load capacitance, Ta = + 25 °C, V_{DD} = 3.3 V, Standard deviation σ	—	—	150	ps
			MB88155 – 1xx Input frequency 20 MHz to 50 MHz, No load capacitance, Ta = + 25 °C, V_{DD} = 3.3 V, Standard deviation σ	—	—	100	ps
			MB88155 – 400 No load capacitance, Ta = + 25 °C, V_{DD} = 3.3 V, Standard deviation σ	—	—	200	ps

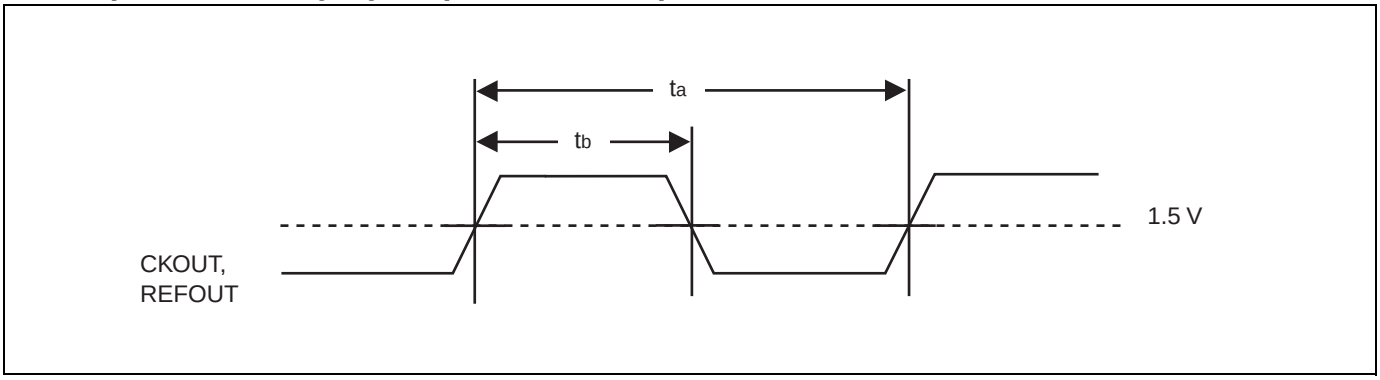
*1 : Duty of the REFOUT output is guaranteed only for the following A and B because it depends on t_{DCI} of input clock duty.

A. Resonator input : When resonator is connected with XIN pin and XOUT pin, and oscillates normally.

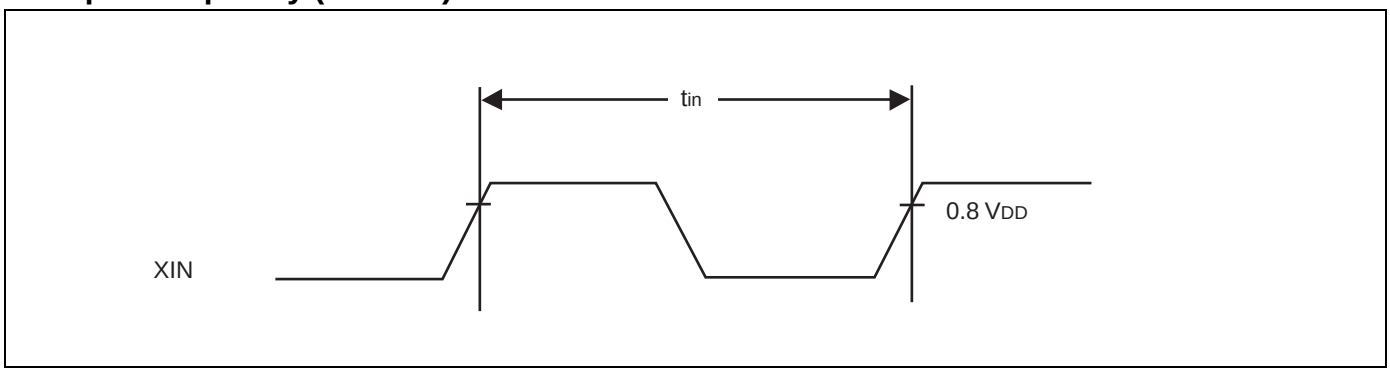
B. External clock input : The input level is Full-swing (V_{SS} – V_{DD}).

*2 : The modulation clock requires stabilization wait time after the IC is turned on or released from power-down mode, or after SEL (modulation factor) or ENS (modulation enable) setting is changed. For the modulation clock stabilization wait time, assure the maximum value for the lock-up time.

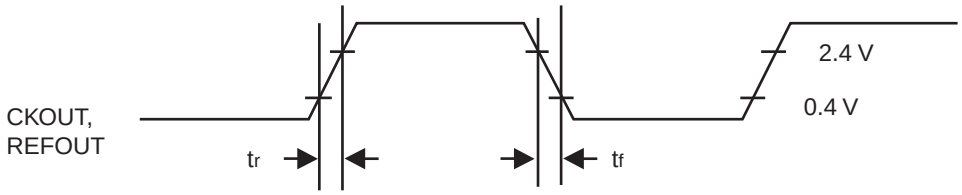
11. Output Clock Duty Cycle (t_{DCC}, $t_{DCR} = t_b/t_a$)



12. Input Frequency ($f_{in} = 1/t_{in}$)

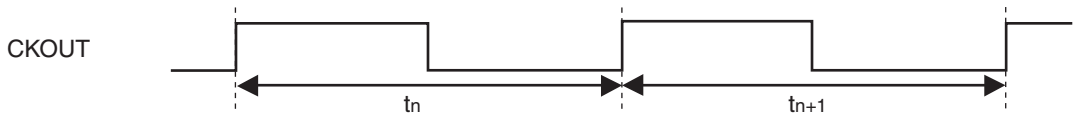


13. Output Slew Rate (SR_C, SR_R)



Note : $SR_C = (2.4 - 0.4)/t_r$, $SR_C = (2.4 - 0.4)/t_f$
$SR_R = (2.4 - 0.4)/t_r$, $SR_R = (2.4 - 0.4)/t_f$

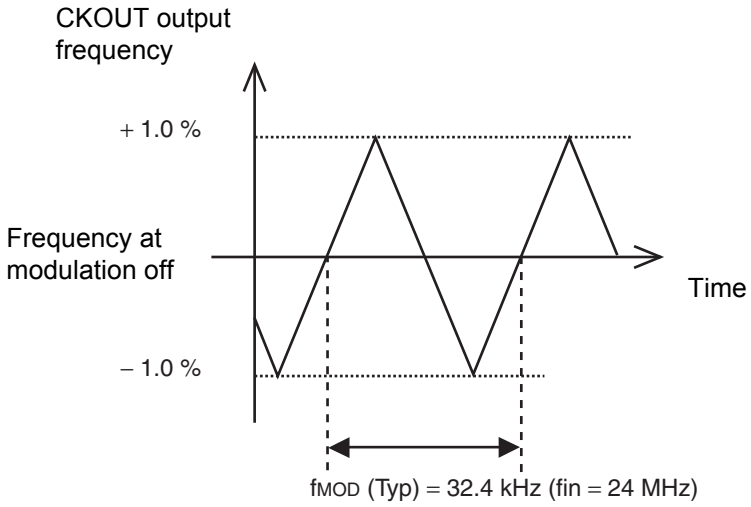
14. Cycle-Cycle Jitter ($t_{JC} = |t_n - t_{n+1}|$)



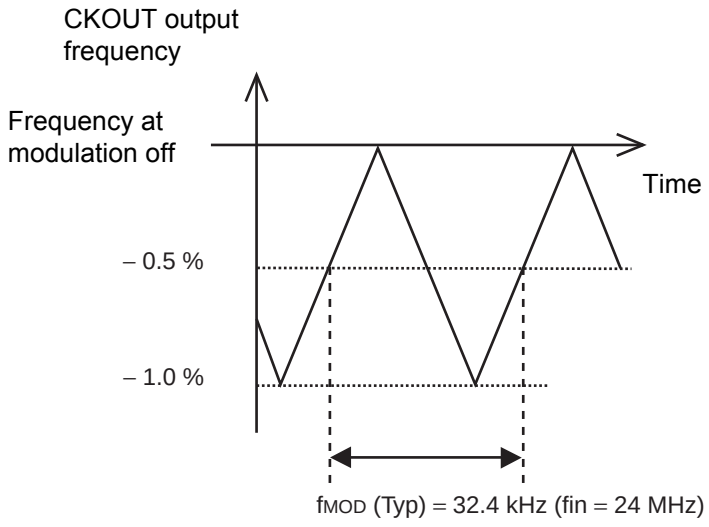
Note : Cycle-cycle jitter indicates the difference between a certain cycle and the immediately succeeding (or preceding) cycle.

15. Modulation Waveform

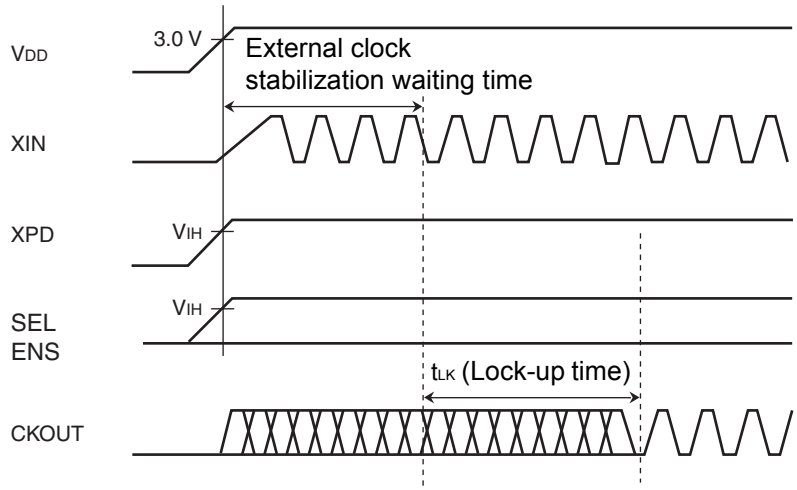
■ Modulation rate ± 1.0%, example of center spread



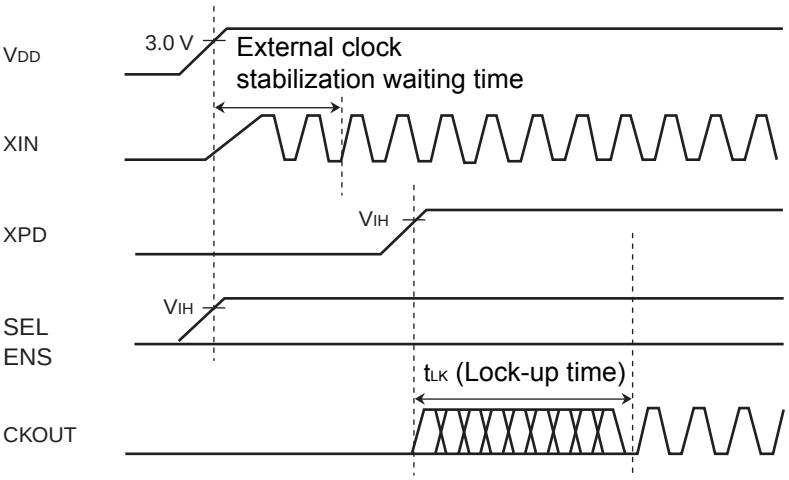
■ Modulation rate − 1.0%, example of down spread



16. Lock-Up Time



If the XPD pin is fixed at the “H” level, the maximum time after the power is turned on until the set clock signal is output from CKOUT pin is (the stabilization wait time of input clock to XIN pin) ＋ (the lock-up time “t_{LK}”). For the input clock stabilization time, check the characteristics of the resonator or oscillator used.



If the XPD pin is used for power-down control, the set clock signal is output from the CKOUT pin at most the lock-up time “t_{LK}” after the XPD pin goes “H” level.

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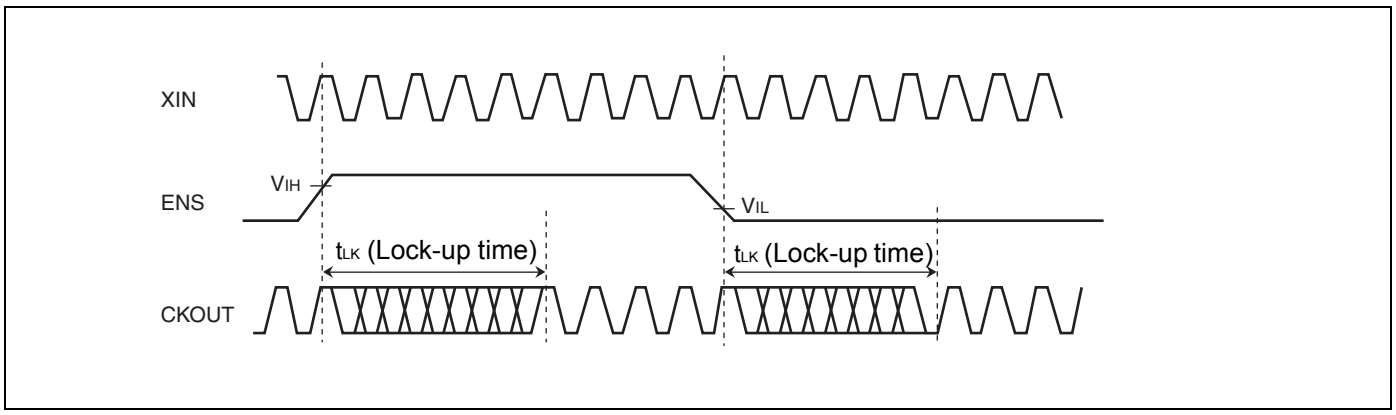


If the ENS pin is used for modulation enable control during normal operation, the set clock signal is output from the CKOUT pin at most the lock-up time "t_{LK}" after the level at the ENS pin is determined.

Note : The wait time for the clock signal output from the CKOUT pin to become stable is required after the IC is released from power-down mode by the XPD pin or after another pin's setting is changed. During the period until the output clock signal becomes stable, neither of the output frequency, output clock duty cycle, modulation period, and cycle-cycle jitter characteristic cannot be guaranteed. It is therefore advisable to take action, such as cancelling a device reset at the stage after the lock-up time has passed.

17. Oscillation Circuit

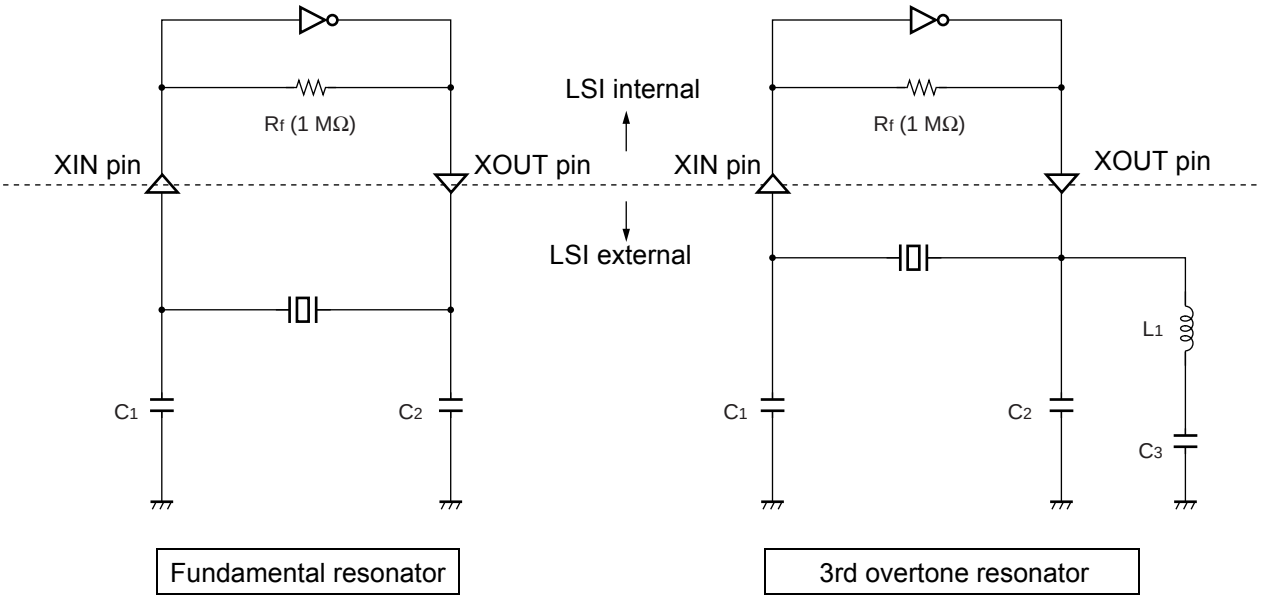
The following schematic on the left-hand side shows a sample connection of a general resonator. The oscillation circuit contains a feedback resistor (1 MΩ) . The values of capacitors (C_1 and C_2) must be adjusted to the optimum constant of the resonator used.

The following schematic on the right-hand side shows a sample connection of a 3rd overtone resonator. The values of capacitors (C_1, C_2, and C_3) and inductor (L_1) must be adjusted to the optimum constant of the resonator used.

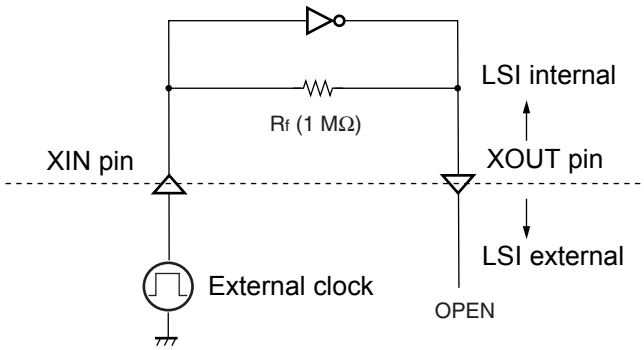
The most suitable value is different by individual resonator. Please refer to the resonator manufacturer which you use for the most suitable value.

To use an external clock signal (without using the resonator) , input the clock signal to the XIN pin with the XOUT pin connected to nothing.

■ When using the resonator

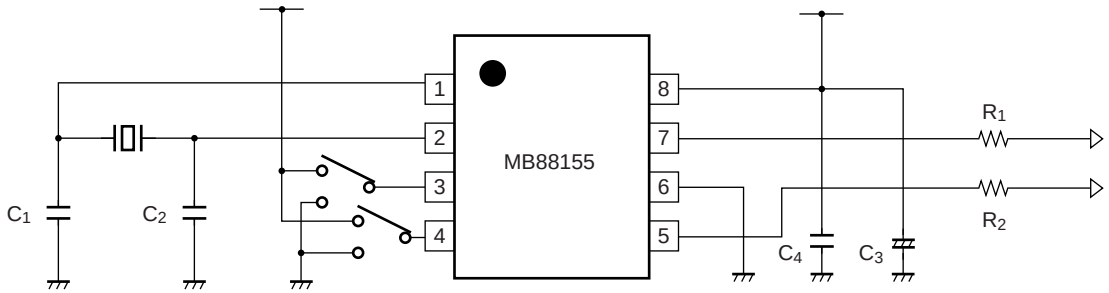


■ When using the external clock



Note : Note that the jitter characteristic of the input clock signal may affect the cycle-cycle jitter characteristic.

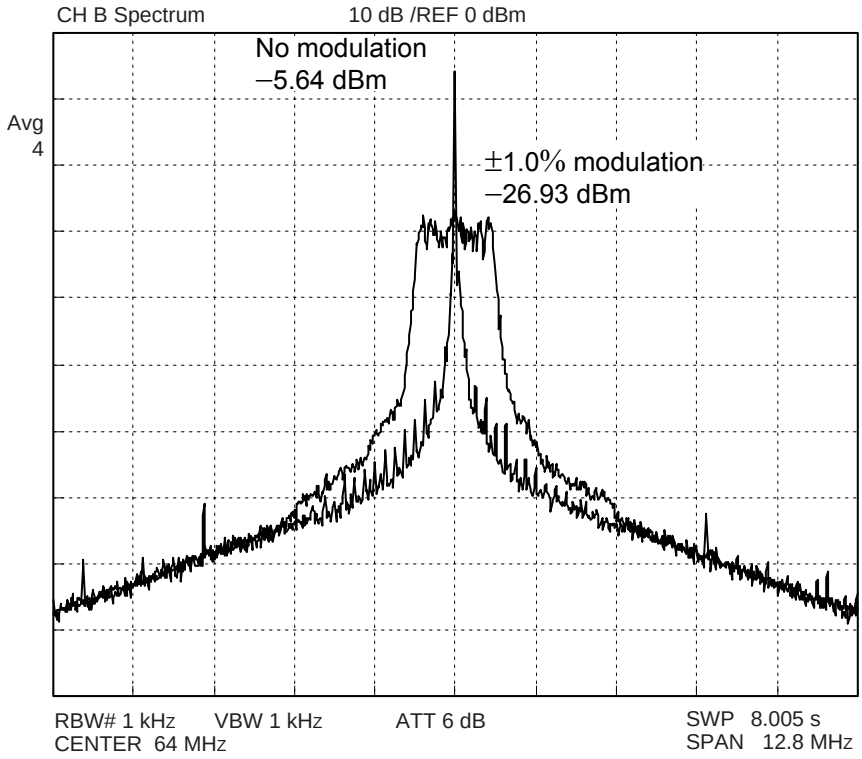
18. Interconnection Circuit Example



C_1, C_2	: Oscillation stabilization capacitance (refer to " Oscillation Circuit")
C_3	: Capacitor of 10 μF or higher
C_4	: Capacitor of about 0.01 μF (connect a capacitor of good high frequency property (ex. laminated ceramic capacitor) to close to this device)
R_1, R_2	: Impedance matching resistor for board pattern

19. Spectrum Example Characteristics

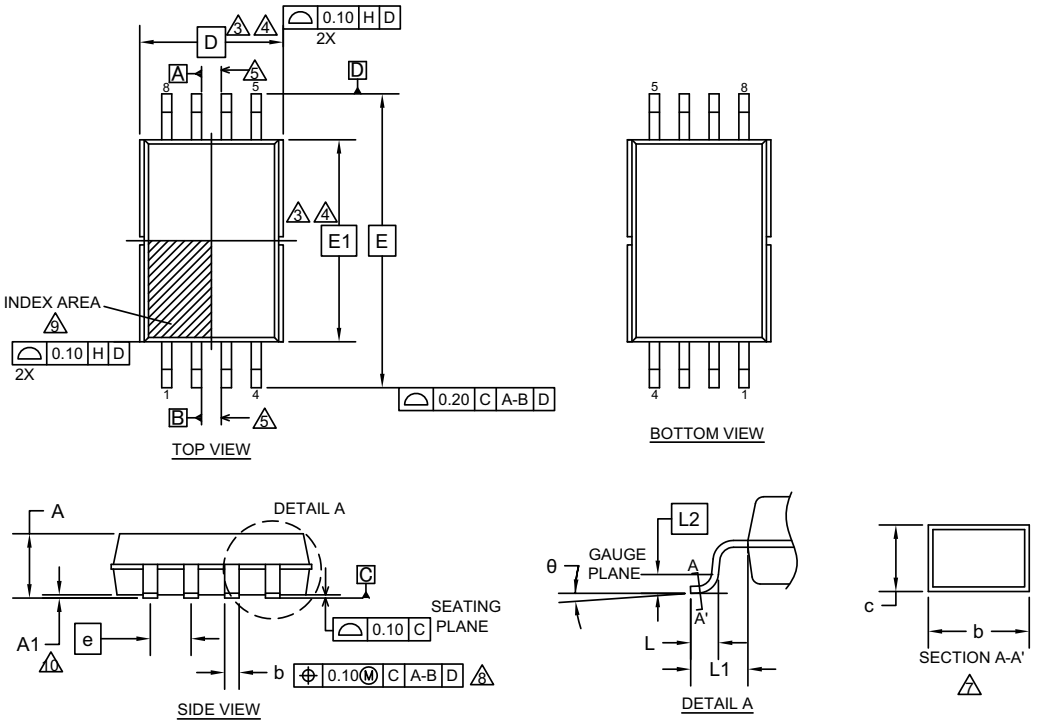
The condition of the examples of the characteristic is shown as follows : Input frequency = 16 MHz (Output frequency = 64 MHz : Using MB88155 (Multiplied by 4))
Power-supply voltage = 3.3 V, None load capacity. Modulation rate = ± 1.0% (center spread).
Spectrum analyzer HP4396B is connected with CKOUT. The result of the measurement with RBW = 1 kHz (ATT use for −6 dB) .



20. Ordering Information

Part Number	Input Frequency	Multiplication Rate	Output Frequency	Modulation Type	Modulation Enable Pin	Power Down Pin	Package	Remarks
MB88155PFT-G-100-JN-EFE1	12.5 MHz to 25 MHz	Multiplied by 1	The same as input frequency	Down spread	Yes	No	8-pin plastic TSSOP (STA008)	Emboss taping (EF type)
MB88155PFT-G-102-JN-EFE1	12.5 MHz to 25 MHz				No	Yes		
MB88155PFT-G-103-JN-EFE1	25 MHz to 50 MHz							
MB88155PFT-G-110-JN-EFE1	12.5 MHz to 25 MHz		The same as input frequency	Center spread	Yes	No		
MB88155PFT-G-111-JN-EFE1	25 MHz to 50 MHz							
MB88155PFT-G-112-JN-EFE1	12.5 MHz to 25 MHz				No	Yes		
MB88155PFT-G-400-JN-EFE1	12.5 MHz to 20 MHz	Multiplied by 4	50 MHz to 80 MHz	Down spread	Yes	No		
MB88155PFT-G-100-JN-ERE1	12.5 MHz to 25 MHz	Multiplied by 1	The same as input frequency	Down spread	Yes	No	8-pin plastic TSSOP (STA008)	Emboss taping (ER type)
MB88155PFT-G-103-JN-ERE1	25 MHz to 50 MHz				No	Yes		
MB88155PFT-G-110-JN-ERE1	12.5 MHz to 25 MHz			Center spread	Yes	No		
MB88155PFT-G-111-JN-ERE1	25 MHz to 50 MHz							
MB88155PFT-G-112-JN-ERE1	12.5 MHz to 25 MHz				No	Yes		
MB88155PFT-G-400-JN-ERE1	12.5 MHz to 20 MHz	Multiplied by 4	50 MHz to 80 MHz	Down spread	Yes	No		

21. Package Dimensions



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	——	——	1.20
A1	0.05	——	0.15
D	3.10 BSC		
E	6.40 BSC		
E1	4.40 BSC		
θ	0°	——	8°
c	0.047	——	0.207
b	0.12	0.22	0.32
L	0.50	0.60	0.70
L 1	1.00 REF		
L 2	0.25 BSC		
e	0.65 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
11. JEDEC SPECIFICATION NO. REF : N/A

002-15912 Rev. **

Document History

Spansion Publication Number: DS04-29119-2Ea

Document Title: MB88155 Spread Spectrum Clock Generator Document Number: 002-08298				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	TAOA	11/09/2006	Initial Release
*A	5568597	TAOA	12/29/2016	Updated to Cypress Template
*B	5998865	TAOA	01/04/2018	Deleated EOL part number: MB88155-101/113/402/410/412 Updated Package Dimensions: Updated to Cypress format Changed the package name from FPT-8P-M07 to STA008

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