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Spread Spectrum Clock Generator

MB88155 is a clock generator for EMI (Electro Magnetic Interference) reduction. The peak of unnecessary radiation noise (EMI) can be attenuated by making the oscillation frequency slightly modulate periodically with the internal modulator. For modulation, the MB88155 supports both center-spreading and down-spreading. It has a non-modulated clock output pin (REFOUT) as well as a modulated clock output pin (CKOUT).

Features

■ Input frequency : 12.5 MHz to 50 MHz (Multiplied by 1)

12.5 MHz to 20 MHz (Multiplied by 4)

■ Output frequency : CKOUT 12.5 MHz to 80 MHz

REFOUT The same as input frequency (not multiplied)

 \blacksquare Modulation rate : \pm 0.5%, $\,\pm$ 1.0% (center spread) , - 1.0%, - 2.0% (Down spread)

■ Equipped with oscillation circuit: range of oscillation 12.5 MHz to 40 MHz (Fundamental oscillation)

40 MHz to 48 MHz (3rd overtone)

■ Modulation clock output Duty: 40% to 60%

■ Modulation clock cycle — cycle jitter: MB88155-1xx 12.5 MHz to 20 MHz less than 150 ps

MB88155-1xx 20 MHz to 50 MHz less than 100 ps MB88155-400 less than 200 ps

■ Low current consumption by CMOS process : 5 mA (24 MHz : Typ-sample, no load)

■ Power supply voltage : 3.3 V ± 0.3 V

■ Operating temperature : -40 °C to +85 °C

■ Package: 8-pin plastic TSSOP



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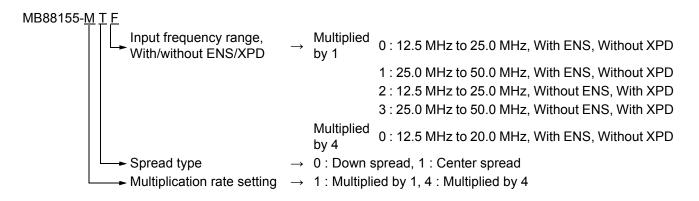
Output Clock Duty Cycle (tDCC, tDCR = tb/ta)	15
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1. Product Lineup

The MB88155 is available in different models: 2 models different in multiplier (\times 1 and \times 4), 2 in modulation type (center-spreading and down-spreading), 2 in input frequency range at a multiplier of 1 (12.5 MHz to 25 MHz and 25 MHz to 50 MHz), and 1 in input frequency range at a multiplier of 4 (12.5 MHz to 20 MHz).

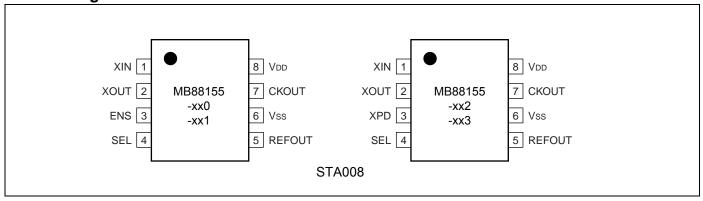
The MB88155 is also available in two versions: modulation-on/off selectable version (with ENS pin) and power-down function built-in version (with XPD pin).



Line-up of MB88155

Product	Input Frequency	Multiplication Rate	Output Frequency	Modulation Type	Modulation Enable pin	Power Down Pin			
MB88155-100	12.5 MHz to 25 MHz			Down	Yes	No			
MB88155-102	12.5 MHz to 25 MHz	Multiplied by 1		spread	No	Yes			
MB88155-103	25 MHz to 50 MHz		Multiplied by 1	Multiplied by 1	Multiplied by 1	The same as			
MB88155-110	12.5 MHz to 25 MHz				input frequency	0 1	Yes	No	
MB88155-111	25 MHz to 50 MHz			Center spread					
MB88155-112	12.5 MHz to 25 MHz			·	No	Yes			
MB88155-400	12.5 MHz to 20 MHz	Multiplied by 4	50 MHz to 80 MHz	Down spread	Yes	No			

2. Pin Assignment



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3. Pin Description

Pin Name	I/O	Pin No.	Description
XIN	I	1	Connection pin of resonator/clock input pin
XOUT	0	2	Connection pin of resonator
ENS/XPD	I	3	Modulation enable pin/power down pin
SEL	I	4	Modulation rate setting pin Down spread, SEL = "L" : Modulation rate -1.0% Down spread, SEL = "H" : Modulation rate -2.0% Down spread, SEL = "L" : Modulation rate $\pm 0.5\%$ Down spread, SEL = "H" : Modulation rate $\pm 1.0\%$
REFOUT	0	5	Non-modulated clock output pin This pin becomes to "L" at power-down.
Vss	_	6	GND Pin
CKOUT	0	7	Modulated clock output pin This pin becomes to "L" at power-down.
V _{DD}	_	8	Power supply voltage pin



4. I/O Circuit Type

Pin	Circuit Type	Remarks
SEL, XPD		CMOS hysteresis input
ENS	50 kΩ Solve Solv	CMOS hysteresis input with pull-up resistor of 50 k Ω (Typ)
REFOUT		 ■ CMOS output ■ IoL = 3 mA ■ "L" output at power-down

(Continued)



(Continued)

Pin	Circuit Type	Remarks
		■ CMOS output
	-	■ IoL = 4 mA
		■ "L" output at power-down
СКОПТ		

Note: For XIN pin and XOUT pin, refer to "Oscillation Circuit".



5. Handling Devices

5.1 Preventing Latch-up

A latch-up can occur if, on this device, (a) a voltage higher than V_{DD} or a voltage lower than V_{SS} is applied to an input or output pin or (b) a voltage higher than the rating is applied between V_{DD} and V_{SS} . The latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use this device, be very careful not to exceed the maximum rating.

5.2 Handling Unused Pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, using a pull-up or pull-down resistor. Unused output pin should be opened.

5.3 The Attention when the External Clock is Used

Input the clock to XIN pin, and XOUT pin should be opened when you use the external clock. Please pay attention so that an overshoot and an undershoot do not occur to an input clock of XIN pin.

5.4 Power Supply Pins

Please design connecting the power supply pin of this device by as low impedance as possible from the current supply source.

We recommend connecting electrolytic capacitor (about 10 μ F) and the ceramic capacitor (about 0.01 μ F) in parallel between Vss and V_{DD} near the device, as a bypass capacitor.

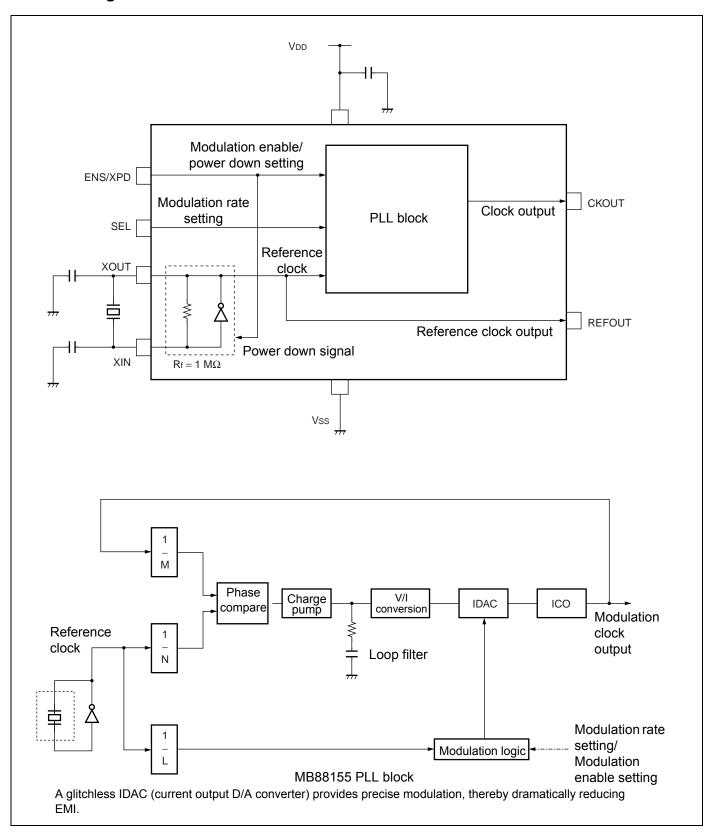
5.5 Oscillation Circuit

Noise near the XIN and XOUT pins may cause the device to malfunction. Design printed circuit boards so that electric wiring of XIN or XOUT pin and the resonator do not intersect other wiring.

Design the printed circuit board that surrounds the XIN and XOUT pins with ground.



6. Block Diagram





7. Pin Setting

The modulation clock requires stabilization wait time after the PIN setting is changed. For the modulation clock stabilization wait time, assure the maximum value for "Lock-up time" in the AC Characteristics list in "Electrical Characteristics".

ENS Modulation Enable Setting

ENS	Modulation				
L	No modulation	MB88155-xx0, xx1			
Н	Modulation	1VID00 133-XXU, XX 1			

Note: Spectrum does not diffuse when "L" is set to ENS pin.

MB88155-xx2, xx3 do not have ENS pin.

XPD Power Down

XPD	Status				
L	Power down status	MB88155-xx2, xx3			
Н	Operating status	IVID00133-XX2, XX3			

Note: When setting "L" to XPD pin, it becomes power down mode (low power consumption mode).

Both CKOUT and REFOUT of output pins are fixed to "L" output during power down.

MB88155-xx0, xx1 do not have XPD pin.

SEL Modulation Rate Setting

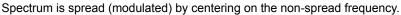
SEL	Frequency				
L	± 0.5%	MB88155-x1x			
	- 1.0%	MB88155-x0x			
Н	± 1.0%	MB88155-x1x			
	- 2.0%	MB88155-x0x			

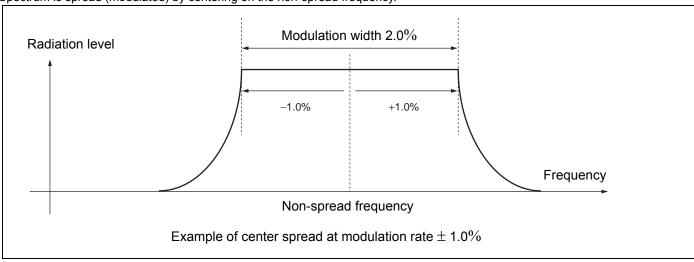
Note: The modulation rate can be changed at the level of the pin.

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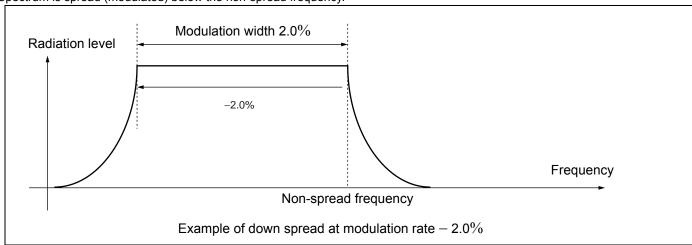
■ Center Spread





■ Down Spread

Spectrum is spread (modulated) below the non-spread frequency.



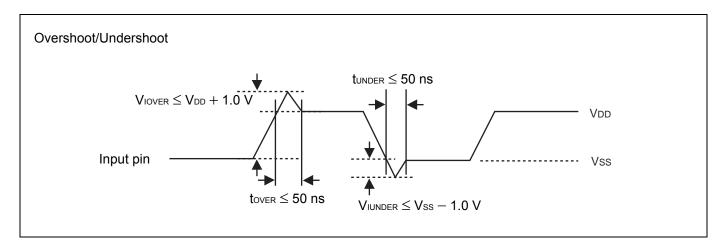


8. Absolute Maximum Ratings

Parameter	Symbol	Rat	ing	Unit	
raiailletei	Symbol	Min	Max	Oilit	
Power supply voltage*	V _{DD}	- 0.5	+ 4.0	V	
Input voltage*	Vı	Vss - 0.5	V _{DD} + 0.5	V	
Output voltage*	Vo	Vss - 0.5	V _{DD} + 0.5	V	
Storage temperature	Тѕт	– 55	+ 125	°C	
Operation junction temperature	TJ	- 40	+ 125	°C	
Output current	lo	- 14	+ 14	mA	
Overshoot	VIOVER	_	$V_{DD} + 1.0 \text{ (tover} \leq 50 \text{ ns)}$	V	
Undershoot	Viunder	$V_{SS} - 1.0 \text{ (tunder} \leq 50 \text{ ns)}$	_	V	

 $^{^{\}star}$: The parameter is based on Vss = 0.0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.





9. Recommended Operating Conditions

(Vss = 0.0 V)

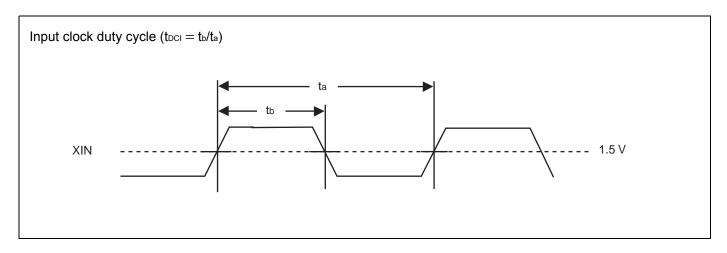
Parameter	Symbol	Pin	Conditions		Value		Unit
	Symbol	FIII	Conditions	Min	Тур	Max	Offic
Power supply voltage	V _{DD}	V _{DD}	_	3.0	3.3	3.6	V
"H" level input voltage	Vін	XIN, SEL, ENS, XPD	_	V _{DD} × 0.8	_	V _{DD} + 0.3	V
"L" level input voltage	VIL	XIN, SEL, ENS, XPD	_	Vss	_	V _{DD} × 0.2	V
Input clock duty cycle	t DCI	XIN	12.5 MHz to 50 MHz	40	50	60	%
Operating temperature	Та	_	_	- 40	_	+ 85	°C

WARNING:

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Cypress representatives beforehand.





10. Electrical Characteristics

■ DC Characteristics

(Ta = -40 °C to +85 °C, V_{DD} = 3.3 V \pm 0.3 V, V_{SS} = 0.0 V)

Daramatar	Cumbal	Pin	Conditions		Value		Unit
Parameter	Symbol	Pin	Conditions	Min	Тур	Max	Unit
Power supply current	Icc	V _{DD}	24 MHz output No load capacitance	_	5.0	7.0	mA
			At power-down	_	10	_	μА
	Vонс	CKOUT	"H" level output Іон = - 4 mA	V _{DD} - 0.5	_	V _{DD}	V
Output voltage	Vohr	REFOUT	"H" level output Іон = - 3 mA				
	Volc	CKOUT	"L" level output IoL = 4 mA	Vss	_	0.4	V
	Volr	REFOUT	"L" level output IoL = 3 mA				
Output impedance	Zoc	CKOUT	12.5 MHz to 80 MHz	_	45	_	Ω
Output impedance	Zor	REFOUT	12.5 MHz to 50 MHz	_	70	_	
Input capacitance	Cin	XIN, SEL, ENS/XPD	$Ta = +25 ^{\circ}C$ $V_{DD} = V_{I} = 0.0 V$ $f = 1 MHz$	_	_	16	pF
Input pull-up resistor	Rpu	ENS	V _{IL} = 0.0 V	25	50	200	kΩ
Load capacitance		REFOUT	12.5 MHz to 50 MHz	_	_	15	pF
	CL	СКОИТ	12.5 MHz to 50 MHz	_	_	15	1
		CROUT	50 MHz to 80 MHz	_		7	



■ AC Characteristics

(Ta = -40 °C to +85 °C, V_{DD} = 3.3 V \pm 0.3 V, V_{SS} = 0.0 V)

Doromotor	Symbol	Pin	Conditions		11::4		
Parameter			Conditions	Min	Тур Мах		Unit
Oscillation	r	XIN,	Fundamental oscillation	12.5	_	40	MHz
frequency	fx	XOUT	3 rd overtone	40		48	
Input frequency	fin	XIN	MB88155 – 1x0, 1x2	12.5		25	MHz
			MB88155 – 1x1, 1x3	25		50	
			MB88155 – 400	12.5	_	20	
		REFOUT	MB88155 – 1x0, 1x2	12.5	_	25	MHz
			MB88155 – 1x1, 1x3 25 —		50		
Output fragues			MB88155 – 400	12.5	_	20	=
Output frequency	fоит	СКОПТ	MB88155 – 1x0, 1x2	12.5	_	25	
			MB88155 – 1x1, 1x3	25		50	
			MB88155 – 400	50		80	1
Output slew rate	SRc	CKOUT	Load capacitance 15 pF, 0.4 V to 2.4 V	0.4	_	4.0	V/ns
	SRR	REFOUT	Load capacitance 15 pF, 0.4 V to 2.4 V	0.3	_	2.0	
Output clock	t DCC	CKOUT	1.5 V reference level	40	_	60	%
duty cycle	t DCR	REFOUT	1.5 V reference level	t _{DCI} - 10*1	_	t _{DCI} + 10*1	
Modulation frequency	fмор	CKOUT	Input frequency at 24 MHz	_	32.4	_	kHz
Lock-up time*2	t LK	CKOUT	_	_	2	5	ms
			MB88155 – 1xx Input frequency 12.5 MHz to 20 MHz, No load capacitance, Ta = $+25$ °C, $V_{DD} = 3.3$ V, Standard deviation σ		_	150	ps
Cycle-cycle jitter	tuc	CKOUT	MB88155 – 1xx Input frequency 20 MHz to 50 MHz, No load capacitance, Ta = $+25$ °C, V _{DD} = 3.3 V, Standard deviation σ	_	_	100	ps
			$\label{eq:mb88155} \begin{array}{l} \mbox{MB88155} - 400 \\ \mbox{No load capacitance,} \\ \mbox{Ta} = +25 \ ^{\circ}\mbox{C}, \mbox{V}_{\mbox{DD}} = 3.3 \mbox{ V}, \mbox{Standard deviation } \sigma \end{array}$	_	_	200	ps

^{*1:} Duty of the REFOUT output is guaranteed only for the following A and B because it depends on tool of input clock duty.

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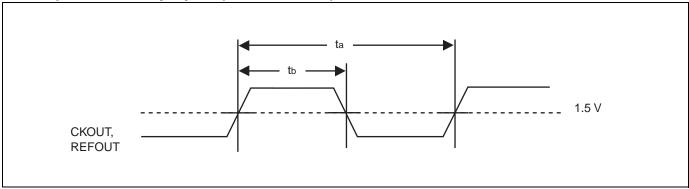
A. Resonator input: When resonator is connected with XIN pin and XOUT pin, and oscillates normally.

B. External clock input: The input level is Full-swing (Vss - VDD).

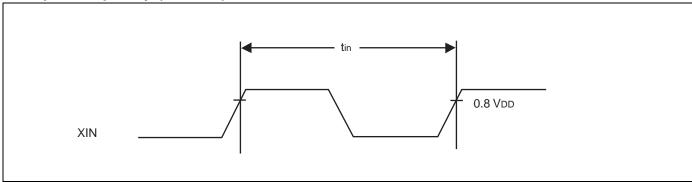
^{*2:} The modulation clock requires stabilization wait time after the IC is turned on or released from power-down mode, or after SEL (modulation factor) or ENS (modulation enable) setting is changed. For the modulation clock stabilization wait time, assure the maximum value for the lock-up time.



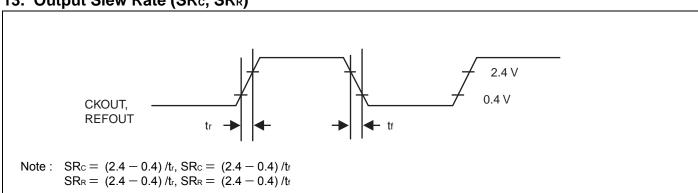
11. Output Clock Duty Cycle (tDCC, tDCR = tb/ta)



12. Input Frequency ($f_{in} = 1/t_{in}$)

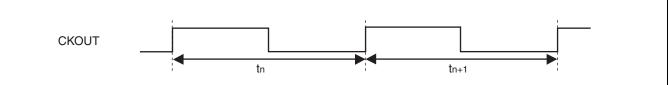


13. Output Slew Rate (SRc, SRR)





14. Cycle-Cycle Jitter ($t_{JC} = |t_n - t_n + 1|$)

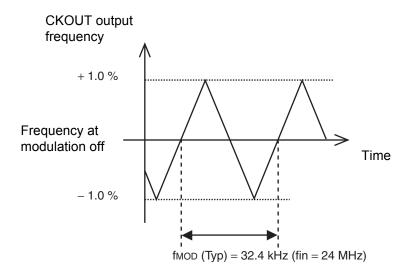


Note: Cycle-cycle jitter indicates the difference between a certain cycle and the immediately succeeding (or preceding) cycle.

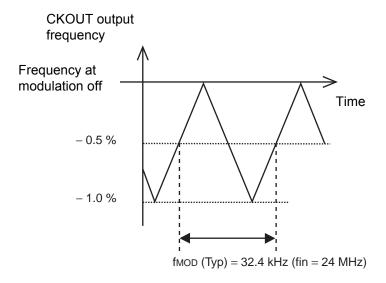


15. Modulation Waveform

■ Modulation rate \pm 1.0%, example of center spread

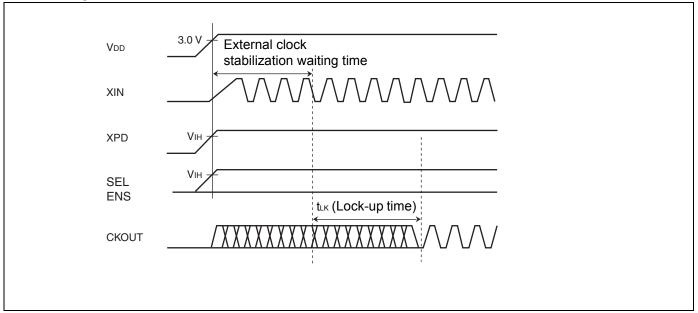


■ Modulation rate - 1.0%, example of down spread

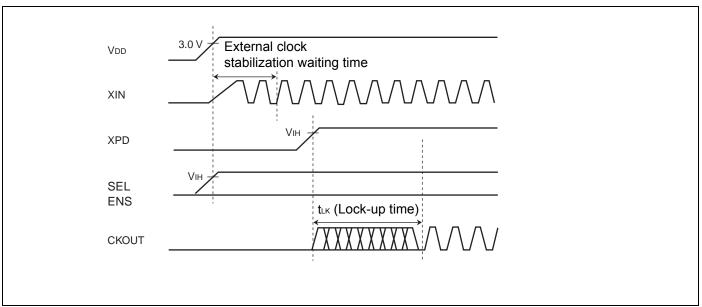




16. Lock-Up Time



If the XPD pin is fixed at the "H" level, the maximum time after the power is turned on until the set clock signal is output from CKOUT pin is (the stabilization wait time of input clock to XIN pin) + (the lock-up time "tlk"). For the input clock stabilization time, check the characteristics of the resonator or oscillator used.

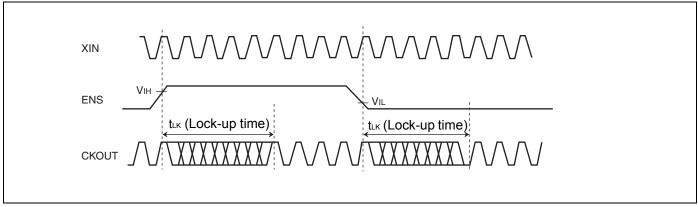


If the XPD pin is used for power-down control, the set clock signal is output from the CKOUT pin at most the lock-up time "tlk" after the XPD pin goes "H" level.

(Continued)



(Continued)



If the ENS pin is used for modulation enable control during normal operation, the set clock signal is output from the CKOUT pin at most the lock-up time "t_k" after the level at the ENS pin is determined.

Note: The wait time for the clock signal output from the CKOUT pin to become stable is required after the IC is released from power-down mode by the XPD pin or after another pin's setting is changed. During the period until the output clock signal becomes stable, neither of the output frequency, output clock duty cycle, modulation period, and cycle-cycle jitter characteristic cannot be guaranteed. It is therefore advisable to take action, such as cancelling a device reset at the stage after the lock-up time has passed.



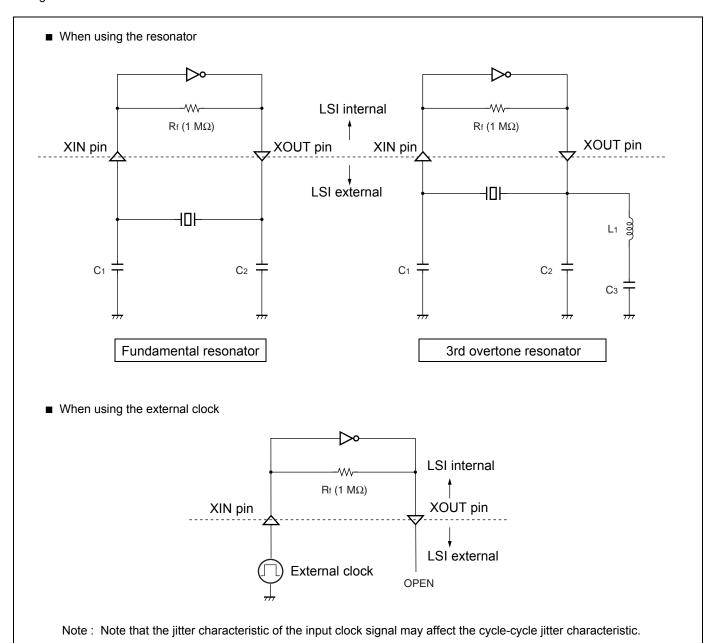
17. Oscillation Circuit

The following schematic on the left-hand side shows a sample connection of a general resonator. The oscillation circuit contains a feedback resistor (1 $M\Omega$). The values of capacitors (C₁ and C₂) must be adjusted to the optimum constant of the resonator used.

The following schematic on the right-hand side shows a sample connection of a 3rd overtone resonator. The values of capacitors (C_1 , C_2 , and C_3) and inductor (L_1) must be adjusted to the optimum constant of the resonator used.

The most suitable value is different by individual resonator. Please refer to the resonator manufacturer which you use for the most suitable value.

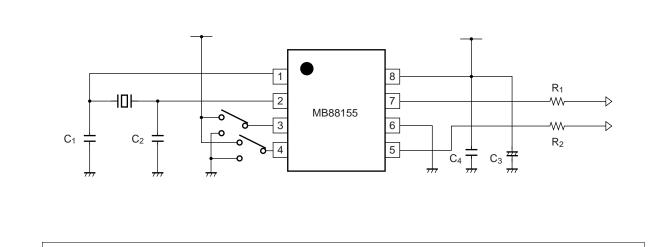
To use an external clock signal (without using the resonator), input the clock signal to the XIN pin with the XOUT pin connected to nothing.



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18. Interconnection Circuit Example



C₁, C₂ : Oscillation stabilization capacitance (refer to "Oscillation Circuit")

 C_3 : Capacitor of 10 μF or higher

 C_4 : Capacitor of about 0.01 μF (connect a capacitor of good high frequency property

(ex. laminated ceramic capacitor) to close to this device)

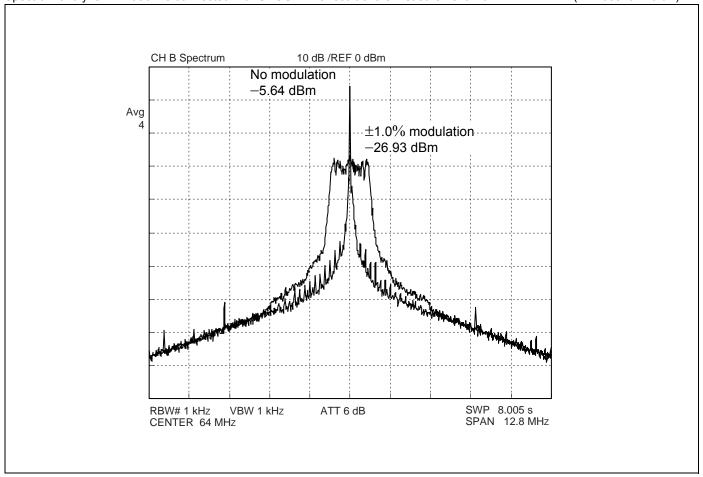
R₁, R₂ : Impedance matching resistor for board pattern



19. Spectrum Example Characteristics

The condition of the examples of the characteristic is shown as follows: Input frequency = 16 MHz (Output frequency = 64 MHz: Using MB88155 (Multiplied by 4))

Power-supply voltage = 3.3 V, None load capacity. Modulation rate = $\pm 1.0\%$ (center spread). Spectrum analyzer HP4396B is connected with CKOUT. The result of the measurement with RBW = 1 kHz (ATT use for -6 dB) .



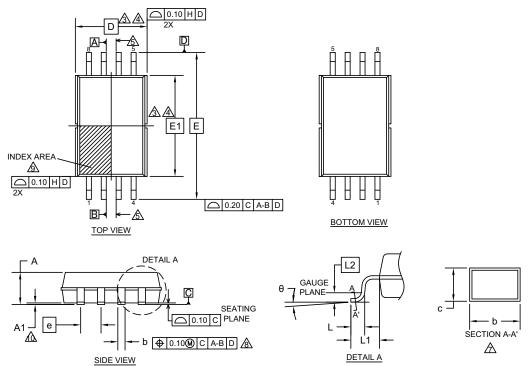


20. Ordering Information

Part Number	Input Frequency	Multiplica- tion Rate	Output Frequency	Modulation Type	Modulation Enable Pin	Power Down Pin	Package	Remarks	
MB88155PFT-G- 100-JN-EFE1	12.5 MHz to 25 MHz	Multiplied by 1	The same as input fre- quency		Yes	No			
MB88155PFT-G- 102-JN-EFE1	12.5 MHz to 25 MHz			as input fre- Down	Down spread	No	Yes		
MB88155PFT-G- 103-JN-EFE1	25 MHz to 50 MHz					res	8-pin plastic TSSOP (STA008)	Emboss taping (EF type)	
MB88155PFT-G- 110-JN-EFE1	12.5 MHz to 25 MHz		The same as input fre- quency		Yes	No			
MB88155PFT-G- 111-JN-EFE1	25 MHz to 50 MHz			as input fre-	Center spread	res	NO	(31A000)	(Er type)
MB88155PFT-G- 112-JN-EFE1	12.5 MHz to 25 MHz				No	Yes			
MB88155PFT-G- 400-JN-EFE1	12.5 MHz to 20 MHz	Multiplied by 4	50 MHz to 80 MHz	Down spread	Yes	No			
MB88155PFT-G- 100-JN-ERE1	12.5 MHz to 25 MHz	-	ed The same as input frequency	Down	Yes	No			
MB88155PFT-G- 103-JN-ERE1	25 MHz to 50 MHz			T1	spread	No	Yes		
MB88155PFT-G- 110-JN-ERE1	12.5 MHz to 25 MHz	Multiplied by 1		as input frequency		Yes	es No	8-pin plastic TSSOP	Emboss
MB88155PFT-G- 111-JN-ERE1	25 MHz to 50 MHz				queriey	Center spread	res	NO	(STA008)
MB88155PFT-G- 112-JN-ERE1	12.5 MHz to 25 MHz				No	Yes			
MB88155PFT-G- 400-JN-ERE1	12.5 MHz to 20 MHz	Multiplied by 4	50 MHz to 80 MHz	Down spread	Yes	No			



21. Package Dimensions



SYMBOL	DIMENSION				
STIVIBOL	MIN. NOM.		MAX.		
Α			1.20		
A1	0.05		0.15		
D	3.10 BSC				
E	6.40 BSC				
E1	4.40 BSC				
θ	0°	_	8°		
С	0.047	—	0.207		
b	0.12	0.22	0.32		
L	0.50	0.60	0.70		
L 1	1.00 REF		=		
L 2	(0.25 BSC			
е	0.65 BSC				

NOTES

- 1. ALL DIMENSIONS ARE IN MILLIMETER.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- ⚠ DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM.

 DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST

 EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH,

 THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING

 ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- ⚠ DATUMS A & B TO BE DETERMINED AT DATUM H.
- 6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
- ⚠ THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
- ⚠ DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
 - THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
- ⚠ THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
- "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO
 THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR
 THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
- 11. JEDEC SPECIFICATION NO. REF: N/A

002-15912 Rev. **



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