

HOTLink II™ SMPTE Receiver Training Clock

Features

- Integrated phase-locked loop
- Low-jitter, high-accuracy outputs
- 3.3V operation

Benefits

- Internal PLL with up to 400-MHz internal operation
- Meets critical timing requirements in complex system designs
- Enables application compatibility

Table 1. Frequency table

Part Number	Outputs	Input Frequency	Output Frequency Range
CY24130-1	2	27 MHz (Driven Reference)	1 copy 27-MHz reference clock output 1 copy of 27-/36-/54-/148.5-/74.25-MHz (frequency selectable)
CY24130-2	2	27 MHz (Crystal Reference)	1 copy 27-MHz reference clock output 1 copy of 27-/36-/54-/148.5-/74.25-MHz (frequency selectable)

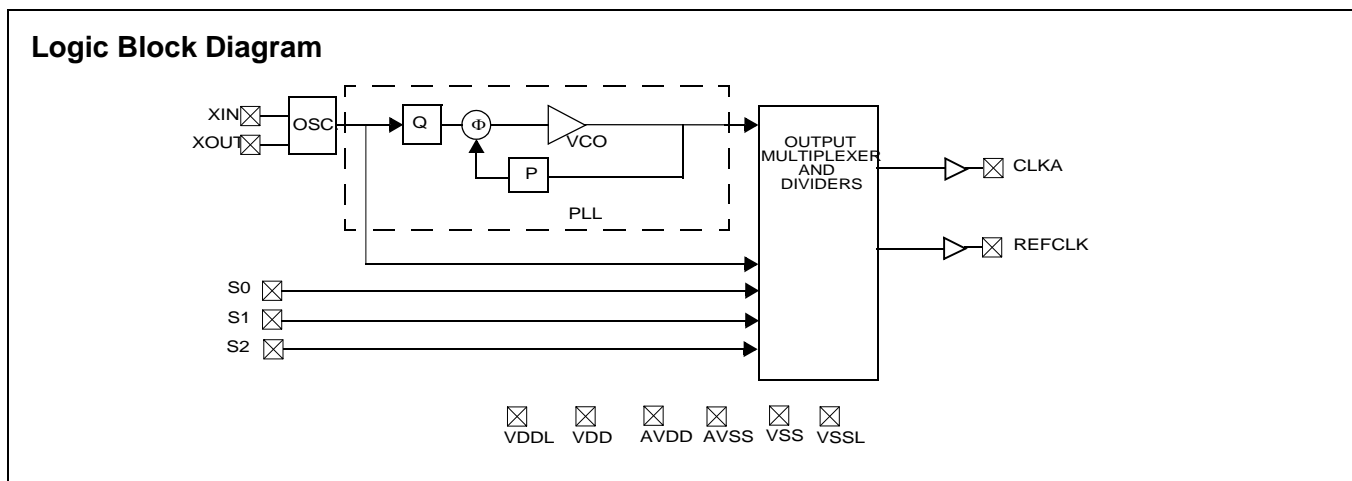
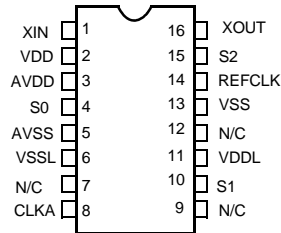


Table 2. Frequency Select Options

S2	S1	S0	CLKA	REFCLK	Units
0	0	0	27	27	MHz
0	0	1	36	27	MHz
0	1	0	54	27	MHz
0	1	1	148.50	27	MHz
1	0	0	74.25	27	MHz
1	0	1	OFF, pulled low	27	MHz
1	1	0	OFF, pulled low	27	MHz
1	1	1	OFF, pulled low	27	MHz

Pin Configuration

Figure 1. CY24130-1, -2, 16-pin TSSOP

Table 3. Pin Definition

Name	Pin Number	Description
XIN	1	Reference Crystal Input.
V _{DD}	2	Voltage Supply.
AV _{DD}	3	Analog Voltage Supply.
S0	4	Frequency Select 0.
AV _{SS}	5	Analog Ground.
V _{SSL}	6	VDDL Ground.
N/C	7	No Connect.
CLKA	8	27-/36-/54-/148.50-/74.25-MHz Clock Output (frequency selectable).
N/C	9	No Connect.
S1	10	Frequency Select 1.
V _{DDL}	11	Voltage Supply.
N/C	12	No Connect.
VSS	13	Ground.
REFCLK	14	Reference Clock Output.
S2	15	Frequency Select 2.
XOUT	16	Reference Crystal Output. Leave floating for -1.

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V _{DD} , AV _{DD}	Supply Voltage	-0.5	7.0	V
V _{DDL}	I/O Supply Voltage	-	7.0	V
T _J	Junction Temperature	-	125	°C
	Digital Inputs	AV _{SS} - 0.3	AV _{DD} + 0.3	V
	Electro-Static Discharge	2	-	kV

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V _{DD} /AV _{DDL} /V _{DDL}	Operating Voltage	3.135	3.3	3.465	V
T _A	Ambient Temperature	0	-	70	°C
C _{LOAD}	Max. Load Capacitance	-	-	15	pF
f _{REF}	Reference Frequency	-	27	-	MHz
C _{LNOM}	Nominal Parallel Crystal Load Capacitance for -2	-	18	-	pF

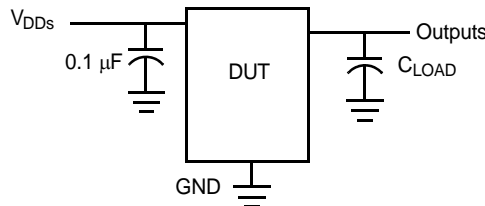
DC Electrical Specifications

Parameter ^[1]	Name	Description	Min.	Typ.	Max.	Unit
I _{OH}	Output High Current	V _{OH} = V _{DD} - 0.5, V _{DD} /V _{DDL} = 3.3V	12	24	-	mA
I _{OL}	Output Low Current	V _{OL} = 0.5, V _{DD} /V _{DDL} = 3.3V	12	24	-	mA
I _{IH}	Input High Current	V _{IH} = V _{DD}	-	5	10	μA
I _{IL}	Input Low Current	V _{IL} = 0V	-	-	10	μA
V _{IH}	Input High Voltage	CMOS levels, 70% of V _{DD}	0.7	-	-	V
V _{IL}	Input Low Voltage	CMOS levels, 30% of V _{DD}	-	-	0.3	V
I _{VDD}	Supply Current	AV _{DD} /V _{DD} Current	-	16	-	mA
I _{VDDL}	Supply Current	V _{DDL} Current	-	14	-	mA

AC Electrical Specifications

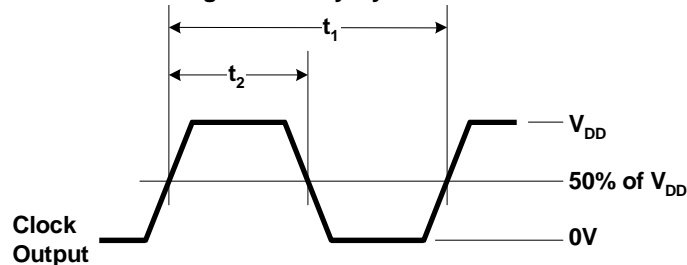
Parameter ^[1]	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in Figure 3; t ₁ /t ₂ , 50% of V _{DD}	45	50	55	%
ER	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V _{DD} , C _{LOAD} = 15 pF. See Figure 4.	0.8	1.4	-	V/ns
EF	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V _{DD} , C _{LOAD} = 15 pF. See Figure 4.	0.8	1.4	-	V/ns
t _g	Clock Jitter	CLKA Peak-Peak Period Jitter	-	100	-	ps
t ₁₀	PLL Lock Time		-	-	3	ms

Figure 2. Test and Measurement Setup



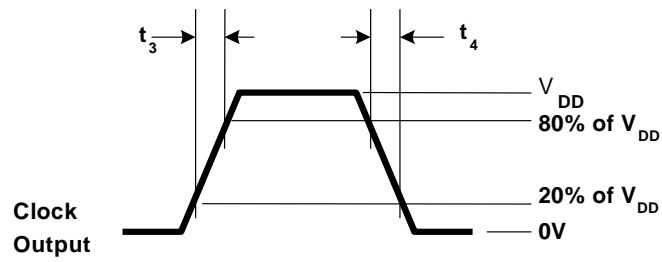
Voltage and Timing Definitions

Figure 3. Duty Cycle Definitions



Note
1. Not 100% tested.

Figure 4. $ER = (0.6 \times V_{DD}) / t_3$, $EF = (0.6 \times V_{DD}) / t_4$



Ordering Information

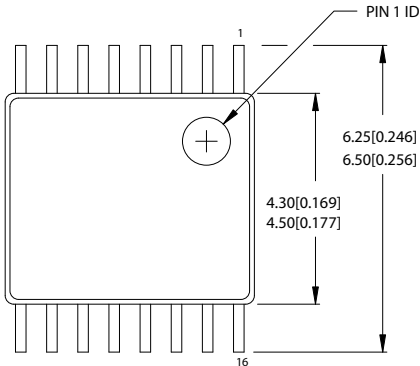
Ordering Code	Package Type	Operating Range	Operating Voltage
Pb-free			
CY24130ZXC-1 ^[2]	16-Pin TSSOP	Commercial	3.3V
CY24130ZXC-1T ^[2]	16-Pin TSSOP – Tape and Reel	Commercial	3.3V
CY24130ZXC-2 ^[2]	16-Pin TSSOP	Commercial	3.3V
CY24130ZXC-2T ^[2]	16-Pin TSSOP – Tape and Reel	Commercial	3.3V
CY24130KZXC-1	16-Pin TSSOP	Commercial	3.3V
CY24130KZXC-1T	16-Pin TSSOP – Tape and Reel	Commercial	3.3V

Note

2. Not recommended for new design.

Package Drawing and Dimensions

Figure 5. 16-lead TSSOP 4.40 MM Body Z16.173

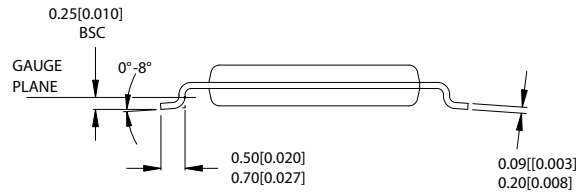
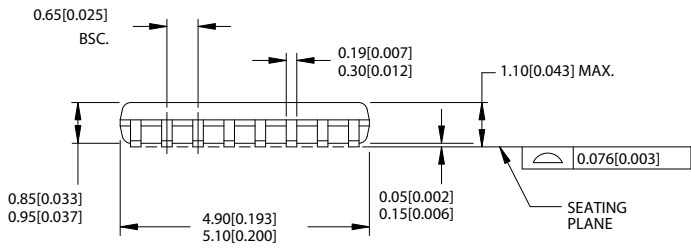


DIMENSIONS IN MM [INCHES] MIN. MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.05 gms

PART #	
Z16.173	STANDARD PKG.
ZZ16.173	LEAD FREE PKG.



51-85091-A

Document History Page

Document Title: CY24130 HOTLink II™ SMPTE Receiver Training Clock				
Document Number: 38-07711				
REV.	ECN NO.	Orig. of Change	Submission Date	Description of Change
**	314514	RGL	See ECN	New Data Sheet
*A	2442066	AESA	See ECN	Updated template. Added Note "Not recommended for new designs." Added part number CY24130KZXC-1, and CY24130KZXC-1T in ordering information table.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer’s representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

PSoC	psoc.cypress.com
Clocks & Buffers	clocks.cypress.com
Wireless	wireless.cypress.com
Memories	memory.cypress.com
Image Sensors	image.cypress.com

PSoC Solutions

General	psoc.cypress.com/solutions
Low Power/Low Voltage	psoc.cypress.com/low-power
Precision Analog	psoc.cypress.com/precision-analog
LCD Drive	psoc.cypress.com/lcd-drive
CAN 2.0b	psoc.cypress.com/can
USB	psoc.cypress.com/usb

© Cypress Semiconductor Corporation, 2005-2008. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress’ product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Infineon:](#)

[CY24130ZXC-1T](#) [CY24130ZXC-1](#) [CY24130ZXC-2](#)